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Cascaded-like High-Step-Down Converter with Single Switch and Leakage Energy Recycling in Single-Stage Structure

Chih-Lung Shen *, Li-Zhong Chen, Tsung-Yung Chuang and Yu-Shan Liang

Department of Electronic Engineering, National Kaohsiung University of Science and Technology, Kaohsiung 82445, Taiwan; 0652807@nkust.edu.tw (L.-Z.C.); f110112104@nkust.edu.tw (T.-Y.C.); ysliang@nkust.edu.tw (Y.-S.L.)

* Correspondence: clshen@nkust.edu.tw; Tel.: +886-7601-1000 (ext. 32515)

Abstract: A cascaded-like high-step-down converter (CHSDC) is proposed in this article, which can steeply convert a high voltage to a much lower level without the utilizing of extreme turns ratio or duty ratio. The proposed converter integrates two buck-boost converters and one forward converter to form a single-stage architecture containing only a single low-side driving switch, which, as a result, can lower the cost and reduce the complexity of the associated control driver. Even in a single-stage single-switch structure, the ability to step down input voltage is as effective as the cascade of two buck-boosts and one forward converter. Meanwhile, the proposed converter can avoid the low efficiency caused by a cascaded structure. Without an additional clamp circuit, the leakage energy stored in the transformer of the CHSDC can be still recycled so as to raise the efficiency of the converter and suppress voltage spikes at the power switch. Converter operation principle and key parameter design are discussed. Moreover, a 200 W prototype is built and then tested to validate the proposed converter and verify the theoretical analysis.

Keywords: high-step-down converter; single-stage; single-switch; cascaded-like configuration; leakage energy recycling; low-side driving

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1. Introduction

Even though electric vehicles (EVs) have to be charged, the power for which comes from fossil-fuel plants, EVs can still reduce carbon dioxide production by 60% as compared with engine-system vehicles. EVs have been challenging the leading position of engine-system vehicles as a matter of course.

EVs commonly have two built-in DC voltage levels for different kinds of power supply, as shown in Figure 1. The purpose of the high-voltage battery bank is mainly to provide power for motor driving. Meanwhile, the low-voltage lithium-ion battery is for in-car auxiliary appliances such as the panelboard, dashcam, lighting, audio and video systems, air conditioner, automatic seat, and power steering wheel. The low-voltage lithium-ion battery has to be charged from the high-voltage bus. However, the low-voltage battery can alternatively be removed. With this approach, the auxiliary appliances will be powered by the high-voltage bus through a step-down converter with a high conversion ratio. No matter whether a low-voltage lithium-ion battery should be installed in EVs, a high step-down converter to steeply lower bus voltage for powering auxiliary appliances is certainly required.

Conventional step-down converters, such as buck-derived DC/DC converters [1–4], can theoretically accomplish a high voltage-conversion ratio by operating under an extreme duty cycle. However, at the operating of an extreme duty cycle, significant conduction loss and switching loss, high voltage stresses, influential ripples, low efficiency of the converter, etc., will inevitably drop the performance of this kind of converter a lot. For efficiency improvement, among the buck-derived converters, some of them utilize soft-switching mechanisms into the converter design to increase efficiency. Nevertheless, an

acceptable efficiency still cannot be obtained under an extreme duty ratio. As considering isolated topologies, the bridge-derived configurations can be a choice [5–9]. However, in order to obtain a huge conversion ratio, a higher turns ratio has to be adopted, which also decreases converter efficiency and then narrows the conversion range. Besides, multiple active switches will increase costs, the complexity of the drier, and the interference of switching noise.

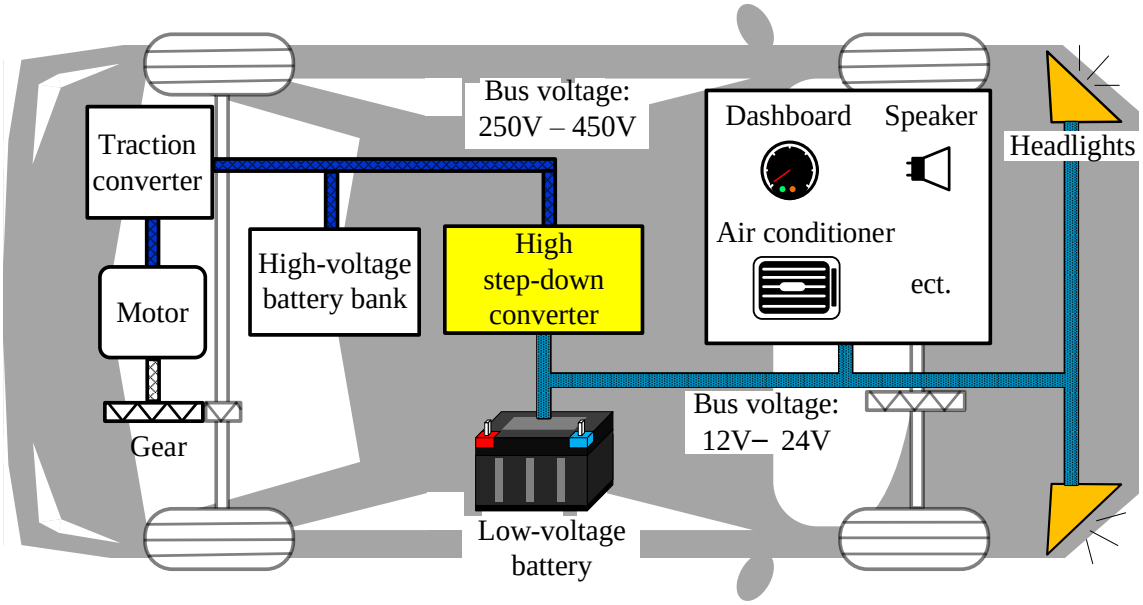

Figure 1. Structure of the power system of electric vehicles.

The structure of a two-/multi-stage converter [10–13] can be an option for achieving an expected voltage gain and for a wide voltage-range operation. With the structure of multi-stages, the parameter tuning will have higher flexibility to average voltage stresses in each stage, which is one advantage of this kind of converter; however, it still has several drawbacks, such as at least two active switches need to be employed and it displays low overall efficiency. Therefore, a cascaded-like converter is developed, which possesses the characteristics of both a high voltage ratio and wide voltage range, the same as that completed by a two-stage converter, and only needs a single switch [14–19]. Nevertheless, their step-down voltage ratios still cannot be as high as for EV applications. Combining transformers into cascaded-like converters to further raise the voltage ratio is, therefore, studied [20–25], but high voltage spikes caused by the leakage inductance of a transformer need to be taken into consideration [21–23]. Usually, a snubber circuit or an active clamped cell is necessarily integrated into converter design [24,25], which accordingly increases cost and circuit complexity.

To step down a high voltage to a much lower level for auxiliary power applications in EV systems as well as overcome the aforementioned problems, a cascaded-like high-step-down converter (CHSDC) is proposed in this paper. As shown in Figure 2, the CHSDC integrates two buck-boost converters and one forward converter to be a single-switch single-stage architecture. It can accomplish a step-down voltage ratio as high as obtained by the three-stage cascade of two buck-boost converters and one forward converter. In addition, the CHSDC intrinsically has the features of leakage energy recycling and galvanic isolation.

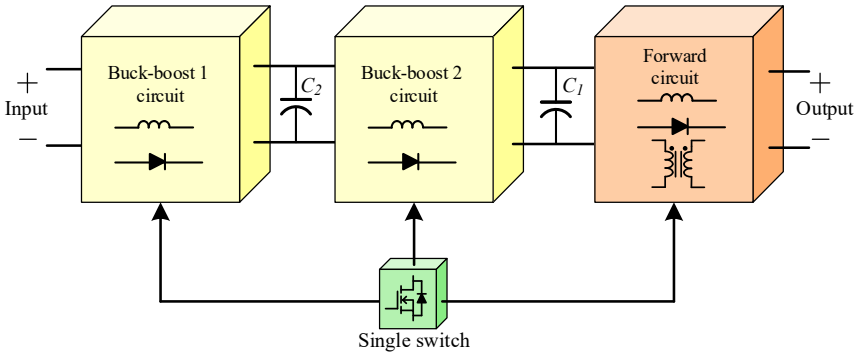

Figure 2. A brief block diagram to illustrate the derivation of the proposed converter.

2. Converter Structure and Operation Principle

The main power circuit of the proposed CHSDC is depicted in Figure 3, which is derived from the integration of dual buck-boost converters and a forward converter to construct a single-stage structure with a single switch and galvanic isolation. Even though only one active switch is adopted, the CHSDC is able to step down input voltage as effectively as the cascade type of two buck-boost converters and one forward converter. The cascade of three converters needs three active switches at least, the worst of which belongs to a multi-stage structure, lowering overall efficiency dramatically. Therefore, the CHSDC is much better than the cascade structure.

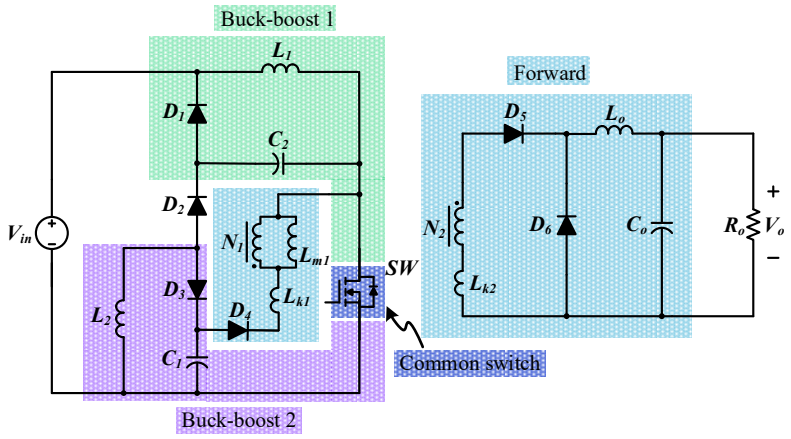

Figure 3. The main power circuit of CHSDC.

As shown in Figure 3, it can be observed that the CHSDC incorporates buck-boost 1, buck-boost 2, and a forward, only using a common switch but still possessing a high conversion ratio achieved by a cascaded multi-stage converter. In the main power circuit, the equivalent of the high-frequency transformer includes a turns ratio of N_2 to N_1, a magnetizing inductance L_{m1}, two leakage inductances L_{k1} and L_{k2}.

To clearly describe the operation of the CHSDC, the definitions of voltage polarity and current direction are shown in Figure 4. To simplify the analysis, the following assumptions are considered:

1. All the capacitors are large enough so that the voltages across them are regarded as constant and ripple-free;
2. All semiconductor devices and diodes are ideal. That is, parasitic parameters can be neglected;
3. The L_{k1} and L_{k2} represent the leakage inductances at the primary side and secondary side of the high-frequency transformer, respectively, values of which both are much smaller than the magnetizing inductance L_{m1};
4. The duty ratio of the switch *SW* will be less than 0.5;

5. The turns ratio of the coupled inductor n is equal to $\frac{N_2}{N_1}$;
6. The inductors L_1 and L_2 in the buck-boost circuits and the inductor L_o in the forward circuit all operate in continuous conduction mode (CCM).

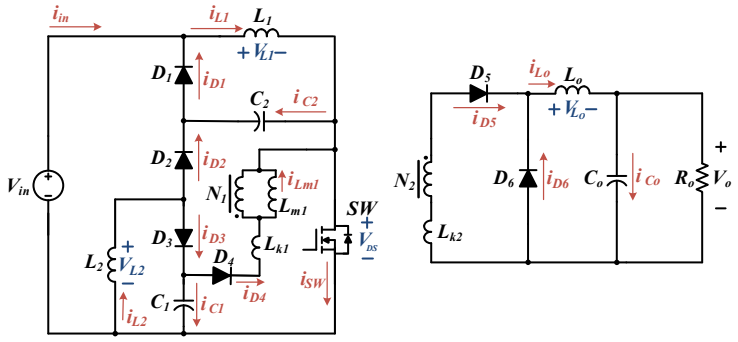

Figure 4. Definitions of voltage polarity and current direction of the proposed converter.

The operation of the proposed CHSDC at steady-state and in CCM can be divided into five modes over one switching cycle. Figure 5 depicts the conceptual key waveforms of this converter, while Figures 6–10 are the equivalents for each mode in turn. In the following, the five operating modes of the converter will be discussed mode by mode.

Mode 1 [t_0~t_1]:

As shown in Figure 6, Mode 1 begins when the power switch SW is turned on at t_0. During the time interval of Mode 1, diodes D_2, D_4, D_5, and D_6 are in forwarding bias, but diodes D_1 and D_3 are reversely biased. During this short-time transition, the current of the leakage inductor L_{k1}, i_{Lk1} increases linearly. Meanwhile, the current flowing through L_{k2}, i_{Lk2} also increases linearly. The energy of inductor L_o is delivered to the load and capacitor C_o. As the increasing current of i_{Lk2} is equal to the current of i_{Lo}, the diode D_6 becomes OFF and this mode ends.

Mode 2 [t_1~t_2]:

Mode 2 lasts from t_1~t_2. The equivalent circuit of Mode 2 is presented in Figure 7, which indicates that the SW, D_2, D_4, and D_5 are still conducting and diodes D_1, D_3, and D_6 are OFF. Inductor L_1 absorbs energy from the input voltage, and capacitor C_2 charges the inductor L_2 through switch SW and diode D_2. In addition, capacitor C_1 forwards its stored energy to the low-voltage side through the high-frequency transformer to supply the output. Thus, the leakage–inductance current i_{Lk1} and magnetizing–inductance current i_{Lm1} are increasing linearly, as does the output–inductor current i_{Lo}. As the switch SW is turned off, the operation of the converter enters the next mode.

Mode 3 [t_2~t_3]:

Mode 3 starts at time $t = t_2$. Figure 8 is the related equivalent, where switch SW and diode D_2 are in OFF state but diodes D_1, D_3, D_4, D_5, and D_6 are in ON-state. During this short period, the energy stored in L_{k1} is recycled to capacitor C_2 and the input voltage through diode D_1. At the same time, the leakage energy of L_{k2} is recycled to the capacitor C_o via the diode D_5. In this mode, capacitor C_2 is also charged by the inductor L_1, and capacitor C_1 is charged by L_2 via diode D_3. This mode ends when leakage energy in L_{k2} releases completely at $t = t_3$.

Mode 4 [t_3~t_4]:

After leakage inductance releases all stored energy, diode D_5 becomes OFF and converter operation will be in Mode 4. As illustrated in Figure 9, the switch SW remains OFF and diodes D_2 and D_5 are reversely biased. On the contrary, diodes D_1, D_3, D_4, and D_6 are forwarded. Leakage inductance L_{k2} keeps recycling its energy. In this time interval, the currents i_{Lk1} and i_{Lm1} decrease linearly. On the low-voltage side, output inductor L_o still supplies for the output as well as capacitor C_o. When the leakage-inductance current

i_{Lk1} and magnetizing-inductance current i_{Lm1} drop to zero at $t = t_4$, the next operation mode begins.

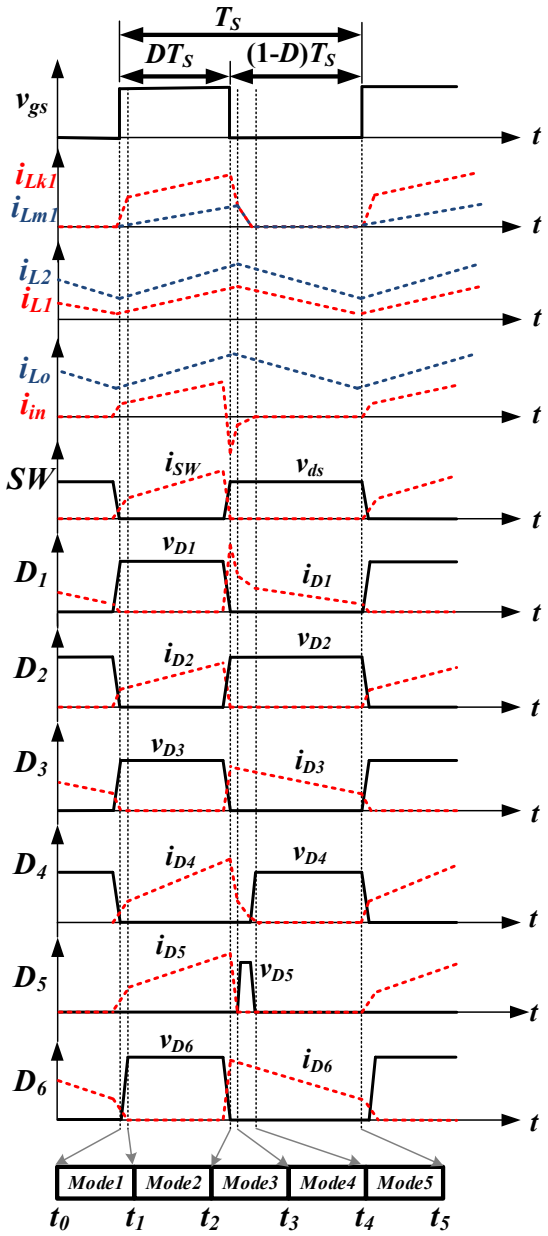

Figure 5. Conceptual key waveforms of the converter in the CCM situation.

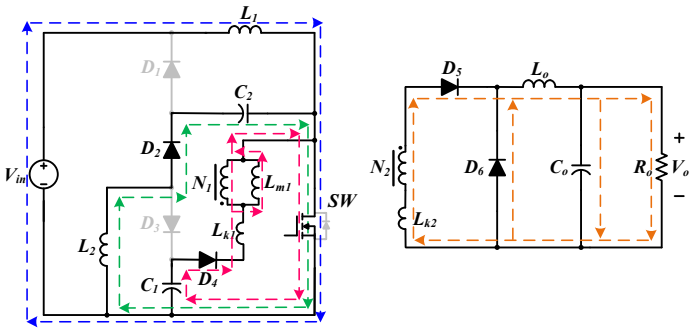

Figure 6. Equivalent circuit of the CHSDC in Mode 1.

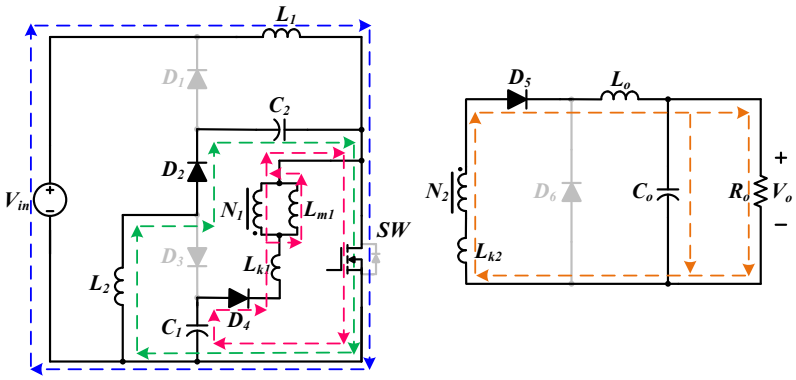

Figure 7. Equivalent circuit of the CHSDC in Mode 2.

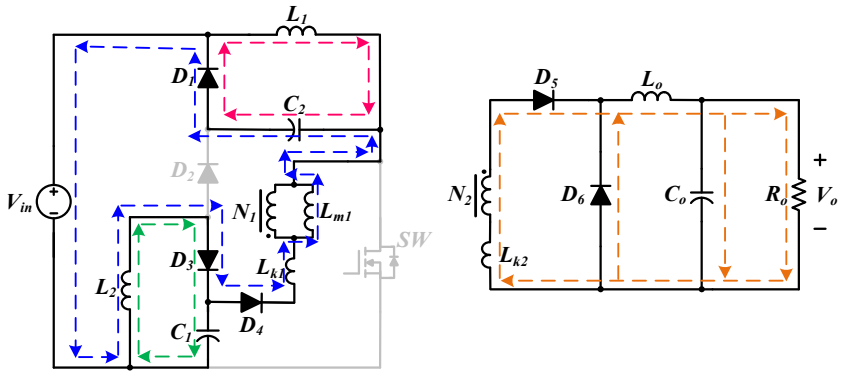

Figure 8. Equivalent circuit of the CHSDC in Mode 3.

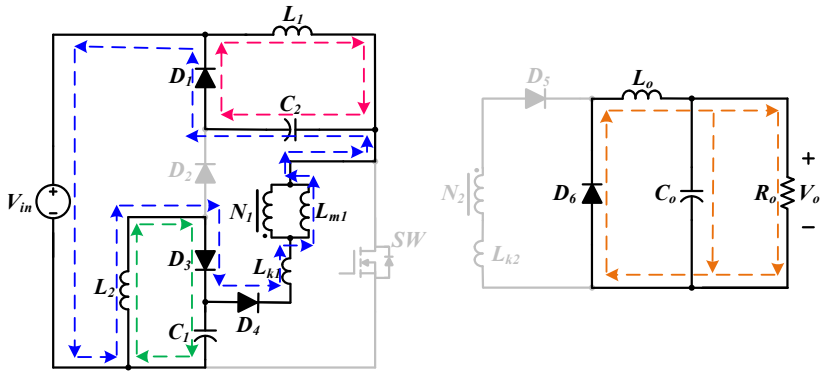

Figure 9. Equivalent circuit of the CHSDC in Mode 4.

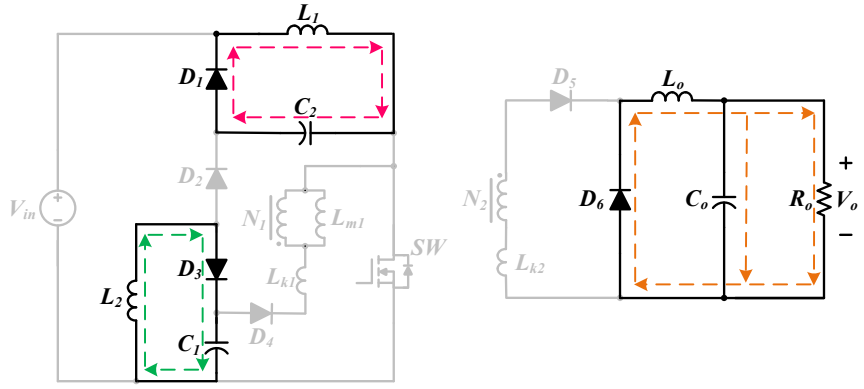

Figure 10. Equivalent circuit of the CHSDC in Mode 5.

Mode 5 [t_4~t_5]:

As indicated in Figure 10, this equivalent circuit is for Mode 5, the switch *SW* is still in OFF-state, diodes D_1, D_3, and D_6 are in forwarding bias, and diodes D_2, D_4, and D_5 are reverse biased. In this mode, capacitor C_2 is charged by inductor L_1 through diode D_1, while inductor L_2 charges capacitor C_1 via diode D_3. The output inductor L_o keeps energy-supplying for the load. This mode ends when switch *SW* is turned on. The complete operation of the converter finishes at $t = t_5$.

3. Steady-State Analysis

3.1. Voltage Gain

The followings discuss the voltage gain derivation of the converter. The definitions of voltage polarity and the current direction are according to Figure 4. Applying the voltage-second balance principle to output inductor L_o yields

$$V_{Lo,on}DT_s+V_{Lo,off}\ (1\ -\ D)T_s=0 \tag{1}$$

in which the $V_{Lo,on}$ and $V_{Lo,off}$ are denoted as the voltages across the inductor L_o during the intervals of *SW* ON and OFF, respectively, D stands for the duty ratio of the active switch, and T_s is switching period. As indicated in Figure 7, while *SW* is in ON state, the voltage of inductor L_1, $V_{L1,on}$, and the voltage of inductor L_2, $V_{L2,on}$, can therefore be found as follows:

$$V_{L1,on}=V_{in} \tag{2}$$

and

$$V_{L2,on}=V_{C2} \tag{3}$$

Additionally, as the switch is ON, the voltage across inductor L_o, $V_{Lo,on}$, is expressed as

$$V_{Lo,on}=nV_{C1}+V_o \tag{4}$$

When switch *SW* is OFF, as depicted in Figure 10, the voltages across inductors L_1, L_2, and L_o are

$$V_{L1,off}=-V_{C2} \tag{5}$$

$$V_{L2,off}=nV_{C1}+V_o \tag{6}$$

and

$$V_{Lo,off}=-V_o \tag{7}$$

respectively. By substituting (4) and (7) into (1), the output voltage V_o is obtained as

$$V_o=nDV_{C1} \tag{8}$$

While applying the criterion of voltage-second balance to the inductors L_1 and L_2 individually, the capacitor voltages V_{C1} and V_{C2} in terms of duty ratio D and input voltage V_{in} can be given as

$$V_{C1}=\left(\frac{D}{1\ -\ D}\right)^2 V_{in} \tag{9}$$

and

$$V_{C1}=\left(\frac{D}{1\ -\ D}\right)V_{in} \tag{10}$$

respectively. Then, substituting (8) into (9), as a result, the converter voltage ratio of output to input is estimated as

$$\frac{V_o}{V_{in}}=\frac{nD^3}{(1\ -\ D)^2} \tag{11}$$

While the CHSDC is in CCM operation, the relationship of voltage gain versus switch duty cycle D, under different turns ratios of the transformer, is illustrated in Figure 11. It can be observed that the CHSDC is capable of stepping down a high input voltage significantly even under the operating with a regular turns ratio. That is, this converter can avoid employing a high turn-ratio transform. As revealed in Figure 11, the CHSDC achieves a conversion ratio of 0.03 at the conditions that turn ratio is 1:3 and duty cycle is 0.34. That is, based on this conversion ratio, the CHSDC can deal with a 400 V input voltage to power a 12 V load.

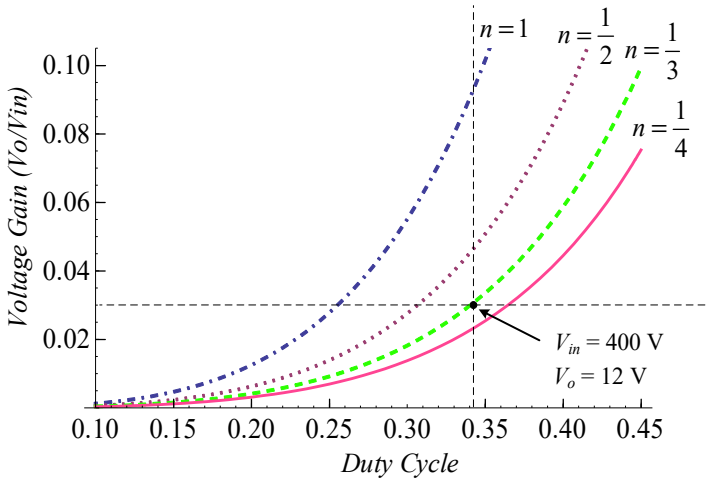

Figure 11. Relationship among voltage gain, duty ratio, and turns ratio.

3.2. Voltage Stresses of Semiconductors

In order to choose a proper power switch and diodes, the determination of voltage stress and current stress for each semiconductor device has to be fulfilled. According to Figure 10, during the period of *SW* OFF, the blocking voltages of the *SW* and diodes D_2, D_4, D_5 can be expressed as

$$V_{SW,stress} = V_{in} + \frac{D}{1-D}V_{in} = \frac{1}{1-D}V_{in} \tag{12}$$

$$V_{D2,stress} = \frac{1-2D}{(1-D)^2}V_{in} \tag{13}$$

$$V_{D4,stress} = \frac{1-D-D^2}{(1-D)^2}V_{in} \tag{14}$$

and

$$V_{D5,stress} = \frac{1-D-D^2}{(1-D)^2}nV_{in} \tag{15}$$

in turn. Similarly, according to Figure 7, during the period of *SW* ON, the blocking voltages of diodes D_1, D_3, and D_6 are, respectively, denoted as follows:

$$V_{D1,stress} = \frac{1}{1-D}V_{in} \tag{16}$$

$$V_{D3,stress} = \frac{D}{(1-D)^2}V_{in} \tag{17}$$

and

$$V_{D6,stress} = \left(\frac{D}{1-D}\right)^2 nV_{in} \tag{18}$$

3.3. Current Stresses of Semiconductors

Since the output inductor L_o is in series with the output port, the inductor current i_{Lo} will be equal to the output current i_o and can be calculated by

$$i_{Lo} = i_o = \frac{V_o}{R} = \frac{nD^3V_{in}}{R(1-D)^2} \tag{19}$$

In (19), R is the load resistance. As referred to Mode 2 and Mode 5, the inductor current i_{Lo} passes through diode D_5 and diode D_6 when SW is ON and OFF, respectively. Therefore, the current stresses of D_5 and D_6 will be identical to each other, which are obtained as

$$i_{D5,stress} = i_{D6,stress} = i_{Lo} = \frac{nD^3V_{in}}{R(1-D)^2} \tag{20}$$

For determining the current stresses of the other semiconductor devices, including D_1, D_2, D_3, D_4, and SW, average currents of L_{m1}, L_1, and L_2 along with the capacitor current of C_1 during SW-ON, that is, $i_{Lm1,avg}$ $i_{L1,avg}$, $i_{L2,avg}$, and $i_{C1,on}$, have to be found in advance. To comprehend the finding, the waveform of i_{Lm1} is depicted in Figure 12, based on which the current $i_{Lm1,avg}$ can be computed as

$$i_{Lm1,avg} = \frac{\Delta i_{Lm1}}{2} = \frac{\Delta i_{Lm1}D'T_s}{2D'T_s}. \tag{21}$$

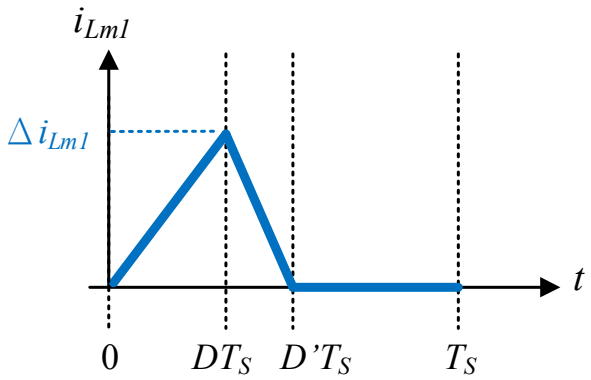

Figure 12. The waveform of magnetizing–inductance current i_{Lm1}.

The Δi_{Lm1} in (21) is equal to

$$\Delta i_{Lm1} = \frac{V_{C1}DT_s}{L_{m1}} \tag{22}$$

Placing Δi_{Lm1} in (22) into (21) yields

$$i_{Lm1,avg} = \frac{DT_s}{2L_{m1}}\left(\frac{D}{1-D}\right)^2 V_{in} = \frac{D^3T_sV_{in}}{2(1-D)^2L_{m1}} \tag{23}$$

Based on Mode 2 and Mode 5, the expresses of $i_{L1,avg}$, $i_{L2,avg}$, and $i_{C1,on}$ can be figured out as follows:

$$Di_{Lm1,avg} = i_{in} \tag{24}$$

$$(1-D)i_{L1,avg} = Di_{L2,avg} \tag{25}$$

and

$$(1-D)i_{L2,avg} = Di_{C1,on} \tag{26}$$

Suppose that the input power will equal output power. That is,

$$V_{in}i_{in} = V_o i_o \tag{27}$$

Since the voltage gain of the CHSDC has been obtained in (11), the input current of the converter can be

$$i_{in} = \frac{nD^3}{(1 - D)^2} i_o \tag{28}$$

Substituting both relationships of (19) and (28) into (24), (25), and (26), individually, the currents of $i_{L1,avg}$, $i_{L2,avg}$ $i_{C1,on}$ are therefore obtained as

$$i_{L1,avg} = \left(\frac{nD^2}{(1 - D)^2}\right)^2 \frac{V_{in}D}{R} \tag{29}$$

$$i_{L2,avg} = \frac{n^2D^4V_{in}}{R(1 - D)^3} \tag{30}$$

and

$$i_{C1,on} = \frac{1 - D}{D} i_{L2,avg} = \frac{n^2D^3V_{in}}{R(1 - D)^2} \tag{31}$$

Because the average current flowing through diode D_1 and the inductance current $i_{L1,avg}$ are the same, the following relationship holds:

$$i_{D1,avg} = i_{L1,avg} = \left(\frac{nD^2}{(1 - D)^2}\right)^2 \frac{V_{in}D}{R} \tag{32}$$

Besides, the average currents of D_2 and D_3 are equal to the inductor current $i_{L2,avg}$, which leads to

$$i_{D2,avg} = i_{D3,avg} = i_{L2,avg} = \frac{n^2D^4V_{in}}{R(1 - D)^3} \tag{33}$$

Concerning the current stress of D_4, it can be determined as

$$i_{D4,avg} = i_{C1,on} = \frac{n^2D^3V_{in}}{R(1 - D)^2} \tag{34}$$

For active switch *SW*, Mode 2 is referred and then, its current stress is denoted as

$$i_{SW,avg} = i_{L1,avg} + i_{L2,avg} + i_{C1,on} \tag{35}$$

Substituting (29), (30), and (31) into (35), the current stress of *SW*, $i_{SW,avg}$, is then obtained as:

$$i_{SW,avg} = \frac{(1 - D + D^2)n^2D^3V_{in}}{R(1 - D)^4} \tag{36}$$

3.4. Inductance Design

To guarantee that the converter operation is in CCM, all the minimum currents of the inductors L_o, L_1, and L_2, that is, $i_{Lo(min)}$, $i_{L1(min)}$, and $i_{L2(min)}$, are set to be zero and accordingly the following relationships hold:

$$i_{Lo(\min)} = i_{L2,avg} - \frac{\Delta i_{Lm1}}{2} = \frac{V_o}{R} - \frac{V_{Lo}}{2L_o}(1 - D)T_s = 0 \tag{37}$$

$$i_{L1(\min)} = i_{L1,avg} - \frac{\Delta i_{L1}}{2} = \left(\frac{nD^2}{(1 - D)^2}\right)^2 \frac{V_{in}D}{R} - \frac{V_{in}D}{2L_1 f_s} = 0 \tag{38}$$

and

$$i_{L2(\min)} = i_{L2,avg} - \frac{\Delta i_{L2}}{2} = \frac{n^2 D^4 V_{in}}{R(1-D)^3} - \frac{V_{in} D^2}{2L_2(1-D)f_s} = 0 \tag{39}$$

Based on (37)–(39), the required minimum inductances of L_o, L_1, and L_2, denotes as $L_{o(min)}$, $L_{1(min)}$, and $L_{2(min)}$, respectively, to ensure the CHSDC is in CCM are determined as

$$L_{o(\min)} = \frac{R(1-D)}{2f_s} \tag{40}$$

$$L_{1(\min)} = \frac{R(1-D)^4}{2n^2 D^4 f_s} \tag{41}$$

and

$$L_{2(\min)} = \frac{R(1-D)^2}{2n^2 D^2 f_s} \tag{42}$$

3.5. Capacitance Design

In the CHSDC, the larger the capacitances are, the smaller the voltage ripples become. In order to suppress voltage ripples within the requirements, estimating for the minimum capacitances should be fulfilled. Voltage variation on a capacitor is given as

$$\Delta V = \frac{i_C \Delta t}{C} = \frac{\Delta Q}{C} \tag{43}$$

with (43), the capacitances of C_1, C_2, and C_o can be derived as:

$$C_1 = \frac{i_{L2,avg}(1-D)T_s}{\Delta V_{C1}} = \frac{n^2 D^4 V_{in} T_s}{R(1-D)^2 \Delta V_{C1}} \tag{44}$$

$$C_2 = \frac{i_{L1,avg}(1-D)T_s}{\Delta V_{C2}} = \frac{n^2 D^5 V_{in} T_s}{R(1-D)^3 \Delta V_{C2}} \tag{45}$$

and

$$C_o = \frac{1}{2}\frac{T_s}{2}\frac{\Delta i_{Lo}}{2\Delta V_o} = \frac{nD^3 V_{in} T_s}{8R(1-D)^2 \Delta V_o} \tag{46}$$

The equivalent series resistance (ESR) in a capacitor will dissipate power and thus lower converter efficiency. It seems that a much higher capacitance should be designed, however, which raises the cost. Therefore, an appropriate capacitance should compromise with voltage ripples. When building the CHSDC prototype, we consider to the voltage ripples of the capacitors C_1, C_2, and C_o should be under 1 V, 5 V and 0.1 V, when the capacitance of each capacitors are 47 μF, 4.7 μF and 470 μF.

3.6. Performance Comparison

Table 1 summarizes the comparison of the proposed converter with other step-down converters. The performance comparison includes voltage gain, the numbers of semiconductor devices, the numbers of capacitors and magnetic elements, isolation features, and the ability of leakage-energy recycling. Table 1 reveals that the merits of the proposed converter contains: having the mechanism of leakage-energy recycling, a lower number of switches, lower capacitance used, and a better voltage gain. As illustrated in Table 1, even though the proposed CHSDC only requires a single power switch, it can still achieve an excellent step-down competence over all possible range of duty ratios, almost surpassing other similar converters. In addition, the CHSDC has the mechanism of leakage-energy recycling and the feature of galvanic isolation. There are six diodes in the proposed converter, which would imply that, because more diodes are utilized, conversion efficiency would be dropped dramatically. However, among all diodes in the CHSDC, two diodes

are located on the low-voltage side. The low-voltage diodes can avoid the converter from consuming too much power. Concerning the number of magnetic elements, since the proposed converter is mainly derived from the integration of two buck-boosts and one forward converter, theoretically, the converter will contain more magnetic components. Nevertheless, from the viewpoint of gaining a higher voltage ratio, it is worthwhile. The designs of the magnetic components are in DCM while operating below two-thirds of the load, which means that lower inductances can be considered. Conduction loss can be accordingly restrained. In addition, leakage energy stored in the transformer of the CHSDC can be recycled. Owing to the inductor design and energy-recycling competence, even though more magnetic components are used, power loss still can be suppressed.

Table 1. Performance comparison among the proposed converter and other recently proposed topologies.

Ref.	**[3]**	**[10]**	**[14]**	**[25]**	**Proposed**
Voltage gain	$\frac{D}{2-D}$	$\frac{D}{n}$	$\frac{D}{2}$	nD^2	$\frac{nD^3}{(1-D)^2}$
MOSFETs	2	6	1	3	1
Diodes	2	0	3	3	6
Capacitors	3	3	2	3	3
Magnetic elements	3	2	2	3	4
Galvanic isolation	No	Yes	No	Yes	Yes
Leakage energy recycling	–	Yes	–	Yes	Yes

4. Experimental Results

To prove the theoretical derivation, illustrate the performance, and verify the validity of the CHSDC, a 200 W prototype is constructed and then tested. The input voltage of the converter is 400 V and the output voltage is 12 V. The key parameters of the prototype are summarized in Table 2. Figure 13a shows the waveforms of the practical input current and the related control signal, while Figure 13b is the corresponding simulations. Figure 13 reveals that the practical measurements can be consistent with the simulations. In addition, Figure 13 also illustrates that energy stored in leakage inductance can be recycled to the input source and the converter can avoid extreme duty-cycle operation even under the full-load condition. The duty ratio of the switch is close to 0.34, instead of operating in a heavy-duty ratio. Figure 14 is the voltage and current waveforms of the active switch with practical measure and simulation. It reveals that the average current of the switch is about 9.5 A, which is close to the calculation result of 9.91 A with (36). The current stresses of D_1–D_6 are calculated with (20) and (32)–(34), individually, then to be 1.48 A, 2.87 A, 2.87 A, 5.5 A, 16.6 A, and 16.6 A, respectively, all of which match with the measurement results of i_{D1} to i_{D6} in Figure 15. In addition, Figure 15a,g demonstrates that diodes D_1 and D_4 both have the feature of zero-current switching (ZCS) during the turn OFF transition. Experimental and simulated current and voltage waveforms of inductors and the output capacitor are also presented in Figures 16 and 17, respectively. Figure 16b shows the simulated inductor currents i_{L1} and i_{L2}, while Figure 16a is their practical measurements. From Figure 16, it can be observed that the inductors L_1 and L_2 are in DCM and CCM, respectively, which have confirmed the theoretical derivation in Section 3.4. Figure 17b is the simulated output voltage v_o and output inductor i_{Lo}, practical measurements of which are demonstrated in Figure 17a. As shown in Figure 17, it can be found that the output inductor L_o is in CCM, and the output voltage is controlled at a stable level of 12 V with a quite small ripple of less than 1%.

Table 2. Parameters and components used in the prototype.

Parameters	Values & Specifications
V_{in} (Input voltage)	400 V
V_o (Output voltage)	12 V
f_s (Switch frequency)	50 kHz
Power rating	200 W
L_{m1} (Magnetizing inductance)	366 µH
L_{k1} (Leakage inductance)	2.3 µH
L_1 (Inductor)	648 µH
L_2 (Inductor)	636 µH
L_o (Inductor)	366 µH
SW (Power MOSFET)	IXFN60N80P (800 V/53 A), Leiden, Netherlands
D_1 (Diode)	DSEP29-06A (600 V/30 A), Leiden, Netherlands
D_2 and D_3 (Diode)	BYC8-600 (600 V/8 A), Eindhoven, Netherlands
D_4 (Diode)	SDP30S120 (1200 V/30 A), Starkville, MS, USA
D_5 and D_6 (Diode)	DSSK 60-02A (200 V/2 × 30 A), Leiden, Netherlands
C_1 (Electrolytic capacitor)	47 µF
C_2 (Electrolytic capacitor)	4.7 µF
C_o (Electrolytic capacitor)	470 µF
n (Transformer turns ratio)	3:1

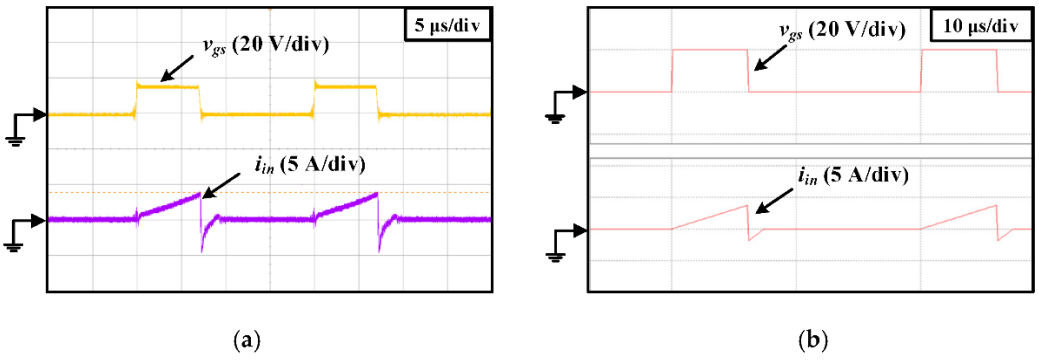

Figure 13. The waveforms of the control signal and the corresponding input current: (**a**) measured waveform, (**b**) simulated results.

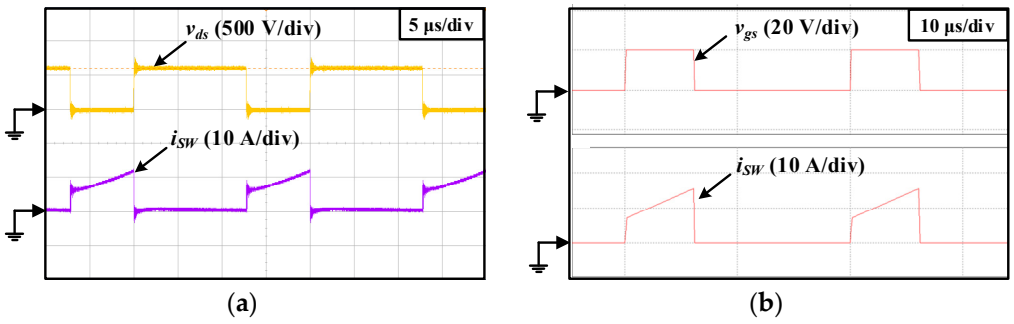

Figure 14. The waveforms: (**a**) measured switch voltage and current, (**b**) simulated control signal and switch current.

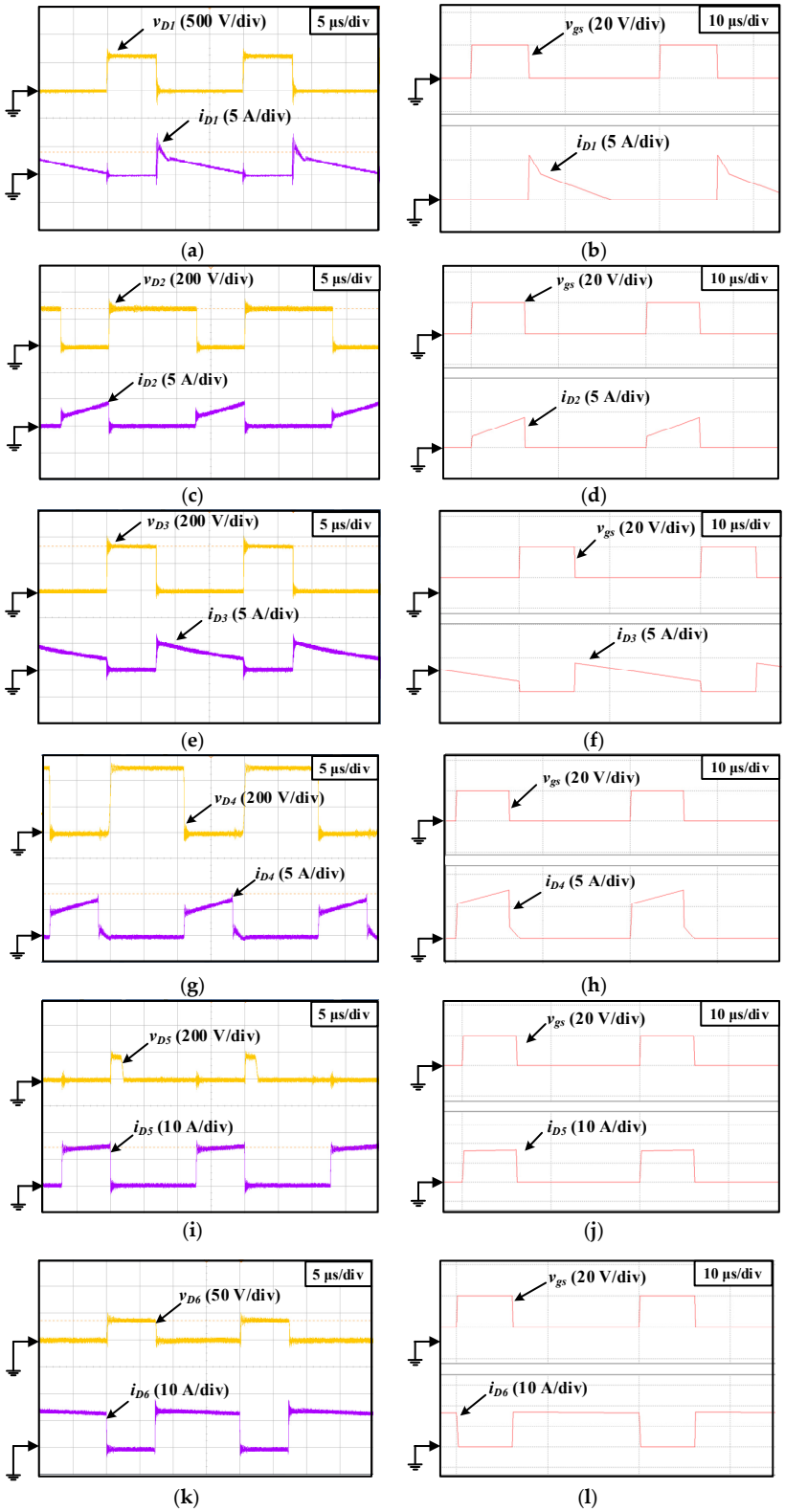

Figure 15. Measured results and simulations of all diodes in the proposed converter: (**a**) practical measurements of diode D_1, (**b**) simulated results of diode D_1, (**c**) practical measurements of diode D_2, (**d**) simulated results of diode D_2, (**e**) practical measurements of diode D_3, (**f**) simulated results of diode D_3, (**g**) practical measurements of diode D_4, (**h**) simulated results of diode D_4, (**i**) practical measurements of diode D_5, (**j**) simulated results of diode D_5, (**k**) practical measurements of diode D_6, and (**l**) simulated results of diode D_6.

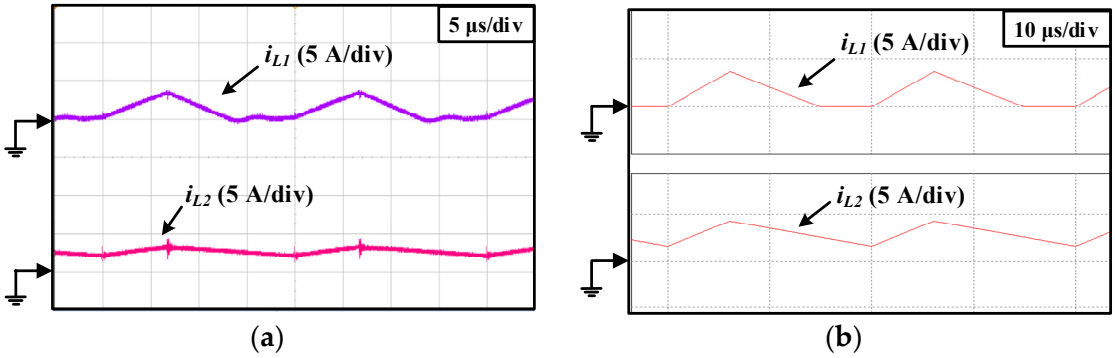

Figure 16. The waveforms of i_{L1} and i_{L2}: (**a**) practical measurements, and (**b**) simulated results.

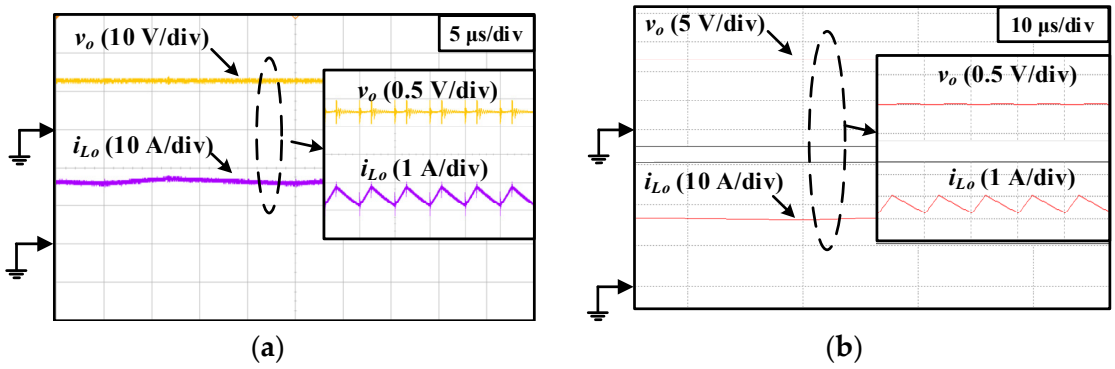

Figure 17. The waveforms of v_o and i_{Lo} with zoomed-in observation: (**a**) practical measurements, and (**b**) simulated results.

Figure 18 gives the voltage gain of the proposed converter in comparison with the step-down converters in [3,10,14,25]. It shows that the proposed converter is better at stepping down a high input voltage than other similar converters. Figure 19 expresses the power budget of the proposed CHSDC while operating in the full-load situation, in which diode loss accounts for 56% of the total loss. Switch loss accounts for 11%, while inductor loss, transformer loss, and capacitor loss are 15%, 11%, and 7%, respectively. The efficiency of the CHSDC is measured per 20 W from light load to full load. Figure 20 depicts the measured results. From this figure, the highest efficiency is around 93% at 140 W and 91% at the full load. Figure 21 is the photograph of the prototype of CHSDC.

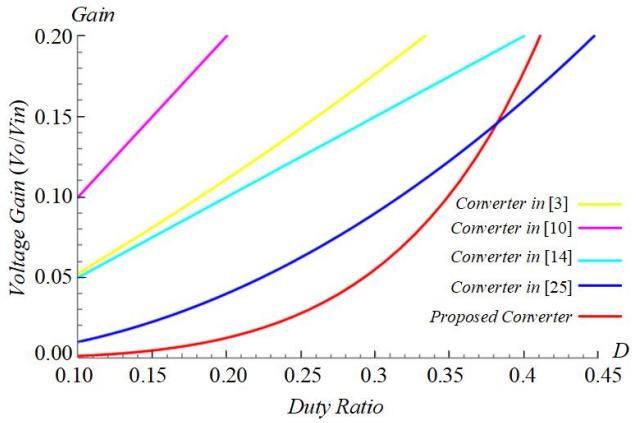

Figure 18. Voltage-gain comparison with other similar converters in [3,10,14,25].

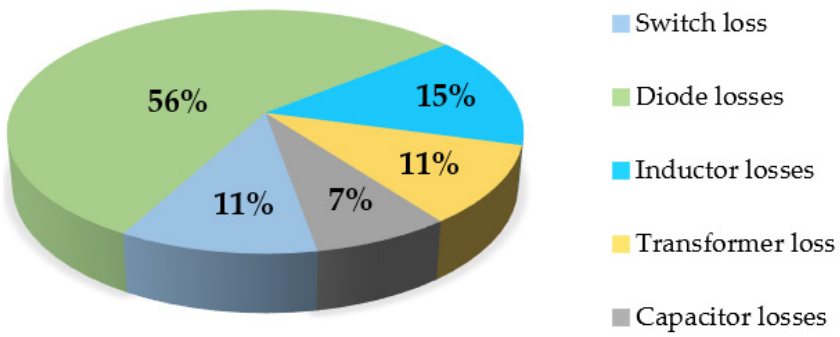

Figure 19. Power budget of the CHSDC.

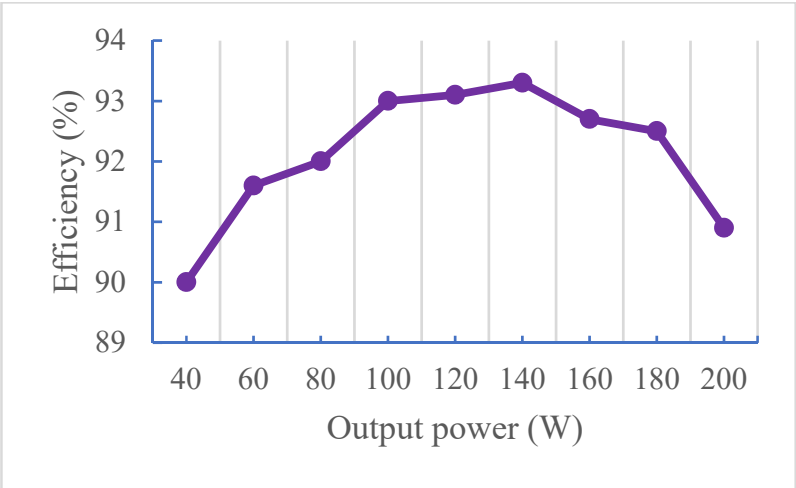

Figure 20. Measured efficiency of the CHSDC from light load to full load.

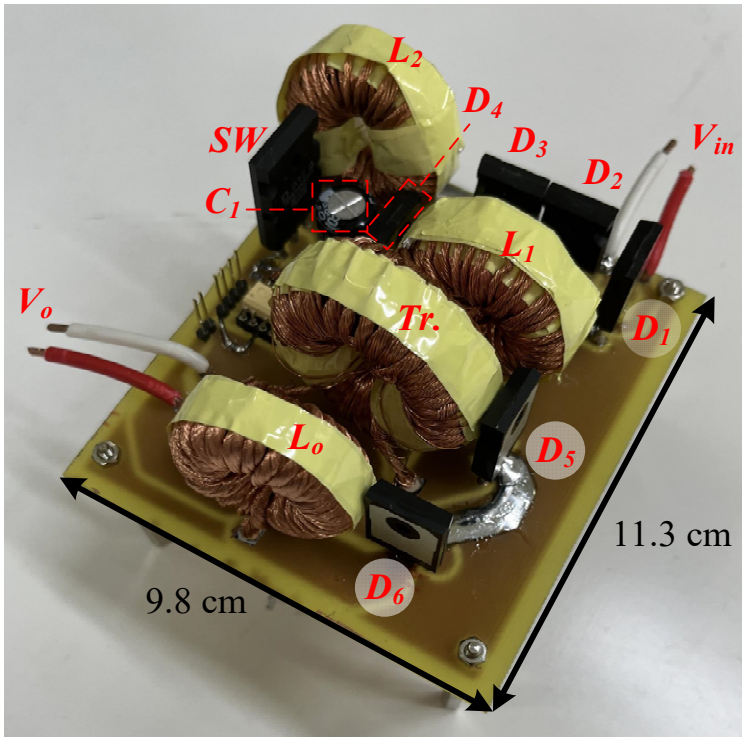

Figure 21. The photograph of the CHSDC.

5. Conclusions

In this article, a high step-down converter is proposed, which is able to accomplish an excellent voltage conversion ratio, avoiding the adopting of high turns ratio and extreme switch cycle. That is, the proposed converter can step down a high input voltage to a much lower level under a regular switch cycle and turns ratio. In the power stage, the CHSDC integrates two buck-boost circuits and one forward circuit to be a single-stage single-switch structure to achieve an excellent voltage conversion ratio which is the same as the effect obtained by the cascade of the three converters. Because only one switch is needed, the complexity of driving circuit design is reduced significantly. The leakage energy stored in the transformer can be recycled for improving the conversion efficiency of the converter and suppressing voltage spikes on the power switch as well. Furthermore, diodes D_1 and D_4 possess ZCS-off features. The operation principle, steady-state analysis, and parameter design of the converter in CCM have been explored. Finally, the correctness of the theoretical analysis and the feasibility of the converter are verified through the measurements from a 200 W prototype.

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