CASCADED MULTILEVEL CONVERTER BASED TRANSMISSION STATCOM: SYSTEM DESIGN METHODOLOGY AND DEVELOPMENT OF A 12kV ±12MVAr POWER-STAGE

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ABSTRACT

CASCADED MULTILEVEL CONVERTER BASED TRANSMISSION STATCOM: SYSTEM DESIGN METHODOLOGY AND DEVELOPMENT OF A 12kV ±12MVAr POWER-STAGE

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This research and development work deals with the design methodology for Cascaded Multilevel Converter (CMC) based Transmission STATCOM (T-STATCOM) and development of a ±12MVAR, 12kV line-to-line wye-connected, 11-level CMC. This CMC module constitutes the basic building block of T-STATCOM systems. Sizing of the CMC module, number of H-Bridges in each phase of the CMC, AC voltage rating of the CMC, the number of paralleled CMC modules in the T-STATCOM system, optimum value of series filter reactors and determination of busbar in the power grid to which the T-STATCOM system is going to be connected are also discussed in the thesis in view of IEEE Std.519-1992, current status of HV IGBT technology and the required reactive power variation range for the T-STATCOM application. In the field prototype of the CMC module, the AC voltages are approximated to sinusoidal waves by Selective Harmonic Elimination Method (SHEM) and by the use of an optimized series input filter reactor. The use of n number of HBs in each phase provides us n number of freedom

in the application of SHEM. One of them is allocated to the fundamental component while n-1 is for the elimination of low order harmonics. Since n is chosen to five in the prototype system, 5th, 7th,11th and 13th harmonic components are successfully eliminated in the AC voltage waveforms of the CMC module. The equalization of DC link capacitor voltages is achieved according to Modified Selective Swapping (MSS) algorithm. MSS is applied every 400μs period if needed to obtain a perfect equalization of DC link capacitor voltages at the expense of higher switching frequency and hence switching losses. In this research work, an L-shaped laminated bus has been designed and the HV IGBT driver circuit has been modified for optimum switching performance of HV IGBT modules in each HB circuit. The performances of the HB circuit and the resulting 11-level CMC module have been obtained not only in the laboratory but also in the field. Design works for HB and the CMC are based on MATLAB and PSCAD simulations. The laboratory and field performance of the HB circuit and CMC module is found to be satisfactory and quite consistent with the theoretical results and design objectives. In addition to these, 154 kV, ±50MVAr T-STATCOM prototype has been designed, implemented and installed at Sincan Transformer Substation-Ankara primarily for the purposes of reactive power compensation and terminal voltage regulation. The T-STATCOM prototype is composed of five parallel operated CMC modules developed within the scope of this PhD thesis research work. The T-STATCOM configuration permits the operation of any number of CMC modules in the range from one to five for experimental purposes. The performance of this T-STATCOM system is also presented in this PhD thesis as a sample application.

Keywords: Transmission STATCOM, Cascaded Multilevel Converter (CMC), Modified Selective Swapping (MSS)

ÖZ

KASKAT ÇOK SEVİYELİ ÇEVİRGEÇ TABANLI İLETİM STATKOM: SİSTEM TASARIM YÖNTEMİ VE BİR 12kV ±12MVAr GÜÇ KATI GELİŞTİRİLMESİ

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Bu araştırma ve geliştirme çalışması, H-Köprülü Çok Seviyeli Çevirgeç temelli İletim STATCOM sistemleri için tasarım yöntemini ve bir adet ±12MVAR, 12 kV, Y-bağlı, 11-seviyeli H-Köprülü Çok Seviyeli Çevirgeç yapısının geliştirilmesini içermektedir. Geliştirilen bu çevirgeç modülü İletim STATCOM sistemleri için temel bir yapı teşkil etmektedir. Ayrıca bu tezde, geliştirilen çok seviyeli çevirgecin gücü, her fazında kullanılacak H-Köprü sayısı, çevirgecin tasarlanacağı AC gerilim değeri, İletim STATCOM sisteminde kullanılacak paralel çevirgeç sayısı, modüle bağlanacak en uygun seri filtre reaktörü değeri ve T-STATCOM'un güç sisteminde bağlanacağı baranın belirlenmesi konuları IEEE 519-1992 standardı, YG IGBT'lerin güncel teknolojisi ve uygulama için istenen reaktif gücün değişim aralağına göre irdelenmiştir. Geliştirilen çok seviyeli çevirgecin AC gerilim şekilleri, Seçici Harmonik Eleme Metodu (SHEM) ve en uygun değerdeki seri filtre reaktörünün kullanılması ile sinüs dalgalarına yaklaştırılmıştır. Her faz için n tane H-Köprü kullanımı SHEM uygulaması için n tane eşitliğin kullanım özgürlüğünü

tanımaktadır. Bu eşitliklerden biri temel bileşen için kullanılırken geri kalan n-1 tanesi de düşük dereceli harmoniklerin yok edilmesi amacıyla kullanılabilmektedir. Geliştirilen prototip sistem için n sayısı beş olarak seçildiğinden çevirgeç çıkış gerilimlerinde 5., 7., 11. ve 13.harmonik bileşenleri başarılı bir şekilde elenmiştir. Çevirgeçte kullanılan DA bağ kondansatör gerilimleri Düzenlemiş Seçici Yer Değiştirmeli algoritması ile eşitlenmiştir. Gerektiğinde 400µs periyotlarla uygulanan bu metod sayesinde yüksek anahtarlama frekansı ve daha fazla kayba rağmen DA bağ gerilimleri için mükemmel bir eşitlik sağlanmıştır. Bu araştırma çalışmasında her H-Köprü için L şeklinde bir lamine bara yapısı tasarlanmış ve YG IGBT'lerde optimum anahtarlama performansı elde etmek için sürücü devreleri değiştirilmiştir. H-Köprü ve elde edilen 11-seviyeli Çevrigeç performansları hem laboratuvarda hem de sahada elde edilmiştir. H-Köprü ve çevirgeç için MATLAB ve PSCAD benzetimleri ile tasarım çalışmaları yürütülmüştür. Laboratuvar ve sahada elde edilen verilerin hem H-Köprü hem de çevirgeç için oldukça tatminkar olmasının yanısıra teorik sonuçlar ve tasarım hedefleriyle gayet uyumlu olduğu gözlemlenmiştir. Bunlara ek olarak, bir adet 154 kV, ±50MVAr İletim STATCOM prototipi tasarlanıp geliştirilmiş ve Ankara'da bulunan Sincan Trafo Merkezinde reaktif güç kompanzasyonu ve bara gerilim düzenlenmesi amaçları için kurulmuştur. Kurulan sistem bu doktora tez çalışmasında geliştirilen beş adet çok seviyeli çevirgecin paralel kullanımından oluşmaktadır. İletim STATCOM yapısı, birden beşe kadar çevirgecin deneysel amaçla kullanılmasına olanak vermektedir. Bu İletim STATCOM sisteminin performansı da ayrıca bir uygulama örneği olarak da tezde verilmiştir.

Anahtar Kelimeler: İletim STATKOM, Çok Seviyeli Çevirgeçler, Düzenlenmiş Seçici Yerdeğiştirme

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NOMENCLATURE

Es′: Internal source voltage referred to CMC side

Xs′: Internal source reactance referred to CMC side

PCC: Point of Common Coupling

Vs′: Fundamental voltage component at Point of Common Coupling (PCC) referred to CMC side

X: Total series reactance including leakage reactance of the coupling transformer referred to CMC side and reactance of input filter reactors

R: Total series resistance including internal resistance of the coupling transformer referred to CMC side and internal resistance of the input filter reactors

Vc: Fundamental component of the CMC AC voltage

Ic: Fundamental component of the CMC line current

θ: Phase angle between $\vec{V}_c$ and $\vec{I}_c$

δ: Power angle between $\overrightarrow{V'_s}$ and $\vec{V}_c$.

Z: Impedance angle, $\tan^{-1}(X/R)$

Ps, Qs: Active and reactive power inputs to T-STATCOM at PCC

Pc, Qc: Active and reactive power inputs to CMC

ABBREVIATIONS

FACTS	Flexible AC Transmission Systems
SVC	Static VAr Compensators
STATCOM	Static Synchronous Compensators
SC	Synchronous Condensers
TCR	Thyristor Controlled Reactor
D-STATCOM	Distribution type STATCOM
GTO	Gate Turn-off thyristors
IGBT	Insulated Gate Bipolar Transistors
IEGT	Injection Enhanced Insulated Gate Transistor
IGCT	Integrated Gate Commutated Thyristors
MV	Medium Voltage
T-STATCOM	Transmission type STATCOM
MC	Multilevel Converter
DCMC	Diode Clamped Multilevel Converters
FCMC	Flying Capacitor Multilevel Converters
CMC	Cascaded Multilevel Converters
HB	H-Bridge
THD	Total Harmonic Distortion
PCC	Point of Common Coupling
TDD	Total Demand Distortion
SHEM	Selective Harmonic Elimination Method
CSS	Conventional Selective Swapping
MSS	Modified Selective Swapping
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
RCVT	RC Type Voltage Transformer

CHAPTER 1

INTRODUCTION

1.1 Overview

Flexible AC Transmission Systems (FACTS) has been defined by the IEEE [1] as a power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability. Nowadays, FACTS are being increasingly used in power systems, to enhance the system utilization and power transfer capacity as well as the stability, security, reliability and power quality of AC system interconnections.

In general, FACTS controllers can be divided into three categories:

1. Series controllers,

2. Shunt controllers

3. Combined series-shunt controllers.

Among FACTS controllers, the shunt controllers have widely been used because of their problem-solving capabilities from transmission to distribution levels. It is well known that by using appropriate amount of compensated reactive current or power, the transmitted power carrying capacity can be increased and the voltage profile of the transmission line can be controlled. Also, shunt controllers can improve transient

stability, and damp power oscillations for the interconnected transmission networks. For distribution networks, they are mainly used for the purposes of power factor correction, flicker mitigation, load balancing and harmonic mitigation.

Shunt controllers can be classified as Static VAr Compensators (SVC) and Static Synchronous Compensators (STATCOM). SVCs use synchronously connected inductor and/or capacitor banks and absorb/generate controllable reactive power. The reactive power is dependent upon the system parameters especially it is directly proportional to the source voltage and any decrease in the source voltage reduce the inductive and reactive current components as shown in Figure 1.1 and hence decreases the reactive power compensation capability of SVC system Figure 1.2 shows a practical

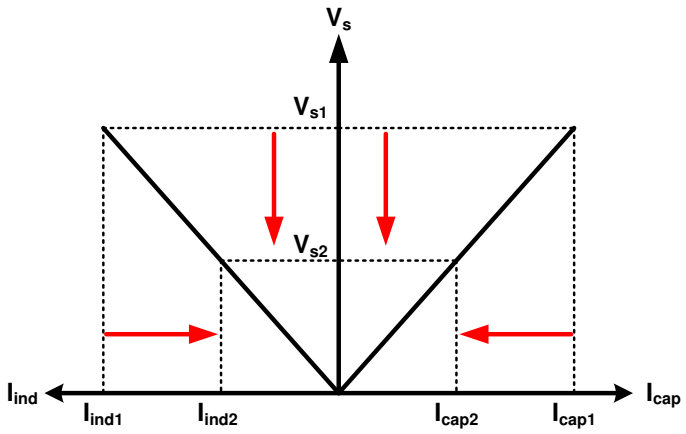


Figure 1.1 V-I characteristic of SVC systems (V_s, I_{cap} and I_{ind} are supply voltage, SVC capacitive and inductive currents, respectively)

Figure 1.2 A practical SVC System [2]

application of an SVC system composed of Thyristor Controlled Reactor (TCR) and fixed capacitor banks installed by TUBITAK-UZAY Power Electronics Department for reactive power compensation of a ladle furnace.

The concept of STATCOM employing turn-off-capability semiconductor based power converters instead of the use of inductor or capacitor banks for VAr generation was firstly disclosed by Gyugyi [3]. In view of reactive power operation, STATCOM systems look like Synchronous Condensers (SC) connected to the power grids. SC is in fact a synchronous generator operating at no load. By changing field current of the machine, the reactive power generated/absorbed is changed. If SC is over-excited by the field current, it generates capacitive reactive power while it is under-excited, it absorbs inductive reactive power. The major drawback of SCs is their relatively slow transient response against rapid load changes. STATCOM may give instant response to the rapidly changes of the power grid thanks to their power converters. Unlike SVCs, their reactive power capability is independent from the supply voltage variations and by switching power converters appropriately; reactive power is manipulated for both capacitive and inductive operating regions. The V-I

characteristics of STATCOM and a practical Distribution type STATCOM (D-STATCOM) system are shown in Figure 1.3 and Figure 1.4, respectively.

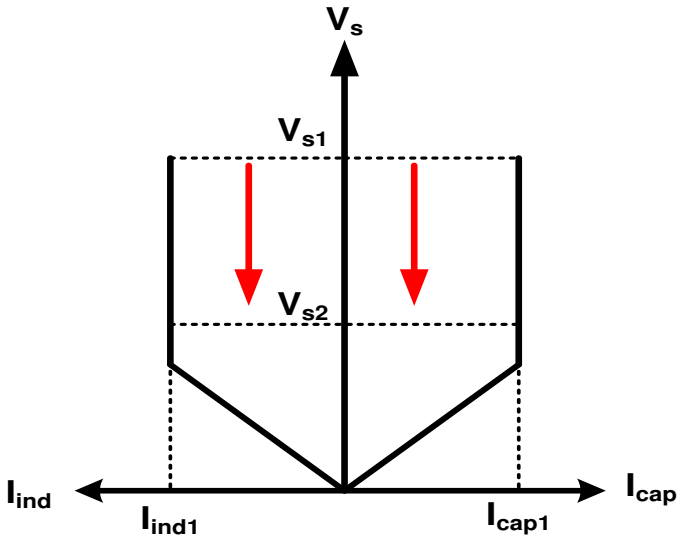


Figure 1.3 V-I characteristic of STATCOM systems (V_s, I_{cap} and I_{ind} are supply voltage, STATCOM capacitive and inductive currents, respectively)

Figure 1.4 A practical D-STATCOM System [4]

Since 1980's, Static Synchronous Compensator (STATCOM) systems have been increasingly used in the transmission, distribution, and utilization of electrical energy [5-27].Some practical applications of STATCOMs are presented in Table 1.1.

Table 1.1 Some practical applications of STATCOM systems

System	Ratings	Converter Topology	Semiconductor Switch
Static VAR Generator, Japan, 1980	20MVA/77kV	Multipulse/2-level Voltage Source Converter (VSC)	Conventional fast switching thyristor (SCR)
Static VAR Generator, Japan, 1993	80MVA/154kV	Multipulse/2-level VSC	Conventional fast switching thyristor (SCR)
TVA STATCON, Tennessee, 1995	±100MVAr/161kV	Multipulse/2-level VSC	4.5kV/4.0kA GTO
Seattle Iron&Metals D-STATCOM, Washington, 1999	5MVA/4.16kV	2-level VSC	1.2kV/0.6kA IGBT
Henan STATCOM, China, 1999	20MVA/220kV	Multipulse/2-level VSC	4.5kV/4.0kA GTO
VELCO STATCOM, Vermont-USA, 2001	2x43MVA/115KV	2-level VSC	6.0kV/6.0kA GTO
SDG&E Talega STATCOM, California, 2002	±100MVAr/138kV	2-level VSC	6.0kV/6.0kA GTO
STATCOM Based Relocatable SVC, England, 2001	±75MVAr/275kV and 400kV	Cascaded Multilevel Converter (CMC), Δ-Connected	6.0kV/6.0kA GTO
Convertible Static Compensator, New York, 2003	2x(±100MVAr)/ 345 kV	3-level Diode Clamped Multilevel Converter (DCMC)	Series operation of GTOs
Shinkansen STATCOM, Japan, 2003	60MVA/ 77kV	2-level VSC	Series operation of 2.5kV/1.8kA Flat Packaged IGBTs
Holly STATCOM, Texas, 2004	±95MVAr/138kV	3-level Diode Clamped Multilevel Converter (DCMC)	Series operation of 2.5kV/1.8kA Press-Pack IGBTs
Tinaz STATCOM, Muğla, 2005	±0.75MVAr/36 kV	2-level Current Source Converter (CSC)	4.5kV/4.0kA IGCT
SVC Plus, New Zeland, 2009	2x(±50MVAr)/ 220 kV	Modular Multilevel Converter (MMC)	Press-Pack IGBT

In these practical STATCOM systems implemented in the field, various power semiconductors have been employed i.e., silicon-controlled rectifiers (conventional fast switching thyristors) [5], Gate Turn-off thyristors (GTO) [6,7,9-11,14], Insulated Gate Bipolar Transistors (IGBT) [8,12,13,15,16,19-22,26,27], Injection Enhanced Insulated Gate Transistor (IEGT) [15] and Integrated Gate Commutated Thyristors (IGCT) [18,23-25]. Two-level, six-pulse bridge converters with relatively high switching frequencies and relatively low installed capacities are usually being the characteristics of Distribution type STATCOM (D-STATCOM) systems [18, 23-25]. These are usually connected to the Medium Voltage (MV) load bus via a step-up coupling transformer. However, Transmission type STATCOM (T-STATCOM) systems have much higher installed capacities and therefore the power semiconductors in their converter system/s should be switched at lower frequencies. That is why in practical applications of T-STATCOM systems either multi-pulse converters based on two-level six-pulse bridge [5-7,9,15] or three-level Neutral Point Clamped (NPC) [17] converters with inter-magnetics or Multilevel Converter (MC)s [10-14,16,18,19-21] are to be utilized. Cascaded Multilevel Converter (CMC)s [12,20-22], and Diode Clamped Multilevel Converter (DCMC)s [10,11,13,14,16,18,19] are generally employed in field prototypes or commercial types of T-STATCOM applications. These systems are connected to the High Voltage (HV) or extra high voltage (EHV) buses of the transmission systems via coupling transformers.

Various topologies, modulation methods, control techniques and application areas of MCs are reviewed in [28-33]. In literature, Multilevel Converters for T-STATCOM applications are classified in three groups:

a) Diode Clamped Multilevel Converters (DCMC),

b) Flying Capacitor Multilevel Converters (FCMC),

c) Cascaded Multilevel Converters (CMC).

The single line diagram and the output voltage waveform of the 5-level DCMC and FCMC are given in Figure 1.5 and Figure 1.6. In DCMC, clamping diodes are used to divide up the DC link voltage for the voltage levels by using series capacitors. The clamping diodes balance out the voltage sharing between the semiconductor switches which are not triggered into conduction. To have the same reverse voltage blocking capability, series operation of clamping diodes are employed. As the number of level increases for the DCMC output voltage, the number of clamping diodes also increases. Due to this fact, DCMC is impractical for high voltage high applications.

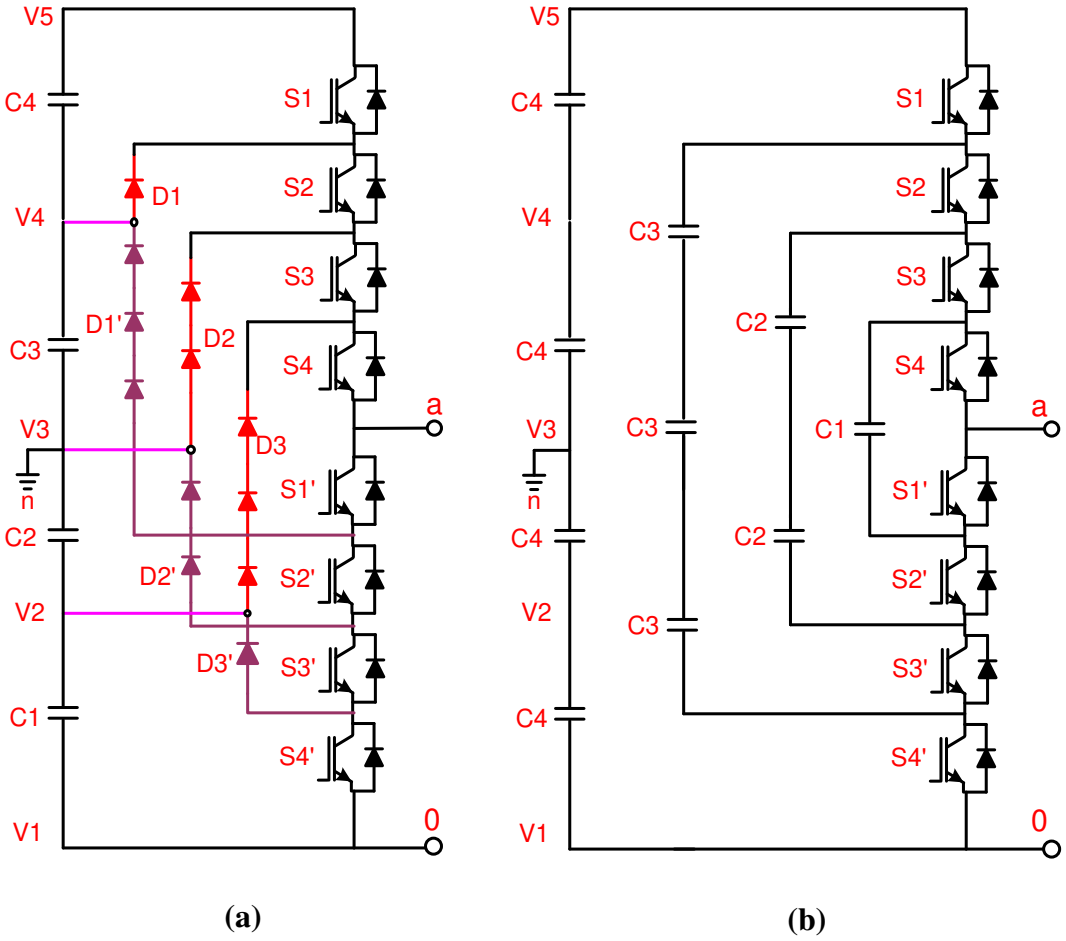


Figure 1.5 One phase single line diagrams of 5-level a) DCMC and b) FCMC

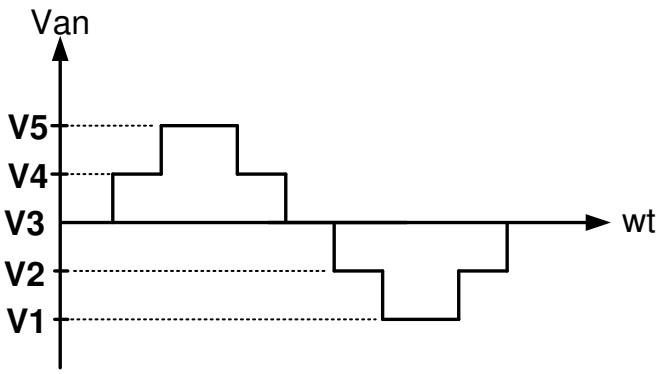


Figure 1.6 The output voltage waveform of 5-level DCMC and 5-level FCMC

In FCMC, instead of clamping diodes in DCMC, clamping capacitors are used in addition to the main DC link capacitors to obtain a staircase output voltage waveform shown by Figure 1.6. By using proper clamping capacitor combinations, it is possible to control the charging of clamping capacitors. As the number of level increases, the number of clamping capacitors increases as well.

To obtain 5-level output voltage waveform shown in Figure 1.6, two series connected H-Bridge (HB) circuits as shown in Figure 1.7 are used. The multilevel converter topology based on the series connection of HBs is called Cascaded Multilevel Converter (CMC). Since CMC topology is based on H-Bridge (HB) circuits connected in series, it has the advantage of modularity and flexibility. Modularized circuit layout and packaging is possible due to the usage of the same structure for each level and there is no need to use clamping diodes or capacitors required for DCMC and FCMC. The modular structure also gives the opportunity to adjust the number of output voltage levels easily by changing only the number of HBs in series.

The comparison of M-level DCMC, FCMC and CMC is given in Table 1.2 in accordance with the number of total power components needed for 3-phase application. The voltage ratings of the devices are taken as equal to have a fair comparison among the converter topologies.

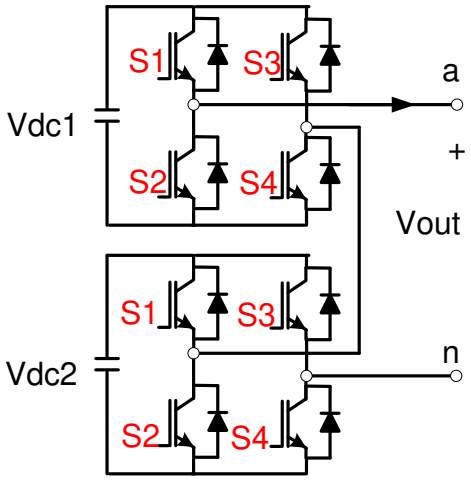


Figure 1.7 One phase single diagram of 5-level CMC

Table 1.2 The total number of required power components for M-level DCMC, FCMC and CMC

M-level Converter Topology			
Converter Type	**DCMC**	**FCMC**	**CMC**
Number of Switching Device	3x2x(M-1)	3x2x(M-1)	3x2x(M-1)
Number of DC Link Capacitors	M-1	M-1	3x(M-1)/2
Number of Clamping Diodes	3x(M-1)x(M-2)	0	0
Number of Clamping Capacitors	0	3x(M-1)x(M-2)/2	0

Although it requires more main DC link capacitors, the least number of needed power components is achieved by the utilization of M-level CMC as can be seen from Table 1.2. A very high amount of the total capacitance is required for the

FCMC topology. This is unacceptable for high voltage levels due to the equalization problem of capacitors as well as the high cost. In DCMC topology with higher levels than three-level configuration, oversized capacitors or complex balancing circuits and methods should be employed in high voltage-high power applications for the equalization problem of DC link capacitors. The usage of series connected clamping diodes also yields the need of voltage sharing circuits which complicates the packaging of practical applications. Due to its modularity, flexibility and less number of power components, CMC topology is the most promising alternative for T-STATCOM applications among the multilevel converters. It is possible to reach high voltage levels by the use of more HBs in series for CMC topology. The only problem is the balancing of the individual DC link capacitor voltages of each HB. This problem can be overcome by employing some equalization methods.

The major operational problem of CMCs is the equalization of DC link capacitor voltages. The equalization of DC link capacitor voltages are investigated and some novel strategies are recommended in [34-52] for various CMC topologies. Commercial CMC-based T-STATCOMs employ either GTO or GCT/IGCT devices with inverse-parallel connected power diodes. To limit di/dt overvoltages on GTOs during turn-off operation, bulky snubber circuits were used [12]. To equalize individual capacitor voltages, high frequency IGBT based auxiliary circuits supplied from low voltage side were employed. Specially designed isolating transformers were used to isolate auxiliary circuits from the power stage of CMC.

An important contribution to the solution of voltage equalization problem of DC link capacitors is known as the Selective Swapping Algorithm [50-52] which can be embedded in the control algorithm of CMC, thus eliminating the need for bulky auxiliary circuits. Although the effectiveness of voltage equalization algorithm decreases as the number of H-bridges connected in series and/or peak-to-peak ripple content of the capacitor voltage increase/s, it provides the lowest switching frequency for the power semiconductors.

1.2 Scope of the Thesis

This research and technology development work deals with the sizing, system and power-stage designs of an HV IGBT based CMC for T-STATCOM applications. System design and the number of H-Bridge (HB)s in each phase of the Y-connected CMC are achieved in view of Total Harmonic Distortion (THD) at Point of Common Coupling (PCC), and also of Total Demand Distortion (TDD) of the line currents and individual harmonic current limits recommended by IEEE Std.519-1992. A 12 kV, ±10 MVAr, 11-level CMC Module power stage with five HBs in each phase is designed and then implemented to deliver ±10MVAr to 154kV transmission bus (PCC) via a series filter reactor and 154/10.5kV coupling transformer. Therefore, the CMC Module presented in this work constitutes the building block of large T-STATCOM systems. The Selective Harmonic Elimination Method (SHEM) is applied to synthesize T-STATCOM voltage waveforms at power frequency (50Hz) and the Modified Selective Swapping (MSS) Algorithm is exercised to balance the DC link capacitor voltages, perfectly at the expense of higher switching frequency, and hence switching losses. The power stage is carefully designed and its performance is optimized in view of the current HV IGBT technology.

A 154kV, ±50 MVAr, 11-level T-STATCOM system by the parallel use of five CMCs built in this work has been implemented in the field primarily for the purposes of reactive power compensation and terminal voltage regulation, and secondarily for power system stability. Since the operating voltage of CMC is chosen to be 10.5 kV (max.12 kV) line-to-line, it is connected to 154 kV line-to-line transmission bus through a specially designed 50/62.5 MVA Y-Y connected (YNyn vector group) coupling transformer and each CMC module is connected to the secondary side of the coupling transformer via a series filter reactor bank.

This research work has made the following original contributions to the area of Cascaded Multilevel Converter based Transmission STATCOM Systems:

- Optimized design for the sizing, system and power stage of Cascaded Multilevel Converter based T-STATCOM systems has been investigated.
- A 12kV, ±10MVAr HV IGBT based CMC has been designed and implemented as a building block of large T-STATCOM systems. Then, a 154kV, ±50MVAr Transmission STATCOM system based on five of this CMC is implemented in the field for the purposes of reactive power compensation and terminal voltage regulation as well as power stability improvement [21].
- The effect of total series inductance on system design has been investigated in details.
- The Conventional Selective Swapping (CSS) Method has been modified and the effect of swapping time on the system performance has been exercised. The comparison of Conventional and Modified Selective Swapping Algorithms has also been presented by the computer simulations and field results.
- The switching strategies have been discussed for Selective Swapping Methods and alternatives for eliminating or reducing the voltage spikes as a result of swappings have also been declared.
- This is the first application of CMC based T-STATCOM with wire-bond HV IGBTs and Modified Selective Swapping (MSS) Algorithm in the world. Thanks to MSS method, the usage of bulky auxiliary circuits for equalization of the DC link voltages has been eliminated and a compact H-Bridge (HB) unit has been designed and implemented.

The outline of the thesis is given below:

In Chapter 2, operation principles of the Cascaded Multilevel Converter based T-STATCOM systems have been discussed in detail. Active and Reactive power control with waveform synthesizing used for STATCOM systems are clearly presented. Moreover, the methods proposed in the literature for the equalization

problem of DC link capacitors used for CMCs have been reviewed with the details of the Modified Selective Swapping Algorithm.

Chapter 3 presents the system design and sizing for CMC and T-STATCOM systems. The major considerations for determining the connection point of T-STATCOM systems are given in view of Total Harmonic Distortion (THD) at Point of Common Coupling (PCC), Total Demand Distortion (TDD) of the line currents and individual harmonic current limits recommended by IEEE Std.519- 1992. Also, the effect of total series inductance on the system performance has been investigated in detail.

The design issues including HB circuit, control system and switching strategies for the application of selective swapping methods for Cascaded Multilevel Converters have been presented in Chapter 4. The choice of power semiconductors and capacitors used in each HB are given with the design details of the laminated busbar with 3-conducting layer.

In Chapter 5, the system implementation with the field performance results have been demonstrated. The waveforms and technical results of the system performance have been given.

Conclusions and recommendations for the future work are given in Chapter 6. All the theoretical and practical considerations of the thesis study is justified and concluded in this chapter once more.

CHAPTER 2

OPERATING PRINCIPLES OF CMC BASED TRANSMISSION STATCOM

2.1 System Description

Figure 2.1 shows single line diagram of a Transmission type Static Synchronous Compensator (T-STATCOM) based on a single Cascaded Multilevel Converter (CMC). It is shown to be connected to Extra High Voltage (EHV) or High Voltage (HV) busbar of the transmission system via a medium voltage (MV) to EHV or HV coupling transformer. Therefore, in Figure 2.1, X_r represents the total leakage reactance of

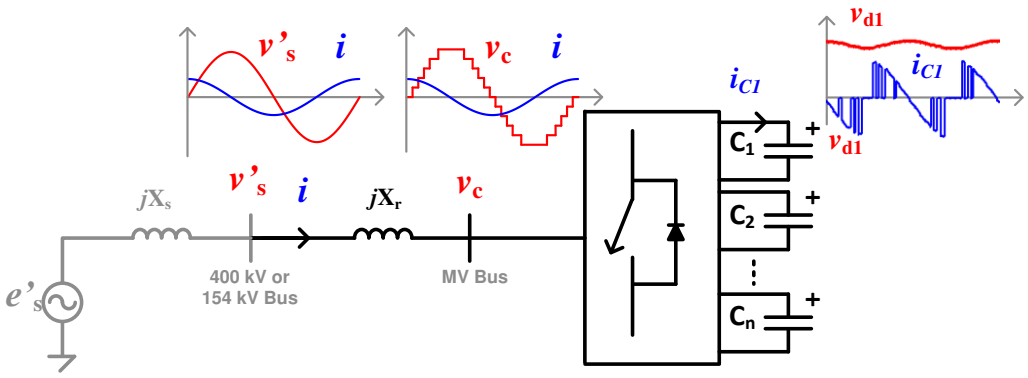


Figure 2.1 Single line diagram of a T-STATCOM based on a single CMC

the coupling transformer and if needed the reactance of the series filter reactor. Waveforms of EHV or HV bus voltage, v_s', line current of T-STATCOM, i, AC voltage of the CMC, v_c, voltage of each DC link capacitor, v_{d1} , and the current through each DC link capacitor, i_{C1} are also sketched on Figure 2.1. e_s', X_s' and v_s' are respectively internal source voltage, source reactance and EHV or HV bus voltage all referred to the CMC side.

Circuit diagram of star-connected CMC consisting of ***n*** number of series connected H-Bridges (HBs) in each phase is as shown in Figure 2.2. ***n*** seriesly connected H-Bridges give ***l*=2n+1** steps in line-to-neutral voltage waveforms and ***l*=4n+1** steps in line-to-line voltage waveforms, where ***l*** is the number of levels from positive peak to negative peak of the waveform under consideration. The DC link of each HB in the CMC is equipped with a DC/DC converter controlled discharge resistor (R) to discharge C when the CMC is disconnected from the supply for inspection or maintenance purpose. L_r is the equivalent inductance of the total filter reactance, X_r, in Figure 2.1. A T-STATCOM system operates at power frequency (50Hz or 60Hz) as a shunt connected Flexible AC Transmission System (FACTS) device and performs one or more than one of the following functions at the EHV or HV bus to which the T-STATCOM is connected:

a. Terminal Voltage Regulation
b. Control of Reactive Power Flow in O/H Lines
c. Power System Stability Improvement

These are achieved by continuously varying the reactive power generated by the T-STATCOM in both capacitive and inductive regions as will be described in the forgoing sections.

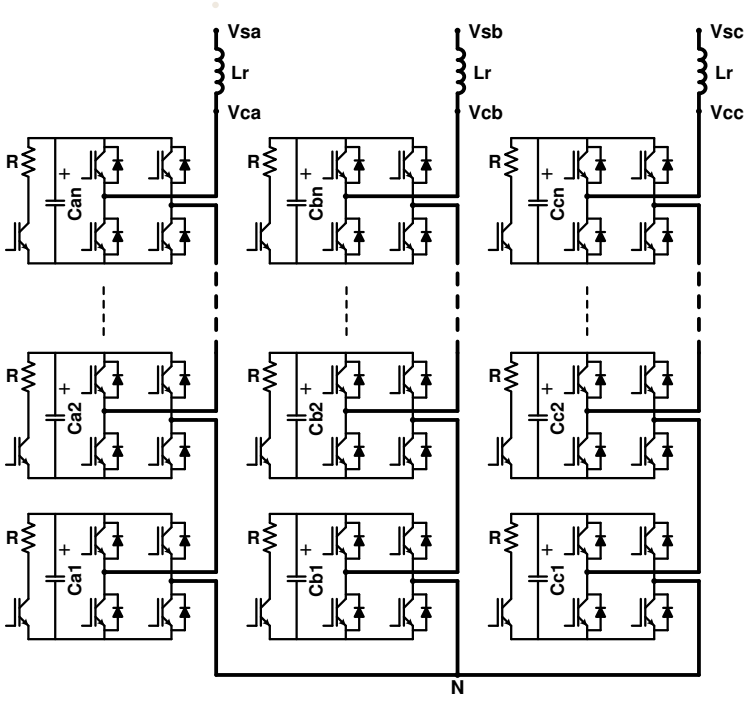


Figure 2.2 Circuit diagram of a star-connected CMC consisting of n series connected HBs in each phase

2.2 Active and Reactive Power Control

Single-phase Y-equivalent circuit model of the T-STATCOM and its phasor diagram are given in respectively in Figure 2.3 and Figure 2.4, where:

E_s': Internal source voltage referred to CMC side

X_s': Internal source reactance referred to CMC side

PCC: Point of Common Coupling

V_s': Fundamental voltage component at Point of Common Coupling (PCC) referred to CMC side

X: Total series reactance including leakage reactance of the coupling transformer referred to CMC side and reactance of input filter reactors

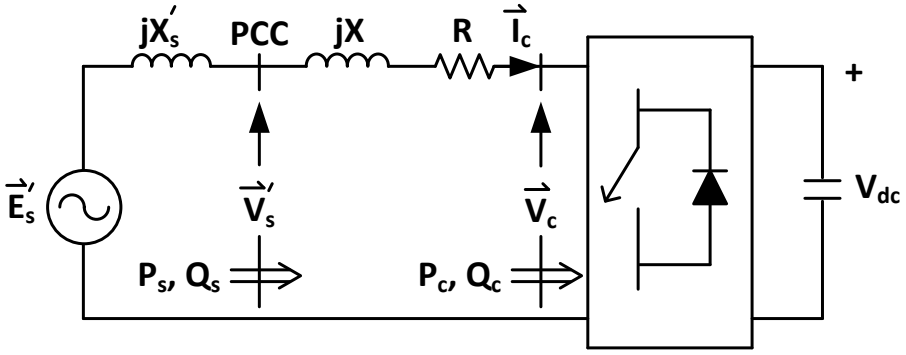


Figure 2.3 Simplified single line diagram of T-STATCOM

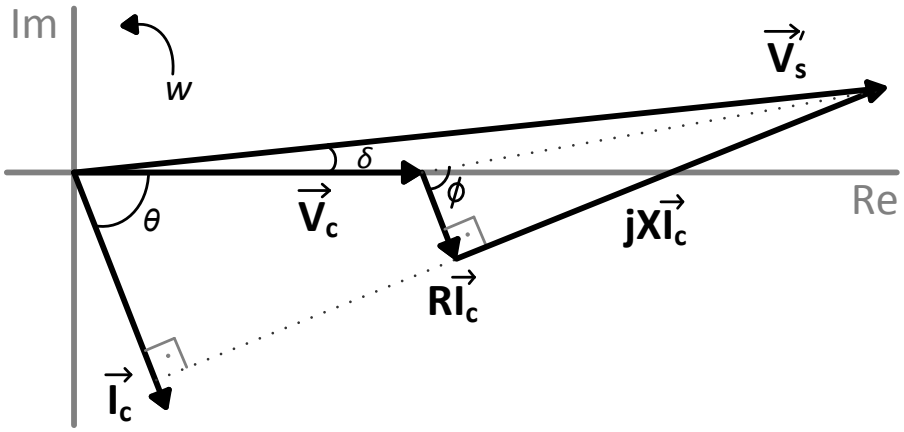


Figure 2.4 Phasor diagram for lossy system (exaggerated)

R: Total series resistance including internal resistance of the coupling transformer referred to CMC side and internal resistance of the input filter reactors

V_c: Fundamental component of the CMC AC voltage

I_c: Fundamental component of the CMC line current

θ: Phase angle between $\vec{V}_c$ and $\vec{I}_c$

δ: Power angle between $\overrightarrow{V'}_s$ and $\vec{V}_c$

ϕ: Impedance angle, $\tan^{-1}$(X/R)

P_s, Q_s: Active and reactive power inputs to T-STATCOM at PCC

P_c, Q_c: Active and reactive power inputs to CMC

The definitions of θ and δ are expressed by the aid of Figure 2.5.

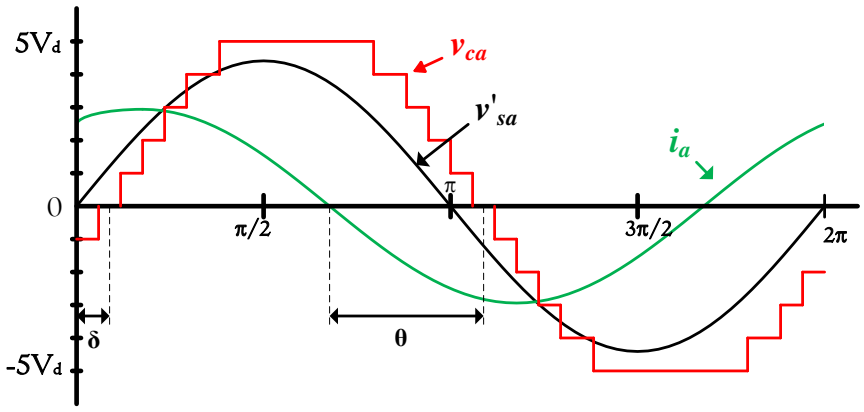


Figure 2.5 The definitions of δ and θ

In Figure 2.4, all voltages and currents are fundamental values and active and reactive powers are per phase values. P_s, P_c, Q_s and Q_c in Figure 2.3 can be expressed respectively as in (1.1)-(1.4), in terms of terminal quantities V_s' and V_c and angles θ and δ without consideration of harmonic components due to their negligible effects.

$$P_s = V'_s I_c \cos(\theta + \delta) \quad (1.1)$$

$$P_c = V_c I_c \cos\theta \quad (1.2)$$

$$Q_s = V'_s I_c \sin(\theta + \delta) \quad (1.3)$$

$$Q_c = V_c I_c \sin\theta \quad (1.4)$$

Since $\vec{V}_c = V_c \angle 0, \vec{I}_c = I_c \angle(-\theta), \overrightarrow{V'_s} = V'_s \angle\delta$;

T-STATCOM Current is $\vec{I}_c = \left(\overrightarrow{V'_s} - \vec{V}_c\right)/(R + jX)$. (1.5)

Complex power input to T-STATCOM:

$$\vec{S}_s = P_s + jQ_s = \overrightarrow{V'_s}\vec{I}_c^{\,*} \quad (1.6)$$

$$\vec{S}_s = \overrightarrow{V'_s}\left(\overrightarrow{V'_s} - \vec{V}_c/R + jX\right)^* = (V'^2_s - V'_s V_c(\cos\delta + j\sin\delta))/(R - jX) \quad (1.7)$$

Multiplying numerator and denominator by *(R+jX)*:

$$\vec{S}_s = (V'^2_s R + jV'^2_s X - V'_s V_c[R\cos\delta - X\sin\delta + j(R\sin\delta + X\cos\delta)])/Z^2 \quad (1.8)$$

where, $Z = \sqrt{(R^2+X^2)}$.

Real power input to T-STATCOM:

$$P_s = Re\{\vec{S}_s\} = (V'_s[V_c X\sin\delta - V_c R\cos\delta + V'_s R]/Z^2) \quad (1.9)$$

Reactive power input to T-STATCOM:

$$Q_s = Im\{\vec{S}_s\} = (V'_s[V'_s X - V_c X\cos\delta - V_c R\sin\delta]/Z^2) \quad (1.10)$$

Complex power input to CMC:

$$\vec{S}_c = P_c + jQ_c = \vec{V}_c\vec{I}_c^{\,*} \quad (1.11)$$

$$\vec{S}_c = \vec{V}_c\left(\overrightarrow{V'_s} - \vec{V}_c/R + jX\right)^* = (V'_s V_c(\cos\delta - j\sin\delta) - V_c^2)/(R - jX) \quad (1.12)$$

Multiplying numerator and denominator by *(R+jX)*:

$$\vec{S}_c = (V'_s V_c[R\cos\delta + X\sin\delta + j(X\cos\delta - R\sin\delta) - V_c{}^2 R - jV_c{}^2 X])/Z^2 \quad (1.13)$$

Real power input to CMC:

$$P_c = Re\{\vec{S}_c\} = (V_c[V'_s X\sin\delta + V'_s R\cos\delta - V_c R]/Z^2) \quad (1.14)$$

Reactive power input to CMC:

$$Q_c = Im\{\vec{S}_c\} = (V_c[V'_s X\cos\delta - V_c X - V'_s R\sin\delta]/Z^2) \quad (1.15)$$

P_c can be related to P_s in terms of power dissipation on R as in (1.16). In a similar way, Q_c can be related to Q_s in terms of the reactive power absorbed by X.

$$P_c = P_s - I_c{}^2 R \quad (1.16)$$

$$Q_c = Q_s - I_c{}^2 X \quad (1.17)$$

Since $I_c{}^2R$ plays no basic part in the control of reactive power and since R is small in comparison with X, R in Figure 2.3 and in (1.9)–(1.10) and (1.14)-(1.15) will be neglected. According to this assumption active power, P transferred between $\overrightarrow{V'}_s$ and $\vec{V}_c$ can be expressed as in (1.18).

$$P = P_s = P_c = (V'_s V_c/X)\sin\delta \quad (1.18)$$

P is very small during the operation of the VSC in the steady state, to supply only the CMC losses and hence δ takes a very small value (δ is around 0.017 rad ≡ 1 degree). For such small values of δ, Sinδ≈δ holds and hence P can be approximated by (1.19):

$$P = (V'_s V_c/X)\delta \quad (1.19)$$

By substituting R=0, (1.10) and (1.15) will reduce respectively to (1.20) and (1.21).

$$Q_s = (V'_s[V'_s - V_c\cos\delta]/X) \quad (1.20)$$

$$Q_c = (V_c[V'_s\cos\delta - V_c]/X) \quad (1.21)$$

Since δ is very small, Cosδ≈1 holds. Hence (1.20) and (1.21) can be approximated to (1.22) and (1.23), respectively.

$$Q_s = (V'_s[V'_s - V_c]/X) \tag{1.22}$$

$$Q_c = (V_c[V'_s - V_c]/X) \tag{1.23}$$

Complex power input, $\vec{S} = P + jQ_s$ to the T-STATCOM is defined according to power sink convention. P is always positive in the steady-state to compensate for coupling transformer, series filter reactor and CMC losses. However, the sign of Q_s depends upon the operation mode of the T-STATCOM, i.e. positive for inductive mode of operation and negative for capacitive mode. θ is positive (≈+π/2) for inductive mode of operation in the steady state while it is negative (≈-π/2) for capacitive mode. The transition between capacitive and inductive mode of operations occurs when $Q_c = {I_c}^2 X$, which corresponds to unity power factor (*pf*) operation of the T-STATCOM at PCC.

Active power into the T-STATCOM is controlled by varying δ in order to keep the DC link capacitor voltages constant at a pre-specified value over the entire operating range in both transient-state and steady-state. δ is always positive in the steady-state under the assumption of R=0. However, δ may have negative values for inductive operation mode of the T-STATCOM ($V_s' > V_c$) when R is not neglected. This occurs for very small values of δ and even for a practical X/R ratio. This phenomenon is apparent from (1.9) and (1.14). This small negative value for δ does not reverse the direction of real power flow for the operation of the system given in Figure 2.3 in the steady-state. For capacitive operation mode however, since $V_s' < V_c$; δ is always positive as can be understood from (1.9) and (1.14).

Q_s and Q_c are controlled by varying V_c by PWM technique. If V_c is made smaller than V_s', T-STATCOM operates in inductive operation mode as can be understood from (1.23). On the other hand, if V_c is made sufficiently higher than V_s', it starts to operate in capacitive operation mode and delivers reactive power to the supply. In practice, the situation is more complex, because the supply is not an infinite bus. That is, the capacitive operation mode causes a rise in the supply voltage, V_s', while the inductive operation, a drop. Figure 2.6 shows the inductive and capacitive modes of operation by illustrating AC output voltage of CMC.

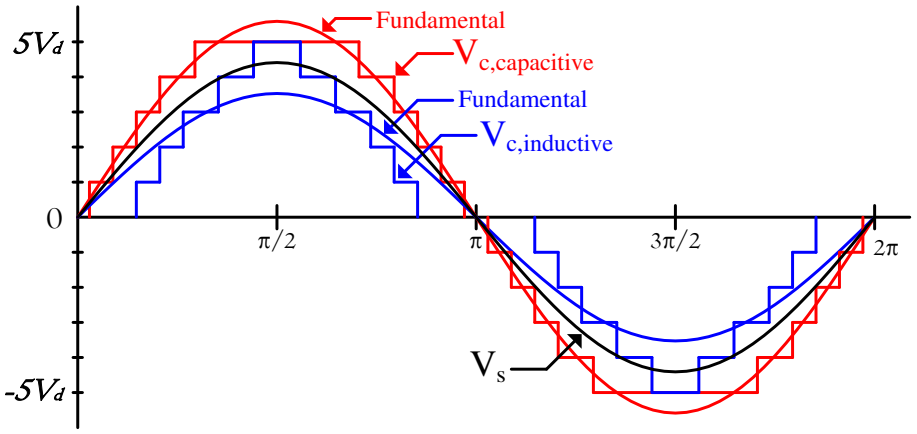


Figure 2.6 Sample line-to-neutral voltage waveforms at the supply side and CMC side (Theoretical)

2.3 Wave Shaping

The input voltage waveform of Cascaded Multilevel Converter (CMC), $V_c(t)$ will be approximated to a pure sinusoidal voltage at supply frequency by using the CMC topology and Selective Harmonic Elimination Method (SHEM). It is well known that

the number of voltage levels, ***l***, in the staircase voltage waveform in Figure 2.2 produced by CMC is defined by (1.24) and (1.25):

l=2n+1 in the line-to-neutral voltage (1.24)

l=4n+1 in the line-to-line voltage (1.25)

where, ***n*** is the number of HBs in one phase. As an example, in the CMC described in this work, five HBs are connected in series in each phase to form a Y-connected multilevel converter topology. This CMC yields 11 voltage levels in the line-to-neutral voltage waveform and 21 voltage levels in the line-to-line voltage waveform.

The use of ***n*** number of HBs in each phase provides us ***n*** number of freedom in the application of SHEM as can be seen in Appendix-A for CMC having 5 HBs in series. One of them is allocated to the fundamental component while ***n-1*** is for the elimination of low order harmonics. For a star-connected CMC, the number of steps in line-to-neutral voltage waveforms (***l=2n+1***), the number of steps in line-to-line voltage waveforms (***l=4n+1***), and the odd harmonics that will be eliminated in line-to-neutral voltage waveforms by SHEM are given in Table 2.1 as a function of number of HBs, ***n*** in each phase. The optimum angles $\theta_1,\theta_2,\ldots,\theta_n$ in [21],[48] which define starting and end points of each pulse in the staircase line-to-neutral voltage waveform of CMC to give minimum harmonic content and hence minimum THD values are calculated off-line by using a hybrid algorithm . The hybrid algorithm is a combination of the genetic algorithm [49], [53] and the gradient based method. First, the genetic algorithm is used for determination of proper initial conditions. Then, these initial conditions are applied to the gradient based method to reach the global minima much faster than the use of genetic algorithm only. These calculations are repeated several times for different modulation indices, M, to cover the whole operating range of the CMC and then stored in a look-up table as described in [21]. Optimum values of $\theta_1,\theta_2,\ldots,\theta_n$ are obtained for different modulation index values so that -Q MVAr to +Q MVAr reactive power control range is divided into N steps and

corresponding results are arranged as a Nx6 Look-up Table. The hybrid algorithm is applied for CMC with three, five and seven HBs to obtain optimum angles with respect to M values to give minimum THD value of line-to-neutral voltages. The obtained M ranges are [2.50-4.23], [1.15-2.52] and [3.26-5.73] with 0.01 resolution for CMC with three, five and seven HBs, respectively. Some sample results of optimum angles with respect to modulation index value, M for mentioned topologies are given Table 2.2 - Table 2.4. As can be seen from Table 2.4 for CMC having seven HBs, there are no solution for optimum angles corresponding to the M ranges of [5.14-5.17] and [5.43-5.55].

Table 2.1 Number of steps in CMC AC voltages and low order voltage harmonics eliminated as a function of number of HBs

Number of HBs, ***n***	Number of steps in voltage		l-to-n voltage harmonics eliminated, ***n-1***
	l-to-n,***l=2n+1***	l-to-l,***l=4n+1***	
3	7	13	5^{th}, 7^{th}
5	11	21	5^{th}, 7^{th}, 11^{th}, 13^{th}
7	15	29	5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}

Table 2.2 Optimum angles with respect to modulation index values for CMC having 3HBs

M	**θ_1(rad)**	**θ_2(rad)**	**θ_3(rad)**
1.15	0.717	1.165	1.570
1.16	0.715	1.159	1.566
1.17	0.713	1.153	1.563
...	**...**	**...**	**...**
2.50	0.239	0.375	0.930
2.51	0.252	0.356	0.922
2.52	0.273	0.327	0.915

As illustrated in Figure 2.7, five pulses with different widths and the same magnitudes (V_d) are to be superimposed in order to create a half-cycle of an 11-level line-to-neutral voltage waveform. This makes necessary assigning five different

Table 2.3 Optimum angles with respect to modulation index values for CMC having 5HBs

M	**θ_1(rad)**	**θ_2(rad)**	**θ_3(rad)**	**θ_4(rad)**	**θ_5(rad)**
2.50	0.620	0.794	0.998	1.208	1.482
2.51	0.621	0.792	0.997	1.204	1.478
2.52	0.621	0.790	0.996	1.200	1.474
...	**...**	**...**	**...**	**...**	**...**
4.21	0.121	0.249	0.414	0.641	1.010
4.22	0.135	0.231	0.418	0.632	1.006
4.23	0.160	0.203	0.423	0.623	1.002

Table 2.4 Optimum angles with respect to modulation index values for CMC having 7HBs

M	**θ_1(rad)**	**θ_2(rad)**	**θ_3(rad)**	**θ_4(rad)**	**θ_5(rad)**	**θ_6(rad)**	**θ_7(rad)**
3.26	0.592	0.735	0.877	1.033	1.199	1.397	1.571
3.27	0.591	0.735	0.876	1.032	1.196	1.393	1.569
3.28	0.591	0.734	0.875	1.030	1.194	1.390	1.568
...	**...**	**...**	**...**	**...**	**...**	**...**	**...**
5.14	**No solution for optimum angles**						
...							
5.17							
5.18	0.156	0.334	0.446	0.653	0.890	1.014	1.167
...	**...**	**...**	**...**	**...**	**...**	**...**	**...**
5.43	**No solution for optimum angles**						
...							
5.55							
...	**...**	**...**	**...**	**...**	**...**	**...**	**...**
5.71	0.077	0.243	0.313	0.469	0.626	0.885	1.098
5.72	0.072	0.248	0.305	0.469	0.621	0.880	1.096
5.73	0.067	0.256	0.293	0.469	0.615	0.876	1.095

angles $\theta_1,\theta_2,\ldots,\theta_5$ in such a way that the harmonic distortion of line-to-neutral voltage waveform will be minimum. 3rd harmonic and its integer multiples will not appear in the line-to-line voltage waveform. There remains only the elimination of dominant voltage harmonics which are the 5th, 7th, 11th and 13th. In a staircase waveform with odd-quarter symmetry, these are eliminated by using SHEM in the work. If a lower harmonic content were allowed in line-to-line voltage waveform, a larger series filter reactor would be needed at the expense of voltage regulation problem.

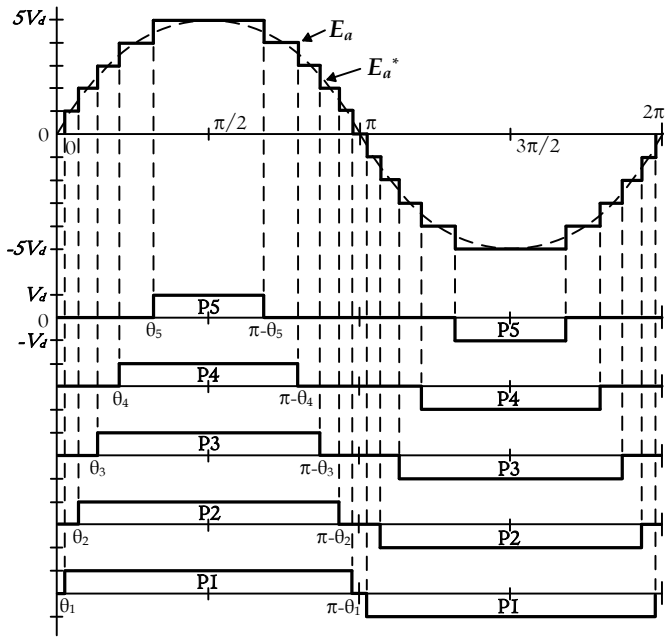


Figure 2.7 11-level line-to-neutral voltage waveform [46]

The rms value of the fundamental component of CMC output voltage V_c can be controlled by adjusting the modulation index, M according to (1.26)-(1.29):

$$V_c = V_{c(ref)} \tag{1.26}$$

$$M = V_{c(ref)}/V_{c(max)} \tag{1.27}$$

$$V_{c\,(max)} = \left(\sqrt{3/2}\right)(4/\pi)V_{dc} \tag{1.28}$$

$$V_d = (V_{dc}/n) \tag{1.29}$$

where, $V_{c(ref)}$ is the set value of fundamental line-to-line rms output voltage of the CMC determined by the controller, $V_{c(max)}$ denotes the maximum value of fundamental line-to-line rms voltage of the quasi-square wave that can be produced by an HB, V_d is the mean DC link voltage of each HB and V_{dc} is the total mean DC link voltage of each CMC phase.

Since M has been defined with respect to the AC output voltage of each HB, the above formulation yields M values greater than unity. As an example, for n=5 and $Q_{s(rated)}$ = ±10MVAr, M should be varied from 3.0 to 3.73 as will be described in Chapter 3 in the prototype of T-STATCOM developed in this work. Some sample results of EMTDC/PSCAD simulations carried out for a ±10MVAr, 10.5 kV CMC under CSS method are shown in Figure 2.8 - Figure 2.9 for inductive and capacitive operation modes, respectively. These waveforms show that 11-level line-to-neutral voltage waveforms and 21-level line-to-line voltage waveforms are successfully formed by the waveform synthesizing method used in this work. Morever, the line-to-neutral voltage waveforms of the CMC with the output voltages of five HB units in phase-A are shown in Figure 2.10 and Figure 2.11. A comparison of voltage waveforms for capacitive mode of operation with those of inductive mode shows the effects of M-control on the widths of all pulses and hence on the CMC output voltage. The widths of the HB output voltages for capacitive operation mode are wider than those for inductive operation mode. Therefore, by controlling the widths of the HB output voltages, the required CMC output voltage is obtained for both capacitive and inductive operation modes by M-control.

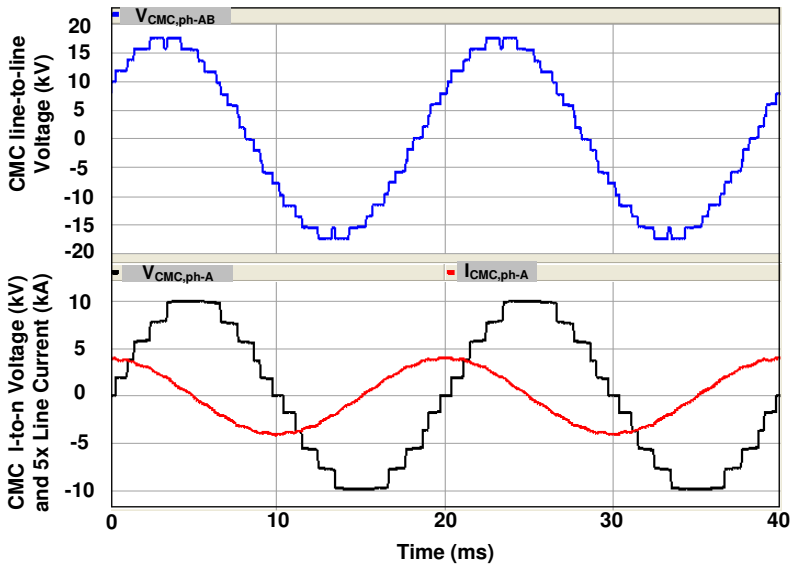


Figure 2.8 CMC line-to-line and line-to-neutral voltages with line current of phase-A for full capacitive case (CSS Method/PSCAD Simulations)

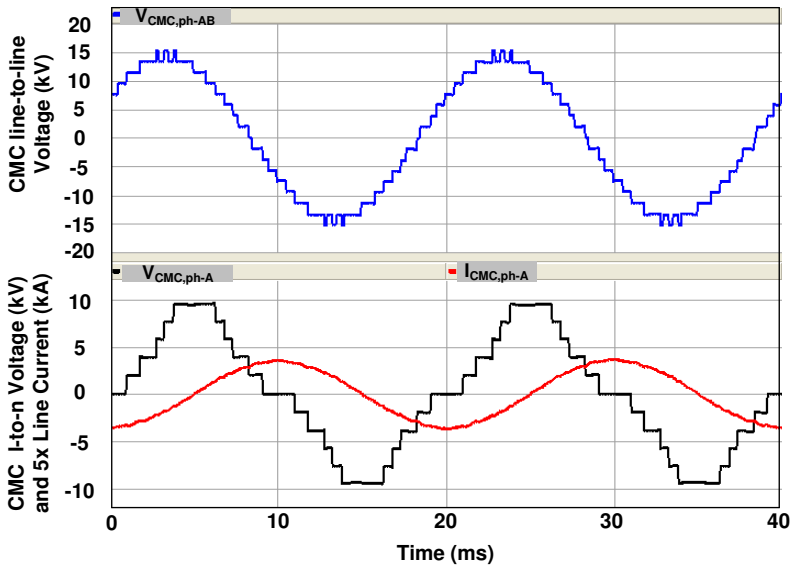


Figure 2.9 CMC line-to-line and line-to-neutral voltages with line current of phase-A full inductive case (CSS method/PSCAD Simulations)

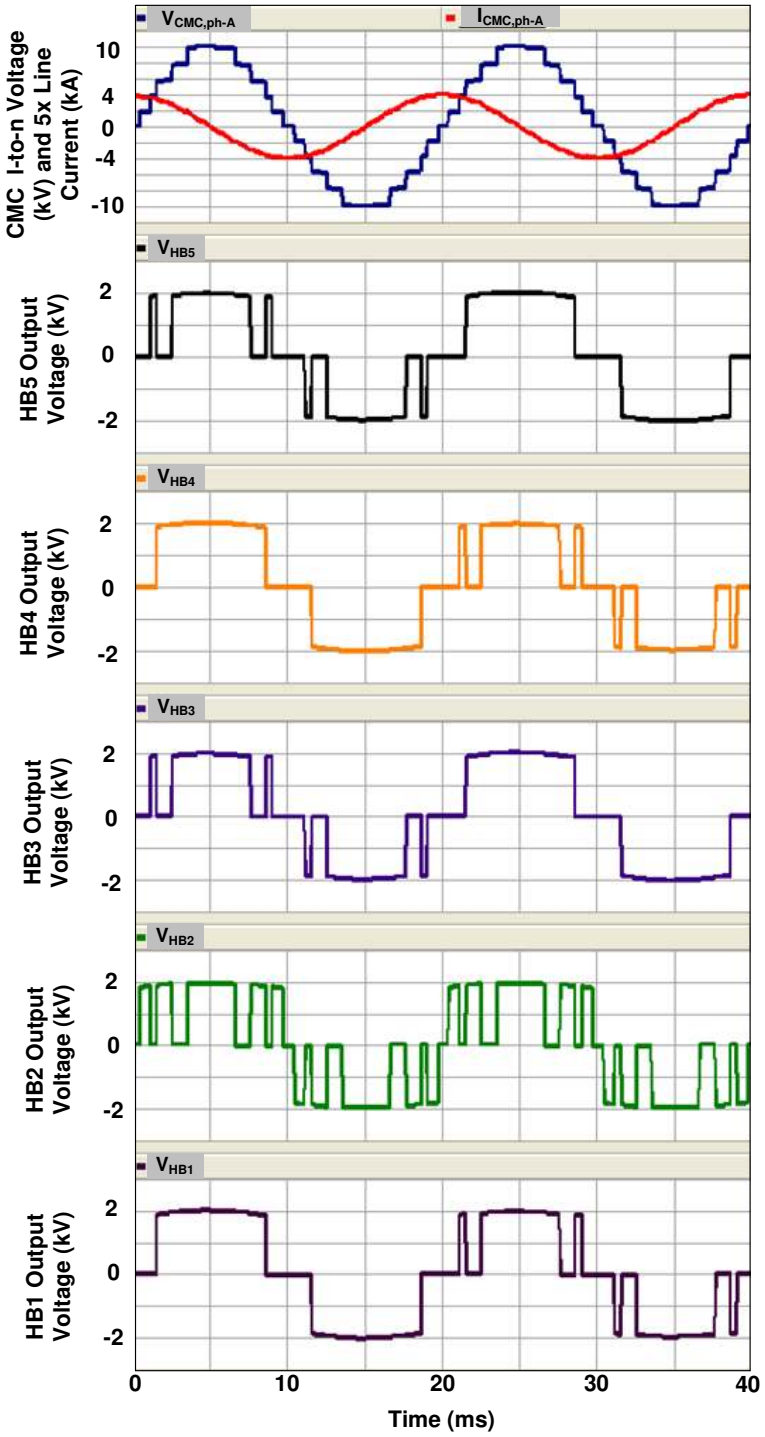


Figure 2.10 CMC line-to-neutral voltage with HB output voltages in phase-A for full capacitive case (CSS Method/PSCAD Simulations)

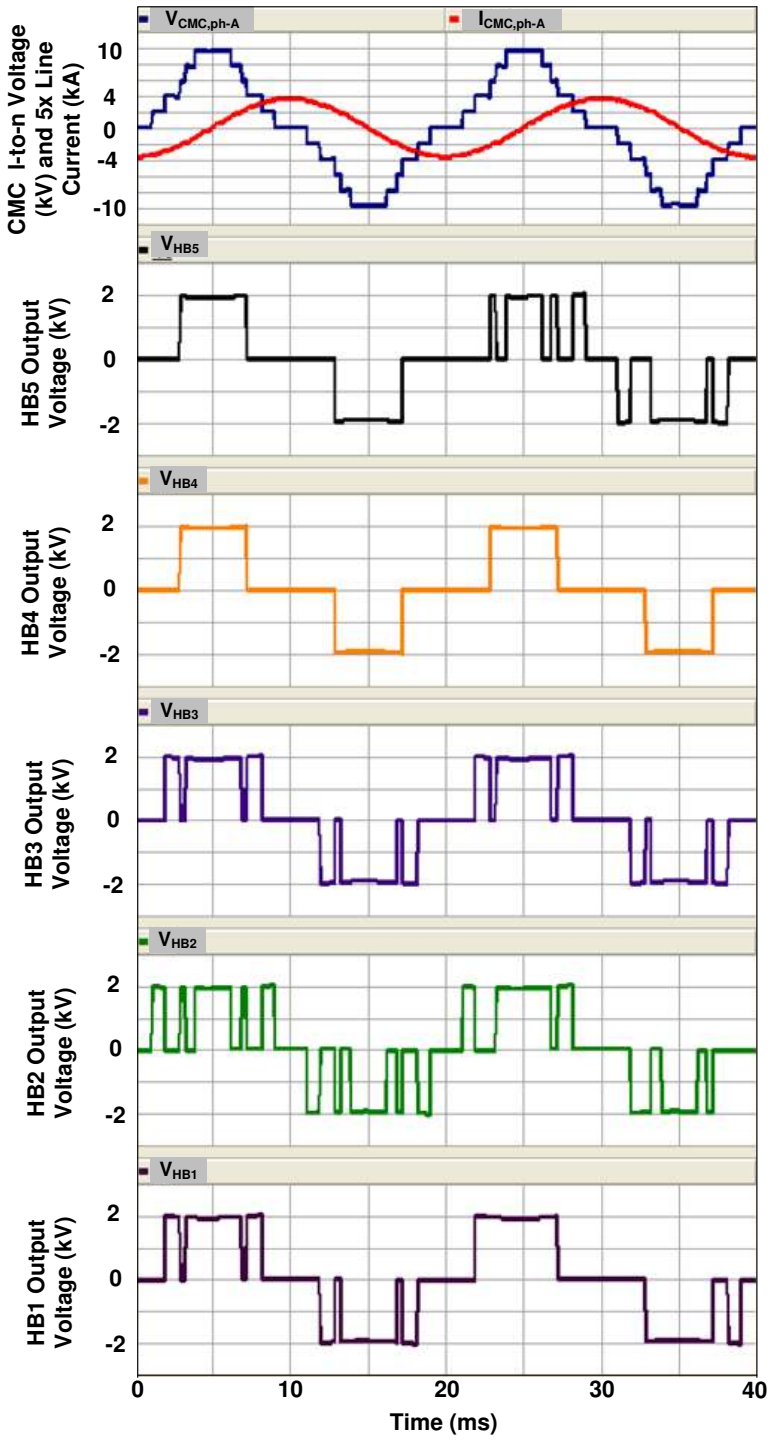


Figure 2.11 CMC line-to-neutral voltage with HB output voltages in phase-A for full inductive case (CSS Method/PSCAD Simulations)

2.4 Voltage Balancing of DC Link Capacitors

The major drawback of multilevel converters is the voltage balancing problem of DC link capacitors [34-52]. For cascaded multilevel converters, there are many methods proposed in the literature. In this work, the selective swapping method is modified and then employed for the designed prototype of T-STATCOM system.

2.4.1 Some Conventional Methods

In [12], to equalize individual capacitor voltages, high frequency IGBT based auxiliary circuits supplied from low voltage side were employed. Specially designed isolating transformers were used to isolate auxiliary circuits from the power stage of CMC. As a result, a bulky H-Bridge design were existed.

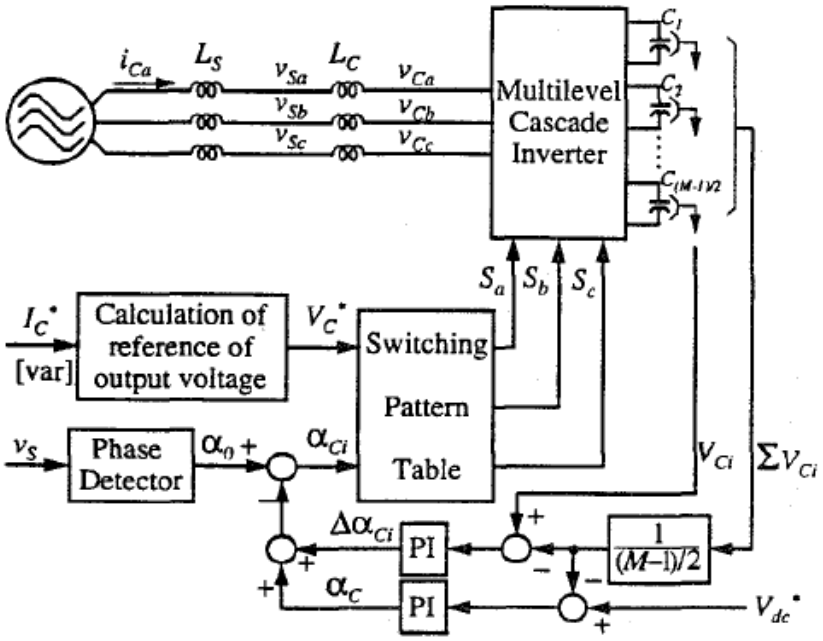


Figure 2.12 The α/Δα method for DC link capacitor balancing [48]

In order to equalize the capacitor voltages in each string, one of the conventional methods adopted is to control the total DC capacitor voltage per phase by adjusting α and individual DC capacitor voltages by shifting switching angles of each HB by an amount of ±Δα [48] as shown in Figure 2.12.

The outer α control-loop is used for real power flow from supply to CMC to compensate the related phase losses while the inner loop ±Δα control-loop is used to shift the output voltage of each HB against line current to equalize the DC link voltages. For M level CMC, there are $((M-1)/2)$ numbers of inner loops to be used for balancing and hence $((M-1)/2)$ numbers of PI controllers should be used. As the number of levels increases, the number of PI controllers also increases. This yields control complexity since the corresponding PI parameters used to determine α and Δα may be time-consuming, and difficult to find. Moreover, the PI controls of α and Δα may interact with each other, resulting in instability.

Another conventional method proposed in [49] is to use α control only with just measuring one DC link voltage as shown in Figure 2.13, and to rotate the switching angles for HBs in every half-cycle as shown in Figure 2.14. The switching patterns for the HBs are fixed during the half-cycle and they change in every half-cycle for each HB. For M level CMC, the equalization for DC links is acheived after M half-cycles of power frequency. Although, the advantage of this method to the α/Δα proposed in [48] is no need for many inner control loops and hence PI controllers, the duration for the equalization of DC link capacitors increases as the number of HB increases, which may not be possible for fast changing loads.

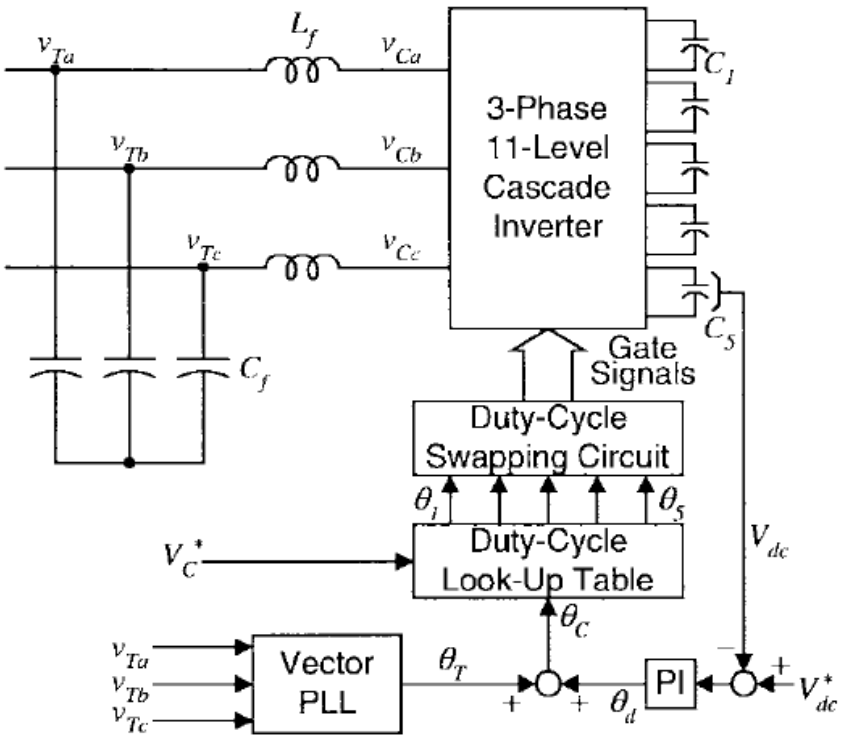


Figure 2.13 The rotational angle method for DC link capacitor balancing [49]

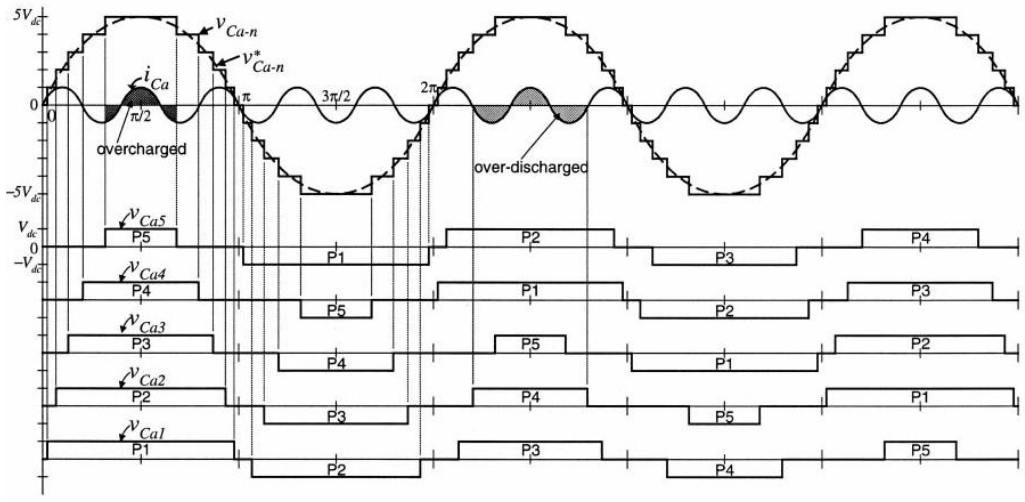


Figure 2.14 The rotational of switching angles [49]

2.4.2 Conventional Selective Swapping (CSS) Method

An important contribution to the solution of voltage equalization problem of DC link capacitors is known as the Selective Swapping Algorithm [50-51] which can be embedded in the control algorithm of the CMC. This method is called the swapping algorithm because at each level change (θ_1 to θ_5 in Figure 2.7), the previous set of HB/s which are in operation is going to be interchanged with a new set in each phase of each CMC module. It is called selective swapping algorithm because the swapping operation is done according to the values of DC link capacitor voltages.

The method uses different redundant combinations of HBs at the instants of level changes for DC link voltage balancing. The redundancy concept can be summarized for a 7-level CMC as follows:

The method uses the redundancy combinations of HBs at each level changes of CMC output voltage as shown in Figure 2.15 - Figure 2.17. As can be understood from the Figure 2.15, for $+3V_d$ and $0V_d$ levels, there is only one mode for these volatage levels. Therefore, at these voltage levels, there is no any swapping operation due to non-existence of a redundancy mode. Also, this is true for the $-3V_d$ voltage level. At $+2V_d$ and $+1V_d$ voltage levels, three different modes can be used as shown in Figure 2.16 and Figure 2.17. For example, from the transition from $0V_d$ to $+1V_d$ level of line-to-neutral voltage of CMC, one of Modes -1, -2 and -3 will be chosen. Also, for the transition from $+1V_d$ to $+2V_d$ voltage level, one of three modes shown in Figure 2.17 will be used with at least one/at most two new incoming HBs. The choice of the modes is determined by the charging or discharging states of the HBs as well as the magnitudes of DC link capacitor voltages. The same conclusions can be drawn for $-1V_d$ and $-2V_d$ voltage levels of CMC line-to-neutral voltages. That is respectively three, three and one redundancy mode occur for $-1V_d$, $-2V_d$ and $-3V_d$ voltage levels. Therefore, for a 7-level CMC, there are 15 modes (seven modes for positive voltage levels, one mode for 0 level and seven modes for negative voltage levels) in total.

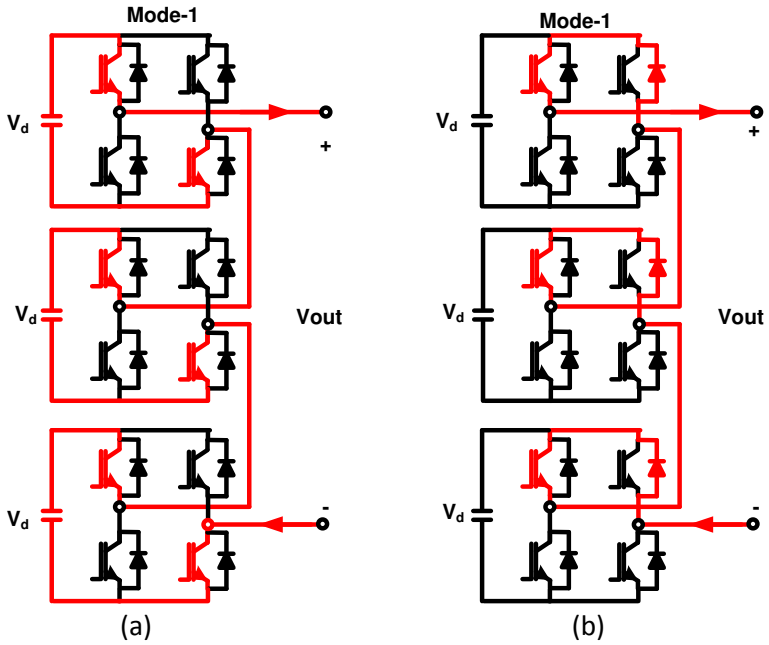


Figure 2.15 Redundant Modes of a) $+3V_d$ and b) $0V_d$ levels

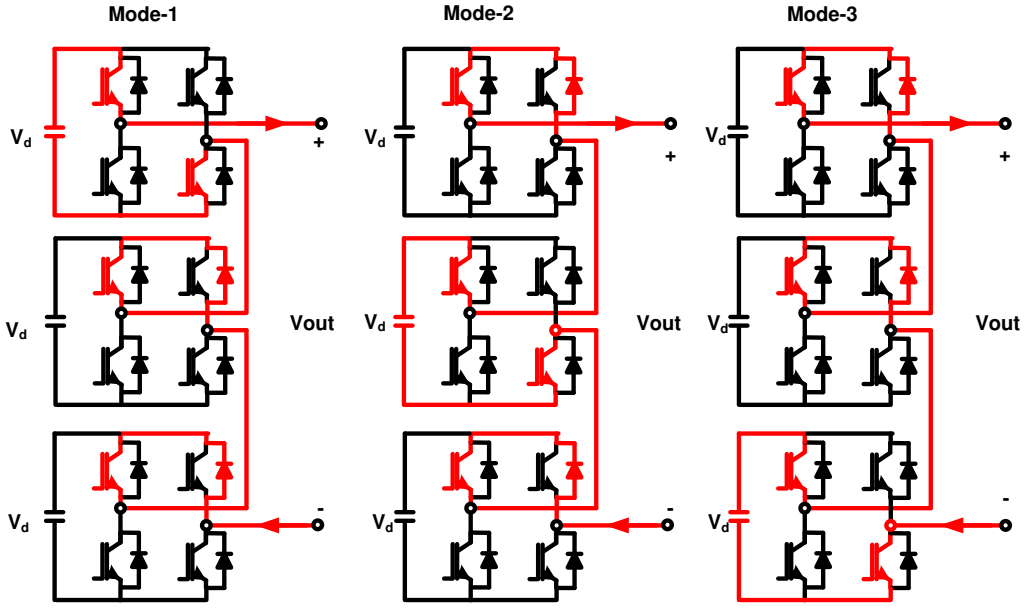


Figure 2.16 Redundant Modes of $+1V_d$ level

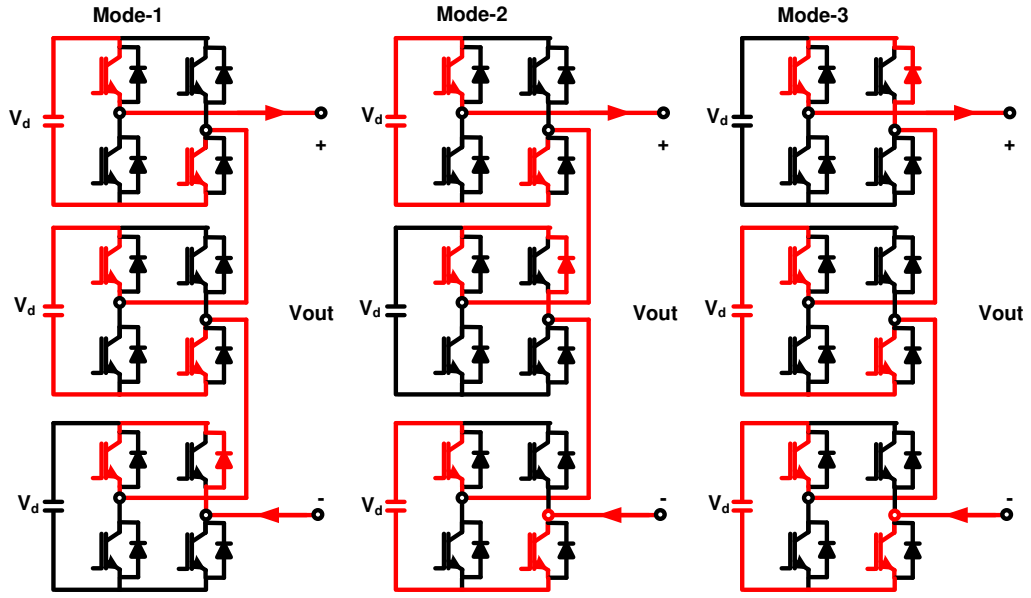


Figure 2.17 Redundant Modes of +2V_d level

The number of redundancy modes are directly proportional to the number of levels for the CMC topology. For example for a 11-level CMC (n=5) and 15-level CMC (n=7), the numbers of redundancy modes are shown in Table 2.5 and Table 2.6, respectively.

Table 2.5 The number of redundancy modes for 11-level CMC

The Voltage Level	Number of Redundancy Modes
0Vd	1
+1V_d,-1V_d	5,5
+2V_d,-2V_d	10,10
+3V_d,-3V_d	10,10
+4V_d,-4V_d	5,5
+5V_d,-5V_d	1,1
Total	63

Table 2.6 The number of redundancy modes for 15-level CMC

The Voltage Level	Number of Redundancy Modes
$0V_d$	1
$+1V_d$,$-1V_d$	7,7
$+2V_d$,$-2V_d$	21,21
$+3V_d$,$-3V_d$	35,35
$+4V_d$,$-4V_d$	35,35
$+5V_d$,$-5V_d$	21,21
$+6V_d$,$-6V_d$	7,7
$+7V_d$,$-7V_d$	1,1
Total	255

From Table 2.5 and Table 2.6, it is concluded that the total number of redundancy modes can be found by:

$$\text{Total Number of Redundancy Modes} = 2^{n+1} - 1 \quad (1.30)$$

where ***n*** is the number of HBs in each phase. Also, it is worth to mention that as the numbers of HBs increase, the numbers of redundancy modes also increase. This may cause the control complexity of DC link equalization algorithm for CMC having higher levels.

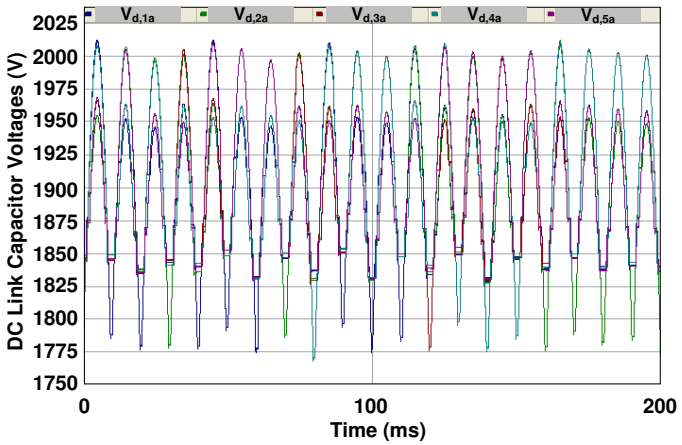
The equalization algorithm uses these redundancy modes for DC link voltage equalization by inspecting the instantaneous DC link capacitor voltages. The individual capacitor voltages are firstly measured in each phase, and then sorted with respect to their instantaneous values. The use of the redundancy modes of HBs at each level change is determined by the charging or discharging states of the HBs which are defined as follows:

If the current and the voltage are both positive or negative, the input power to the HB converter is positive and hence the associated DC link capacitor is going to be charged. On the other hand, if one of these quantities is positive while the other is negative, the input power to HB is negative and hence the associated DC link capacitor is going to be discharged. Therefore, in order to determine which HB/s are

going to be operated at each level change, the values of individual DC link capacitor voltages, polarity of the HB output voltage and direction of the line current should be measured.

The polarity of the output voltage to HBs is determined indirectly by using a PLL circuit which is locked to line-to-neutral voltage at PCC. The digital signal produced by PLL is phase advanced or delayed by power (load) angle, δ in Figure 2.5 to determine the zero crossing point of the CMC module fundamental line-to-neutral voltage. After determining the new status of DC link capacitors (charging or discharging) by this way, HBs having the lowest DC link voltages will be put into operation for charging and HBs having the highest DC link voltages, for discharging mode of operations. This method is called the Conventional Selective Swapping (CSS) in the work. The CSS gives minimum switching frequency for the power semiconductors.

The CSS performance on the equalization of DC link capacitor voltages for a 12 kV, ±10MVAr, 11-level CMC having 9.2mF capacitance value for each HB has been showed by the carried out computer simulations both for full inductive and capacitive operation modes as given in Figure 2.18 - Figure 2.20. The individual DC link voltages of five HBs in three phases of CMC for the case of full capacitive is almost equal and circulates around 1900 V mean DC voltage as shown in Figure 2.18. However, the peak-to-peak ripple value of DC link voltage of HB1 in phase-A of the CMC for inductive operation case is around 225V as shown in Figure 2.19 whereas those for capacitive operation mode is around 180V. The DC link voltages of the 1st HBs in three phases are also almost equal as shown in Figure 2.20. These results show that the CSS method is succesfull for the balancing of DC link voltages of individual HBs in CMC in the expense of higher variations in peak-to-peak ripple voltage.



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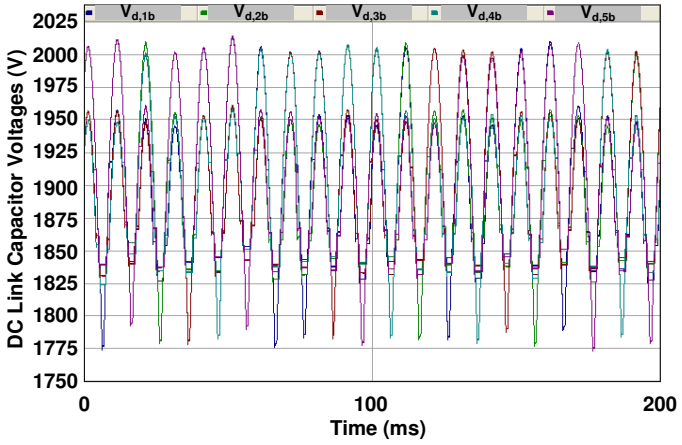

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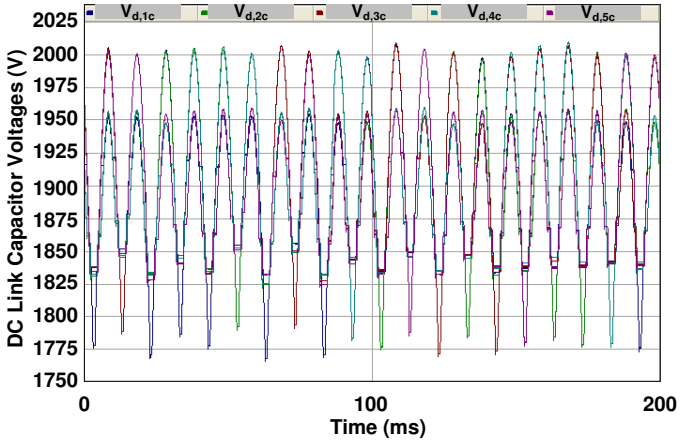
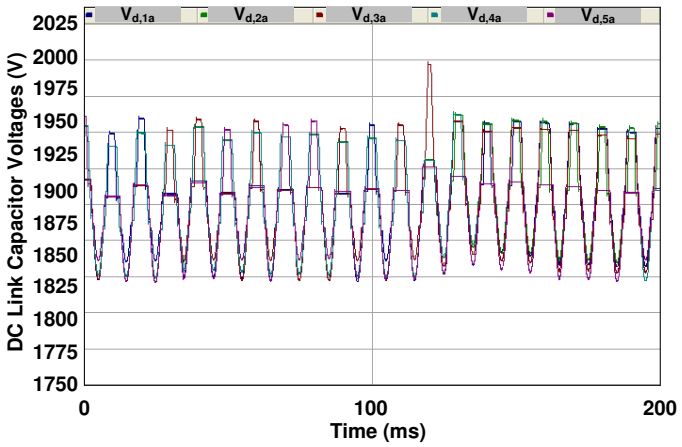


(c)

Figure 2.18 The variations in the instantaneous DC link voltages of a) phase-A, b) phase-B and c) phase-C HBs of 11-level CMC for full capacitive case (PSCAD Simulations)



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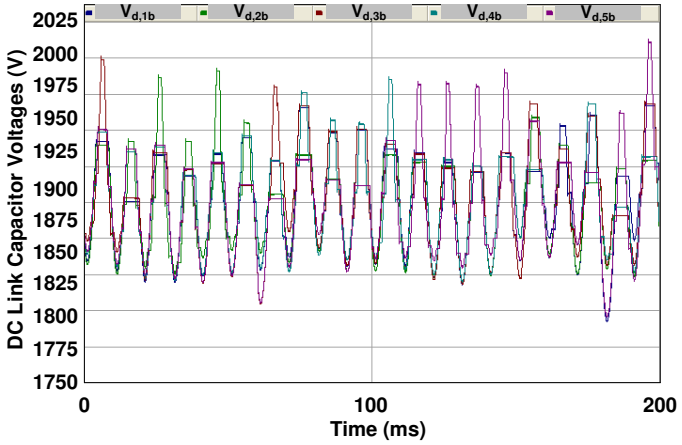

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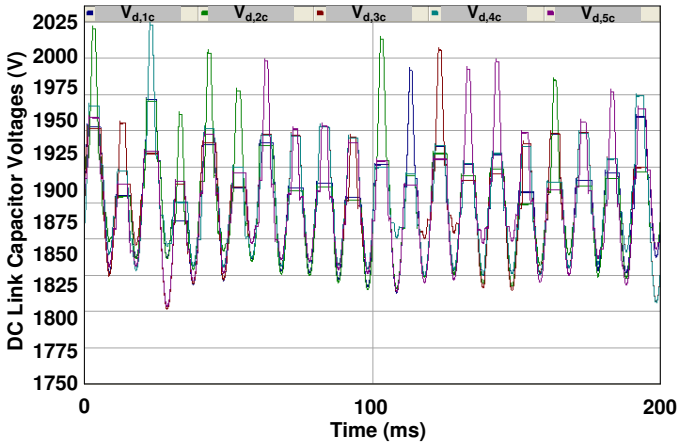
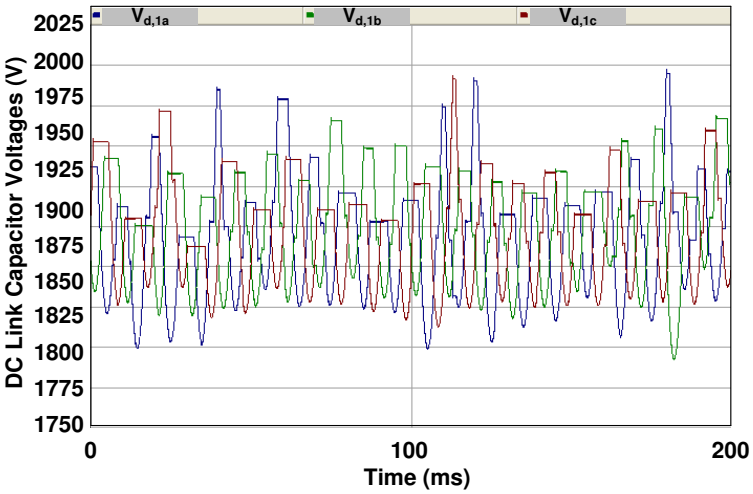
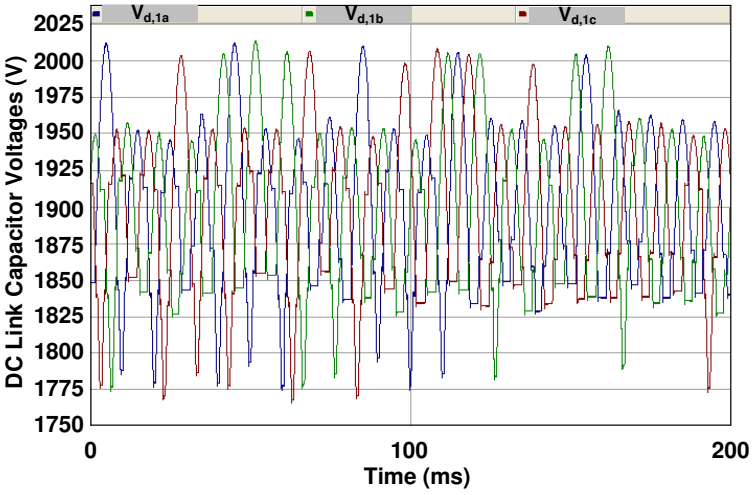


(c)

Figure 2.19 The variations in the instantaneous DC link voltages of a) phase-A, b) phase-B and c) phase-C HBs of 11-level CMC for full inductive case (PSCAD Simulations)



(a)



(b)

Figure 2.20 The variations in the instantaneous DC link voltages of 1st HBs in three phases of 11-level CMC for a) full inductive, b) full capacitive cases (PSCAD Simulations)

2.4.3 Modified Selective Swapping (MSS) Method

The major drawback of the CSS is the higher variations observed in the DC link capacitor voltages as the number of HBs in each CMC is reduced. In order to

eliminate this drawback, the CSS is modified and then applied to T-STATCOM described in the thesis. In the Modified Selective Swapping (MSS) algorithm, selective swappings are applied not only at level changes but continuously at a pre-specified frequency during the operation of the CMC. Figure 2.21 illustrates the application of the MSS method proposed in the thesis in comparison with the CSS. The only difference of MSS with CSS is the application of swappings for a specified time not only the level changes but also during the levels. The flowchart of MSS method proposed in the thesis is given in Figure 2.22.

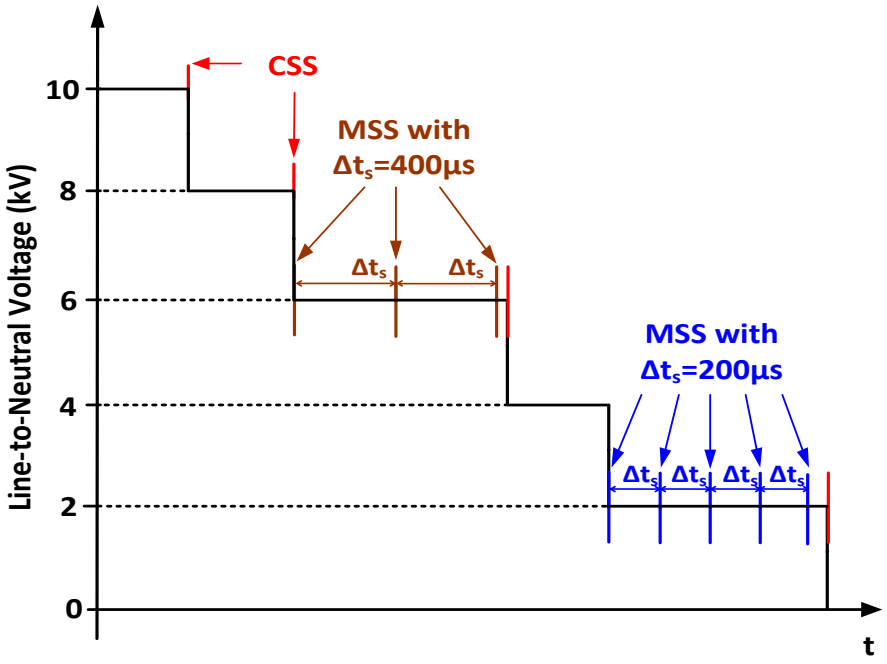


Figure 2.21 The illustration of CSS and MSS

Some simulations are carrid out for a ±10MVAr CMC having five series HBs with 1900 V DC link voltages and 9.2mF capacitance values to compare the effects of

CSS and MSS methods for both full inductive and capacitive operation modes as shown in Figure 2.23 and Figure 2.24.

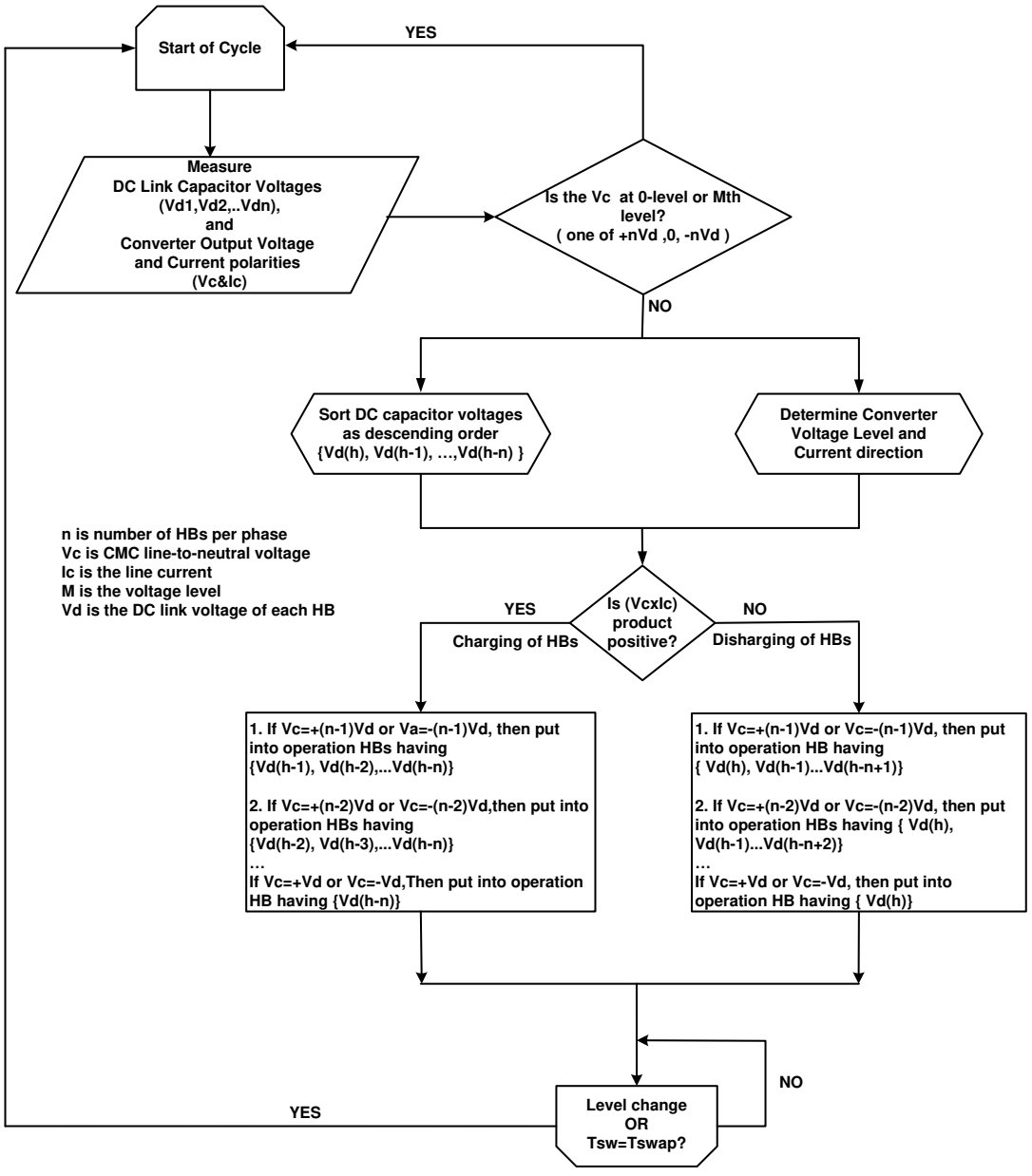
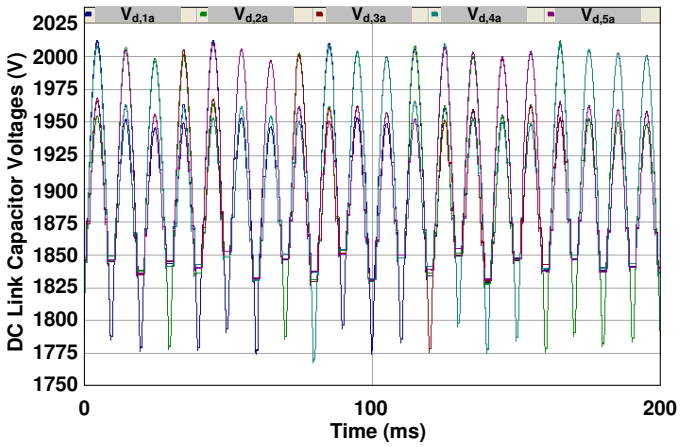


Figure 2.22 The flowchart for MSS method employed in M-level CMC



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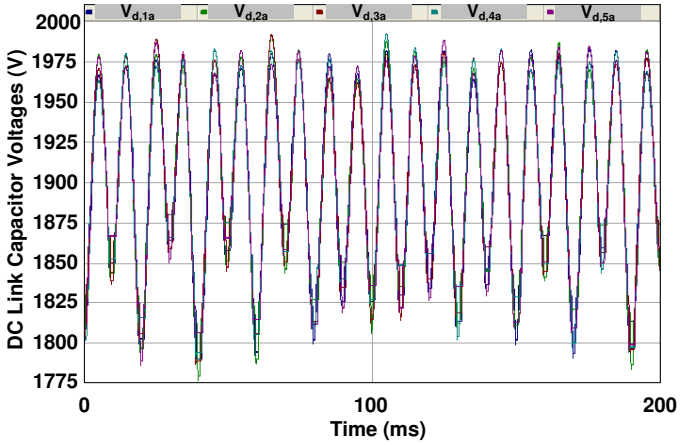

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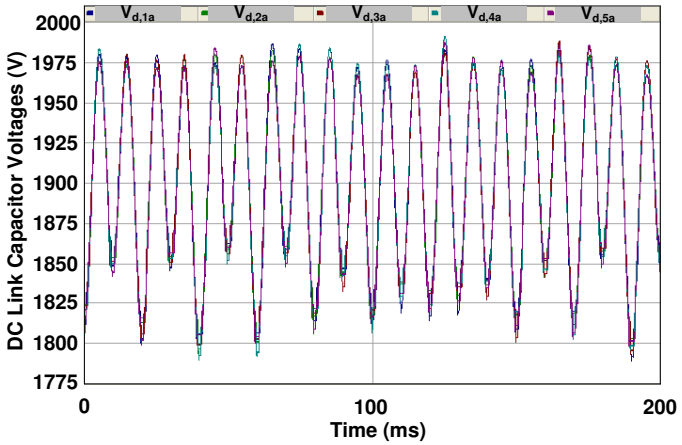
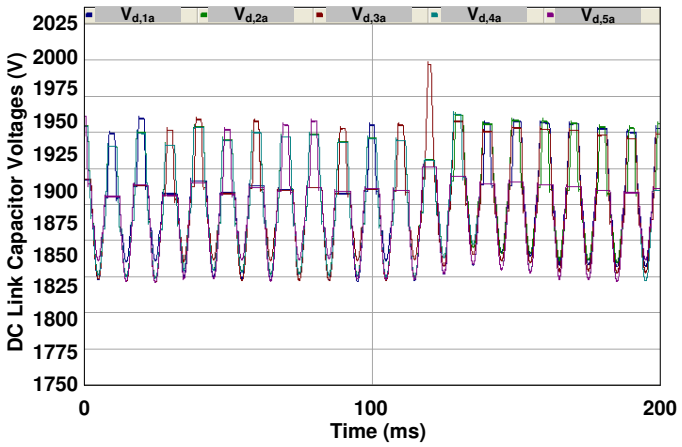


(c)

Figure 2.23 The variations in the instantaneous DC link voltages of the CMC under a) CSS, b) MSS with Δt_s=400 µs and c) MSS with Δt_s=200 µs for full capacitive case (PSCAD Simulations)



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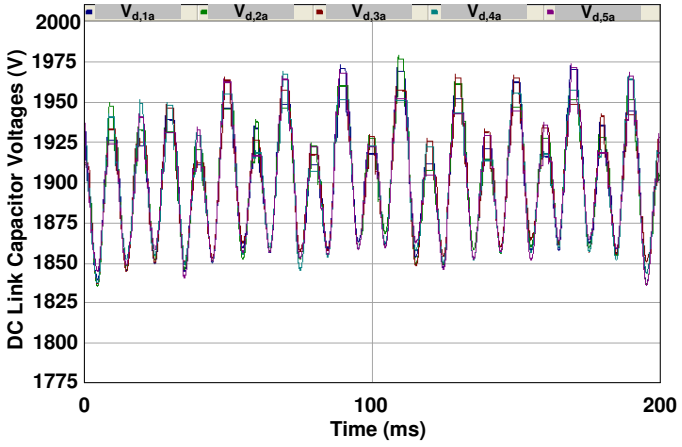

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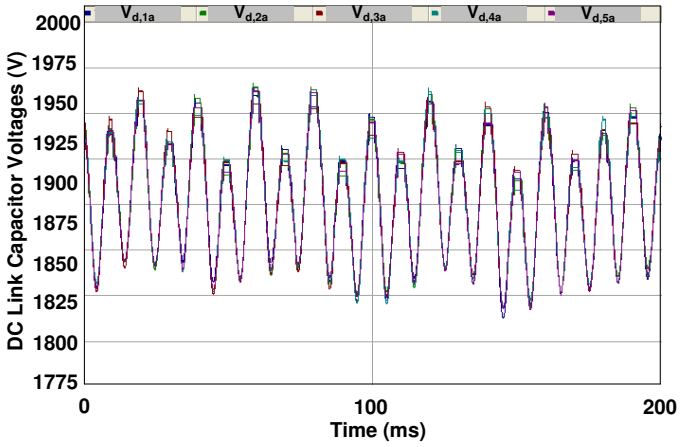


(c)

Figure 2.24 The variations in the instantaneous DC link voltages of the CMC under a) CSS, b) MSS with Δt_s=400 µs and c) MSS with Δt_s=200 µs for full inductive case (PSCAD Simulations)

It is obvious that MSS methods are superior to CSS method on the equalization of DC link capacitor voltages for both full inductive and full capacitive cases as shown in Figure 2.23 and Figure 2.24. A perfect balancing is achieved for both MSS methods with Δt_s=200µs and Δt_s=400µs. The only difference between them is the values of peak-to-peak variations in DC link voltages and the effective switching frequency of the power semiconductors.

In MSS method, the most important parameter is the determination of the swapping time, Δt_s. From the simulation works, it has been concluded that as the Δt_s value decreases, the instantaneous, δV_d and mean peak-to-peak, ΔV_d voltage variations in DC link voltage decrease. However, the switching frequency of the power semiconductors and hence the power losses increase. Therefore, a comprimise should be made between variations in DC link voltages and the switching frequency of the power semiconductors when determining the swapping period, Δt_s. Such a work is also conducted for a ±10MVAr CMC having five HBs with 1900 V DC link voltages and 9.2mF capacitance values for both full inductive and capacitive operations. The variations in DC link voltage of HB1 in phase-A of the CMC are tabulated for CSS and MSS with some Δt_s values as shown in Table 2.7 ansd Table 2.8.

Table 2.7 The variations in DC link voltage of HB1 in phase-A of 11-level CMC operating at -10MVAr (Theoretical)

Method Applied	**Capacitive Mode**				
	δV_d(V)	**δV_d(%)**	**ΔV_d(V)**	**ΔV_d(%)**	**Switching Frequency (Hz)**
CSS	225	11,8	42	2,2	200
MSS (Δt_s=200µs)	170	9,0	13	0,7	700
MSS (Δt_s=400µs)	180	9,5	18	0,9	500
MSS (Δt_s=600µs)	200	10,5	19	1,0	350
MSS (Δt_s=800µs)	210	11,1	37	1,9	300
MSS (Δt_s=1000µs)	220	11,6	40	2,1	250

Table 2.8 The variations in DC link voltage of HB1 in phase-A of 11-level CMC operating at +10MVAr (Theoretical)

Method Applied	Inductive Mode				
	δV_d(V)	δV_d(%)	ΔV_d(V)	ΔV_d(%)	Switching Frequency (Hz)
CSS	180	9,5	35	1,8	250
MSS (Δt_s=200µs)	122	6,4	10	0,5	650
MSS (Δt_s=400µs)	120	6,3	10	0,5	500
MSS (Δt_s=600µs)	125	6,6	14	0,7	400
MSS (Δt_s=800µs)	130	6,8	17	0,9	350
MSS (Δt_s=1000µs)	160	8,4	28	1,5	300

The following conclusions can be drawn from the simulation works conducted for 11-level CMC at ±10MVAr ratings:

a. MSS methods are superior to CSS method on the equalization of DC link capacitor voltages for both full inductive and full capacitive operation modes.
b. Although the effective switching frequency of the power semiconductors under CSS method is less, the variations in instantaneous peak-to-peak and mean voltages of DC link voltages for HBs are higher than those of under MSS method. This is an important result since it gives a chance to choose a lower capacitance value for MSS method than CSS method for the same design value of DC link instantaneous peak-to-peak voltage. As an example, the instantaneous peak-to-peak DC link voltage of HB1 under CSS method is 180 V while it is 120V when MSS with Δt_s=400µs is employed to the same HB unit. There is a 33% decrease in variations in DC link voltages of each HB under MSS method which may result in using the capacitance values of 0.67 times of those for HBs under CSS method. Therefore, it is economically beneficial to apply MSS method especially for the CMCs having high number of HBs in series for high voltage- high power applications.

c. The variations in instantaneous peak-to-peak and mean voltages decrease with MSS methods with low values of Δt_s while the effective switching frequency of power semiconductors increases. Therefore, for practical applications, a compromise should be made between the instantaneous peak-to-peak voltage and the effective switching frequency.

d. For full inductive operation mode, all CSS and MSS methods achieve the percentage limit value for the variations in peak-to-peak DC link voltage for an HB unit as shown in Figure 2.25.

e. The variations in the DC link instantaneous peak-to-peak voltage of an HB unit is over the limit value for CSS method applied to the CMC at 10 MVAr capacitive operation mode as shown in Figure 2.25. Also, MSS method with Δt_s=200µs and Δt_s=400µs can only achieve the design value for both full capacitive and inductive operation modes.

f. Beyond a Δt_s value such as Δt_s=1000µs, no difference exists between CSS and MSS methods for variations in DC link instantaneous peak-to-peak voltages.

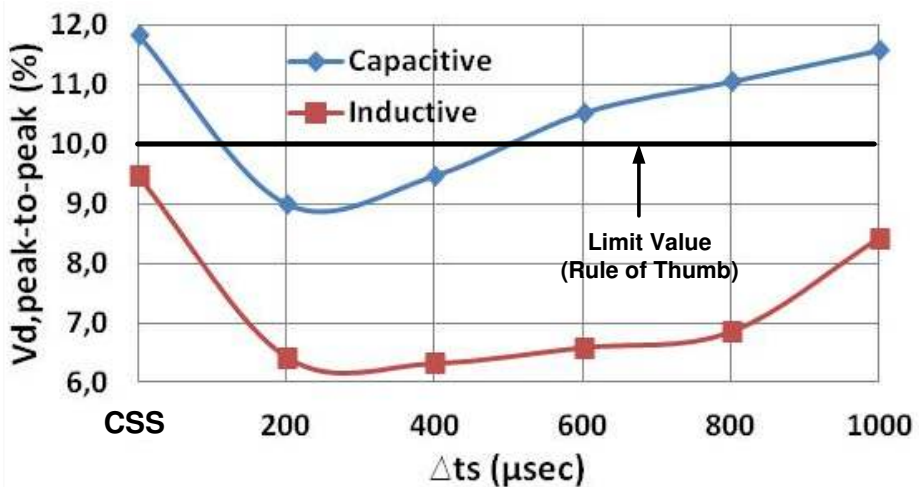


Figure 2.25 The performance of CSS and MSS methods on the instantaneous peak-to-peak variations in the DC link voltage of an HB unit (Theoretical)

In the field tests of the T-STATCOM, the MSS has been applied at a pre-specified period of Δt_s=400μs and also of Δt_s=200μs, at the expense of higher switching frequency and hence switching losses. The effects of MSS on voltage balancing problem and switching frequency will be discussed in Chapter 5 of the thesis in comparison with those of CSS by field test results.

CHAPTER 3

SYSTEM DESIGN AND SIZING

3.1 Introduction

This chapter of the thesis describes the general principles applicable to the design of the T-STATCOM systems in view of:

a. IEEE harmonic standards,
b. supply conditions,
c. ratings of power semiconductors available in the market,
d. reactive power demand of the over-headline or transmission bus to which the T-STATCOM is connected.

These design issues include:

a. the sizing of H-Bridge (HB) and Cascaded Multilevel Converter (CMC),
b. the determination of the number HBs in each phase of the CMC,
c. the determination of the number of parallel operated CMCs
d. the calculation of optimum value of total series filter reactance.

3.2 Determination of Connection Point and Sizing of T-STATCOM

A T-STATCOM system may be connected to the power grid in two different ways as summarized in Figure 3.1 and Figure 3.2. The existing parts of the power grid are shown by grey-colored components in Figure 3.1 and Figure 3.2., while the major

components of the T-STATCOM by black-colored lines. If a power transformer operating at partial loads is present in the area at which the T-STATCOM system will be installed, the T-STATCOM may be connected to the MV side of this transformer as shown in Figure 3.1. For this case, the Point of Common Coupling (PCC) should be taken as the MV side of the power transformer.

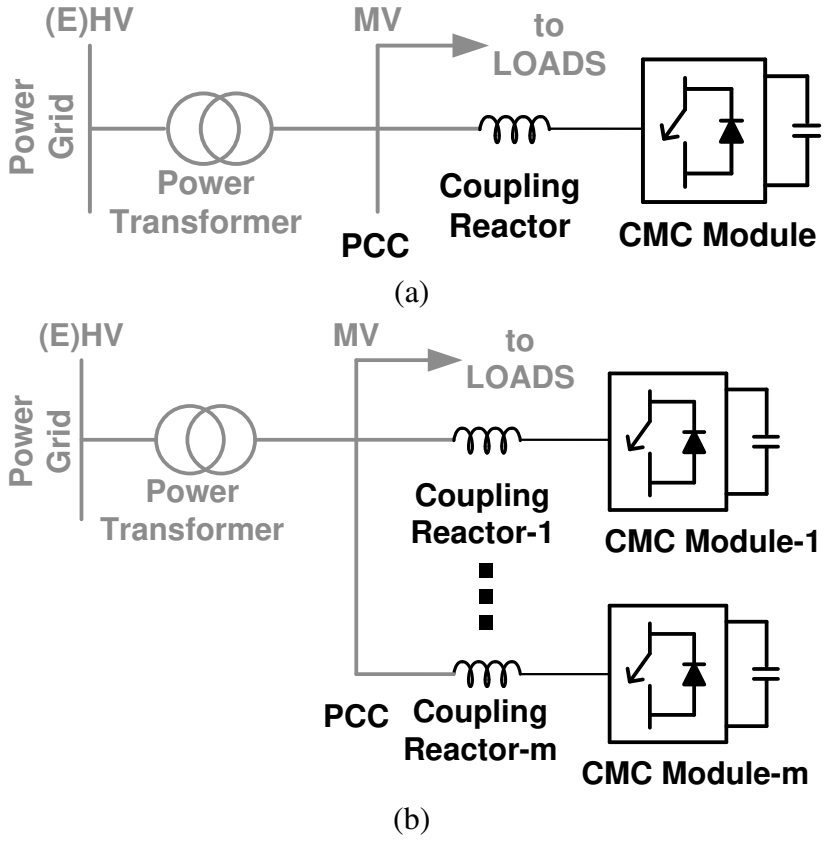


Figure 3.1 Connection alternatives for T-STATCOM system ((a) and (b) connection to the MV side of existing power transformer)

Alternatively, the T-STATCOM system may be connected to one of the EHV or HV buses at the same location of the power grid via a specially designed coupling transformer as shown in Figure 3.2.

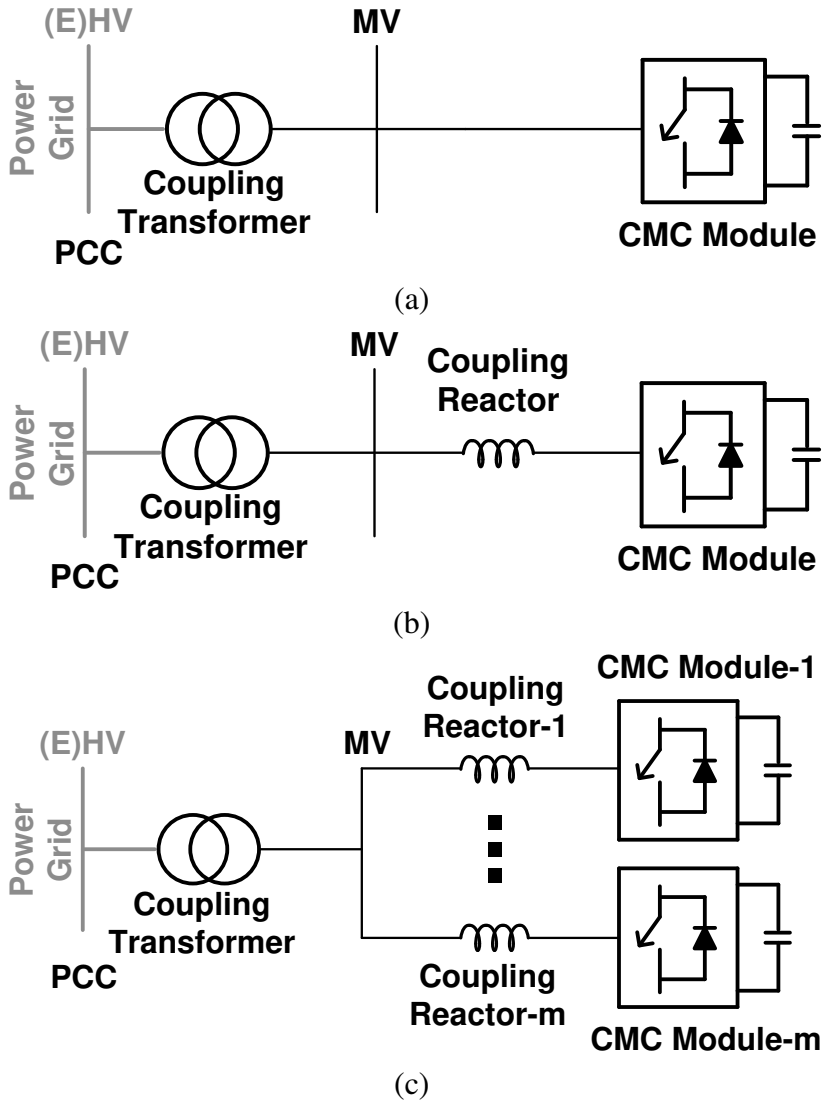


Figure 3.2 Connection alternatives for T-STATCOM system ((a),(b),and (c) connection to the power grid via a special coupling transformer)

Since several loads are supplied from the MV bus at PCC in Figure 3.1-a, a series filter reactor bank is an inevitable part of the T-STATCOM in order to suppress voltage harmonics produced by the CMC module as well as for the control of the T-STATCOM. If a coupling transformer with sufficiently high leakage reactance can be designed and manufactured, and at the same time EHV or HV power grid bus is

sufficiently strong, an independent series filter reactor may not be used as illustrated in Figure 3.2-a.

Before connecting an industrial plant or a FACTS device to the PCC, the designer must be sure that the system under design should comply with the harmonic standards such as IEEE Std. 519, 1992 [53]. Since MV buses are vulnerable to harmonic distortion because of their relatively large source reactances, the designer should pay special attention to the connection point of the T-STATCOM as will be described in the foregoing section. Permissible regions for TDD and THD limits as recommended in IEEE Std.519, 1992 are graphically illustrated in Appendix-B for weak and strong supply conditions as a function of PCC voltage.

On the other hand, the installed capacity of T-STATCOM system should be determined carefully in view of the inductive and capacitive reactive power requirements and their daily, monthly and annual variations. Depending on slowly varying component of the reactive power demand, circuit breaker-switched shunt capacitor banks and shunt reactor banks may be considered as auxiliary system components for the T-STATCOM based FACTS applications. These auxiliary components are not shown in Figure 3.1 and Figure 3.2. Furthermore, if the maximum reactive demand of the T-STATCOM application is larger than the attainable MVAr rating of one CMC module, more than one CMCs are to be operated in parallel as shown in Figure 3.1-b and Figure 3.2-c. For such cases, series filter reactor banks become an essential part of the system in order to maintain a good current and reactive power sharing between CMC modules.

3.3 Sizing of CMC Module

It is obvious that maximum attainable VAr rating for each CMC module is largely dictated by the current status of commercially available power semiconductors such as High Voltage Insulated Gate Bipolar Transistors (HV IGBT). The variations in

maximum allowable peak current in commercially available HV IGBTs by June 2012 are given in Appendix-C as a function of the DC link voltage of HB. By using these data, maximum attainable CMC ratings ($\pm Q_c$) are calculated as a function of rated AC voltage of CMC (V_c) for three different CMC topologies with three, five and seven series connected HBs and given in Figure 3.3. Rated AC voltage of CMC in Figure 3.3 can be chosen among the standard AC voltages specified in IEC Standard Voltages [54]. This voltage is determined by the coupling transformer secondary voltage to which CMC module is to be connected as described in Subsection III-A. DC link voltages, V_d of each HB in the CMC are marked on Figure 3.3 for each CMC topology and for all CMC voltages. For these V_d values, rated collector-emitter voltages and maximum rated collector currents of commercially available HV IGBTs can be read from the figure given in Appendix-B. Therefore the maximum attainable CMC ratings in Figure 3.3 are calculated by PSCAD simulations by considering collector-emitter voltage ratings, maximum available collector current ratings, Safe Operating Areas (SOAs) of the required HV IGBTs and the number of HBs in each phase of associated CMC.

It is seen from Figure 3.3 that maximum Q_c ratings of each CMC module are obtained for seven series connected HBs in each phase and utilizing 1700V, 3600A and 6500V, 750A HV IGBTs respectively for 7.2 kV and 36 kV line-to-line CMC voltage ratings. Although, this choice (seven HB in series, l=15 levels in line-to-neutral voltages) yields minimum harmonic distortion in line-to-line voltages and line currents, its major drawback is the complexity of the power stage and the control system.

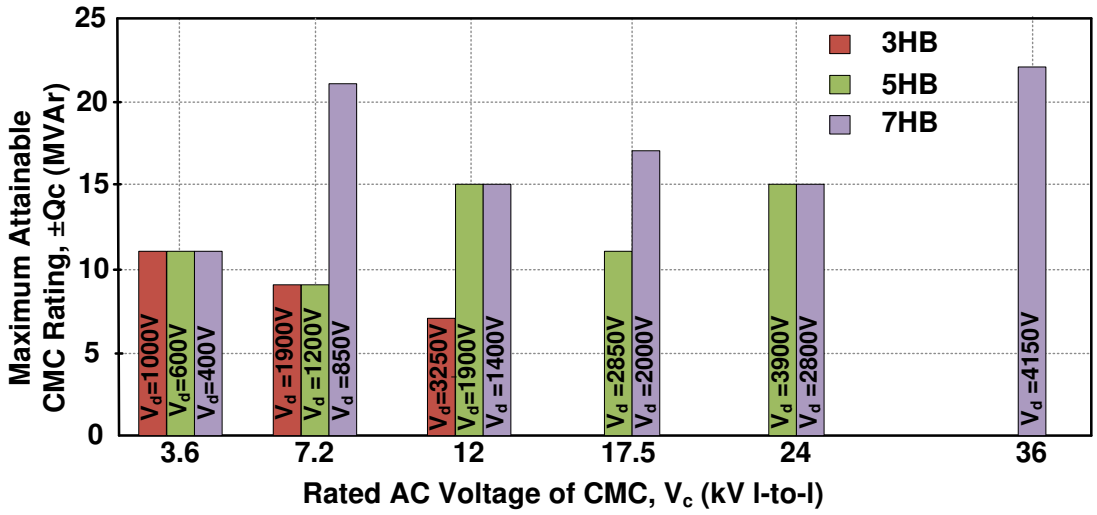


Figure 3.3 Maximum attainable CMC ratings calculated as a function of rated AC voltage of CMC (V_c) for three different CMC topologies (in view of HV IGBT technology by June 2012)

From the Figure 3.3, the followings can be concluded for the investigated three CMC topologies:

a. The maximum attainable VAr ratings of CMC modules designed for 3.6 kV PCC voltages are equal for the three CMC topologies by the utilization of the same HV IGBTs with the rating of 1700V, 3600A. Therefore, the choice of CMC topology for 3.6 kV AC voltage depends upon the supply condition in view of THD and TDD.

b. CMC topology with 7HB gives the maximum VAr rating as well as being the best choice for harmonic contents of line-to-line voltages and line currents in the expense of the complexity of power stage and control system for 7.2 kV applications. It uses 1700V, 3600A HV IGBTs.

c. For 12 kV applications, the CMC topologies with five and seven series connected HBs have the same Q_c ratings by using 3300V, 1500A HV IGBTs. If PCC is strong enough against harmonic distortion for current and voltage, CMC with five HBs is the best alternative due to less number of power semiconductors and economic considerations.

d. CMC topologies with five and seven HBs are only the applicable alternatives for 17.5kV and 24 kV AC rated voltages. The maximum Q_c rating is obtained by CMC topology with seven HBs by the use of 4500V, 1200A HV IGBTs for 17.5 kV applications. 6500V, 900A HV IGBTs are utilized in the power stages of the CMC topologies with five and seven HBs for 24kV. Since both topologies have the same MVAr capacity, TDD and THD considerations of the power system at which T-STATCOM is connected determine the choice among them.
e. The CMC with seven HBs is the only applicable solution for 36 kV STATCOM applications by using 6500V, 900A HV IGBT modules.

The CMC topology with five series connected HBs is a compromise between system complexity and maximization of the CMC VAr rating. In this work, a field prototype of 12kV line-to-line, 11-level CMC is designed and implemented by using 3300V, 1200A HV IGBTs (MITSUBISHI CM1200HC-66H). This CMC can produce successfully ±12MVAr at its terminals and the resulting T-STATCOM can deliver 10 MVAr capacitive to and absrob 14 MVAr inductive from 154kV PCC. These practical values verify the findings for 12 kV line-to-line rated AC voltage of 11-level CMC in Figure 3.3 (rated Q_c would be ±15 MVAr if 3300V, 1500A HV IGBT were used).

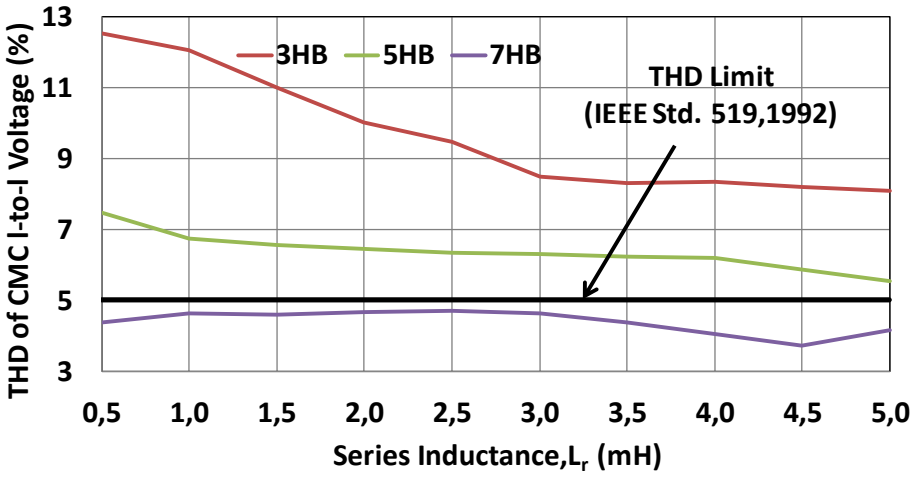
3.4 Design of Series Filter Reactor

The performance of the T-STATCOM system at PCC in view of voltage and current harmonic distortion limits specified in [53] is affected not only by the short-circuit MVA of busbar to which the T-STATCOM is connected and the number of HBs in each phase of the CMC but also by the inductance of the total series filter reactor. Therefore, the choice of the series L_r is a critical issue in the system design. For the whole results obtained in this subsection, it is assumed that PCC voltage is 12 kV

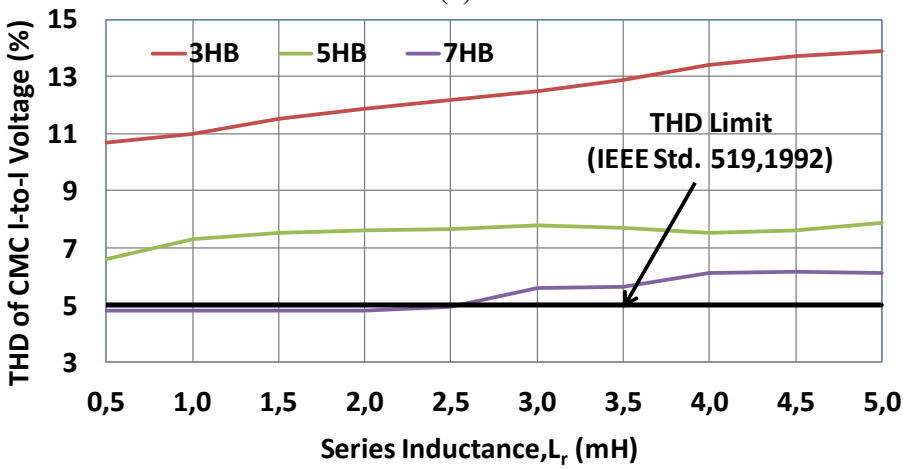
line-to-line, T-STATCOM rating is ±10MVAr and before the connection of the T-STATCOM, voltage waveforms at PCC are purely sinusoidal.

3.4.1 THD Values in AC Input Voltage of CMC

The THD values in AC input voltage of CMC topologies with three, five and seven HBs are given in Figure 3.4 for full inductive and full capacitive operating modes. For capacitive operation mode, the THD values decreases as series filter inductance value increases. However, only CMC topology with seven HBs is under the limit value specified by IEEE 519-1992. The THD values of all three topologies investigated in this work for full inductive operation mode increase and are over the limit value as the series inductance value increases. This is due to lower modulation index values corresponding to higher inductive reactive power consumed by large inductances. As the modulation index values are getting smaller during inductive mode of operation, the widths of the HBs output voltages are being narrowed, and hence the AC input voltages of the CMC have more harmonic content. Therefore, the THD value in AC input voltage of CMC rises when the series filter inductance takes higher values. For capacitive case, when series filter inductance value rises, to compansate the voltage drop on it, a higher modulation index value is used and the widths of output voltages of HBs are being expanded. Therefore, the AC input voltages of the CMC have less harmonic content than those for inductive operation mode.



(a)

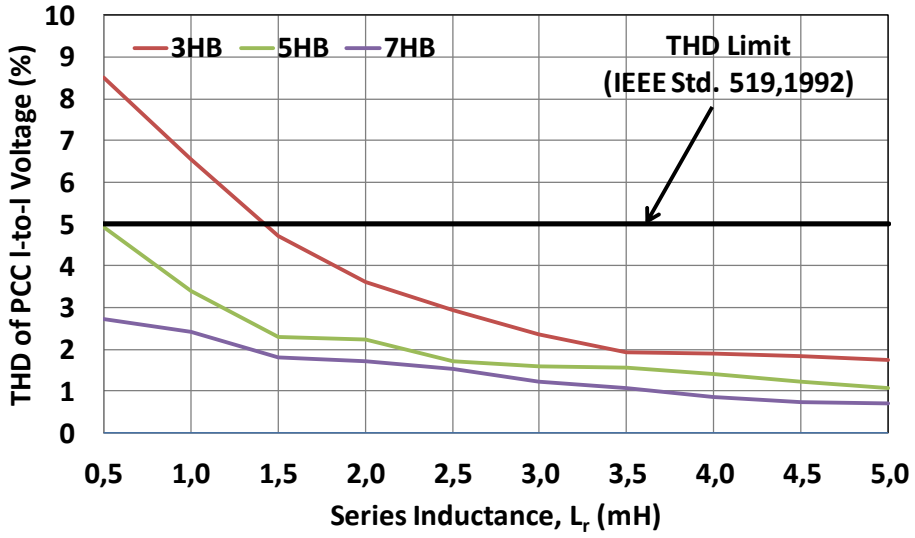


(b)

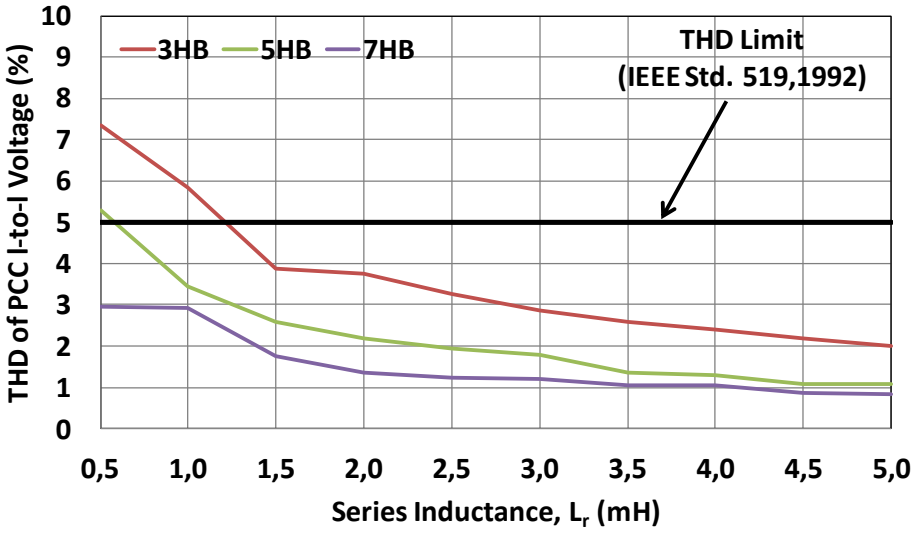
Figure 3.4 THD variations against series inductance for AC input voltage of CMC Topologies ((a) Capacitive Case; (b) Inductive Case)

3.4.2 Effect of Series Filter Inductance on THD and TDD

In the case where the T-STATCOM is connected to the MV side of an existing power transformer (Figure 3.1), the variations in THD of PCC line-to-line voltages and TDD of the line currents against series filter inductance will be as given in Figure 3.5 for CMC topologies with three, five and seven HBs.



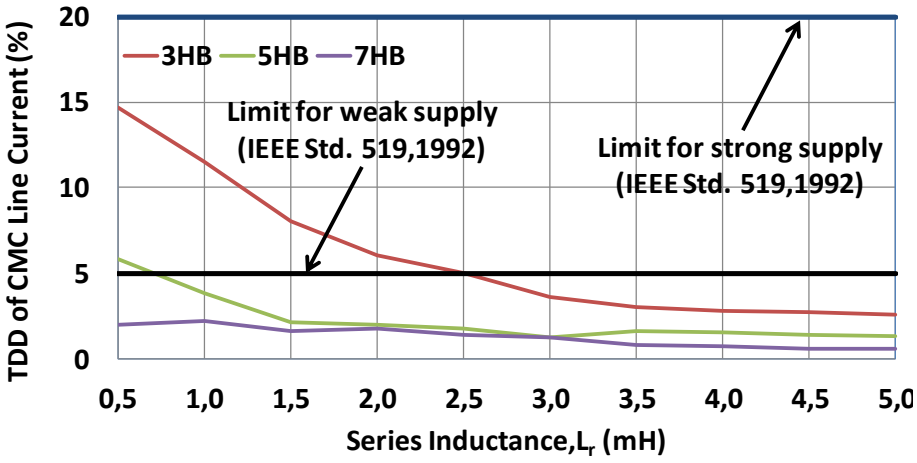
(a)



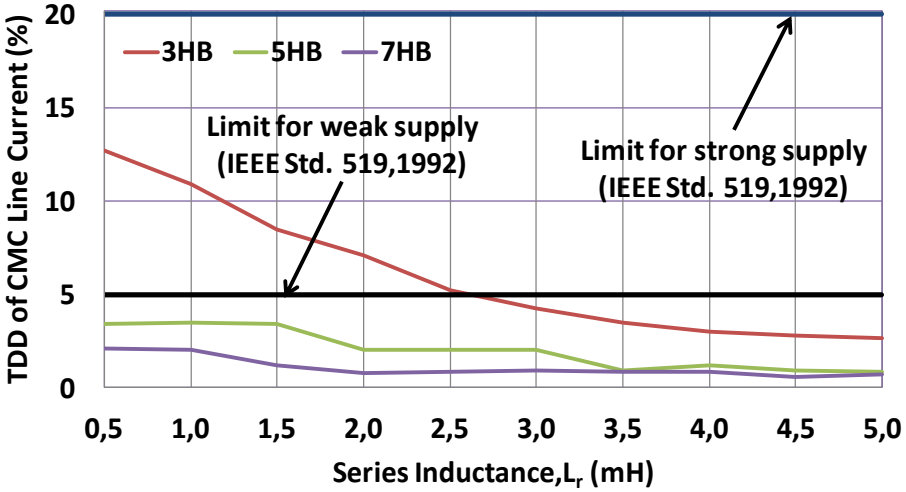
(b)

Figure 3.5 THD variations against series inductance for CMC Topologies at MV PCC ((a) Capacitive Case; (b) Inductive Case)

The results in Figure 3.6 corresponding to CMC topology with three HBs show that larger L_r values should be used to comply with TDD limit especially for weak supplies.



(a)

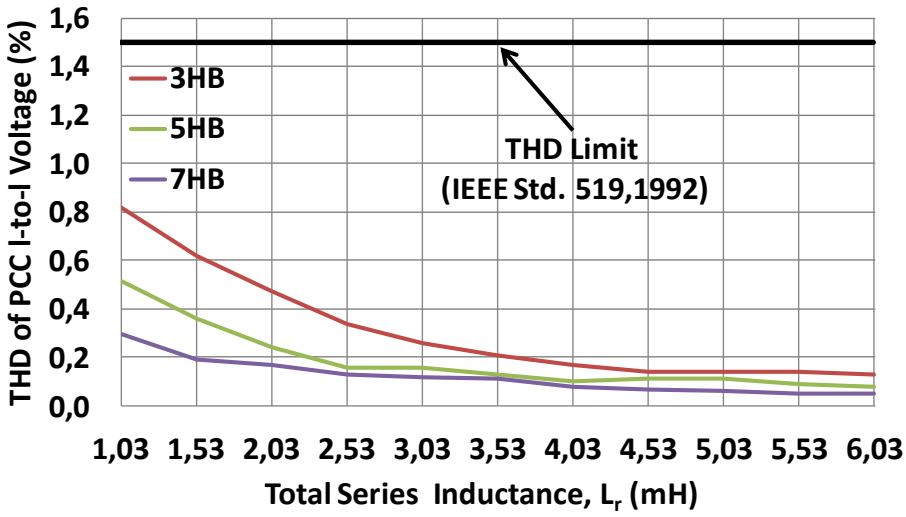


(b)

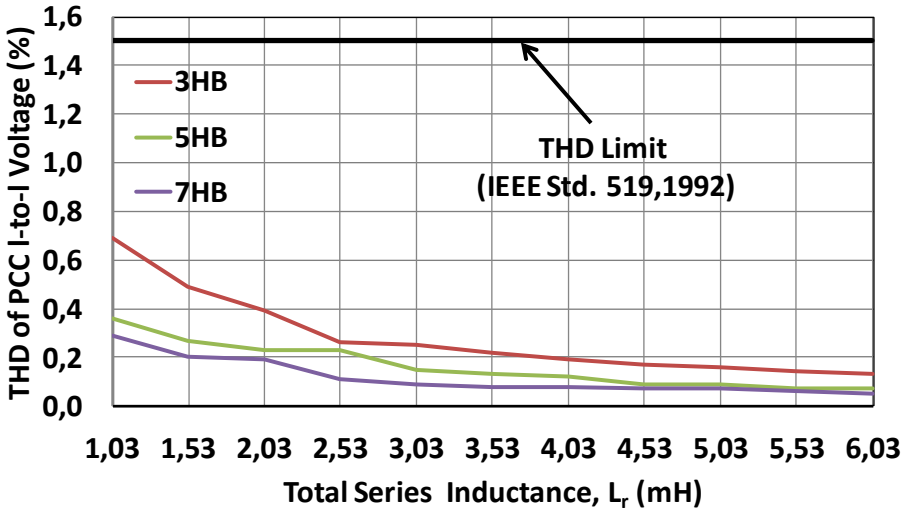
Figure 3.6 TDD variations against series inductance for CMC Topologies at MV PCC ((a) Capacitive Case; (b) Inductive Case)

In the case where the T-STATCOM system is going to be connected to 154 kV HV bus via a series filter reactor bank and a 154/10.5kV coupling transformer, the above analyses are repeated and the variations in THD and TDD are given in Figure 3.7 and Figure 3.8. Total series inductance in Figure 3.7 is the sum of leakage reactance of the coupling transformer referred to CMC side and reactance of the series filter

reactor bank. The results in Figure 3.7 shows that THD limits in [52] does not constitute a constraint in the selection of both the number of HBs and L_r.



(a)

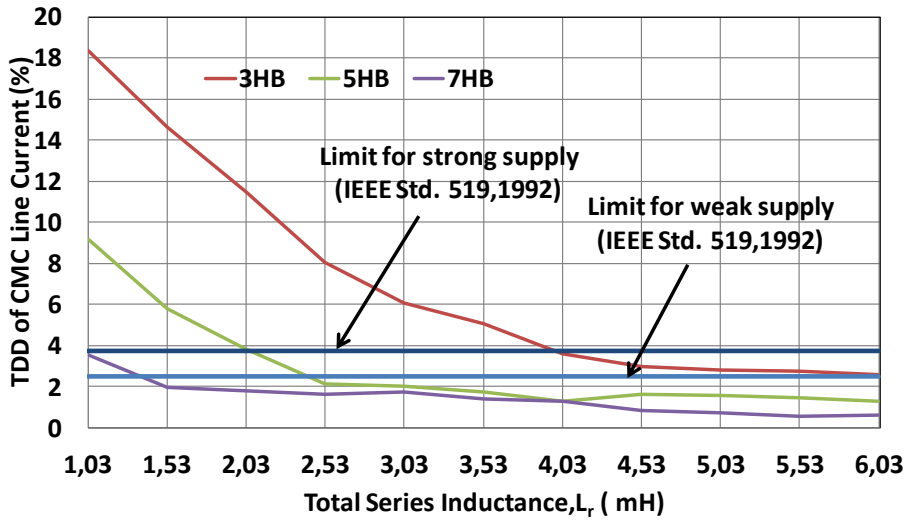


(b)

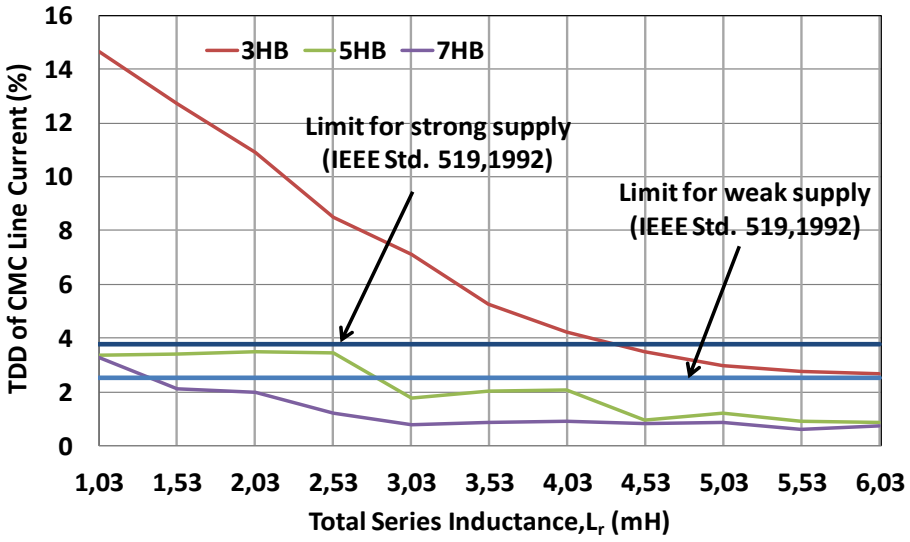
Figure 3.7 THD variations against total series inductance for CMC Topologies at HV PCC ((a) Capacitive Case; (b) Inductive Case)

However, Figure 3.8 shows that the choice of number of HBs and L_r value are critical design issues in order to comply with TDD limits in [53]. Therefore, in the

design of the field prototype of the T-STATCOM system, a CMC with five HBs should be preferred and a total series inductance greater than 2.75mH should be chosen.



(a)



(b)

Figure 3.8 TDD variations against total series inductance for CMC Topologies at HV PCC ((a) Capacitive Case; (b) Inductive Case)

3.4.3 Effect of Series Filter Inductance on DC Link Voltage and Modulation Index Values

Another factor affecting the choice of total series inductance, L_r is the design value of DC link voltage. It is highly desirable to keep DC link voltage constant at the design value from full inductive to full capacitive operation modes for an ideal T-STATCOM system. The variations in DC link voltage, V_d, against total series inductance, L_r, for different values of modulation index, M for the investigated CMC topologies with three,five and seven HBs are shown in Figure 3.9 - Figure 3.11. The optimum values of L_r and the associated M ranges are marked on the same figures. L_r values for CMC topologies are chosen according to THD and TDD values explained in Subsection 3.4.2.

The CMC with three HBs can achieve the TDD limit value only for L_r value greater than 4.3mH as seen in Figure 3.8 when the CMC is installed at a strong supply for full inductive operation mode. For weak supply conditions, this topology can comply with harmonic standards specified in IEEE 519-1992 for very large L_r values which may not be feasible. The maximum safe value of DC link voltage for the chosen HV IGBTs was 3250V as seen in Figure 3.3. The optimum operation point for the CMC with three HBs is marked on Figure 3.9 with the the choices of L_r=4.3mH and V_d=3250 V. Therefore, the corresponding M range is [1.66-2.32] as shown in Figure 3.9.

The minimum L_r value to overcome THD and TDD limit values specified by IEEE 519-1992 for CMC having seven HBs is 1.4mH as shown in Figure 3.8. The maximum safe value of DC link voltage for the chosen HV IGBTs was chosen 1400V as can be seen in Figure 3.3. A total series inductance value greater than 1.4mH should be applied to the CMC design to have a higher resolution in reactive power variation against load changes. Therefore, Lr=2.53mH is chosen, and the M value will vary between 4.16 and 4.93 as can be seen in Figure 3.10.

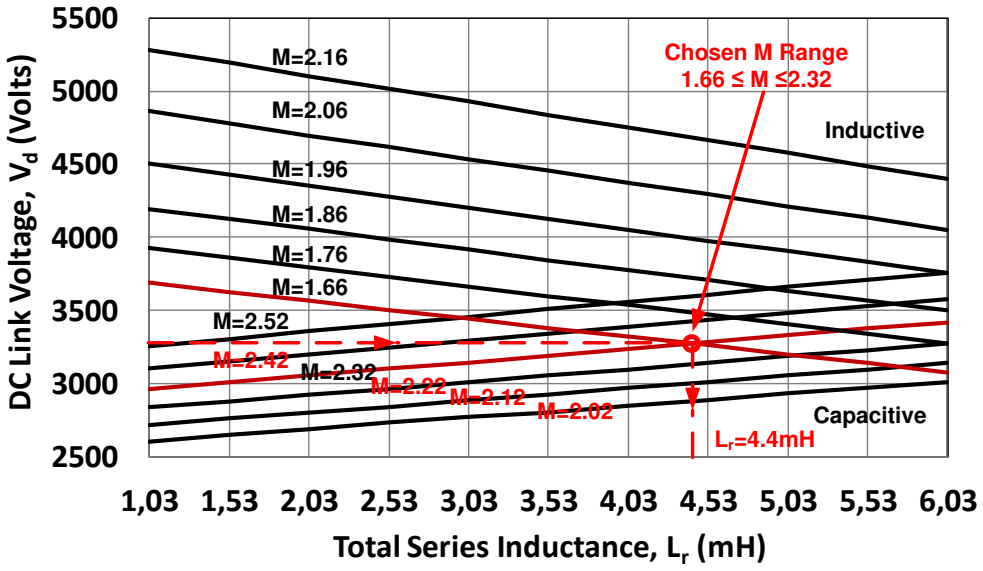


Figure 3.9 Variations in DC link voltage against total series inductance for different values of modulation index, M in the case of CMC with 3HBs/Theoretical

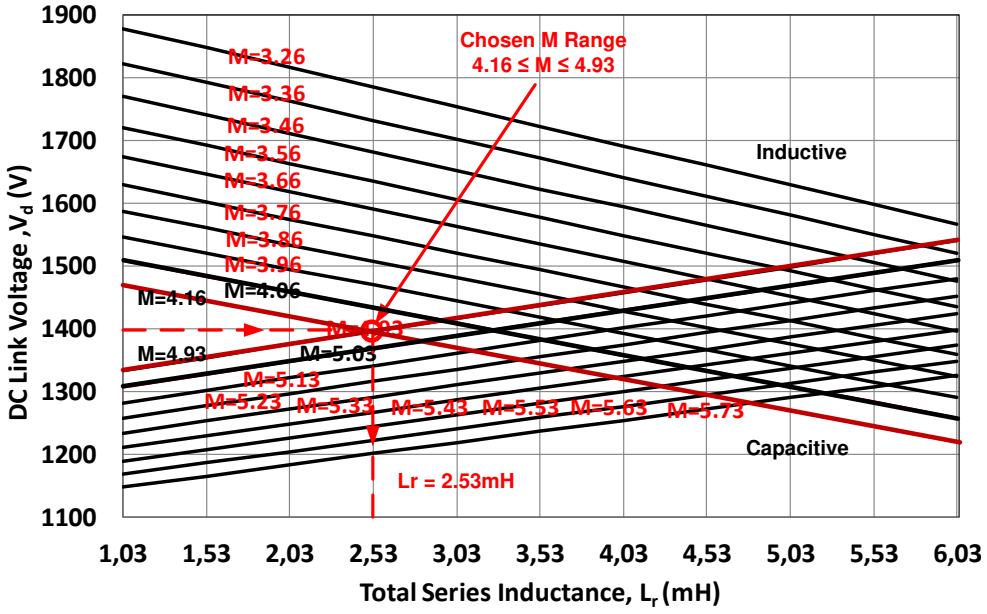


Figure 3.10 Variations in DC link voltage against total series inductance for different values of modulation index, M in the case of CMC with 7HBs/Theoretical

For CMC topology with five HBs, as can be understood from this Figure 3.11, M can be varied between 2.5 and 4.23 for the chosen CMC topology with SHEM. Although such a wide variation range for M improves the resolution in VAr generation, this choice needs a very large L_r resulting in very high CMC voltage regulation and reactor losses. The minimum permissible value of L_r for the field prototype was found to be 2.75mH (Figure 3.8) and maximum safe value of the mean DC link voltage for the chosen HV IGBTs was 1900V (Figure 3.3). If L_r=2.75mH were chosen in the design, M will vary in between 3.63 and 3.10 from full capacitive to full inductive operation mode as shown in Figure 3.11. This is obviously a narrow variation range for M.

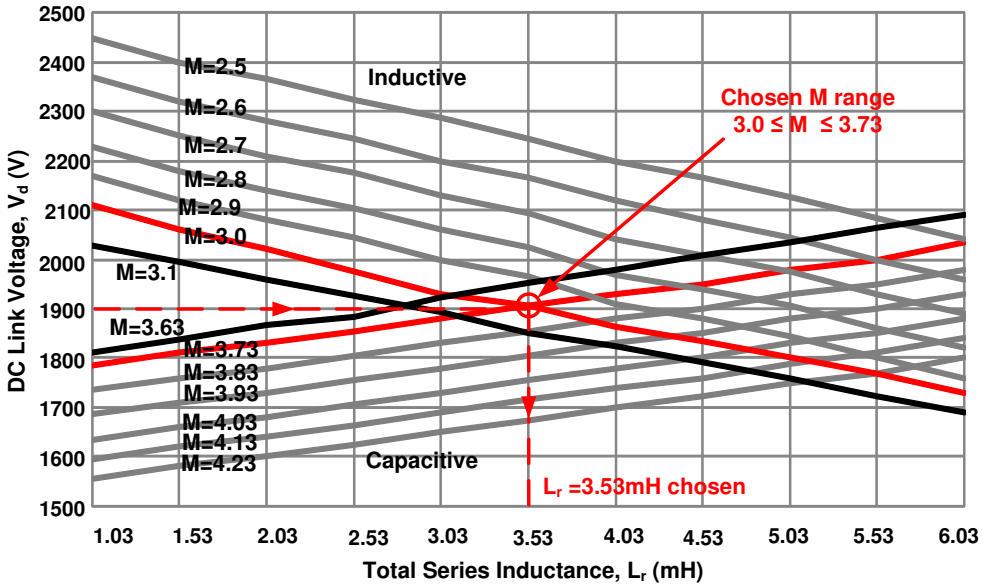


Figure 3.11 Variations in DC link voltage against total series inductance for different values of modulation index, M in the case of CMC with 5HBs/Theoretical

Therefore, in the design and implementation of the field prototype of the T-STATCOM, a total series inductance of L_r = 3.53 mH (1.03 mH transformer leakage

inductance + 2.5 mH series filter inductance on per-phase-Y basis) is chosen as marked on Figure 3.11. This yields an M variation range from 3.0 to 3.73 in keeping DC link voltage constant at V_d=1900 Volts mean. Field test results have shown that owing to the non-idealities in the field prototype of the T-STATCOM system, some variations around V_d=1900V are expected. As observed from the results of the field tests, these variations do not exceed ±12.5 V over the entire operating range in the steady-state, indeed.

3.4.4 Effect of Series Filter Inductance on AC Input Voltage of CMC

Figure 3.12 shows the variations in AC input voltage of CMC topologies with three, five and seven HBs for both full inductive and capacitive operation modes against the series filter inductance. Having large L_r is not desirable because the variation in AC input voltage of the CMC from full inductive operation to full capacitive operation becomes significantly high.

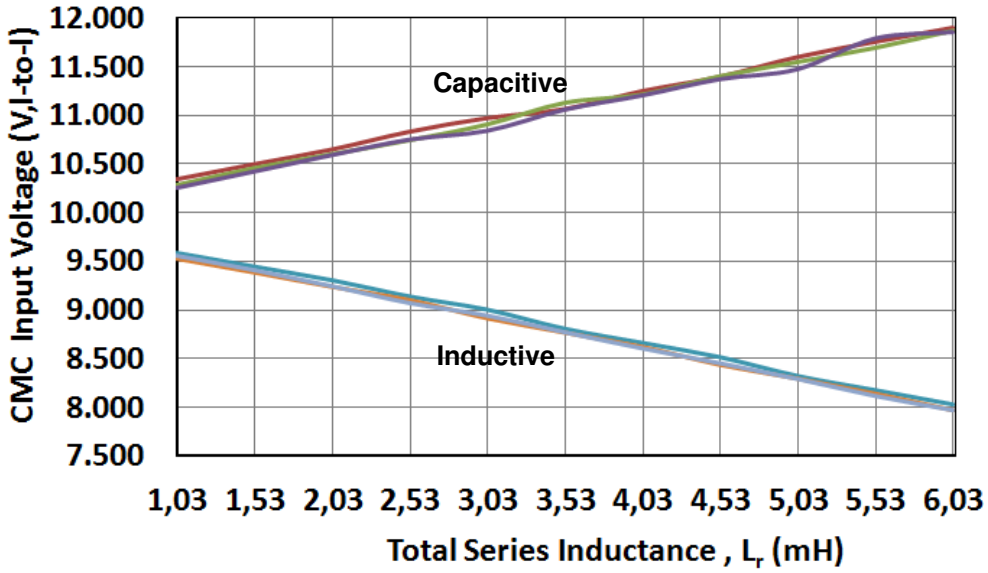


Figure 3.12 Effect of series filter inductance on CMC input voltage

Therefore, in order to keep voltage regulation of the CMC at a reasonable low value, a series filter reactor bank with relatively small L_r should be chosen.

3.4.5 Conclusions

The followings can be concluded from the work carried out in this chapter:

a. When connecting a T-STATCOM system to an existing power transformer, a series filter reactor bank/s should be used for both the use of a single and paralleled CMCs.
b. When specially designed transformer is only used for a T-STATCOM system, the series filter reactor bank may not be used for a single CMC module if leakage reactance of the transformer is sufficient. When CMC modules are used in parallel to reach higher MVAr ratings for T-STATCOM systems, it is compulsory to use series filter reactor banks to share current equally and for control purposes.
c. The maximum attainable VAr rating for CMC modules is largely dictated by the current status of commercially available power semiconductors such as High Voltage Insulated Gate Bipolar Transistors (HV IGBTs).
d. The number of HBs in series for CMC topology is not only the parameter on complying with THD and TDD limits specified in IEEE 519-1992. The series filter inductance value has also a great effect on THD and TDD limits. Therefore, chosing L_r value for CMC topologies is a crucial issue when designing the system.
e. As the value of series filter inductance rises, the THD and TDD values decrease for CMC topologies with three, five and seven HBs while the variations in AC input voltage of the CMC from full inductive operation to full capacitive operation becomes significantly high.
f. There is an optimum point of DC link voltages and M-range values for each CMC topology in view of complying with THD and TDD limits.
g. The effects of series filter inductance value on the system design are shown in Table 3.1.

Table 3.1 The effects of series filter inductance on system design

Subject	Advantages	Disadvantages
The use of larger series filter inductance, L_r	• Lower THD and TDD values • Wider M range, and hence a satisfactory resolution for Q	• High variatons in AC input voltage of CMC • Higher power losses • Higher cost • Higher DC link voltage

h. The comparison of three CMC topologies investigated in this work for the application at 12 kV, ±10MVAr at PCC is shown in Table 3.2.

Table 3.2 The comparison of CMC topologies with three, five and seven HBs

Parameters	CMC Topology of		
	3 HBs	**5 HBs**	**7 HBs**
Series Filter Inductance, L_r (mH)	4.4	3.53	2.53
DC Link Voltage, V_d (Volts)	3250	1900	1400
Modulation Index Range, M	1.66-2.32	3.0-3.73	4.16-4.93
The Resolution for Reactive Power (kVAr)	150	135	130
HV IGBT Module	6.5kV/0.9kA	3.3kV/1.5kA	2.5kV/1.5kA
The Complexity of Control System	Low	Moderate	High
The Complexity of Power Stage	Low	Moderate	High
Applicable to Strong Supply	Yes	Yes	Yes
Applicable to Weak Supply	No	Yes	Yes

Although the implementation of CMC with three HBs is easy in the view of complexity at power stage and control system, it can not be used for weak supply conditions without a very large seris filter inductance values. The CMC with seven

HBs in the best solution for yielding minimum harmonic distortion in line-to-line voltages and line currents, its major drawback is the complexity of the power stage and the control system. Therefore, the CMC topology with five series connected HBs is a compromise between system complexity and maximization of the CMC VAr rating. In this work, a field prototype of 12kV line-to-line, ±10MVAr, 11-level CMC module is designed and implemented by using 3300V, 1200A HV IGBTs.

CHAPTER 4

DESIGN OF A CASCADED MULTILEVEL CONVERTER (CMC) MODULE

4.1 Design of CMC Module

In this work, a 3-phase, Y-connected, 11-level (n=5), ±12MVAr H-Bridge based Cascaded Multilevel Converter (CMC) module shown in Figure 4.1 is designed and implemented. AC voltage of the CMC is chosen to be V_c = 12 kV line-to- line and its constant DC link voltage is V_{dc}=9500V. In each phase of the CMC, five HB circuits are connected in series and the DC link voltage of the designed HB is V_d=1900Volts mean. HB units used in each phase of CMC module have been placed on the shelves which are built up of a specially designed Glass-fiber Reinforced Polyester (GRP) with 3x5 matrix structure as shown in Figure 4.1.

In this section, the design considerations for CMC module and the HB circuit with the selection of its major components like power semiconductors, laminated busbars, and DC link capacitors have been presented. Moreover, the control system with its structure and its major functions for a CMC module is also given in this section. The designed and implemented 12kV, ±12MVAR, 11-level CMC module is the basic

building block for large T-STATCOM systems. It is possible to reach larger MVAr ratings of T-STATCOM systems by parallel use of these CMC modules.

Figure 4.1 Designed and implemented 3-phase, 12kV, ±12 MVAr, Y-connected 11-level CMC module

4.1.1 Design of the H-Bridge (HB) Circuit

H-Bridge circuits are the basic units for the power stages of CMC modules. In fact, **n** number of HBs can be connected in series for each phase of CMC to reach the

desired AC voltage at which CMC is implemented. This gives a modularized circuit layout and packaging for CMC due to the usage of the same structure for each level.

4.1.1.1 The structure and operation of HB Circuits

Figure 4.2 shows the single line diagram of an H-Bridge (HB) circuit with its typical output voltage. In an HB circuit, as power semiconductors, there are four conventional wire-bond HV IGBT modules in which antiparallel diodes are used with IGBT parts in the same packages. These IGBT modules are mounted on cold plates for high power practical applications. The DC link capacitors are connected to these IGBT modules via (+) and (-) DC buses which are designed generally as laminated busbars. Gate Drive (GD) circuits are used to control each IGBT module as shown in Figure 4.2.

The output voltage of an HB circuit have three voltage levels of the, namely $+V_d$, 0 and $-V_d$. The polarity of the output voltage of the HB is positive, and equal to the DC link voltage, $+V_d$ if HV IGBT modules of 1 and 3 are triggerred to conduction while the polarity of output voltage is negative, and equal to $-V_d$ if HV IGBT modules of 2 and 4 are triggerred to conduction as shown in Figure 4.2-b. The operation states of the IGBT and diode parts of the HV IGBT modules are dependent upon the direction of the current. As an example, if polarity of the current flowing through the HB circuit is taken as positive, $+V_d$ is obtained as ouput voltage of HB by the operation of diodes, D1-D3. The same output voltage is also seen by the operation of S1-S3 when current flowing out of the HB. Zero voltage level exits when current is by-passed through the DC link voltages. There are four different current paths formed by the operation of one of the IGBT and diode parts of upper or lower HV IGBT modules to reach zero voltage level as marked on Figure 4.2-b. The operation states of the HB circuit is shown in Table 4.1. The direction of the current is taken as positive when flowing through the HB circuit for the operation states in Table 4.1.

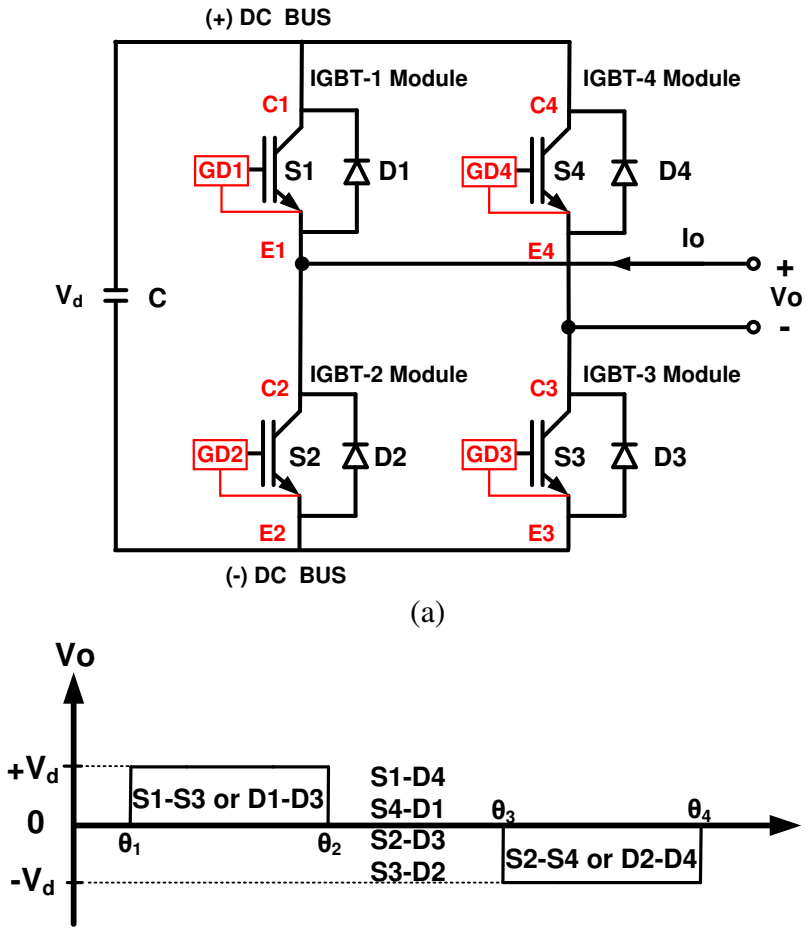


Figure 4.2 Single line diagram of
(a) the HB Circuit and (b) its typical output voltage

Table 4.1 The operation states of the HB Circuit

STATE Number	STATE	Vout	Components Conducting
1	S1-S3 ON;S2-S4 OFF	$+V_d$	D1 and D3 if $I_o>0$ S1 and S3 if $I_o<0$
2	S2-S4 ON;S1-S3 OFF	$-V_d$	S2 and S4 if $I_o>0$ D2 and D4 if $I_o<0$
3	S1-S4 ON;S2-S3 OFF	0	D1 and S4 if $I_o>0$ S1 and D4 if $I_o<0$
4	S2-S3 ON;S1-S4 OFF	0	S2 and D3 if $I_o>0$ S3 and D2 if $I_o<0$

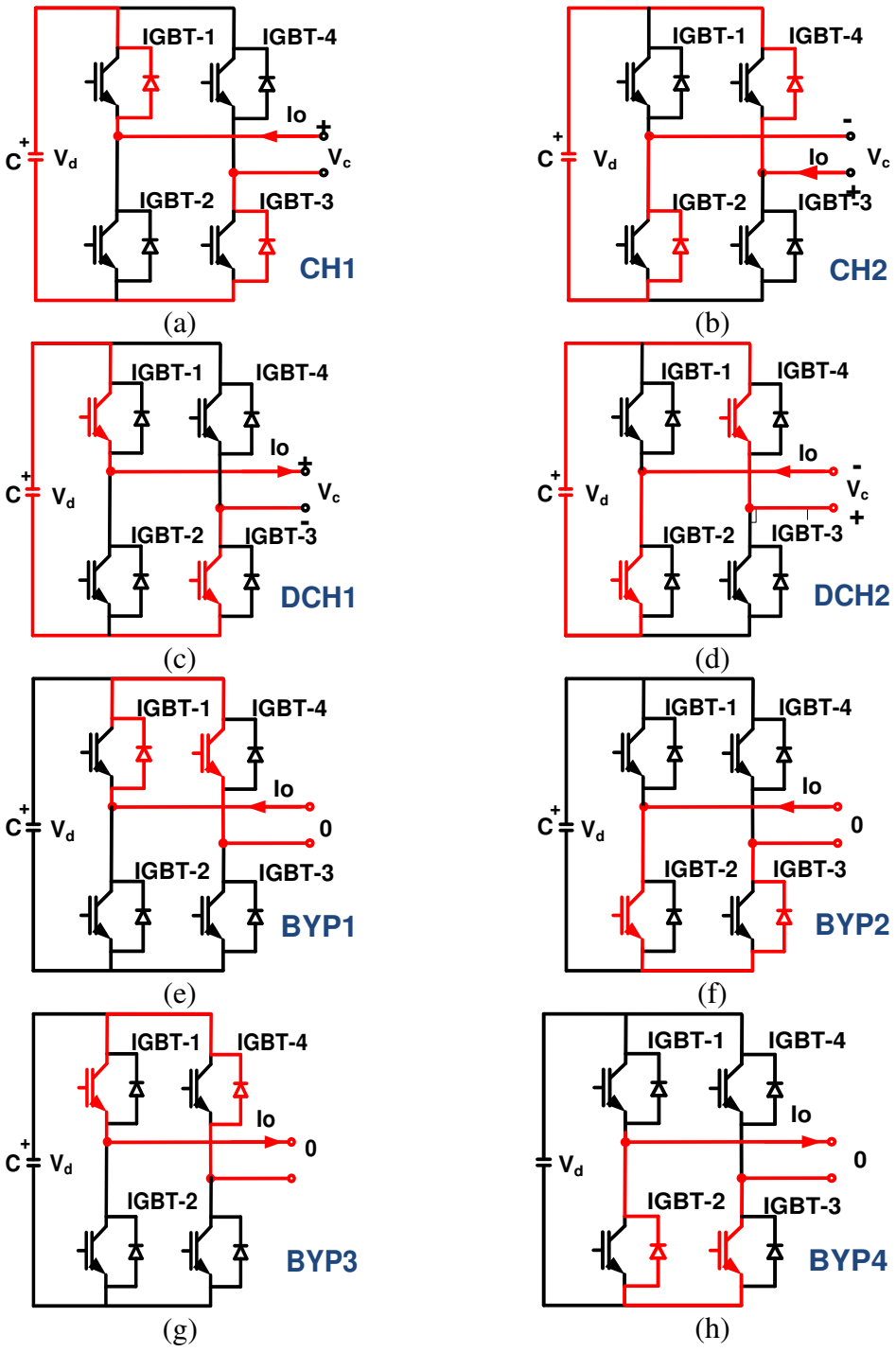
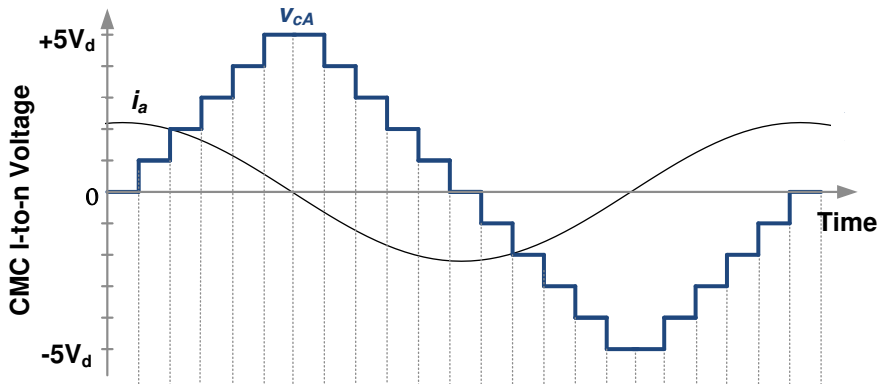


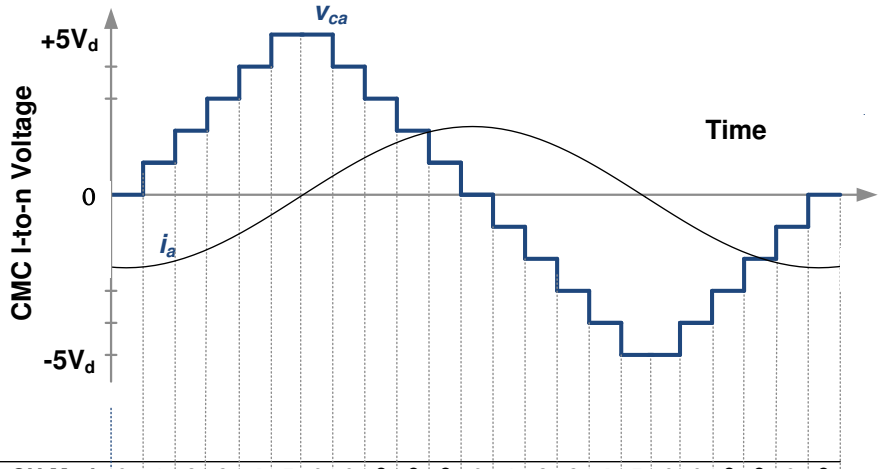
Figure 4.3 The operation modes of HB: a) Charging-1(CH1), b) Charging-2(CH2) ,c) Discharging-1 (DCH1), d) Discharging-2 (DCH2), e) By-pass-1 (BYP1), f) By-pass-2 (BYP2), g) By-pass-3 (BYP3), h) By-pass-4 (BYP4)

To synthesize 11-level line-to-neutral voltage for capacitive mode and inductive of operation modes as seen in Figure 4.4 and Figure 4.5, respectively by using five HBs in each phase of the CMC, at any time each HB circuit should be operated in one of the following modes shown in Figure 4.3: a. **Charging (CH)**, b. **Discharging (DCH)**, and c. **By-pass (BYP)**. All possible operation modes of each HB are marked on Figure 4.4 and Figure 4.5 by CH1, CH2, DCH1, DCH2, BYP1, BYP2, BYP3, BYP4.



Number of HBs in CH Mode	0	1	2	3	4	5	0	0	0	0	0	0	1	2	3	4	5	0	0	0	0	0	0
Operation Mode	-	CH1	CH1	CH1	CH1	CH1	-	-	-	-	-	-	CH2	CH2	CH2	CH2	CH2	-	-	-	-	-	-
Number of HBs in DCH Mode	0	0	0	0	0	0	5	4	3	2	1	0	0	0	0	0	0	5	4	3	2	1	0
Operation Mode	-	-	-	-	-	-	DCH1	DCH1	DCH1	DCH1	DCH1	-	-	-	-	-	-	DCH2	DCH2	DCH2	DCH2	DCH2	-
Number of HBs in BYP Mode	5	4	3	2	1	0	0	1	2	3	4	5	4	3	2	1	0	0	1	2	3	4	5
Operation Mode	BYP1	BYP1	BYP1	BYP1	BYP1	-	-	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	-	-	BYP1	BYP1	BYP1	BYP1	BYP1
Number of HBs in BYP Mode	5	4	3	2	1	0	0	1	2	3	4	5	4	3	2	1	0	0	1	2	3	4	5
Operation Mode	BYP2	BYP2	BYP2	BYP2	BYP2	-	-	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	-	-	BYP2	BYP2	BYP2	BYP2	BYP2

Figure 4.4 11-level line-to-neutral voltage waveform with definition and sequence of HB operation modes for capacitive operation of the CMC



Number of HBs in CH Mode	0	1	2	3	4	5	0	0	0	0	0	0	1	2	3	4	5	0	0	0	0	0	0
Operation Mode	-	DCH1	DCH1	DCH1	DCH1	DCH1	-	-	-	-	-	-	DCH2	DCH2	DCH2	DCH2	DCH2	-	-	-	-	-	-
Number of HBs in DCH Mode	0	0	0	0	0	0	5	4	3	2	1	0	0	0	0	0	0	5	4	3	2	1	0
Operation Mode	-	-	-	-	-	-		CH1	CH1	CH1	CH1	-	-	-	-	CH1	-	CH2	CH2	CH2	CH2	CH2	-
Number of HBs in BYP Mode	5	4	3	2	1	0	0	1	2	3	4	5	4	3	2	1	0	0	1	2	3	4	5
Operation Mode	BYP3	BYP3	BYP3	BYP3	BYP3	-	-	BYP1	BYP1	BYP1	BYP1	BYP1	BYP1	BYP1	BYP1	BYP1	-	-	BYP3	BYP3	BYP3	BYP3	BYP3
Number of HBs in BYP Mode	5	4	3	2	1	0	0	1	2	3	4	5	4	3	2	1	0	0	1	2	3	4	5
Operation Mode	BYP4	BYP4	BYP4	BYP4	BYP4	-	-	BYP2	BYP2	BYP2	BYP2	BYP2	BYP2	BYP2	BYP2	BYP2	-	-	BYP4	BYP4	BYP4	BYP4	BYP4

Figure 4.5 11-level line-to-neutral voltage waveform with definition and sequence of HB operation modes for inductive operation of the CMC

The operation mode of any HB in the CMC at any time and duration of this mode are determined by modulation index value, M and DC link equalization method (MSS with $\Delta t_s = 400\mu s$). Furthermore, M dictates how many of five HBs are to be operated in by-pass mode at any time. As an example, in order to create $+2V_d$ voltage level in line-to-neutral voltage waveform, two HBs should be operated in discharging or charging mode while the others should be operated in by-pass mode.

On the other hand, which HBs are to be operated in charging or discharging mode, is dictated by the equalization algorithm of DC link capacitor voltages. For each step of

the 11-level line-to-neutral voltage waveform, operation modes for all HBs and the number of HBs in each mode are also marked in Figure 4.4 and Figure 4.5. In order to avoid complexity in the explanations, the theoretical line-to-neutral voltage waveform and associated table are prepared for Conventional Selective Swapping (CSS) method. However, in this work Modified Selective Swapping (MSS) method has been applied to prototype CMC in order to obtain a better equalization of DC link capacitor voltages. Therefore, on $\pm V_d$, $\pm 2V_d$, $\pm 3V_d$, and $\pm 4V_d$ voltage levels, two switchings from one HB to another HB on the average may take place according to MSS algorithm with Δt_s =400µs as shown in Figure 4.6.

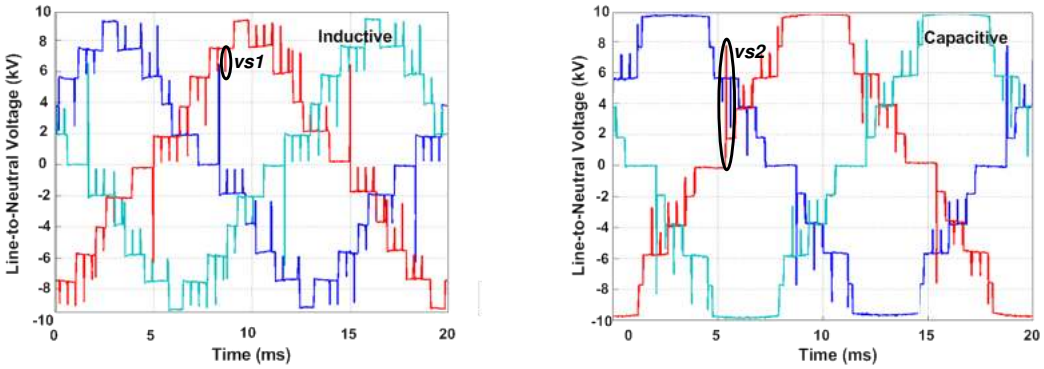


Figure 4.6 Voltage spikes superimposed on the line-to-neutral CMC voltages with MSS method (Δts =400µs, field data)

In other words, at each swapping instants, the operation mode of one HB is changed from charging or discharging mode to by-pass mode while the operation mode of another HB is from by-pass mode to charging or discharging mode. Voltage spikes arising from the application of MSS method and superimposed on 11-level line-to-neutral voltage waveforms do not lead to an operational problem for the T-STATCOM and power system because they are successfully suppressed by the total

series reactance as can be observed from line-to-neutral voltage waveforms in Figure 4.7 recorded by the Resistive-Capacitive voltage transformers at 154kV PCC.

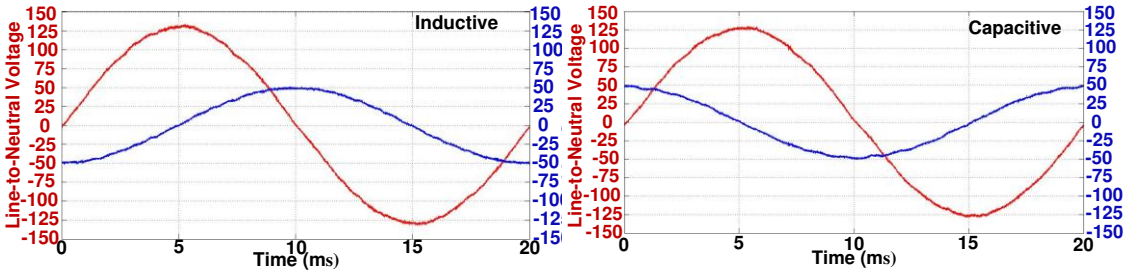
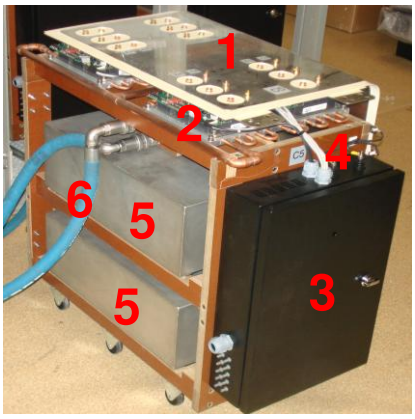


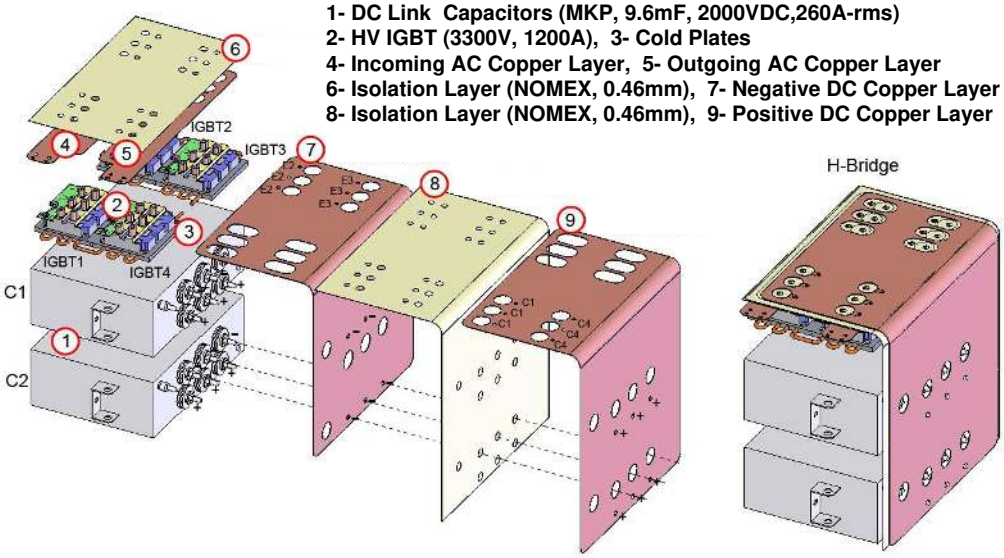
Figure 4.7 Line-to-neutral voltage and line current waveforms recorded in the field at 154kV PCC

The general view and structure of the HB unit designed in this work are shown in Figure 4.8. The compact, and withdrawable, ±840 kVAr HB unit has a laminated L-shape laminated busbar system with minimized stray inductance of L_{stray}=75nH and two pairs of 3300V, 1200A, wire-bond HV IGBTs (Mitsubishi, CM1200HB-66H) mounted on two cold plates (R-Theta). Fiber reinforced composites (FRC) were used as the construction materials for HBs to keep clearances at a minimum, and to have a strong mechanical structure. Further flexibility is achieved by quick couplings for water connection to cold plates and by using some special connectors for connection of fiber optics and the power supply cables entering to the front panel.



1- L-Shaped Laminated Busbars
2- 3.3kV, 1.2kA HV IGBTs with drive circuits
3- Front Panel with optical connectors
4- Fiber Reinforced Composite based structure
5- DC link capacitors connected in parallel
6- Flexible water hoses with quick couplings

(a)



(b)

Figure 4.8 General view (a) and structure (b) of the designed HB

4.1.1.2 L-shaped Laminated Bus Design with 3-conducting Layers

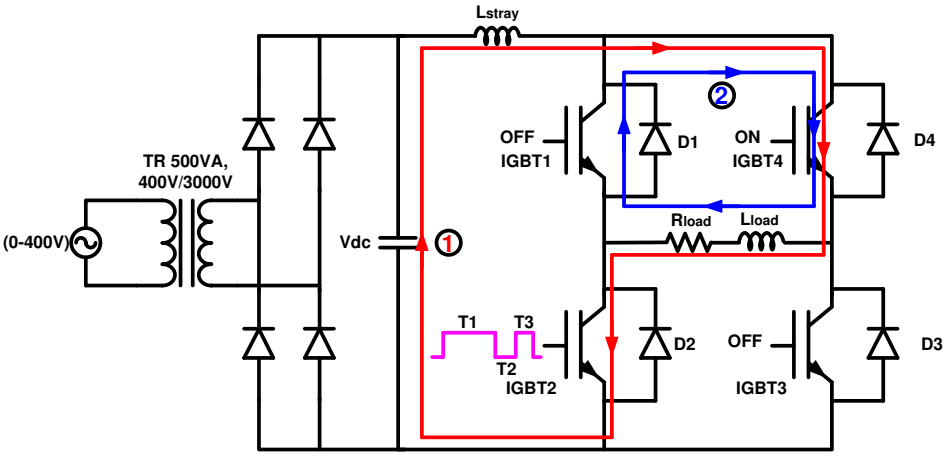
Minimization of stray inductance between HV IGBT modules and DC link is the most critical part of the power stage design. During the turn-on period of an HV IGBT part of the module, for example in the upper half of HB, the complementary

free-wheeling diode in the lower half turns off. If the total stray inductance can be kept at a sufficiently low value (less than 100nH), the HV IGBT turns on in 500ns-1.5µs, as given in manufacturer datasheets. On the other hand, it is advantageous to have a large stray inductance during turn-on period in order to maintain a slower rise of the collector current, i_c, thus, reducing the reverse recovery current of the complementary free-wheeling diode in the same leg and keeping the operating point in its safe operating area. This will obviously increase turn-on losses. However, the presence of a large stray inductance than the usual values leads to serious problems in the turn-off period of the HV IGBT. In this period, voltage across the stray inductance $L_{stray}(di_c/dt)$ which is superimposed on the DC link voltage, V_d will then appear across collector-emitter terminals of outgoing HV IGBT. If V_{ce} exceeds 2400V for the chosen 3.3kV/1.2kA HV IGBT Module, IGBT may enter to the active region as a result of active clamping property of the standard IGBT drivers [26]. In this work, a compromise is made between the turn-on and turn-off behaviors of the HV IGBTs. This is achieved by the followings:

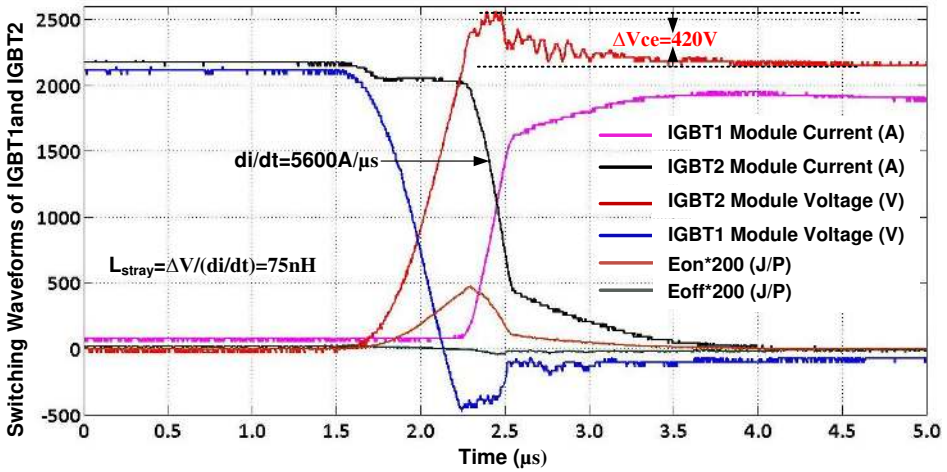
1. Using laminated bus technology, L_{stray} is reduced to 75nH for each HB;
2. By modifying the standard IGBT driver circuit, turn-on time is prolonged to 2.5µs;
3. Using DC link capacitors with very low equivalent series inductances (L_{self}=50nH//50nH) and directly mounting them on the laminated bus to minimize the wiring inductance.

Turn-on and turn-off performances of HV IGBT modules in the HB shown in Figure 4.9 are recorded in the laboratory by using the test circuit in Figure 4.9-a. The gate signal applied to IGBT2 module is also marked on the same figure. During this test, first IGBT2 and IGBT4 are turned on (current path-1 in Figure 4.9-a) and then IGBT2 is turned off resulting in free-wheeling path-2 in order to obtain turn-off behavior of IGBT2. Finally, IGBT2 is retriggered into conduction before reverse recovery current ceases in order to obtain reverse recovery current of the anti-parallel diode of the IGBT1 module. The variations in voltages and currents of two HV IGBT

modules in the same leg and their turn-on and turn-off losses are plotted in Figure 4.9-b. From the results of these tests, ΔV_{ce} and di_c/dt are measured to be 420V and 5600A/µs, respectively. These yield $L_{stray}= \Delta V_{ce}/(di_c/dt)$=75nH. Since operating point remains in the Safe Operating Area (SOA) of the IGBT part, no need to use a snubber circuit.



(a)



(b)

Figure 4.9 Performance of HB in the Laboratory (a)Test Circuit, and (b) switching waveforms of IGBT1, D1and IGBT2

4.1.1.3 Selection of Power Semiconductor Switches

The computer simulation results carried out by EMTDC/PSCAD program for switching waveforms of power semiconductors have been showed in Figure 4.10 - Figure 4.15 for the cases of full capacitive (-10 MVAr) and full inductive (+10 MVAr) operation modes at the Point of Common Coupling (PCC) during steady state conditions. The DC link voltages of HBs in CMC are kept constant at 1900VDC for both cases. Conventional Selective Swapping (CSS) and Modified Selective Swapping (MSS) Methods have been applied to the system to get familiar about the effective switching frequencies of power semiconductors. The CSS is applied at level changes while MSS is applied not only level changes but also mid levels at a specified time of Δt_s.

The current waveforms of all power semiconductors, I_{sw1}, I_{sw2}, I_{sw3} and I_{sw4} are shown with the output voltage of the AC voltage of HB1 of phase-A and 11-level phase-A line-to-neutral voltage of CMC module under CSS method, MSS method with $\Delta ts=200\mu s$ and MSS method with $\Delta ts=400\mu s$ for the equalization of DC link capacitors. The power semiconductors of SW1 (upper half) and SW2 (lower half) constitute one leg of HB circuit while the power semiconductors SW3 (lower half) and SW4 (upper half) constitute the other leg.

For all current waveforms of power semiconductor switches showed in Figure 4.10 - Figure 4.15, the inverse parallel diodes are operating at the positive cycles while the IGBT parts are operating at the negative cycles. By inspecting the AC voltage of HB, line-to-neutral voltage of CMC voltage and current waveforms of the switches as shown in Figure 4.10 - Figure 4.15, it can be easily understood the charging (CH), discharging (DCH) and By-pass (BYP) operation modes of HB circuit which are marked as A, B and C, respectively as well as the instants of selective swapping operation. For example, since the direction of current and the polarity of HB output

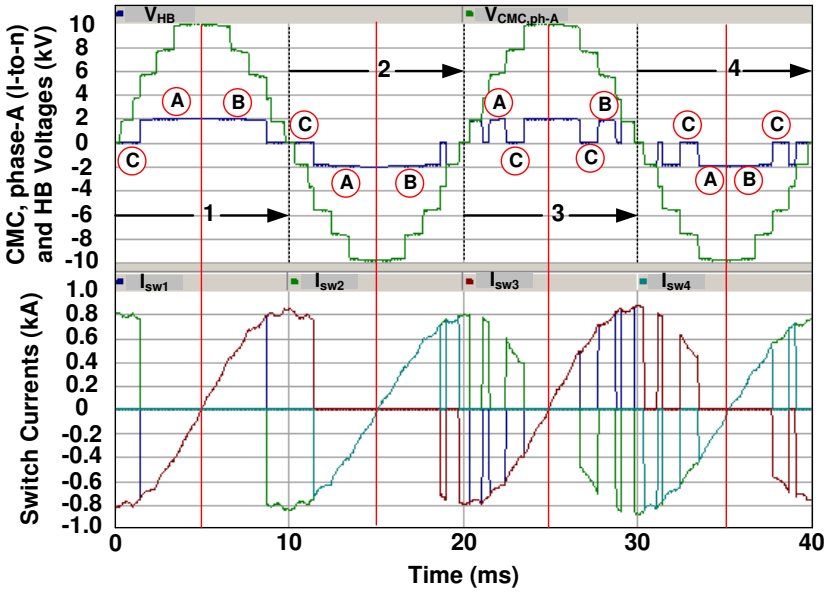


Figure 4.10 Power semiconductors current, HB output and CMC l-to-n voltages waveforms for Q=-10MVAr at PCC with CSS method (PSCAD Simulations)

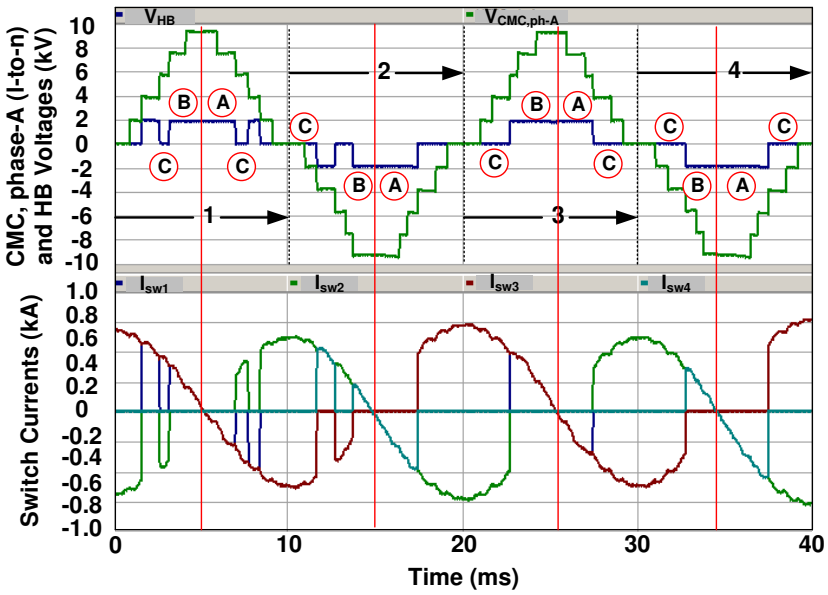


Figure 4.11 Power semiconductors current, HB output and CMC l-to-n voltages waveforms for Q=+10MVAr at PCC with CSS method (PSCAD Simulations)

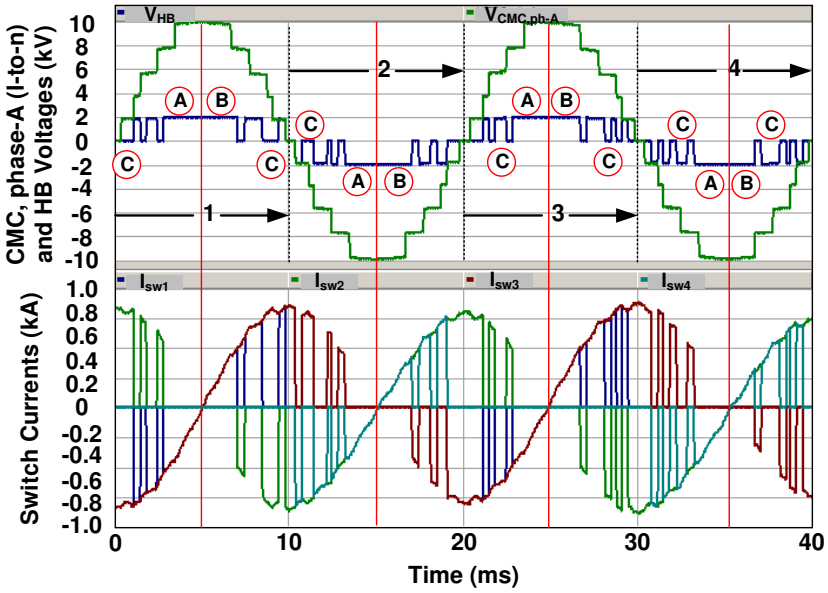


Figure 4.12 Power semiconductors current, HB output and CMC l-to-n voltages waveforms for Q=-10MVAr at PCC with MSS method at Δt_s=400µs (PSCAD Simulations)

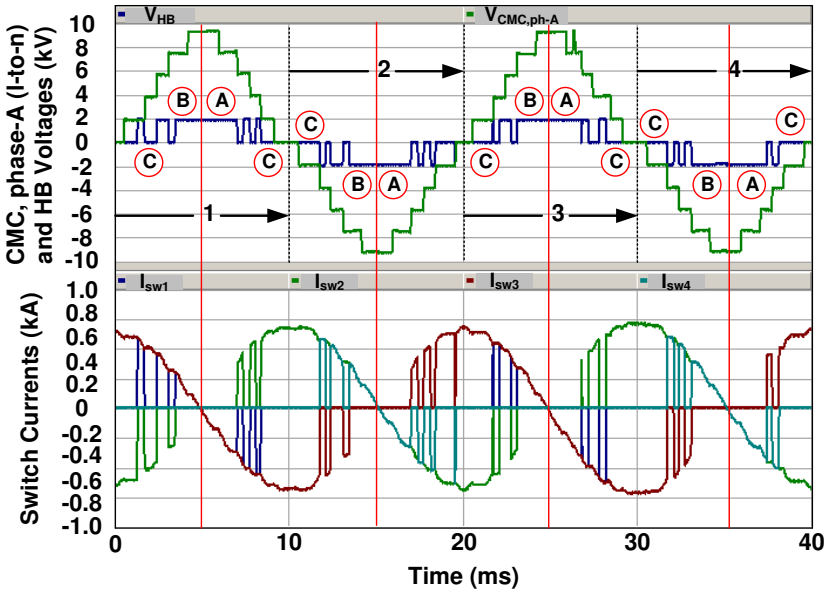


Figure 4.13 Power semiconductors current, HB output and CMC l-to-n voltages waveforms for Q=+10MVAr at PCC with MSS method at Δt_s=400µs (PSCAD Simulations)

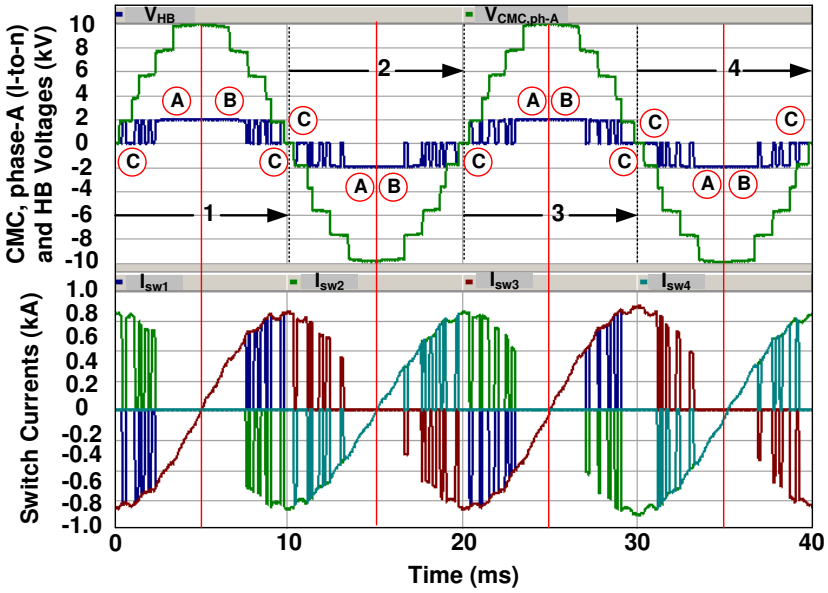


Figure 4.14 Power semiconductors current, HB output and CMC l-to-n voltages waveforms for Q=-10MVAr at PCC with MSS method Δt_s=200µs (PSCAD Simulations)

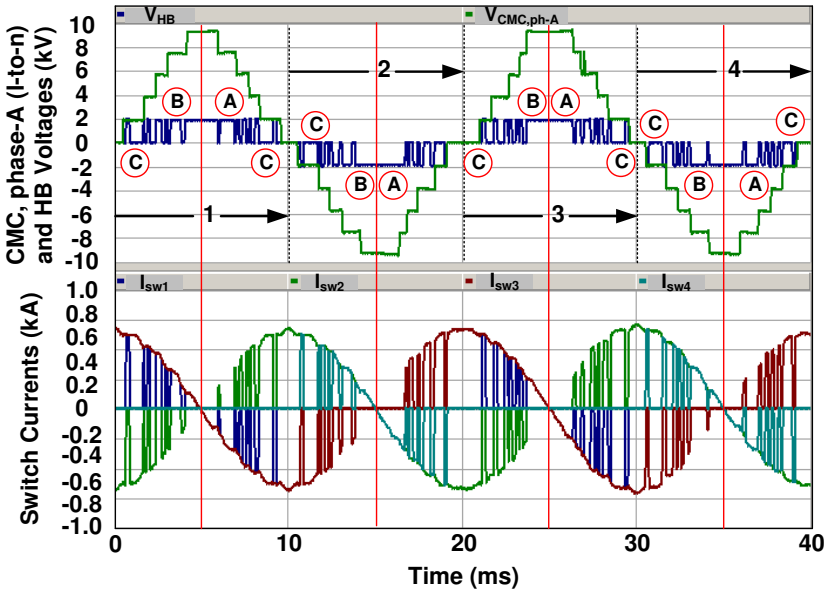


Figure 4.15 Power semiconductors current, HB output and CMC l-to-n voltages waveforms for Q=+10MVAr at PCC with MSS method at Δt_s=200µs (PSCAD Simulations)

voltage is positive between 0 to 5ms at the point marked as A in Figure 4.10, the investigated HB circuit is in charging (CH) mode from 2kV level which is $+V_d$ to 10kV level which is $+5V_d$. However, the same HB circuit is in operation from 10kV level to 2kV level while the direction of the current is negative and the polarity of HB output voltage is positive. During that time, HB is in discharging (DCH) mode and marked as B on the same figure. After that the AC voltage of HB becomes zero which means it is in by-pass (BYP) mode and the operation of swapping occurs at this instant.

The points of C marked on Figure 4.10 - Figure 4.15 are the instants of selective swapping operations for both CSS and MSS methods. In CSS method, these instants occur at the level changes as shown in Figure 4.10 and Figure 4.11, while for MSS methods they may occur at mid levels as well as the level changes as shown in Figure 4.12 - Figure 4.15. As the number of zero voltage levels marked by C in the line-to-neutral voltage waveforms increases it means the power semiconductors are frequently switched. Therefore, the effective switching frequency of semiconductors under MSS method is more than those under CSS method as shown in Figure 4.10 - Figure 4.15. Moreover, the effective switching frequency of power semiconductors under MSS method with Δt_s=200µs is higher than those of MSS method with Δt_s=400µs for both inductive and capacitive operation modes as can be seen the numbers of A, B and C marks on the Figure 4.12 - Figure 4.15.

Table 4.2 shows the number of swappings and the effective switching frequency of power semiconductors of the HB1 of the CMC under CSS and MSS methods for both full capacitive and full inductive operations during two power frequency cycles (40 ms). The effective switching frequency for power semiconductors has been calculated as the number of pulses for each switch in 1 second.

Table 4.2 Effective Switching Frequency of Semiconductors with CSS and MSS methods

Method	Operation Mode	The number of swappings	The effective switching frequency of power semiconductors			
			f_{sw1}	f_{sw2}	f_{sw3}	f_{sw4}
CSS Method	**Inductive**	8	100	125	100	75
	Capacitive	13	150	150	150	150
MSS Method with Δt_s=400µs	**Inductive**	20	225	275	275	250
	Capacitive	25	275	300	350	325
MSS Method with Δt_s=200µs	**Inductive**	45	700	675	650	675
	Capacitive	42	600	550	550	625

According to Table 4.2, the maximum effective frequency value has been obtained as 700Hz for SW1 during full inductive case of MSS method with Δts=200µs. Therefore, the power semiconductor to be chosen for HB units should have ability to be switched with this frequency. Since the DC link voltage has been chosen 1900V and the maximum switch current is around 800A,peak as seen from the simulation results given in Figure 4.10 - Figure 4.15, 3300V, 1200A HV IGBT can be used for this application. In the literature [26], it is stated that HV IGBTs with the ratings of 3300V and 1200A can be used for the frequency range of 0.8 kHz - 2.0 kHz. However, it is recommended to use these devices at most 1 kHz to reduce the converter losses to 1% of total losses [26]. Since the maximum switching frequency is below 1 kHz for designed CMC, 3.3kV/1.2kA HV IGBT modules can be safely used.

There are different manufacturers producing 3300V, 1200A HV IGBT modules in the market. HV IGBT modules produced by Mitsubishi (CM1200HC-66H) and DYNEX (DIM1200ESM33-F000) have the best performance when comparing them with others in view of both conduction and switching losses. However, Mitsubishi

CM1200HC-66H has been selected as power semiconductor switches for this application because of short lead time and the lower cost.

The failure rate (FIT) is one of another significant criterion for selection of HV IGBT modules. The failure rate of power semiconductor switches is directly dependent on the applied voltage. Powerful cosmic rays flow through the semiconductors when exposed to high voltage for a long time and the device may destruct abruptly [55]. The cosmic ray withstand capability of the semiconductors are explained by the curves showing the applied voltage versus 100FIT failure rate. 1 FIT failure rate is equal to one failure at 10^9 hours. The cosmic ray withstand capability of the CM1200HC-66H has been showed in Figure 4.16 [55].

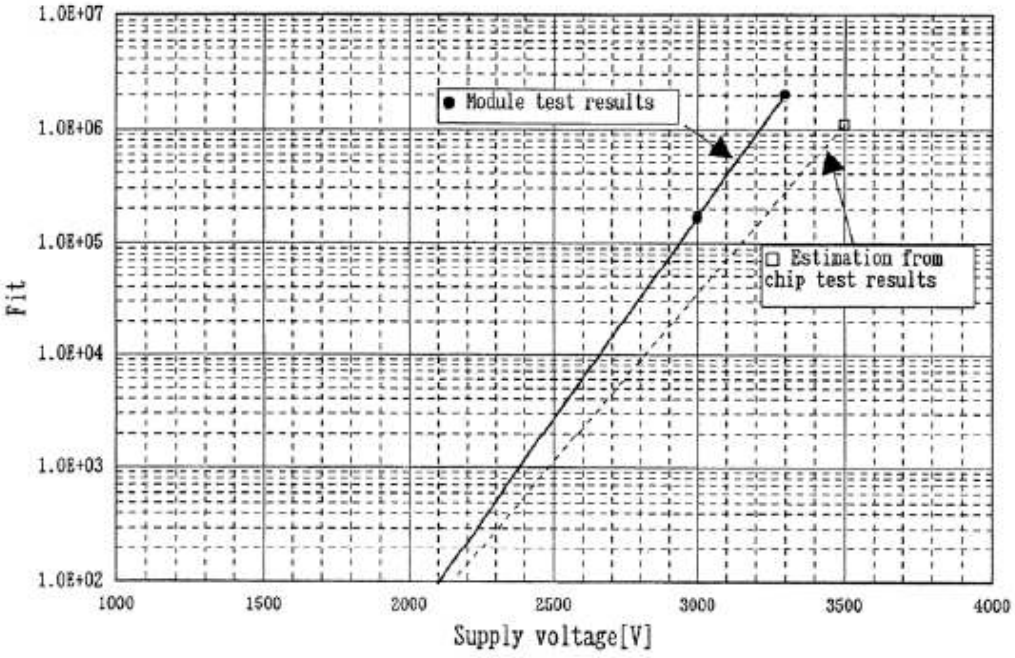


Figure 4.16 Relationship of FIT values and applied DC link voltages for Mitsubishi CM1200HC-66H HV IGBT [55]

It is seen that the DC link voltage at 100FIT is 2100V. FIT rate is increasing drastically when exceeding this limit value. Therefore, 3300V, 1200A HV IGBTs should not be exposed to the voltage over 2100V for all operating conditions to extend their lifetime.

4.1.1.4 Optimization of IGBT Switching Waveforms

Figure 4.9-a in Subsection 4.1.1.2 has been used as the IGBT switching test circuitry with the passive elements of L_{stray}=75nH, R_{load}=1Ω and L_{load}=200µH for HB units in the laboratory. IGBT1 and IGBT 3 modules are turned off, and IGBT4 module is turned on for the whole test duration. Consecutively, a turn-on signal of 1.2ms, a turn-off signal of 30µs and second turn-on signal of 100µs have been applied to IGBT2 module. During the first turn-on time, the current circulates through the path-1 (DC link capacitors, IGBT4, R_{load}, L_{load}, IGBT2) and rises to a value of 2100A for IGBT under a DC link voltage of 2100V. Applied turn-off signal to IGBT2 module, the current flows through the diode part of IGBT1, D1 (current path-2) for a time of 30µs and then another turn-on signal is applied to IGBT2. Therefore, the turn-on and turn-off waveforms are recorded for IGBT1 and IGBT2 modules. During the turn-on of IGBT2 module, the reverse recovery characteristic of the inverse parallel diode of IGBT1 is also obtained. Turn-on and turn-off performances of HV IGBT modules used in the HB shown in Figure 4.8 are recorded in the laboratory by using the test circuit in Figure 4.9-a.

The worst case in the transient state is taken to be the transition of the operating point for T-STATCOM from full capacitive to full inductive or vice versa in nearly 80-100ms. Moreover, if the standard IGBT driver circuit were not modified to prolong the turn-on time to 2.5µs, IGBT module voltage and current waveforms would be as in Figure 4.17 for the defined the worst case. By use of standard gate drive circuits, diode reverse recovery current, I_{rr} reaches 1500A and peak turn-on current of IGBT tends to exceed 2400A. Although the actual SOAs are wider than those of datasheets

specified by the device manufacturer (APPENDIX-D), the use of a standard driver circuit will shorten the economic life of HV IGBT modules. That is why the IGBT driver circuit is modified in this research work.

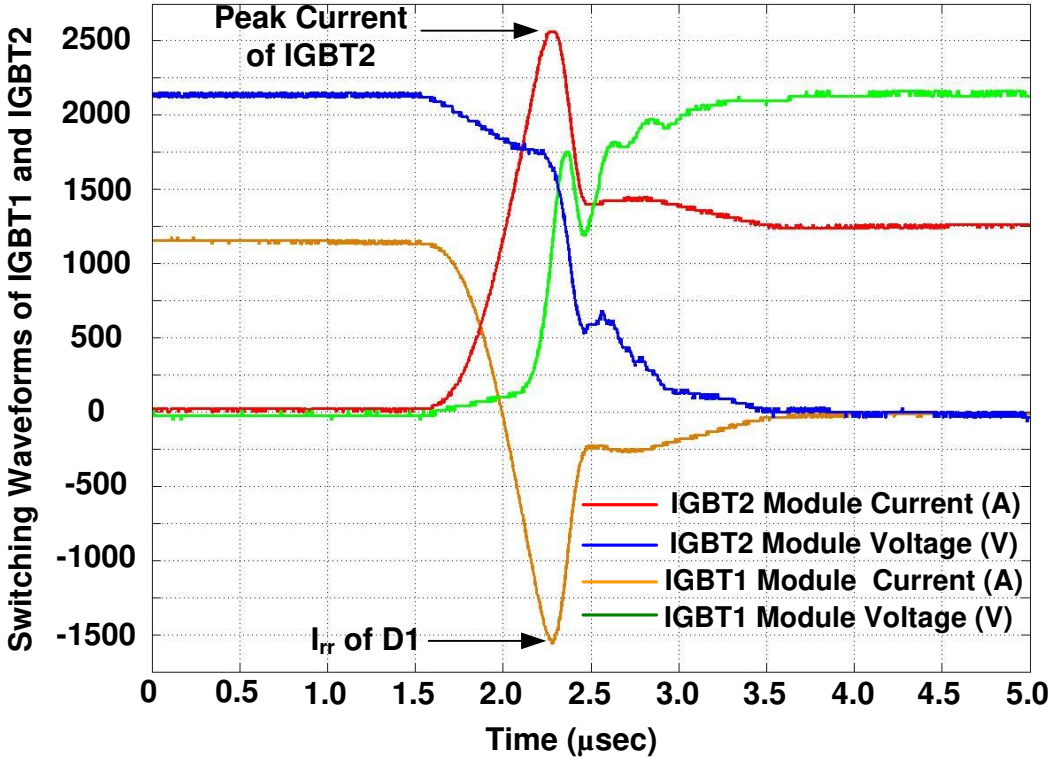


Figure 4.17 The switching waveforms during turn-on of IGBT2 with standard gate driver circuit at nearly I_c(rated)

For the purpose of the decreasing the I_{rr} and hence peak turn-on currents of related HV IGBT modules, the modification is made on the gate drive circuits by increasing the turn-on control resistance, $R_{g(on)}$ from 2.0 Ω to 3.2 Ω. After modifying gate driver circuit, the turn-on time is found to be 2.5µs for HV IGBT modules. This reduces reverse recovery current of anti-parallel diodes to I_{rr}=1250A and hence peak turn-on current of IGBT2 to 2250 A as shown in Figure 4.18 for the worst case in the

transient state of the CMC operation. Therefore, after modification made on driver circuits, the diode and IGBT parts of HV IGBT modules can be safely operated since their current and voltage magnitudes remain inside the related SOAs.

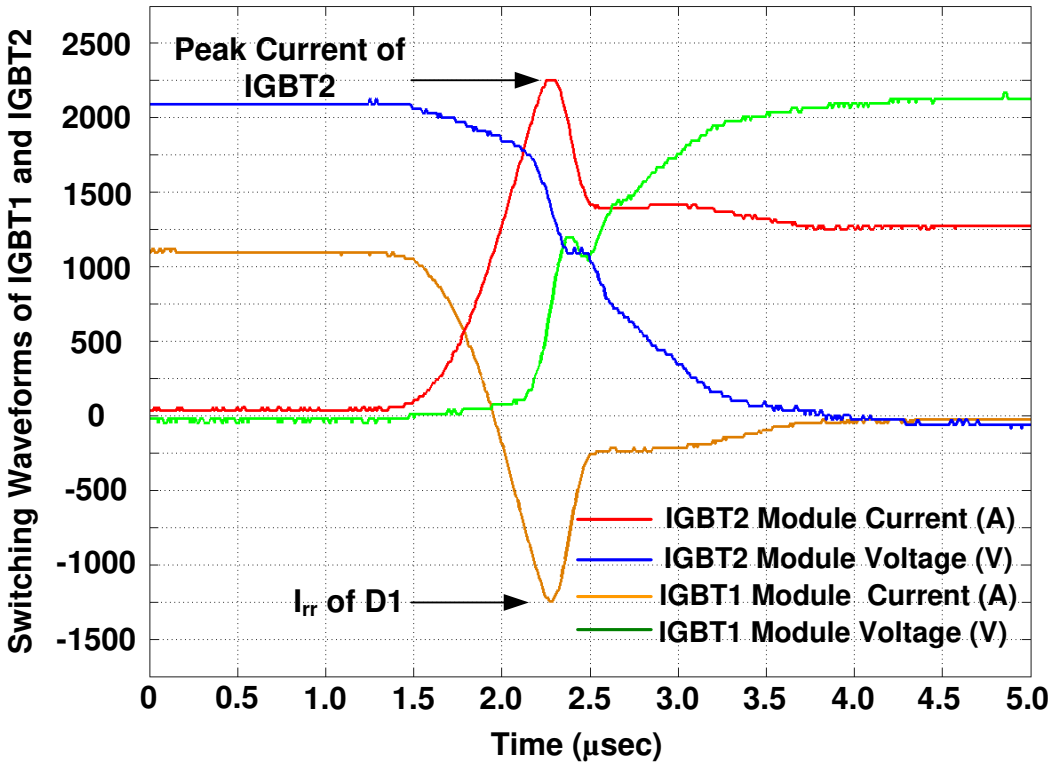


Figure 4.18 The switching waveforms during turn-on of IGBT2 with modified gate driver circuit at nearly I_c(rated)

Moreover, reducing the reverse recovering current of diode part will negatively effect the turn-on loss, E_{on} of IGBT part. That is the E_{on} value of the HV IGBT inreases. However, the reverse recovery loss, E_{rr} of diode part decreases. The comparisons of diode reverse recovery and IGBT peak currents with turn-on and

reverse recovery losses for diode and IGBT parts of the modules have been given in Table 4.1 for the use of standard and modified gate driver circuits.

Table 4.3 The comparison of diode reverse recovery and IGBT peak currents, and turn-on and reverse recovery losses for IGBT modules

The Parameters under investigation	The use of Standard Gate Driver Circuit	The use of Modified Gate Driver Circuit
Turn-on Resistance, $R_{g(on)}(\Omega)$	2.0	3.2
Diode Reverse Recorvery Current, I_{rr}(A)	1500	1250
IGBT Peak Turn-on Current	2600	2250
Turn-on Loss, E_{on} (J/pulse)	2.08	2.44
Reverse Recovery Loss, E_{rr} (J/pulse)	0.69	0.62

Although reverse recovery loss, E_{rr} of the diode part decreases by a percentage of 10.11%. the turn-on loss, E_{on} of the IGBT part increases by a percentage of 17.30% as can be seen from Table 4.3.

4.1.1.5 Choice of DC Link Capacitor

In the DC link of each HB, low-ESR and -ESL power electronic capacitors are to be used. In the design work, the variations in peak-to-peak ripple content of the capacitor voltage, δV_d against DC link capacitance are calculated by simulations and the variations in δV_d are given in Figure 4.19 when CMC is under CSS method for the equalization of the DC link capacitor voltages of each HB unit. Among the DC link equalization methods employed in this work, since it gives the maximum percentage of peak-to-peak variation in DC link voltage for the same value of capacitance as shown in Table 2.7 and Table 2.8 in Chapter-2, CSS method is applied for the DC link capacitor voltage the equalization method for all simulations

carried out in this subsection as the worst case. Moreover, the total series filter inductance has been taken as 3.53mH for the simulations.

For the chosen HV IGBT modules, the DC link voltage of each HB was taken to be 1900V DC. It is kept constant in the steady-state over the entire operating range of the T-STATCOM by controlling the active power flow from the supply and also by the DC link capacitor voltage equalization method applied to the CMC.

In view of the maximum allowable ripple content, 10% ripple content in DC link voltage of 1900V is taken as a rule of thumb. Therefore, the DC link capacitance of each HB is chosen to be 9.2mF to have peak-to-peak variations in DC link voltages of the designed CMC lower than the specified limit both for inductive and capacitive mode of operations as shown in Figure 4.19.

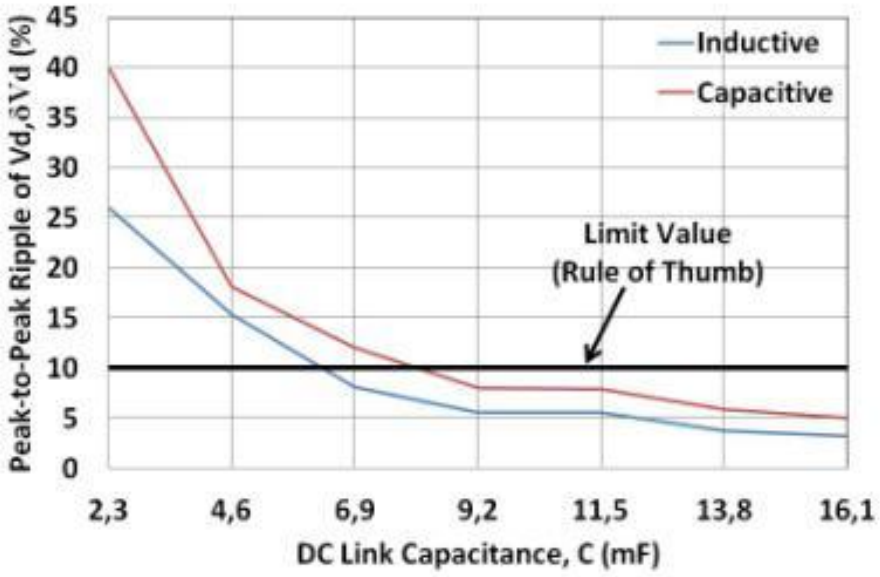


Figure 4.19 The variations in peak-to-peak voltage ripple against capacitance value

9.2mF is implemented by using two paralleled 4.6mF DC link capacitor units as shown in Figure 4.8. By this way, equivalent series inductance and resistance of DC link capacitor bank are halved.

Some sample results of simulations carried out for DC link capacitors are given in Figure 4.20 and Figure 4.21 for both full capacitive and full inductive operations of 11-level ±10MVAr CMC having 9.2mF capacitance value and 1900V DC for each HB unit. In Figure 4.20 and Figure 4.21, the DC link voltage and current variations and the output voltage of HB1 in phase-A for 100ms duration are presented. The charging (CH), discharging (DCH) and by-pass (BYP) modes for HB1 can be understood from Figure 4.20 and Figure 4.21 by evaluating the DC link capacitor voltage and current with the output voltage of HB1.

The regions marked on Figure 4.20 by pink dashed lines from 1 to 5 are corresponding CH, DCH, BYP, CH and DCH modes, respectively for -10 MVAr capacitive operation while those marked on Figure 4.21 are corresponding DCH, CH, BYP, DCH and CH, respectively for 10 MVAr inductive operation of the designed CMC. Since the line current is advanced by 90 degrees from HB1 output voltage for full capacitive operation, in region 1 given in Figure 4.20, the direction of the line current is positive. The polarity of HB1 output voltage is also positive at the same region. Therefore, the DC link capacitor of HB1 is charged and the DC link voltage is increasing. The direction of the line current of CMC is changed from positive to negative in region 2 of Figure 4.20 while the polarity of the HB1 output voltage is positive and hence the DC link capacitor starts to discharge. Therefore, the DC link voltage is decreasing. When the HB1 output voltage is at zero voltage, the DC link capacitor is by-passed and hence the DC link voltage is constant for this operation mode shown as region 3 in Figure 4.20. The same expression can be done for inductive mode of operation as shown in Figure 4.21.

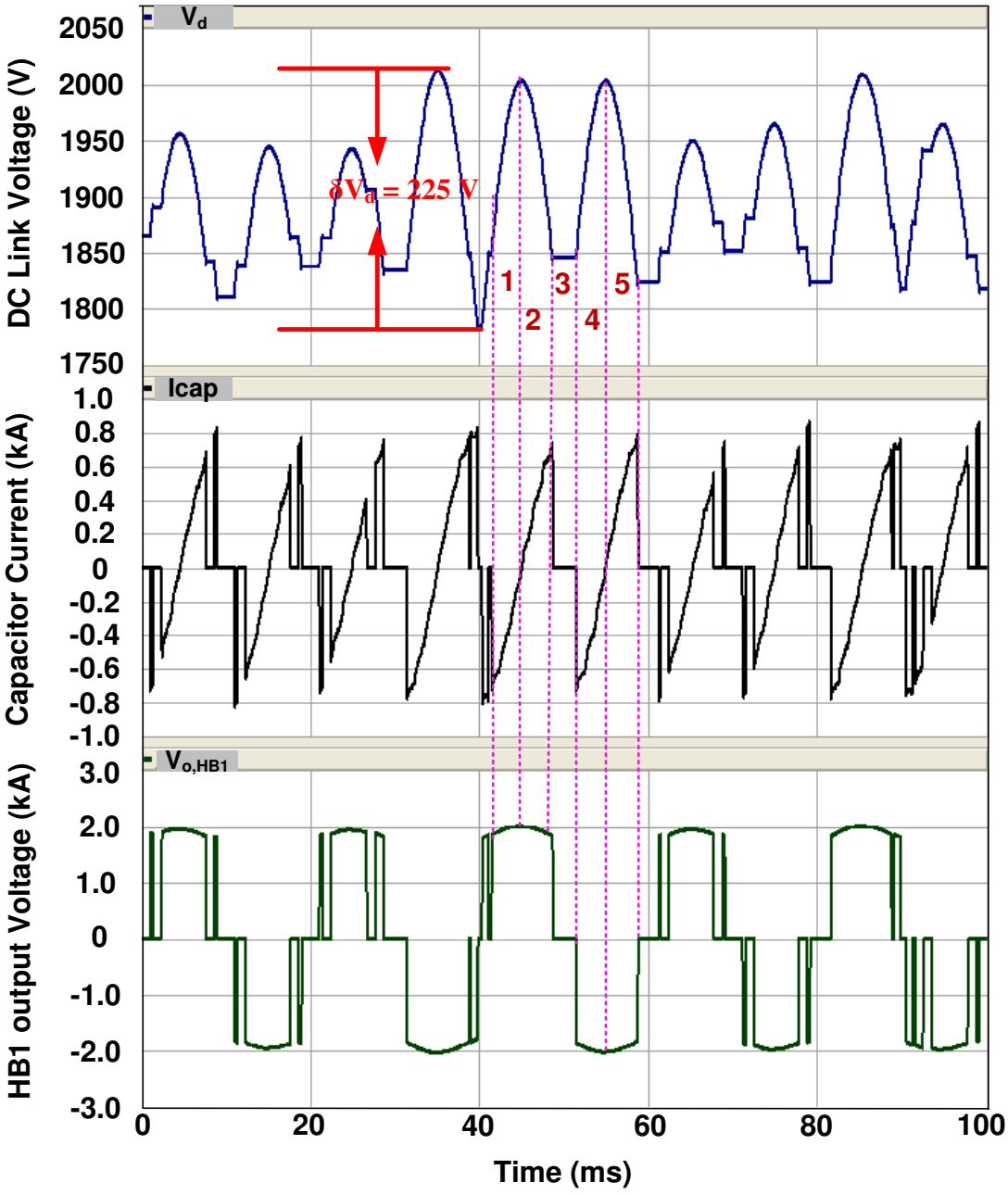


Figure 4.20 The variations in DC link voltage and current of HB1 with its output voltage for Q=-10 MVAr at PCC (PSCAD Simulations)

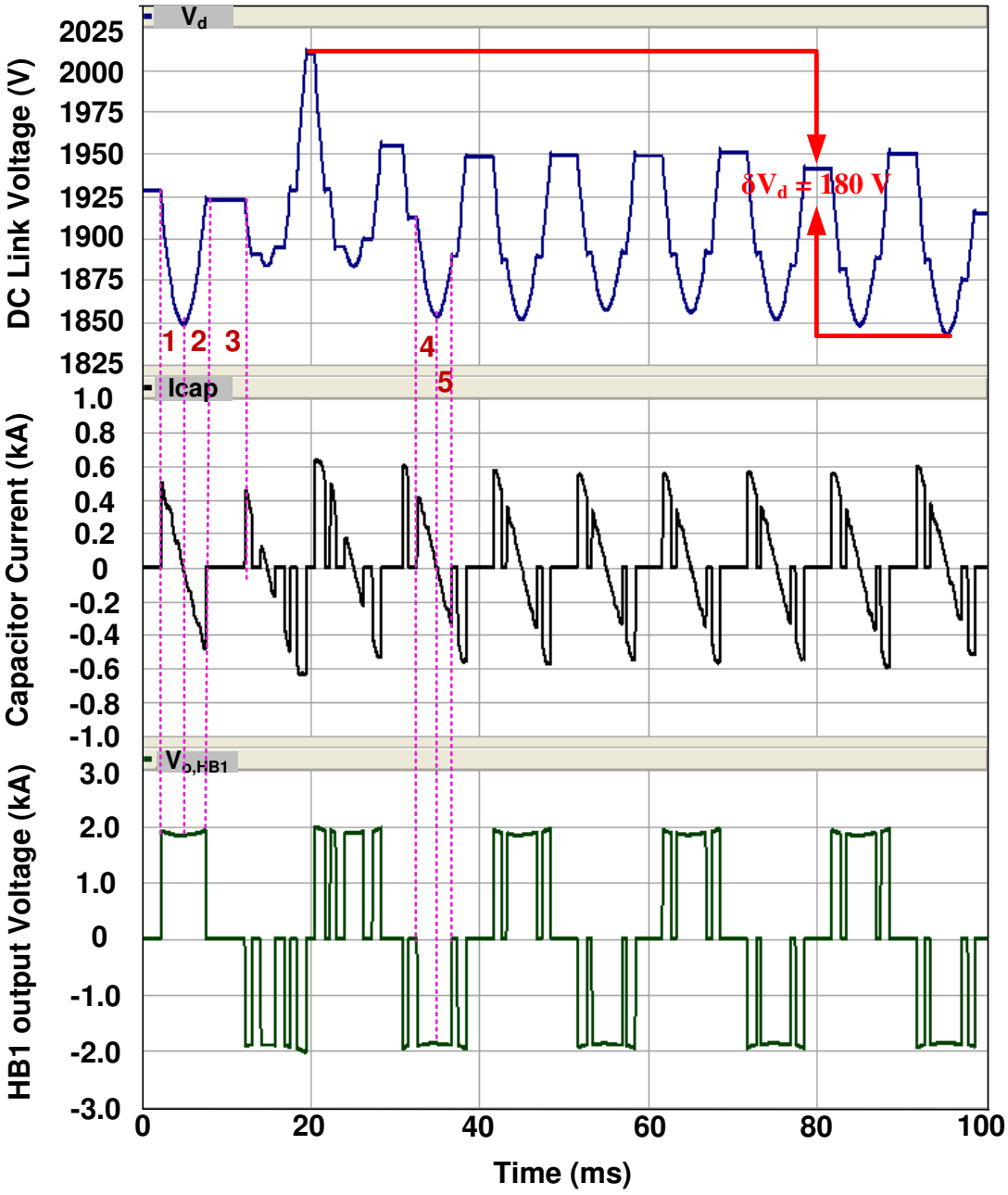


Figure 4.21 The variations in DC link voltage and current of HB1 with its output voltage for Q=+10 MVAr at PCC (PSCAD Simulations)

The peak-to-peak voltage variations for full inductive and full capacitive cases are obtained as 225V and 180V, respectively as shown in Figure 4.22 and Figure 4.23.

In Figure 4.22 and Figure 4.23, the variations of harmonic content in DC link voltage and current of HB1 in phase-A for 100ms duration are presented for both full capacitive and full inductive operation modes.

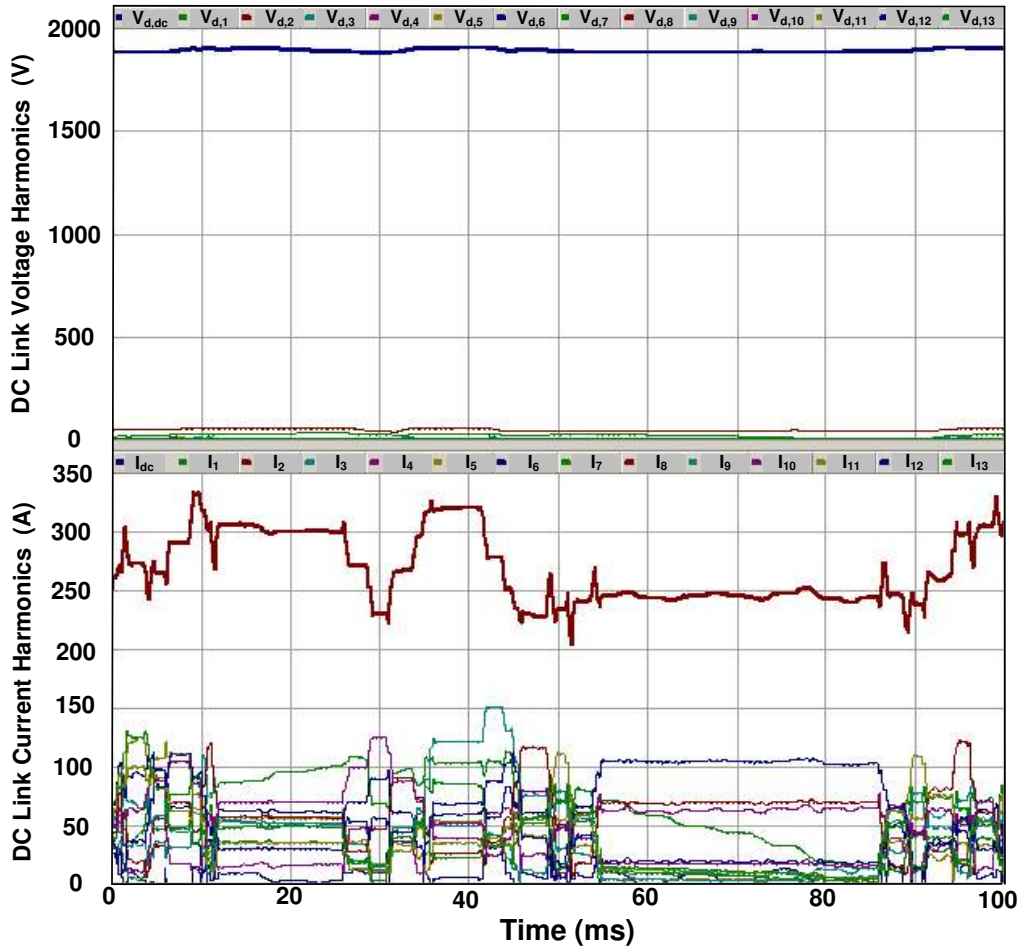


Figure 4.22 The variations of harmonic components in DC link voltage and current for Q=-10 MVAr at PCC (PSCAD Simulations)

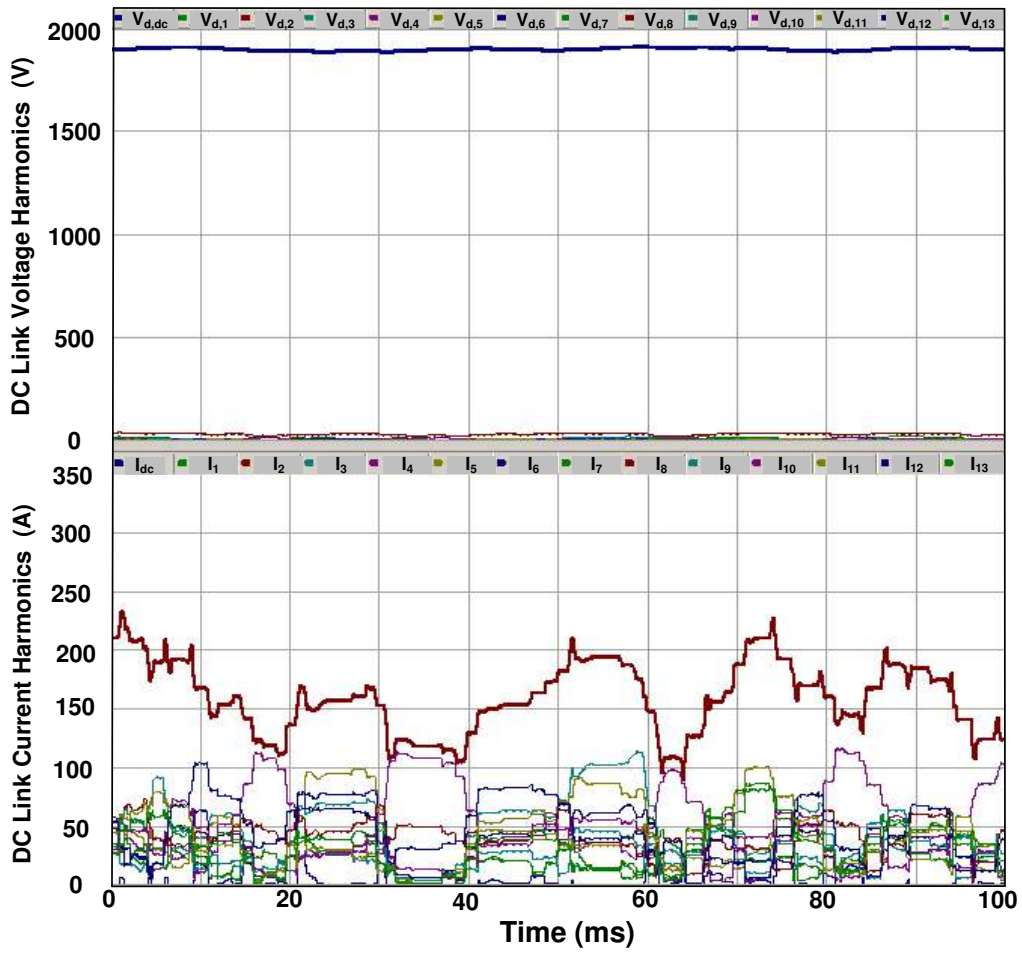


Figure 4.23 The variations of harmonic components in DC link voltage and current for Q=+10 MVAr at PCC (PSCAD Simulations)

The following conclusions have been found from the carried simulations for DC link capacitor used in each HB circuit:

1) Although, the instantaneous DC link voltage exceeds 2000V, the mean DC link voltage circulates around 1900V DC. Therefore, the choice of 2000V DC mean for DC link capacitors is enough for the design. Also, a maximum true rms current value of 475 A is obtained for full capacitive operation mode.

2) The peak-to-peak voltage value in DC link voltage at full capacitive operation is δV_d=225V which is higher than the obtained δV_d=180 V for full inductive

Table 4.4 Current Harmonic Components seen in DC link current for both full capacitive and full inductive operation modes

Harmonic Number	Full Capacitive Currents (A)	Full Inductive Currents (A)
1	78	77
2	370	252
3	66	34
4	140	30
5	19	48
6	102	16
7	60	49
8	25	47
9	48	67
10	64	60
11	39	66
12	129	43
13	18	35
14	75	17
15	14	31
16	4.5	28
17	10	17
18	27	6
19	7	15
20	58	21
21	6	15
22	51	28
23	8	18
24	28	7
25	12	5
26	5	22
27	12	16
28	38	12
29	14	8
30	55	16
31	14	5
TRUE RMS	**475 A**	**316 A**

operation due to the higher modulation index. The same conclusion is true for the peak-to-peak values of capacitor currents.

3) While the DC harmonic component is the highest one for the DC link voltage, 2^{nd} harmonic component for the DC link current is the maximum one, as expected. The voltage harmonic components other than DC are quite low and can be disregarded.
4) Although the 2^{nd} harmonic current in DC link current is the highest for both full capacitive and full inductive operation modes, some other components apart from 2^{nd} harmonic component with relatively high magnitudes can also be observed. Therefore, during the design of the DC link capacitors, these harmonic components should also be considered when determining the rated current value of DC link capacitors. Theese harmonic components in DC link current up to 31 with true rms values for full capacitive and full inductive operations have been listed in Table 4.4.

From carried out simulations, a pair of custom designed Metallized Polypropylene Film (MKP) type DC link capacitors with ratings of 2000VDC, 4.6mF, 260A,rms have been designed for each HB unit and produced by ELECTRONICON. These MKP type DC capacitors are used for power electronics applications with nonlinear currents and voltages with low equivalent self inductance (ESL) and equivalent series resistance (ESR) values. The ESL value is very crucial for power semiconductor switches due to peak voltages occurring during turn-off operations of IGBT modules. The ESR value refers the losses of the capacitors. ESL and ESR values are 50nH and 0.25mΩ for a unit of designed capacitor, respectively. Since a pair of them is connected in parallel for each HB, these values halve to 25nH and 0.125 mΩ. Field test results given in Chapter-5 show that δV_d does not exceed 9% (170V) over the entire operating range of the T-STATCOM thus showing the success of the choice of the DC link capacitance.

4.2 Design of Control System

The block diagram of the digital control system for a 154/10.5 kV, ±10MVAr T-STATCOM based on an 11-level Cascaded Multilevel Converter is as shown in Figure 4.24.

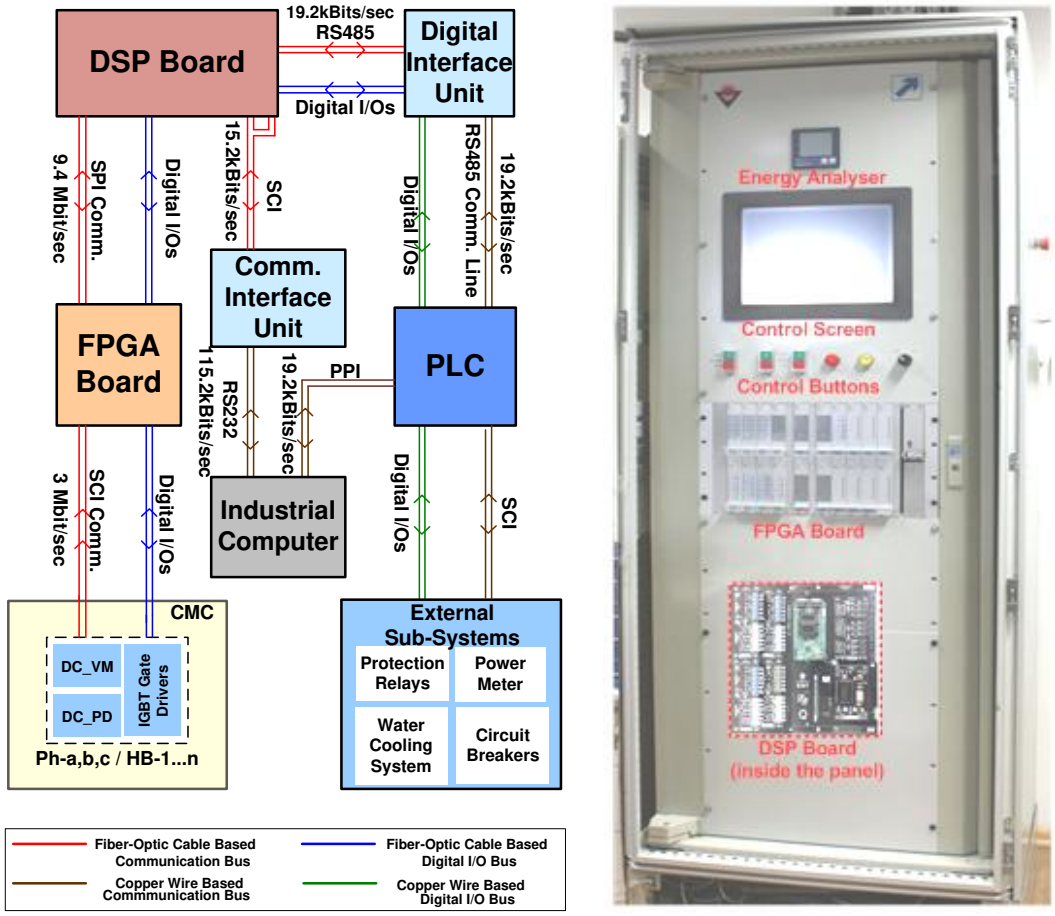


Figure 4.24 The block diagram of the digital control system of CMC with control panel

It is mainly composed of a DSP board, an FPGA board, a PLC and an industrial computer. The design and implementation of multi-DSP and -FPGA based fully digital control system for **m** number of parallel operated cascaded multilevel converters have been described in [22]. Technical specifications and the type numbers of Integrated Circuit (IC) boards which are used in the CMC application are given in Table 4.5.

Table 4.5 Technical Specifications of IC Boards in Figure 4.24

Name of the IC board	Number of Controller ICs on each board	Type number	Technical specifications
DSP Board	2	Texas Instruments TMS320F28335	150 MHz, 32 bit, Floating Point DSP
FPGA Board	1	Xilinx Spartan 3 XCS1500	
µController in DC_VM	1	Cypress PSoC CY8C27443	
PLC	-	Siemens S7226	3 MHz CPU, 24 kB RAM
Communication Interface Unit	-	Custom Design	
Digital Interface Unit	-	Custom Design	
Industrial Computer	-	Advantech Uno 3072	Celeron M 1GHz CPU, 1GB RAM

The control system diagram for the designed CMC module is also shown in Figure 4.25. The DSP board is basically responsible for the calculation of modulation index value, M, the determination of control function (Q-mode or V-mode) and some protection facilities while the FPGA board is mainly responsible for the equalization

of DC link capacitor voltages, the determination of CSS or MSS method to applied for equalization purpose and production of firing signals for IGBT modules used in CMC as well as some protection facilities. The digital control system implemetation of this work is applied by the project team as expressed in Acknowledgments.

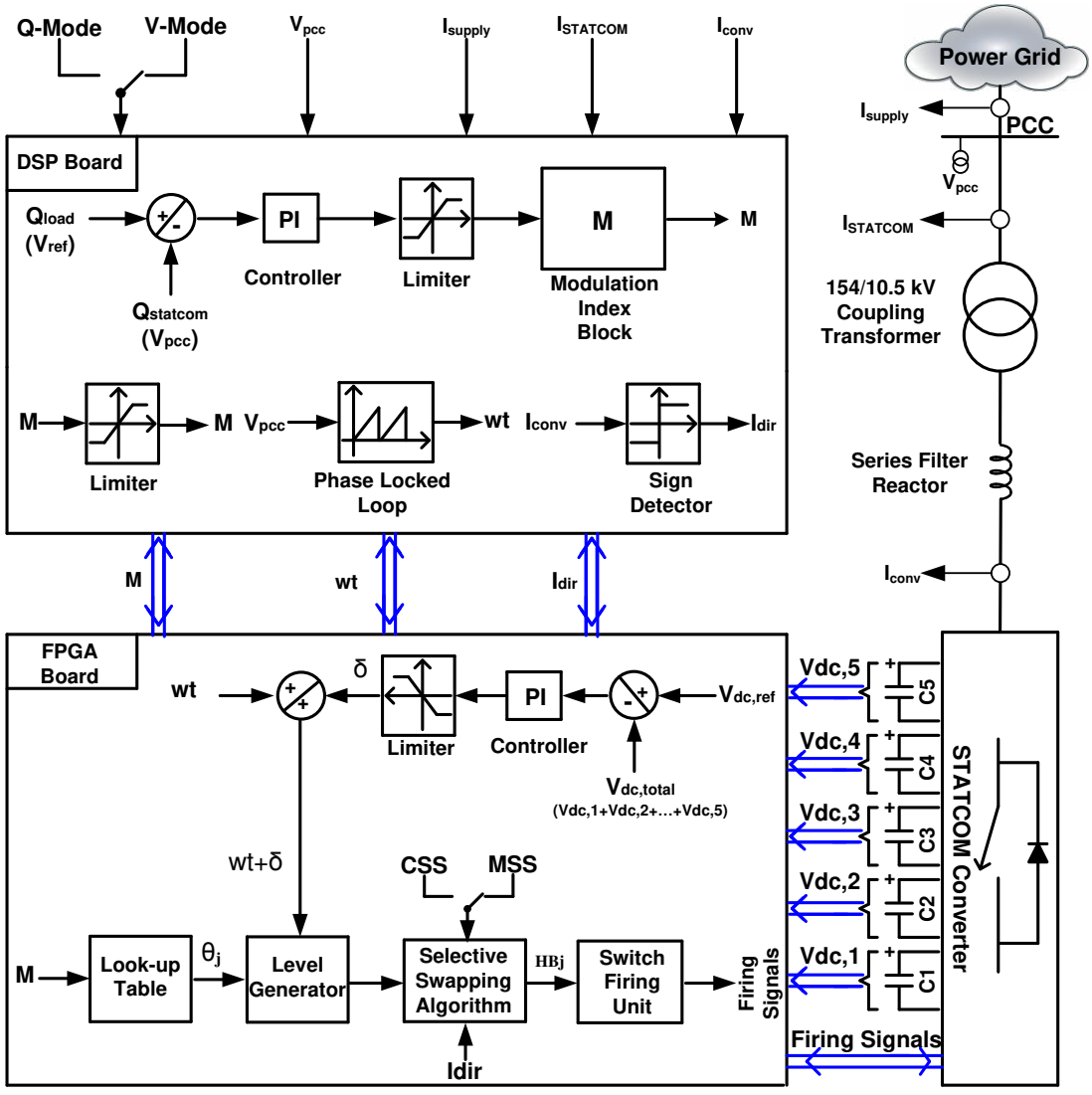


Figure 4.25 The diagram of control system for the designed CMC module

4.2.1.1 DSP Board

The DSP board contains two DSP chips: one for major control functions and serial communication with PLC, while the other for major protection functions.

Operation mode of the T-STATCOM system is set by the operator and kept active by the DSP Board . It can be operated in either reactive power compensation mode (Q-mode) or terminal voltage regulation mode (V-mode) by using a selector switch as shown in Figure 4.25.

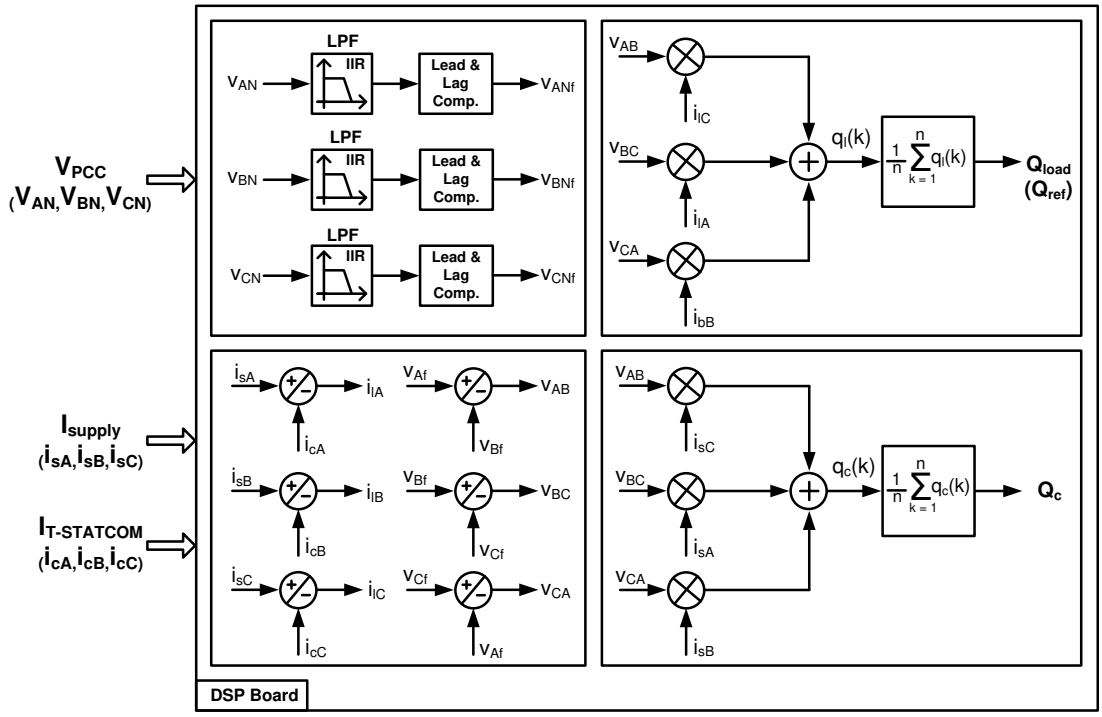


Figure 4.26 Generation of Q_{ref} and Q_c by DSP Board

The operation in Q-mode tends to reduce the reactive power flow in between 154 kV bus and the power grid in Figure 4.25 to zero. Q_{ref} that will be generated by the T-STATCOM is calculated by the DSP Board from the sampled data (25 kS/s per channel) of the line-to-neutral voltages at PCC (v_{AN}, v_{BN}, v_{CN}) , supply side line currents (i_{sA}, i_{sB}, i_{sC}), and line currents of T-STATCOM system (i_{cA}, i_{cB}, i_{cC}) as shown in Figure 4.26.

Reactive power consumption of the load side, Q_{load} is calculated from (4.1) by the DSP Board.

$$Q_{load} = Q_{supply} - Q_{T-STATCOM} \tag{4.1}$$

where, Q_{supply} and $Q_{T\text{-}STATCOM}$ are the reactive powers on the supply and T-STATCOM sides, respectively.

Since Q_{ref} = Q_{load} for unity power factor (pf) operation, then the DSP Board calculates modulation indices for M the CMC by using the digitally implemented proportional-integral (PI) controller in Figure 4.25. However in Terminal Voltage Regulation mode (Mode-V), the DSP Board calculates modulation index value to bring the voltage at PCC (V_{PCC}) to its reference value (V_{ref}) set by the operator.

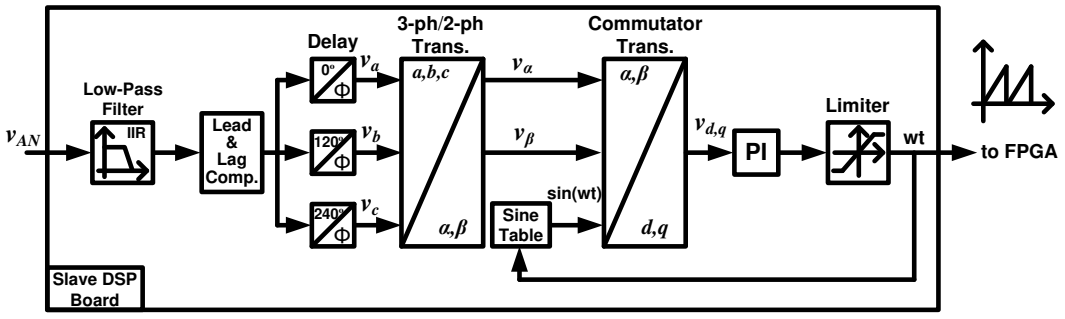


Figure 4.27 PLL generation by the DSP Board

Since the CMC should be synchronized with the supply voltage at PCC during its operation, the necessary Phase-Locked Loop (PLL) signal is generated by the DSP Board. The DSP Board generates three PLL signals one for each line-to-neutral voltage. Figure 4.27 shows the block diagram representation of the digital PLL implementation. To approximate the performance of the digital implementation to that of an equivalent analog PLL circuit, the supply voltage waveform has been continuously sampled at a rate of 25 kS/s and the sine table in Figure 4.27 is composed of 2048×1 array over one complete cycle

In order to equalize DC link capacitor voltages, selective swapping algorithm can be used as explained in Chapter-2. This makes necessary the determination of the direction of the CMC line currents. For this purpose the DSP Board samples the corresponding line current waveforms at a rate of 25 kS/s, calibrate the associated AC signal and make decision whether the current is greater than zero at each sampling instant. The DSP Board then sends a pulse train (1 for positive and 0 for negative current values) via SPI communication link to the FPGA Board.

The computed active and reactive powers, P and Q and rms values of AC quantities, V and I for the CMC by the DSP Board are sent to the industrial computer in Figure 4.24 for monitoring purposes.

According to the calculated 20 ms and 1 s averaged rms values of V, the DSP Board carries out over/under voltage and unbalanced protection functions for the CMC module. However the overcurrent protection is carried out on the basis of both the instantaneous and rms values of CMC line currents. The DSP Board is also equipped with an analog overcurrent protection circuit for further reliability. If digital over/under voltage or unbalance protection algorithm detects a signal exceeding the

pre-specified limits, an alarm signal will be generated and sent to FPGA to turn off IGBTs. On the other hand, if the digital overcurrent algorithm detects a signal exceeding pre-specified limits, a trip signal will be generated and sent to the Circuit Breakers (CB) to isolate the T-STATCOM system and the associated FPGA to turn off the IGBT modules of the CMC.

4.2.1.2 FPGA Board

FPGA Board is composed of an FPGA chip, a multiplexer circuit, fiber optic transmitters/receivers and other peripheral devices. The major functions of the FPGA board can be summarized as follows:

a. CMC losses are compensated by allowing active power flow from the supply to the T-STATCOM system. Active power flow is controlled by load angle, δ. To control the value of δ, FPGA Board first compares total DC link voltage V_{dc} of the CMC with its reference value, then processes the error signal with a PI controller as shown in Figure 4.25. This means that, the AC voltage waveform synthesized by the FPGA should be shifted by δ with respect to supply voltage at PCC. Therefore, the PLL signal sent by the DSP Board should be shifted by angle δ during the implementation of the active power control by the FPGA Board. To improve the waveform synthesizing task, the discrete PLL signal is approximated to a continuous signal by applying linear interpolation technique.
b. The optimum angles $\theta_1,\theta_2,\ldots,\theta_5$ according to SHEM are calculated off-line as a function of M and then stored in the memory of the FPGA in a look-up table (204x6 matrix). The FPGA board extracts optimum angles from look-up table once for every 40µs period by using M value sent by the control DSP chip.
c. The DC link capacitor voltages are equalized by using MSS method during the operation of the CMC. This will be achieved by FPGA board by using

current direction signal sent by protection DSP chip, and the instantaneous DC link capacitor voltage signals sent by the DC_VM circuit.

d. Upon the request of control DSP chip, the FPGA board creates the necessary turn-on and turn-off signals for IGBTs to charge the DC link capacitors successfully during the pre-charging period. Upon the request of the PLC, the FPGA board discharges the capacitors by activating the DC_PD circuit in Figure 4.24. Each DC_PD Board is composed of power stage of a chopper circuit supplying controlled power to an external discharge resistor and an analog protection circuit. DC_PD Board receives controlled duty ratio signals from FPGA in order to keep the power dissipation of the discharge resistor constant during the discharge period.
e. A smooth transition between different Q or V settings is aimed at the design of the control system. This will minimize the oscillations in current, voltage and reactive power in transition periods and hence reduce the settling time. The extreme operating condition is the transition from full capacitive to full inductive operation mode, or vice versa. For this purpose, first, the changes in the modulation index have been applied only at zero crossing points of the CMC line current by the FPGA Board.

FPGA board also carries out some protection functions such as short circuit protection of IGBTs, over temperature, overvoltage protection of DC link capacitors, etc..

4.2.1.3 Programmable Logic Controller (PLC)

The Programmable Logic Controller (PLC) in Figure 4.24 achieves control actions according to the signals received from the DSP Board and external sub-systems via digital/analog I/Os and data acquisition and state monitoring actions received from

the same system elements via serial communication channels. The major operational features of the PLC are as described below:

a. The PLC carries out data acquisition, state monitoring and fault diagnosis actions according to the signals taken from the DSP Board and external sub-systems.
b. The operation state of the T-STATCOM system (on/off operation of circuit-breakers and the load-break switch) is commanded by the PLC according not only to the protection signals received from the de-ionized water cooling system but also to on/off or protective signals received from other system elements.
c. Remote control signals can be actuated by the PLC.
d. Some of the fault/failure signals are received from other control system elements and then classified by the PLC for the activation of automatic re-closing system. The de-ionized water cooling system is therefore turned on by the PLC before re-closing action of the main CB to provide cooling service for power semiconductors. The classified and unclassified fault/failure data are also sent to the industrial computer in Figure 4.24 for monitoring purpose.

4.3 Switching Strategies for the Application of Selective Swapping

In this work, the switching strategy chosen in the application of both CSS and MSS causes voltage spikes with magnitudes $\pm V_d$, $\pm 2V_d$, $\pm 3V_d$ and $\pm 4V_d$ superimposed on the 11-level line-to-neutral voltage waveform as given in Figure 4.6. As an example, in Figure 4.6 the voltage spike marked by ***vs1*** can be explained by the aid of Figure 4.28 which is drawn for the three transition modes of CMC phase-A. Initially, line-to-neutral voltage is, $+4V_d$ and the status of the switches are as marked in Figure 4.28 by Mode-1. At the MSS instant (Δt_s=400μs), interchange HB5 by HB4 by turning off both IGBT4 module of HB5 and IGBT3 module of HB4 and at the same

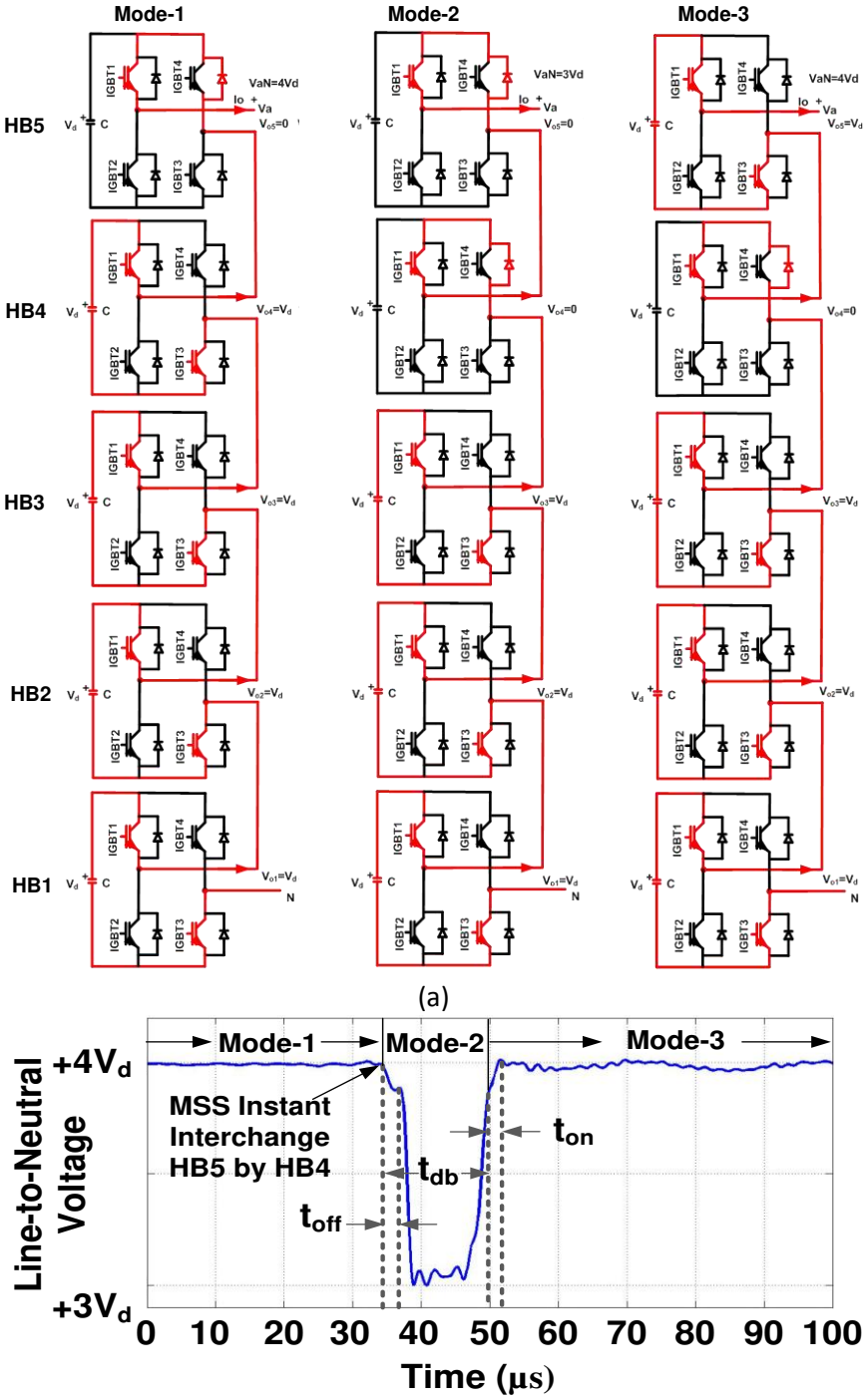


Figure 4.28 Illustration of a) operation modes of IGBT modules in phase-A of the CMC before (Mode-1), during (Mode-2) and after (Mode-3) the MSS operation b) voltage spike $-V_d$ superimposed on $+4V_d$ level (Field data)

time initialize the dead-band period (t_{db}=13µs). This operation mode is illustrated by Mode-2 in Figure 4.28. When IGBT3 module in HB4 is successfully turned off, the negative AC current of HB4 starts to circulate through anti-parallel diode of IGBT4 module of HB4 resulting in BYP mode. At the end of the dead-band period, both IGBT3 module of HB5 and IGBT4 module of HB4 are turned on resulting in DCH mode for HB5. This operation mode is illustrated by Mode-3 in Figure 4.28.

The switching strategy described above causes a drop in line-to-neutral voltage waveform from $+4V_d$ to $+3V_d$ and back to $+4V_d$ for a period of nearly 15.5µs owing to the operation of the incoming HB5. If the MSS operation takes place on $\pm 3V_d$ voltage level of line-to-neutral voltage waveform, depending upon the number of incoming HBs, either $\pm V_d$ or $\pm 2V_d$ voltage spike will be superimposed on the voltage waveform. Similarly, MSS operations on $\pm 2V_d$ and $\pm V_d$ may yield voltage spikes either of $\pm V_d$, $\pm 2V_d$, $\pm 3V_d$ and $\pm V_d$, $\pm 2V_d$, $\pm 3V_d$, $\pm 4V_d$, respectively.

An alternative switching strategy can reduce only the duration of voltage spikes to turn-off time of IGBTs at the expense of a more complex control algorithm. This can be achieved by sending the turn-off signal to the gate of the IGBT of outgoing HB just at the end of the dead-band period. It is worth to note that these voltage spikes can not reflect to PCC since they are successfully absorbed by the input filter reactor of the CMC.

At the transition instants from 0 to $\pm V_d$ voltage level of line-to-neutral voltage waveform, always a voltage spike of $\pm 4V_d$ is superimposed on 0 voltage level (Figure 4.6). As an example, in Figure 4.6 the voltage spike marked by ***vs2*** can be explained by the aid of Figure 4.29 which is drawn for the three transition modes of CMC phase-A. In Mode-1 of Figure 4.29, all HBs are operating in BYP mode resulting in 0 line-to-neutral voltage. In order to produce $+V_d$ voltage level in the

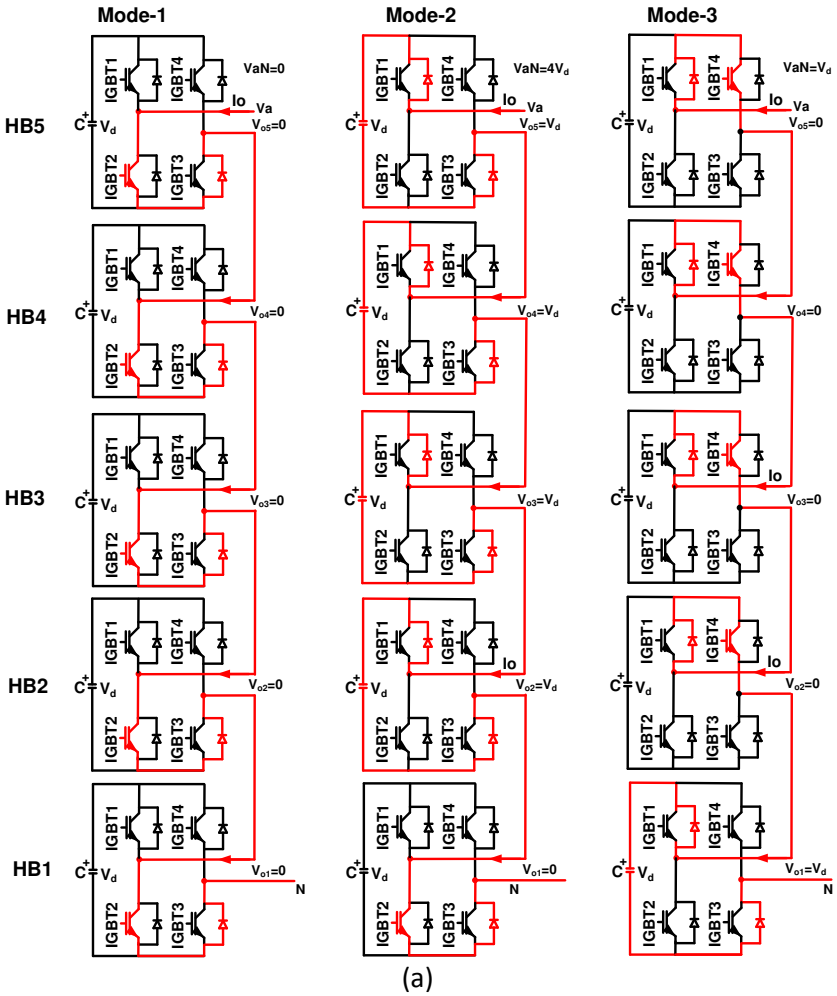


Figure 4.29 Illustration of a) operation modes of IGBT modules in phase-A of the CMC before (Mode-1), during (Mode-2) and after (Mode-3) the MSS operation b) voltage spike +4V_d superimposed on zero level (Field data)

line-to-neutral voltage waveform, operation mode of HB1 is to be switched from BYP mode to CH mode as illustrated in Mode-3 of Figure 4.29. This is achieved by turning off IGBT2s and IGBT3s of HB2 to HB5 and at the same time IGBT2 of HB1. Therefore, in Mode-2 of Figure 4.29, HBs from 2 to 5 produces a voltage spike of $+4V_d$. At the end of dead-band period, IGBT1 of HB1, and IGBT2s and IGBT3s of the remaining four HBs is turned on resulting $+V_d$ voltage level in line-to-neutral voltage waveform.

This switching strategy is preferred in order to equalize the utilization of IGBT modules and to simplify the switching algorithm. In summary, this switching strategy is applied by monitoring the zero crossings of the voltage waveforms by the use PLL circuit and thus producing $+4V_d$ voltage spike at the transition instant from 0 to $+V_d$ on the positive half cycle and $-4V_d$ at the transition from 0 to $-V_d$ on the negative half cycle for capacitive operation mode. The reverse is true for inductive mode of operation.

An alternative to the above switching strategy is to monitor the line currents of CMC instead of line to neutral voltage waveforms. On the negative half cycle of the CMC current, IGBT2 of HB1 (Mode-1) is turned off and after dead-band period IGBT1 of HB1 is turned on. This switching strategy will eliminate Mode-2 on Figure 4.29 and associated voltage spike. This switching strategy may fail when CMC is producing very small amounts of reactive power and hence fundamental current owing to the presence of 17^{th} and 19^{th} current harmonic components.

A better but more complex switching strategy can be recommended based on the line-to-neutral voltage waveforms and hence PLL signals. In this method, one complete cycle of the voltage waveform is to be divided into two parts from $\pi/2$ to $3\pi/2$ and from $3\pi/2$ to $5\pi/2$ and applying switchings at the positive peak and negative

peak of the line-to-neutral voltage waveforms for changing by-pass modes instead zero crossing points. This strategy will eliminate $\pm 4V_d$ voltage spikes in Figure 4.29.

CHAPTER 5

THE IMPLEMENTATION OF T-STATCOM SYSTEM AND FIELD PERFORMANCE RESULTS

5.1 The Implementation of T-STATCOM System

In this research and technology development work, a 154 kV, ±50 MVAr, H-Brdige (HB) based Multilevel T-STATCOM composed of five 12 kV, ±12 MVAr Cascaded Multilevel Converter (CMC) designed in Chapter 4 has been implemented primarily for the purposes of reactive power compensation and terminal voltage regulation, and secondarily for power system stability. Figure 5.1 shows the schematic diagram of the implemented 154 kV, ±50 MVAr T-STATCOM system. Five 12 kV, ±12 MVAr Cascaded Multilevel Converter (CMC) modules are connected in parallel via air-core reactors. The combination of these five CMC modules is then connected to 154 kV bus via a 154/10.5 kV, 50/62.5 MVA, Y-Y connected coupling transformer. The neutral point of the primary is solidly grounded while that of the secondary is grounded via a 6.93Ω grounding resistor to limit line-to-ground fault current to 1 kA. The T-STATCOM system is equipped with a digital control system which uses the basic control architecture described in Chapter 4 for an CMC. The only difference is

the usage of a Master DSP Board with five Slave DSP Boards. The Master DSP Board manages all control and most of the protection facilities by sending the necessary commands to the Slave DSP Boards of each CMC module. All controllers are built up by using up-to-date Digital Signal Processor (DSP, TI-TMS320 F28335) and Field Programmable Gate Array (FPGA, XILINX Spartan-3, 1,500,000-gate) technologies. 11-level line-to-neutral voltage and hence 21-level line-to-line voltage waveforms are created by using five series connected H-Bridges in each phase of the Y-connected CMC module.

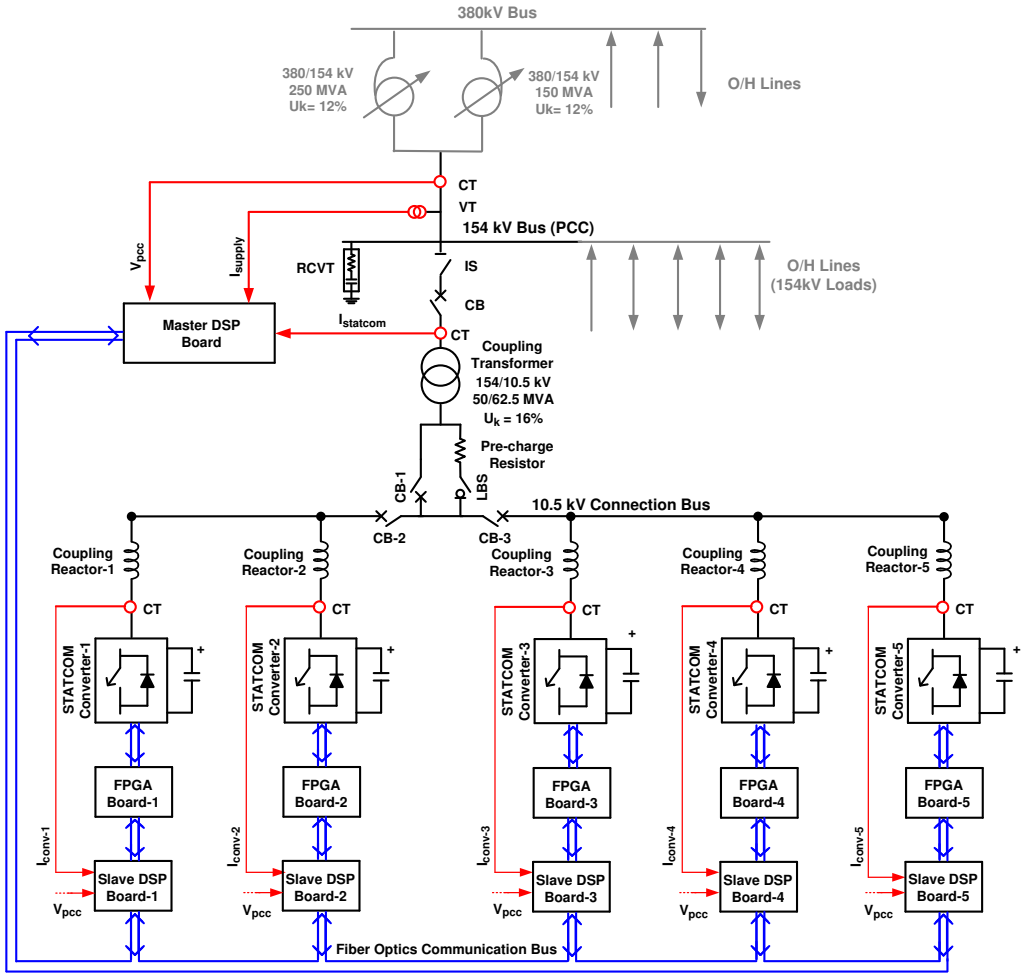


Figure 5.1 Simplified single line diagram of the implemented T-STATCOM

The developed 154kV, ±50 MVAr T-STATCOM system has been installed in 380 kV/154 kV Sincan Transformer Substation, Ankara as shown in Figure 5.2. Table 5.1 summarizes the technical specifications of each HB, CMC module and the resulting T-STATCOM system. The coupling transformer (ONAN/ONAF), high voltage (HV) and medium voltage (MV) switchgear equipment, input filter reactors and the water-

Table 5.1 The technical specifications of the installed T-STATCOM system

T-STATCOM	
Rated Power	±50 MVAr
Rated Voltage	154 kV
Coupling Transformer	Y-Y, 154/11.1 kV, 50/62.5 MVA, 16% u_k
Number of CMC Modules in Parallel	5
Cascaded Multilevel Converters (CMC)	
Rated Power	±12 MVAr
Rated Voltage	10.5 kV (max.12kV)
Number of H-Bridges per phase	5
Number of Levels in Voltages	11 Levels Line-to-Neutral, 21 Levels Line-to-Line
Harmonics Eliminated by SHEM	5^{th}, 7^{th}, 11^{th}, 13^{th}
Coupling Reactors	2.5mH, air core
Cooling System	De-ionized water cooling
H-Bridges (HB)	
Rated Power	±840 kVAr
Rated Voltage	1.8 kV rms
Power Semiconductor	3300V, 1200A HV IGBT with parallel inverse diode
Effective Switching Frequency	500Hz
Design Value of DC Link Voltage	1900Vdc
DC Link Capacitor* **Metallized Polypropylene (MKP)*	9.2mF (4.6mF//4.6mF) ±10%
	260A rms, 2000Vdc
	250V peak-to-peak ripple

(a)

(b)

(c)

(d)

Figure 5.2 154 kV, ±50 MVAr T-STATCOM based on 11-level CMC installed at 380kV/154kV Sincan Transformer Substation
((a) Interior view of trailer with power stages, (b) Control cabinets, (c) Trailer for ±50 MVAr T-STATCOM on road (WxLxH:3700mmx16800mmx4300mm), and (d) General view of T-STATCOM)

to-air heat exchanger of this system are installed outdoor (Figure 5.2-d). The power stages of five CMC modules, the control system cabinets and part of the de-ionized water cooling system excluding water-to-air heat exchanger are placed into a non-magnetic container mounted on a trailer (Figure 5.2-c). This makes possible easy relocation of the T-STATCOM to another problematic point of the transmission system whenever this is required.

5.1.1 Power System Characteristics

This subsection describes the electrical power system characteristics of the 154 kV Point of Common Coupling (PCC) transmission bus at which the implemented 154kV, ±50MVAR T-STATCOM system is connected at Sincan Transformer Substation, Ankara before installation of the system. The PCC side electrical characteristics are given in Table 5. 2. The maximum SCMVA value is around 5300MVA at 154kV for PCC and the corresponding 3-phase solidly short circuit current is 19.87 kA at rated voltage.

Table 5. 2 The electrical characteristics of the power system at which T-STATCOM system is connected

Nominal Voltage	154 kV
Maximum Voltage	170 kV
Short Circuit Level (SCMVA)	5300MVA at 154 kV

Many overhead (O/H) lines longer than 100 km length in around Ankara are connected to the 154kV bus at which the T-STATCOM system has been connected. In the daytimes, the reactive power variation of the PCC is generally inductive-reactive due to industrial loads fed by the O/H lines while during the nighttime the

variation in the reactive power changes to the capacitive-reactive due to Ferranti Effect of the O/H lines because of light load condition.

Some measurements have been taken continuously from November of 2008 to June of 2009 by the high accurate class Power Quality (PQ) analyzers. The all electrical parameters of the power system described in this subsection are measured according to IEC 61000-4-30 standard [56]. The variations in the reactive power and line-to-neutral voltages of 154 kV bus are shown in Figure 5.3 and Figure 5.4**.** Also, the maximum monthly inductive-reactive and capacitive-reactive variations from November of 2008 to June of 2009 have also listed in Table 5.3. From Table 5.3, it is obvious that the variations in the reactive power at PCC are between 60 MVAr inductive-reactive and -40 MVAr capacitive-reactive in the year of 2009 before the installation of the T-STATCOM system. Therefore, at least five 12kV, ±12MVAr CMC modules should be operated in parallel to have +60MVAr inductive-reactive and -40MVAr capacitive-reactive power. As can be seen from the Figure 5.4, the line-to-neutral voltage of the PCC is over 89kV (root three of 154 kV) almost for the whole measurement time period.

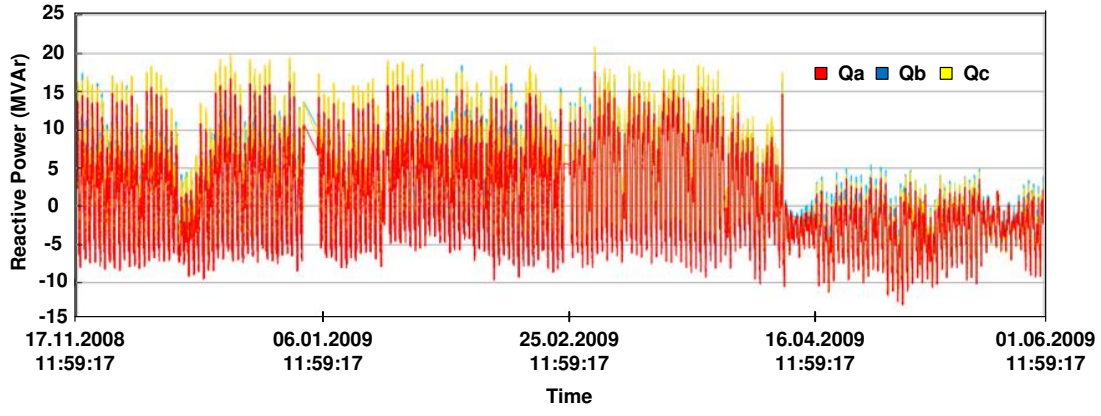


Figure 5.3 The variations in reactive power per phase at PCC side (Nov.2008-June.2009, field data)

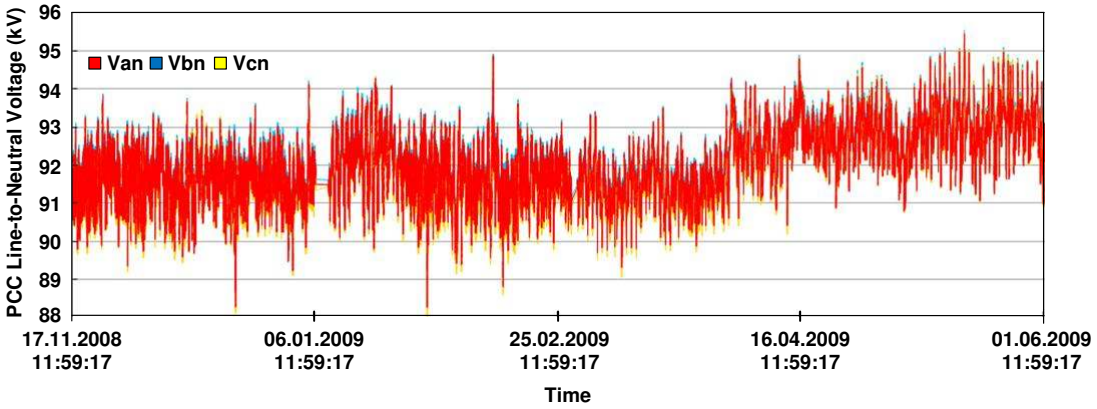


Figure 5.4 The variations in PCC side line-to-neutral voltages (Nov.2008-June.2009, field data)

Table 5.3 The monthly maximum reactive power variations of the PCC from Nov.2008 to June.2009

Time	Max. Inductive Reactive Power	Max. Inductive Reactive Power
November 2008	+48 MVAr	-22 MVAr
December 2008	+50 MVAr	-25 MVAr
January 2009	+50 MVAr	-22 MVAr
February 2009	+50 MVAr	-27 MVAr
March 2009	+60 MVAr	-27 MVAr
April 2009	+50 MVAr	-35 MVAr
May 2009	+15 MVAr	-40 MVAr
June 2009	+20 MVAr	-30 MVAr

This is because of the dynamic operation of tap changers installed for autotransformers used in the substation and the high SCMVA value of the PCC. Therefore, the need of voltage regulation for the PCC is not needed so much for HV PCC bus. However, to show effectiveness of T-STATCOM on voltage regulation, Voltage Regulation Mode (V-Mode) is also inserted into the digital control of T-STATCOM.

Another crucial point for the design is the harmonic content of line currents and line-to-neutral voltages of the PCC. These values are given in Figure 5.5 and Figure 5.6 with the associated limit values defined by IEEE Std.519-1992.

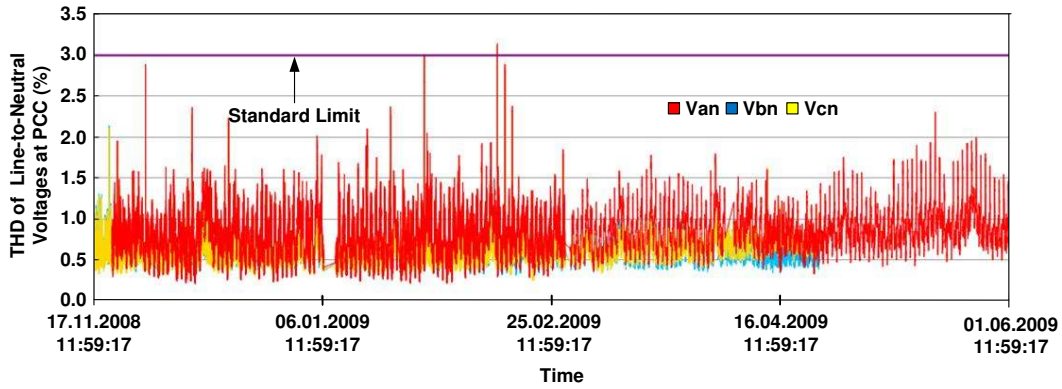


Figure 5.5 The variations in THD of PCC line-to-neutral voltages (Nov.2008-June.2009, field data)

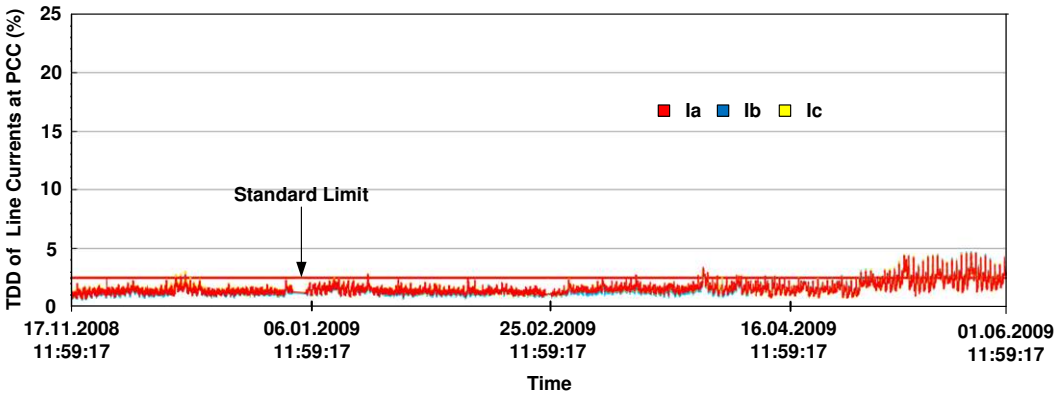


Figure 5.6 The variations in TDD of PCC line currents (Nov.2008-June.2009, field data)

The Total Harmonic Distortion (THD) values for line-to-neutral voltages are below the limit value assigned in IEEE 519-1992 during the measurement period as shown

in Figure 5.5. However, the variations in Total Demand Distortion (TDD) for line currents sometimes circulate around the limit value as seen Figure 5.6. Figure 5.7 shows the variations of 3rd, 5th, 7th and 9th harmonic components in phase-A line current of PCC. Although, 3rd, 7th and 9th harmonic components are below the specified value in IEEE Std.519-1992, the 5th harmonic component exceeds the limit value for a percentage of 33% of the total measurement period.

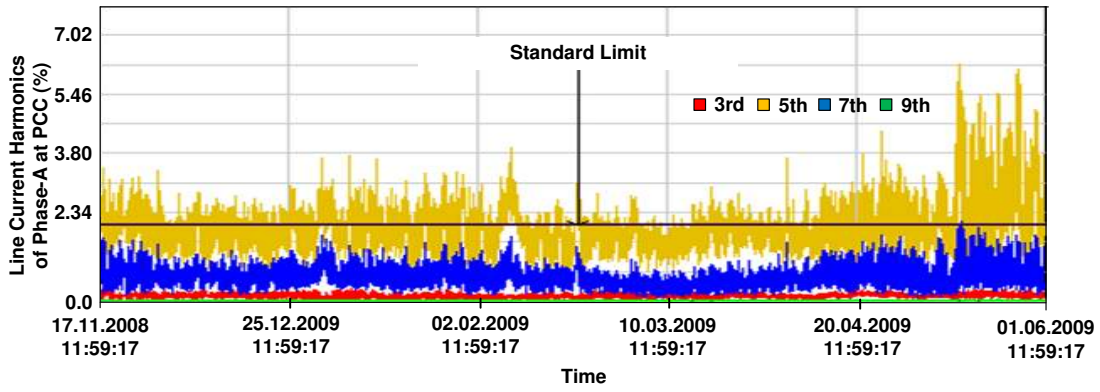


Figure 5.7 The variations in 3rd, 5th, 7th and 9th harmonic components of PCC phase-A line current (Nov.2008-June.2009, field data)

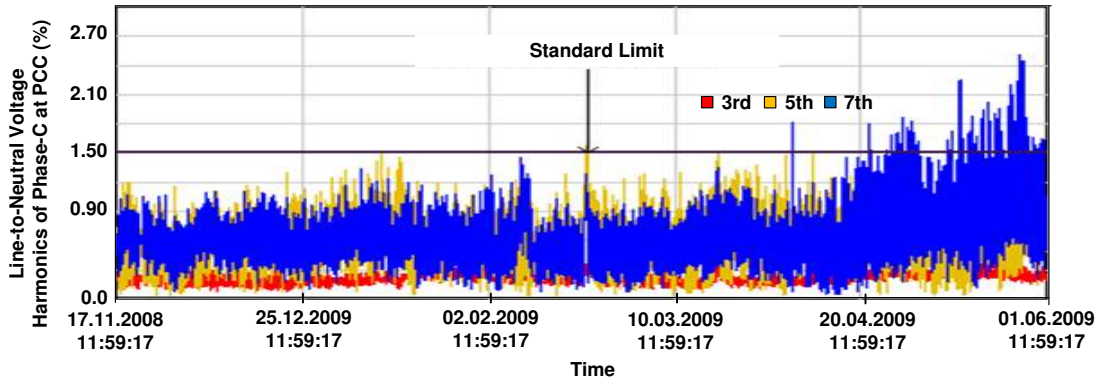


Figure 5.8 The variations in 3rd, 5th and 7th harmonic components of PCC phase-C line-to-neutral voltage (Nov.2008-June.2009, field data)

The variations of 3rd, 5th and 7th harmonic components of PCC phase-C line-to-neutral voltage are shown Figure 5.8 and only 7th harmonic component exceeds the standard limit specified in IEEE Std.519-1992 for a percentage of only 1.2% of the total measurement period.

Therefore, the implemented T-STATCOM system should not contribute to raise THD and TDD values as well as the highest harmonic components seen in line currents and phase voltages of the PCC.

5.2 Field Performance Results

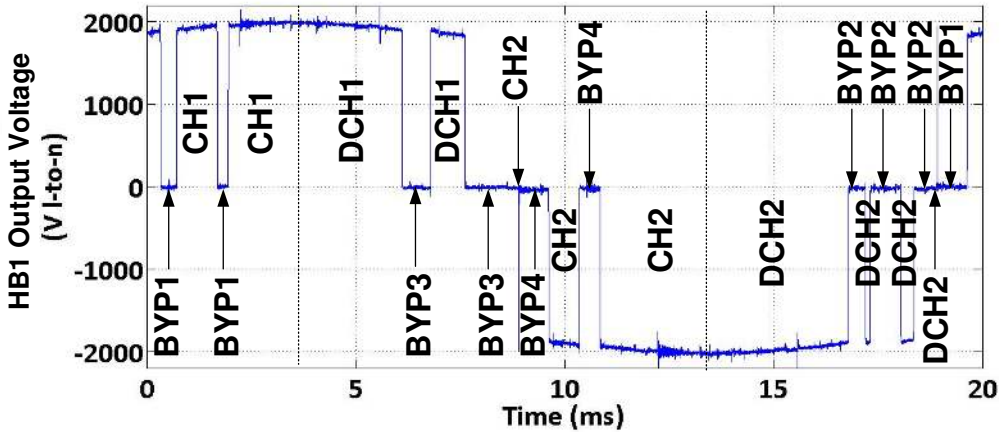
5.2.1 Field Performance of HB

In order to avoid any undefined operational state for H-Bridge (HB) circuits, the gates of all IGBT modules in each HB receive either +15V DC or -15V DC control signal. When -15V DC is applied, the IGBT part turns off but its anti-parallel diode may carry negative module current. However, when +15V DC is applied, the IGBT part not necessarily triggers into conduction but its anti-parallel diode may carry the negative module current. Therefore, when each IGBT module receives a turn-on signal which part of the module is going to be triggered into conduction depends on the sign of the associated HB current.

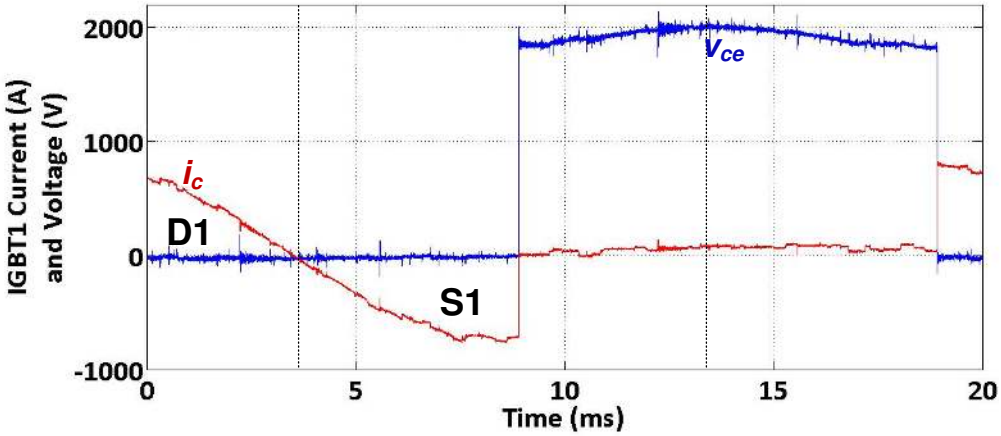
In one leg of an HB, if the conducting IGBT part of one of the modules is going to turned off while the IGBT part of other module in the same lag is going to be turned on, this operation should be carried out with a delay of minimum 5µs (dead-band) for HV IGBTs in general, in order to prevent DC link capacitor from being short-circuited through two IGBTs (shoot-through). In this work, dead-band, t_{db} was set to 13µs to be on the safe side. 2.5µs turn-on time for the incoming IGBT introduces a further delay to the switching operation.

In order to illustrate the successful operation of each HB in the field, the AC voltage waveform of HB1 in phase-A, collector-emitter voltages and collector currents of IGBT1 and IGBT4 modules in the upper half of HB1 are recorded in the field over one complete cycle (20ms) and given in Figure 5.9. Charging, discharging and by-pass periods of HB1 in phase-A are also marked on Figure 5.9-a. Conduction periods for IGBT and anti-parallel diode parts of modules -1 and -4 are marked respectively by S1, D1, S4 and D4 on Figure 5.9-b and -c. Output voltage polarity, current direction, CH, DCH, and BYP modes of HB1 in phase-A of the CMC which are shown in Figure 5.9 can be matched with those of previously constructed in Figure 4.5 and Figure 4.6 in Chapter 4.

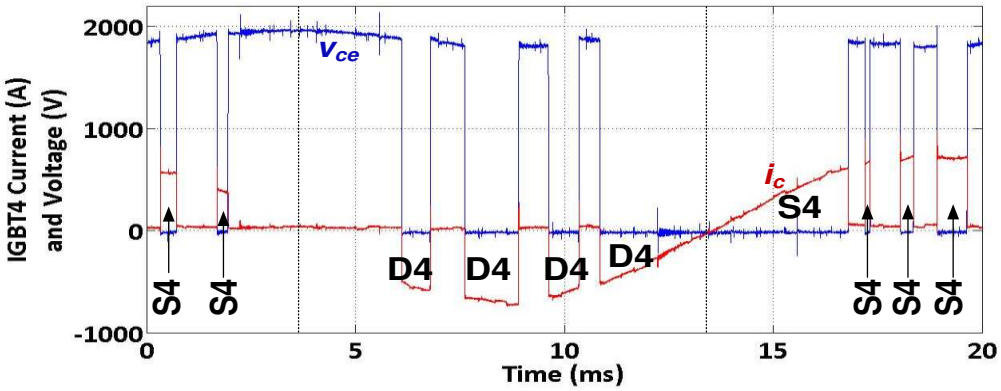
In order to make the controller a memoryless system, a simple switching strategy is applied at level changes and swapping instants. If a level change or swapping should occur in the positive half-cycle of the HB voltage, IGBT modules in upper half of the HB are controlled in order to provide a short circuit path to by-pass current (BYP1 and BYP3). However, on the negative half-cycle of the HB voltage, IGBT-2 and -3 modules of the lower half of the HB will carry the bypass current (BYP2 and BYP4 modes in Fig.13). Unfortunately, this operation strategy results in unequal utilization IGBT modules. As an example, for the sample record given in Figure 5.9, IGBT3 and -4 modules are switched more frequently than IGBT1 and -2 modules. This is because by-pass modes from BYP1 to BYP4 are not applied consecutively as can be understood form Figure 5.9-a since the applied switching strategy is a memoryless one. If a more complex control software were developed and then utilized in order to keep the previous operation states of all IGBT modules continuously in the FPGA memory, BYP1 mode in Figure 5.9-a would be followed by BYP2 mode sequentially under the positive half-cycle of the HB current, however for the negative half-cycle of the HB current BYP3 and BYP4 modes would be applied sequentially.



(a)



(b)



(c)

Figure 5.9 Field performance of HB1 in phase-A over one-cycle a) HB1 output voltage and its operation modes b) IGBT1 module voltage and current waveforms c) IGBT4 module voltage and current waveforms

This switching strategy would nearly equalize the switching frequencies and conduction periods of all IGBT modules in each HB circuit. The field records in Figure 5.9 show that each HB circuit is successfully designed, implemented and operated with a simple and memoryless control strategy.

5.2.1.1 Switching Waveforms of IGBT Modules

Turn-on and turn-off behaviors of the IGBT1 and IGBT2 modules in the same leg of HB1 in phase-A of CMC prototype are also recorded in the field as shown in Figure 5.10 and Figure 5.11 when the T-STATCOM is delivering 10MVAR to PCC. These records correspond to transition of operation mode of HB1 from DCH to BYP. Since the field records in in Figure 5.10 and Figure 5.11 have been obtained for nearly

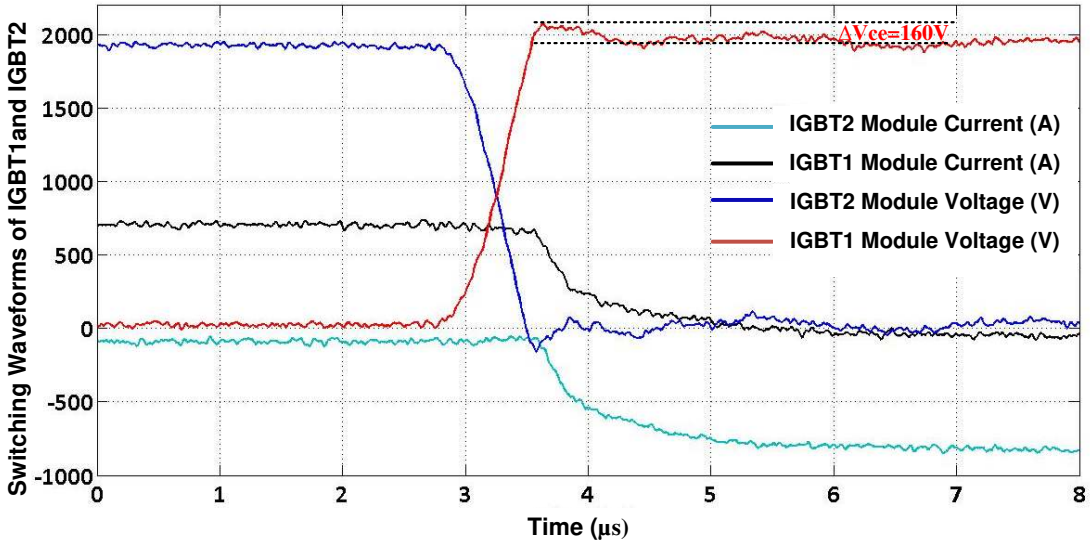


Figure 5.10 Switching Waveforms of IGBT1 and IGBT2 in the field for I_c=770A for turn-off characteristics

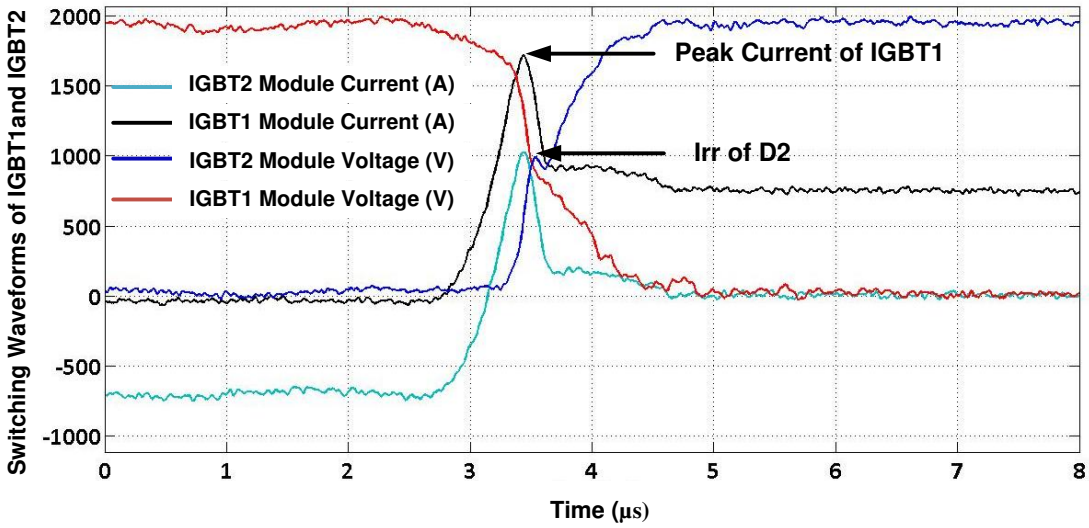


Figure 5.11 Switching Waveforms of IGBT1 and IGBT2 in the field for I_c=770A for turn-on characteristics

rated current of I_c=770 A peak which is lower than the collector current of I_c=2175A exercised in the laboratory switching test, a lower voltage spike of ΔV_{ce} = 160V was recorded (Figure 5.10). The diode reverse recovery and IGBT peak current values are 1000A and 1750, respectively as shown in Figure 5.11. The field test results of the HB unit show that switching performances of HV IGBT modules are quite satisfactory and consistent with design objectives.

5.2.1.2 DC Link Current and Voltage Waveforms

The variations in DC link voltage and current of HB1 in phase-A of CMC Module-1 of T-STATCOM system has been measured by an HV probe and a Rogowski coil for a duration of 100 ms as seen in Figure 5.12 when T-STATCOM delivering -50 MVAr full capacitive to the PCC. The CMC Module-1 is under MSS method with Δts=400µs for the equalization of DC link capacitor voltages during the test and all quantities are taken as 1 µs averaged data. Due to exposing high EMI/EMC interference from the noisy environment of the test, the Rogowski coil could not especially measure the current values at zero points accurately. The peak value of the

DC link voltage is under 2000 V which is safe for DC link capacitors as seen from Figure 5.12.

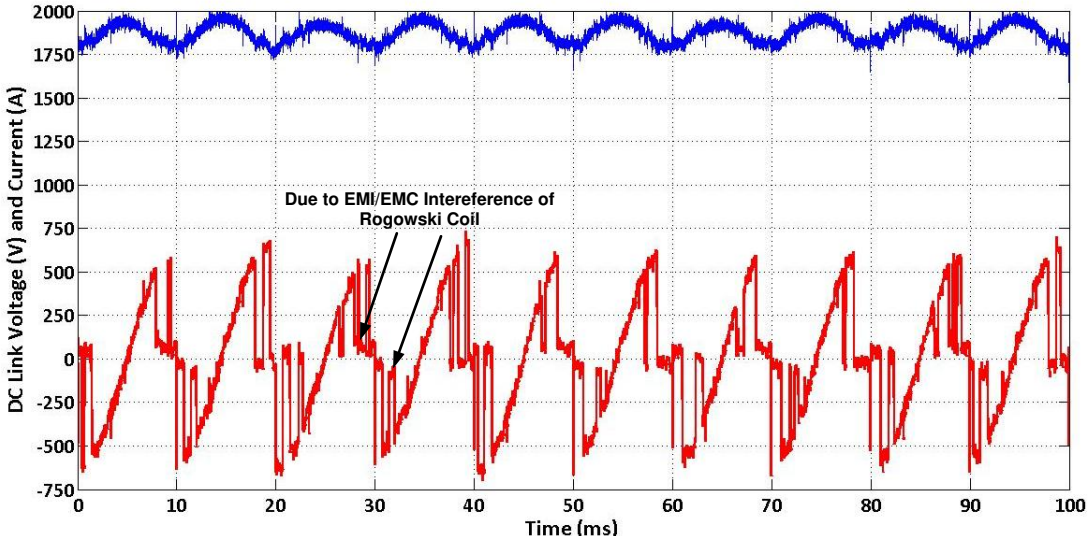


Figure 5.12 DC link voltage and current of HB1 in phase-A of CMC module-1 when T-STATCOM delivers -50MVAr to the PCC (1µs averaged field data)

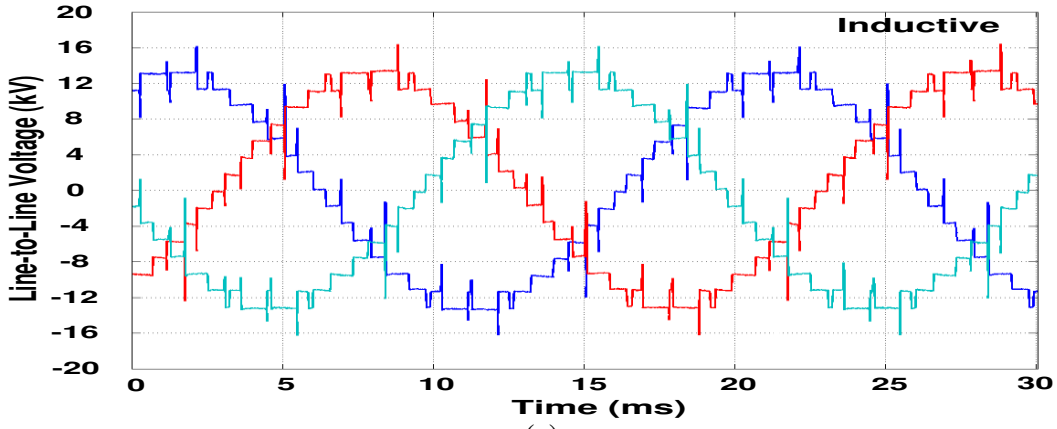
5.2.2 Field Performance of CMC Module

5.2.2.1 Voltage Waveforms at the Input of CMC

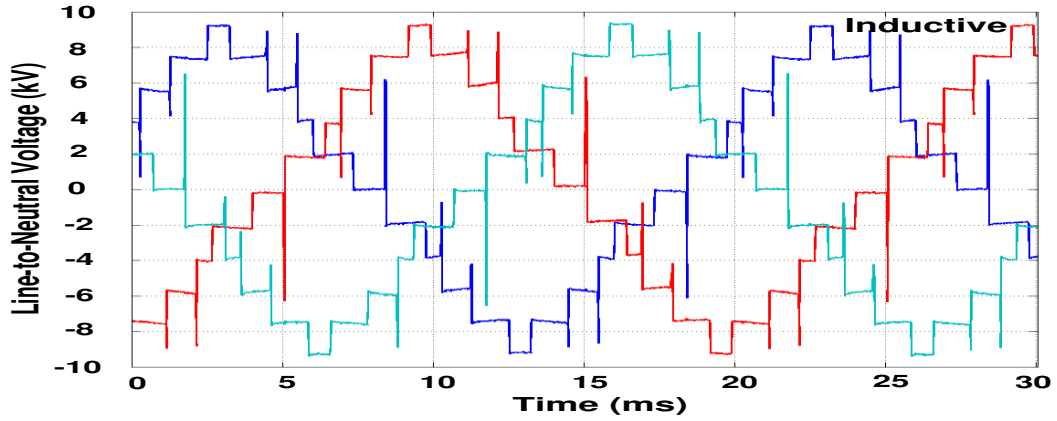
In this subsection, line-to-line and line-to-neutral voltage waveforms at the AC input terminals of a CMC will be given when it is producing rated MVAr in both the inductive and capacitive regions. Figure 5.13 - Figure 5.16 show the voltage waveforms when the CMC is operated with CSS and Modified Selective Swapping with Δt_s=400µs. These waveforms show that the CMC successfully create 11-level line-to-neutral and 21-level line-to-line voltage waveforms regardless of the selective swapping technique applied.

The conventional or modified selective swapping method applied to the CMC module causes generation of voltage spikes superimposed on line-to-neutral voltage waveforms as can be observed from Figure 5.13-b to Figure 5.16-b. These will also reflect to the line-to-line voltage waveforms from Figure 5.13-a to Figure 5.16-a. The cause of voltage spikes in line-to-neutral voltages is the swapping method (conventional or modified selective swapping method) applied to the CMC module as described in Chapter 4.1.3. During the swapping period, the conducting IGBT is turned off and an appropriate IGBT in another HB is going to be turned on with a delay of 13µs (deadband) in order to prevent the capacitor from being short-circuited through two IGBTs (shoot-through) on the same leg in any HB.

Therefore in the swapping period, the current closes its path through the antiparallel diodes of the HB whose capacitor is bypassed. This will impose $+V_d$ or $-V_d$ on the line-to-neutral voltage of the associated CMC module depending upon the direction of the current. These voltage spikes have a duration of nearly 15.5µs (13µs deadband + nearly 2.5µs turn-on time). Depending upon the voltage level in the line-to-neutral voltage waveform at which the associated HBs are going to be interchanged for swapping purpose, the magnitude of the overshoot or undershoot may be V_d, $2V_d$, $3V_d$ or $4V_d$.

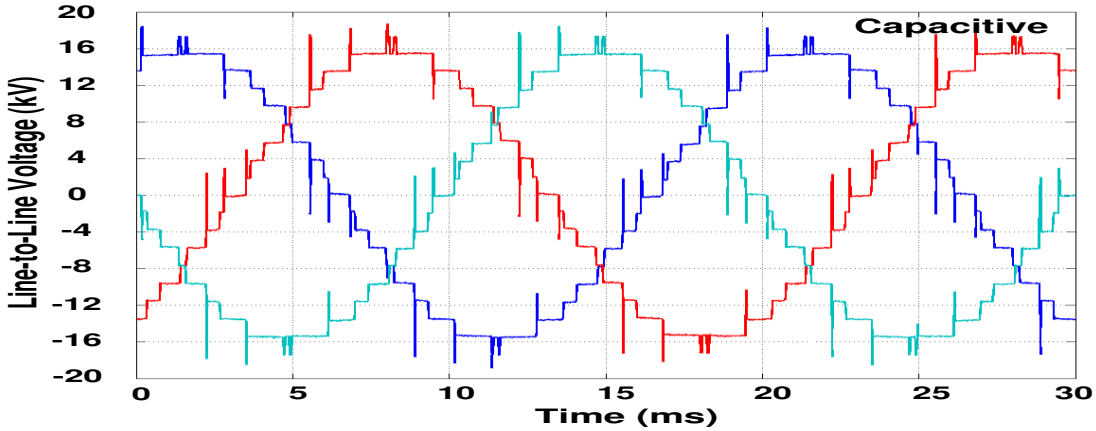


(a)

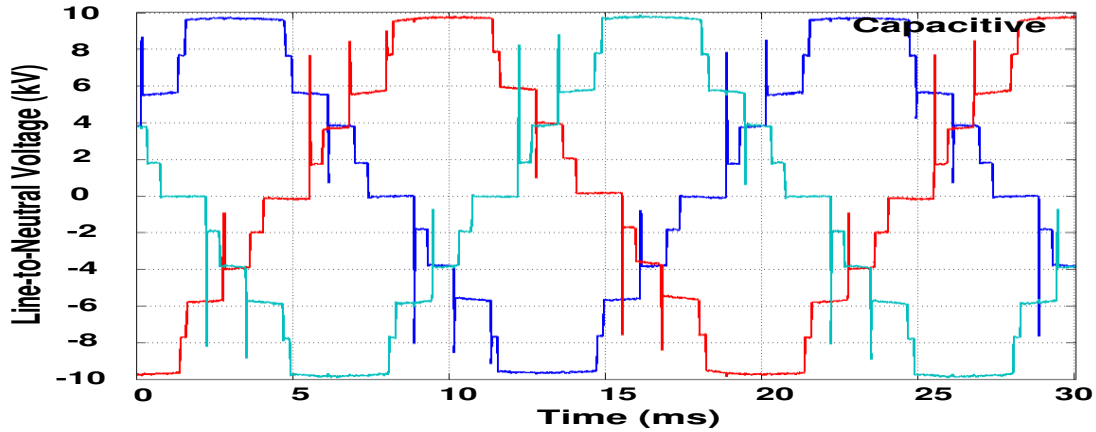


(b)

Figure 5.13 The waveforms of a) line-to-line and b) line-to-neutral voltages for a CMC at full inductive operation mode under Conventional Selective Swapping (CSS) method

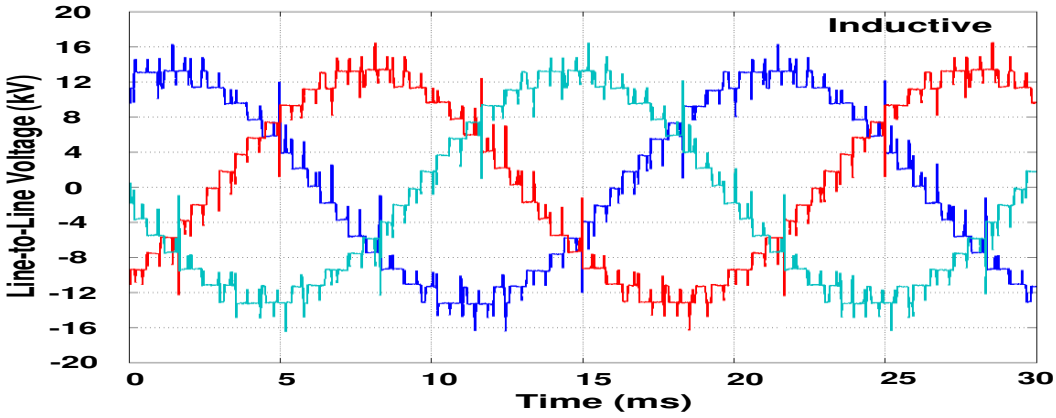


(a)

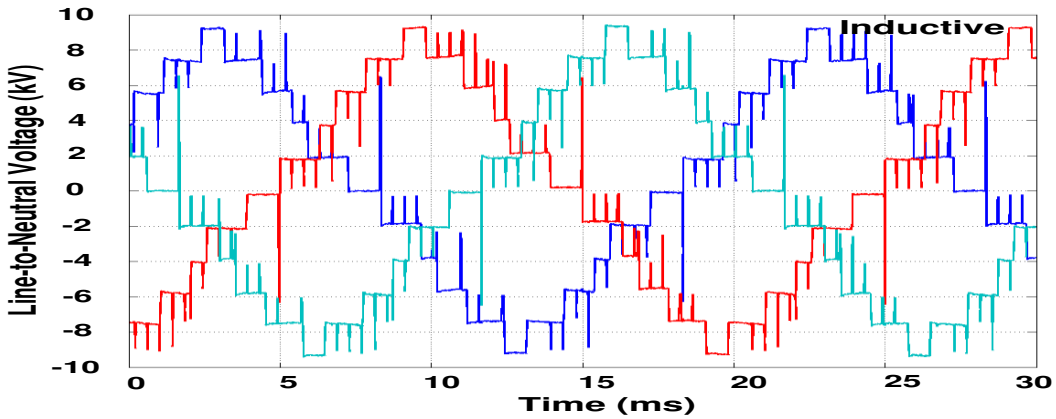


(b)

Figure 5.14 The waveforms of a) line-to-line and b) line-to-neutral voltages for a CMC at full capacitive operation mode under Conventional Selective Swapping (CSS) method



(a)



(b)

Figure 5.15 The waveforms of a) line-to-line and b) line-to-neutral voltages for a CMC at full inductive operation mode under Modified Selective Swapping (MSS) method with Δt_s=400µs

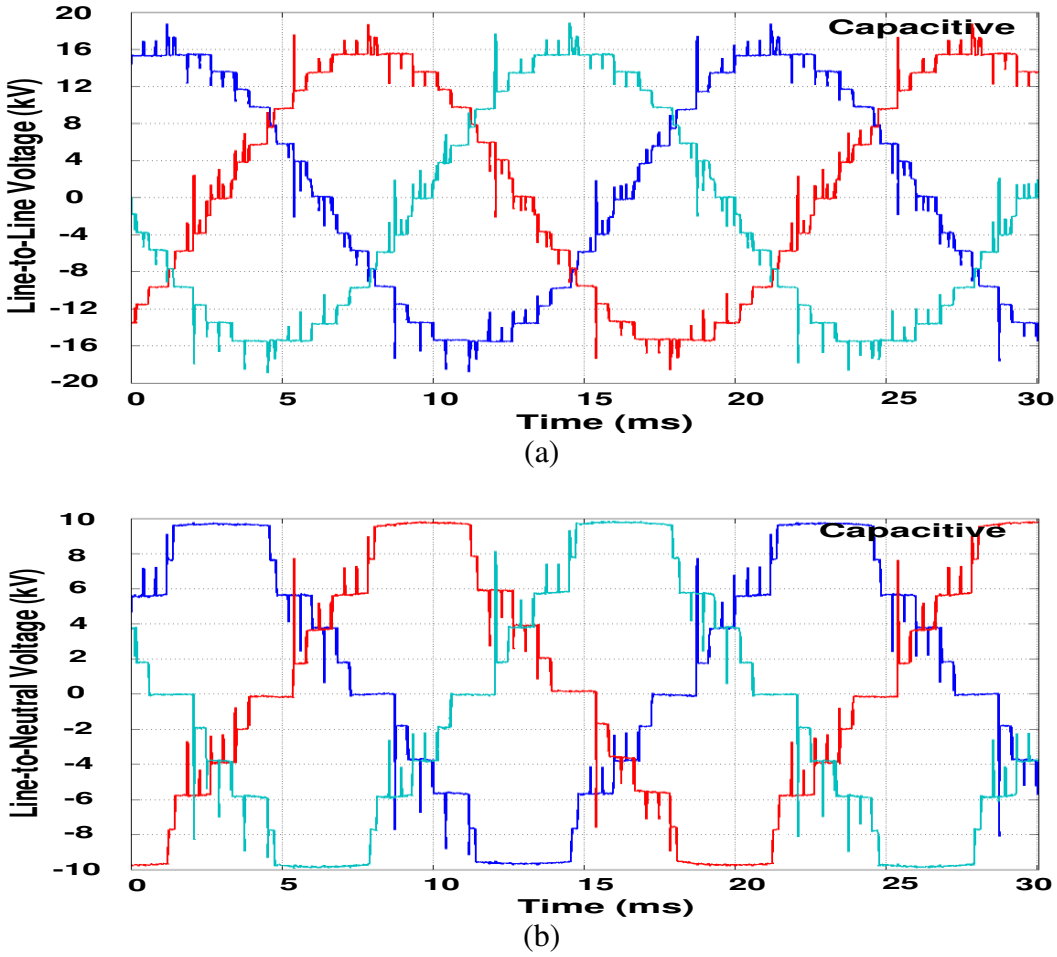


Figure 5.16 The waveforms of a) line-to-line and b) line-to-neutral voltages for a CMC at full capacitive operation mode under Modified Selective Swapping (MSS) method with Δt_s=400µs

The duration of these spikes can be reduced by choosing a smaller deadband in the design at the expense of a lower safety factor against the risk of shoot-through. Minimum value of the deadband is nearly 5µs. Spikes with magnitudes of $\pm 3V_d$ and $\pm 4V_d$ can be eliminated by optimum utilization of the switching devices at the expense of more complex control software as described in Chapter 4.1.3. These spikes do not reflect to the supply buses to which the T-STATCOM is connected

because they will be absorbed by the properly chosen series filtering reactors of the system.

Harmonic contents of the line-to-neutral and the line-to-line voltage waveforms just at the input of the CMC are given in Table 5.4 and Table 5.5 for rated inductive and capacitive operation modes, respectively.

Table 5.4 CMC voltage harmonics at +10MVAr

Harmonic Number	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)	V_{ab}(%)	V_{bc}(%)	V_{ca}(%)
1	100	100	100	100	100	100
3	12.6	12.2	12.0	0.1	0.1	0.2
5	0.5	0.4	0.5	0.4	0.4	0.5
7	0.3	0.2	0.3	0.2	0.2	0.3
11	0.1	0.2	0.1	0.2	0.2	0.1
13	0.5	0.6	0.6	0.5	0.6	0.5
17	3.0	3.0	3.0	3.0	3.0	3.0
19	2.8	2.8	2.8	2.8	2.8	2.8
21	2.0	2.1	2.1	0.1	0.1	0.1

Table 5.5 CMC voltage harmonics at -10MVAr

Harmonic Number	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)	V_{ab}(%)	V_{bc}(%)	V_{ca}(%)
1	100	100	100	100	100	100
3	10.7	10.4	10.4	0.1	0.1	0.1
5	0.7	0.5	0.5	0.6	0.5	0.6
7	0.2	0.1	0.2	0.2	0.2	0.1
11	0.1	0.1	0.2	0.1	0.1	0.1
13	0.4	0.4	0.5	0.4	0.5	0.4
17	3.3	3.3	3.3	3.3	3.3	3.3
19	3.1	3.1	3.1	3.1	3.1	3.1
21	0.1	0.1	0.1	0.1	0.1	0.1

Following conclusions can be drawn from Table 5.4 and Table 5.5:

1. The SHEM applied in this research work successfully minimizes 5th, 7th, 11th and 13th harmonics in the line-to-neutral voltage waveforms.
2. Although the 3rd harmonic component is significant in the line-to-neutral waveforms, it becomes vanishingly small in line-to-line voltage waveforms.

5.2.2.2 Transient Performance of CMC Module

Figure 5.17 shows the the transient performance of the one of the CMC modules for the transitifon from capacitive to inductive modes of operation.. These voltage and current records are made at the AC input of one of the CMCs. The Q_{set} is varied from 40 MVAr capacitive to 40 MVAr inductive. In both set of records, modulation changes are made at zero crossing points of line current waveforms by the controller.

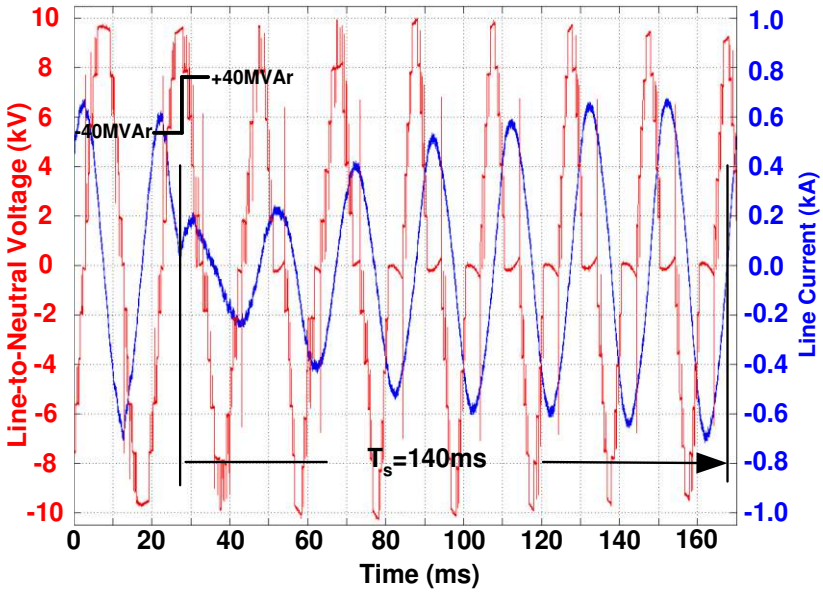


Figure 5.17 The transient-free transitions of CMC without feedforward controller (CMC-side field data)

It is seen from Figure 5.17 that modulation index changes made at current zeros provide a smooth transition between two operating points and no any extreme changes in both current and voltage waveforms. A feedforward block based on the power angle, δ against the modulation index value, M obtained by the field tests has been applied to the closed-loop controller of DC link voltage for T-STATCOM system. Figure 5.18 illustrates the benefits of the feedforward controller which reduces the settling time from 140ms to 100ms.

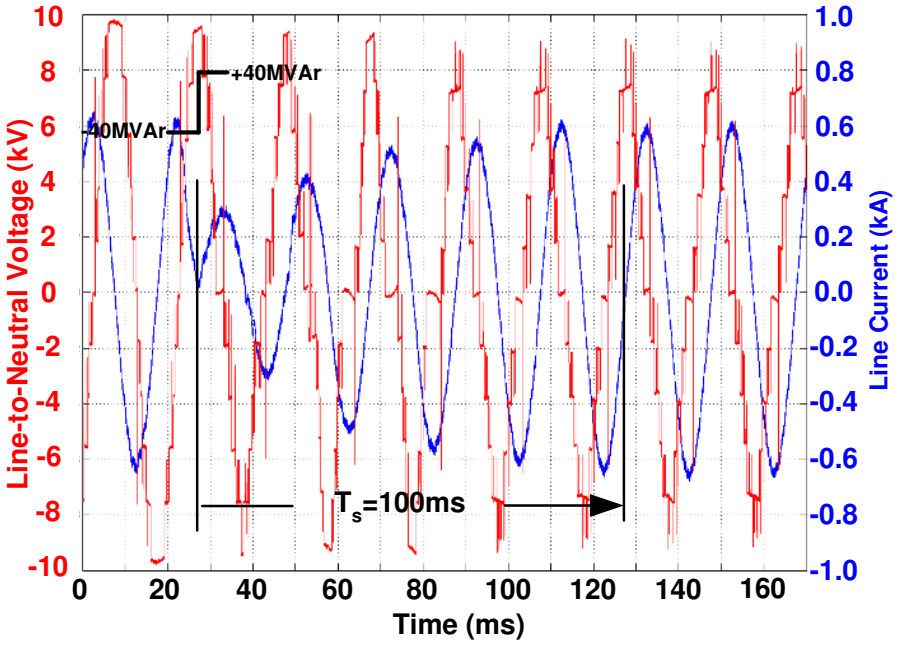
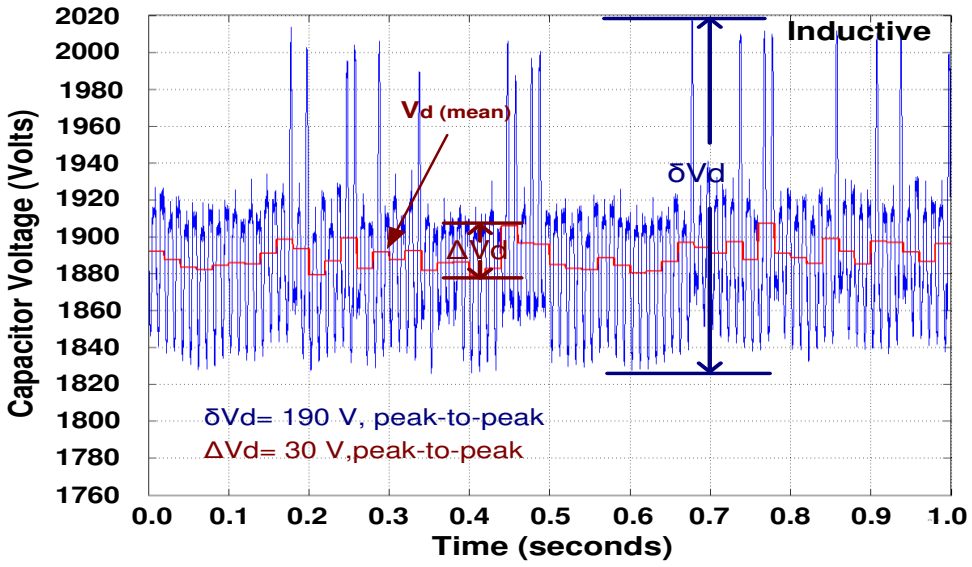


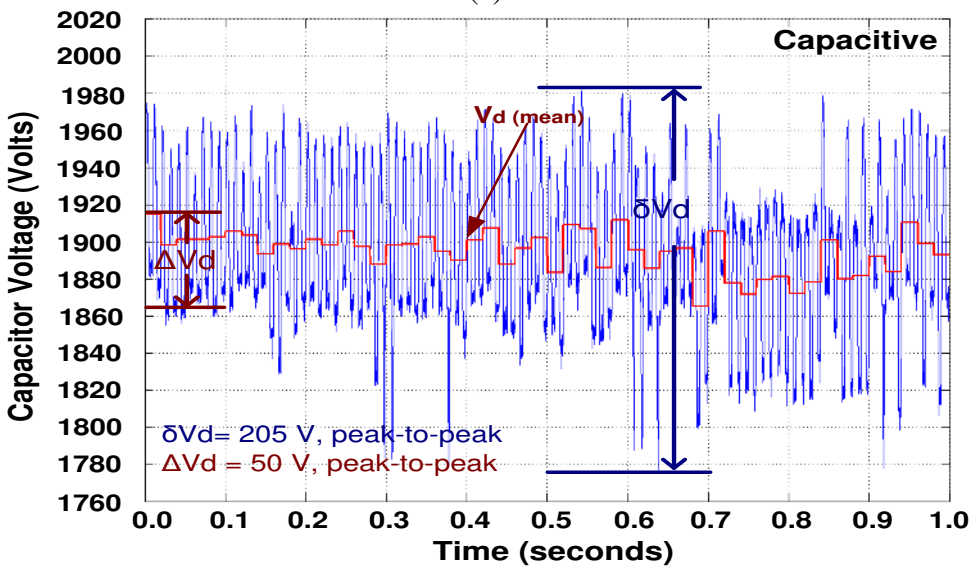
Figure 5.18 The transient-free transitions of T-STATCOM with feedforward controller (CMC-side field data)

5.2.2.3 Performance of Selective Swapping Methods on Balancing DC Link Capacitor Voltages

The performance of MSS method in balancing the DC link voltages is investigated by using field test results. MSS is also compared with CSS in view of the instantaneous voltage peak-to-peak ripple, δV_d, and peak-to-peak mean dc link voltage ripple, ΔV_d, of DC link voltage and effective switching frequency, $f_{sw(eff)}$ (number of turn-ons in 1 second per switch). Figure 5.19 - Figure 5.21 show the variations in instantaneous values of DC link capacitor voltage for CSS and MSS methods (sampling rate=1MHz). The variations in mean DC voltages ($V_{d,mean}$) are also marked on the same waveforms (20ms averaged data).

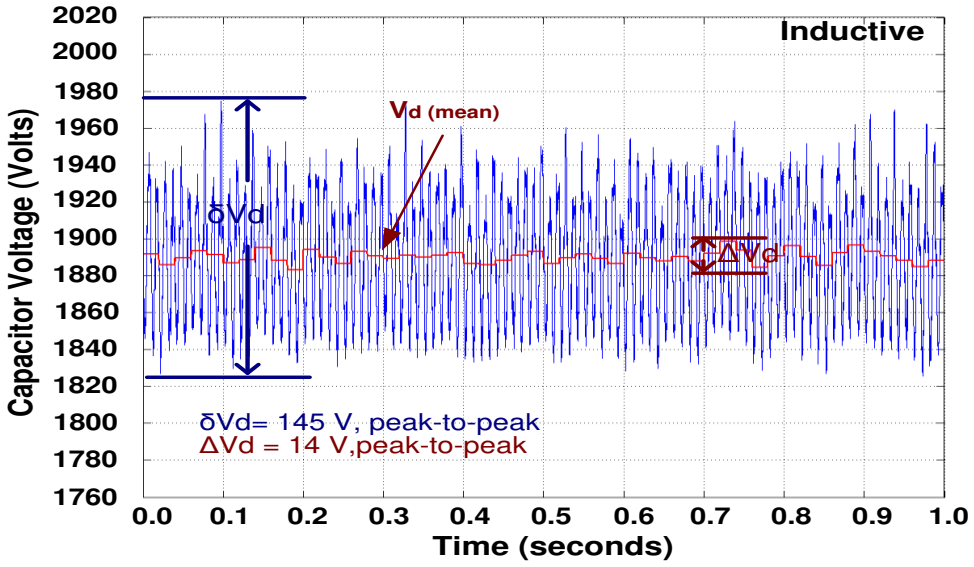


(a)

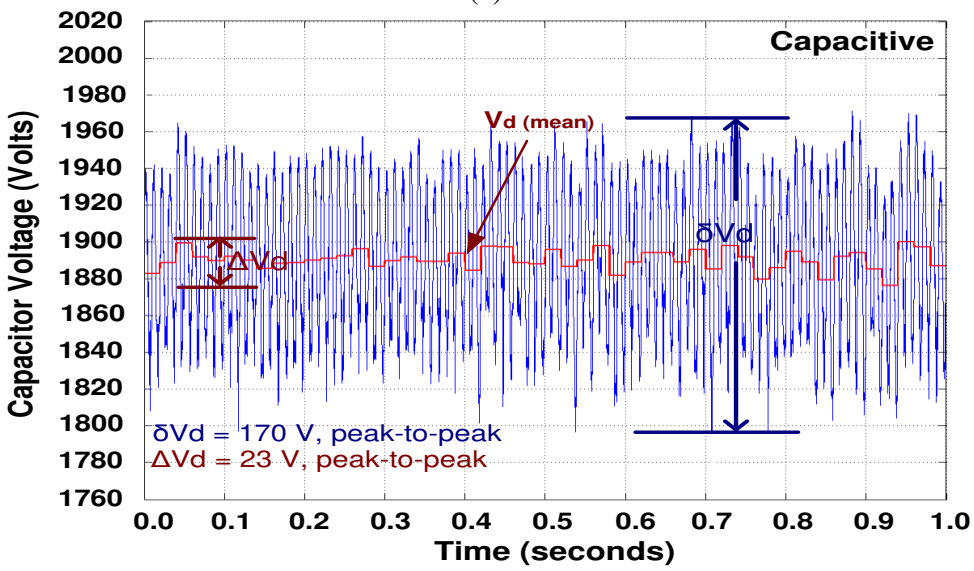


(b)

Figure 5.19 Variations in the DC link voltage of an H-Bridge under Conventional Selective Swapping (CSS) ((a) full inductive case, (b) full capacitive case, field data)

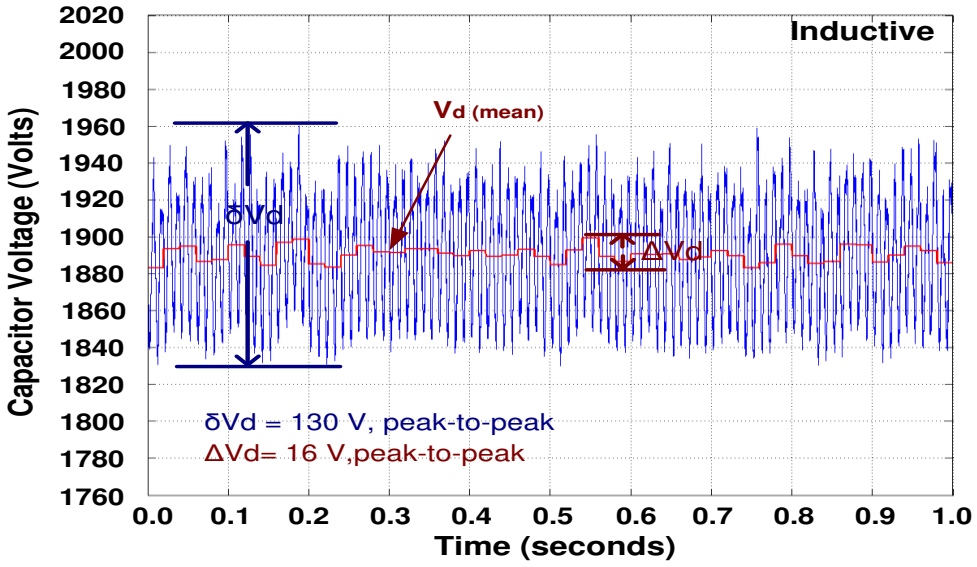


(a)

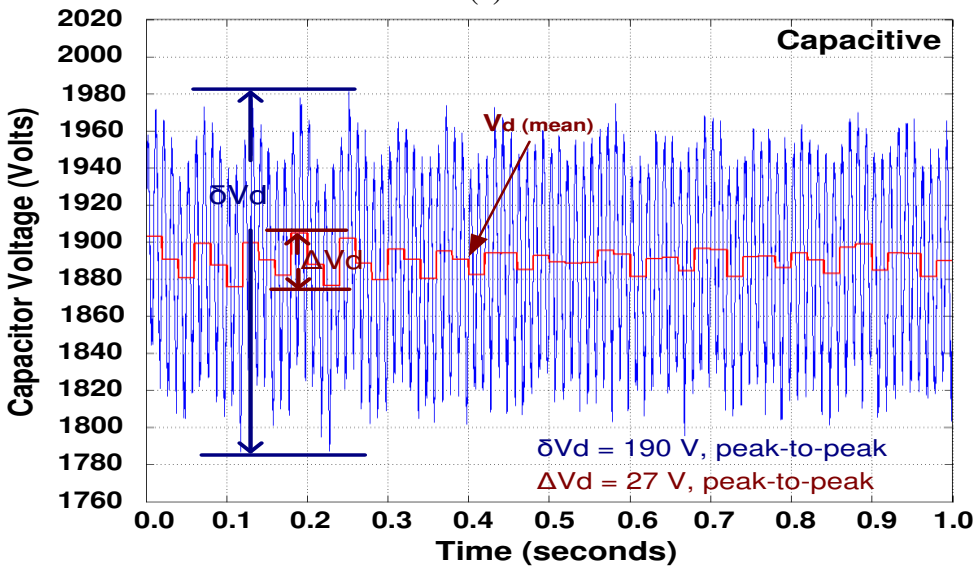


(b)

Figure 5.20 Variations in the dc link voltage of an H-Bridge under MSS method with Δt_s =400 µs
((a) full inductive case; (b) full capacitive case, field data)



(a)



(b)

Figure 5.21 Variations in the dc link voltage of an H-Bridge under MSS method with Δt_s =200 µs
((a) full inductive case; (b) full capacitive case, field data)

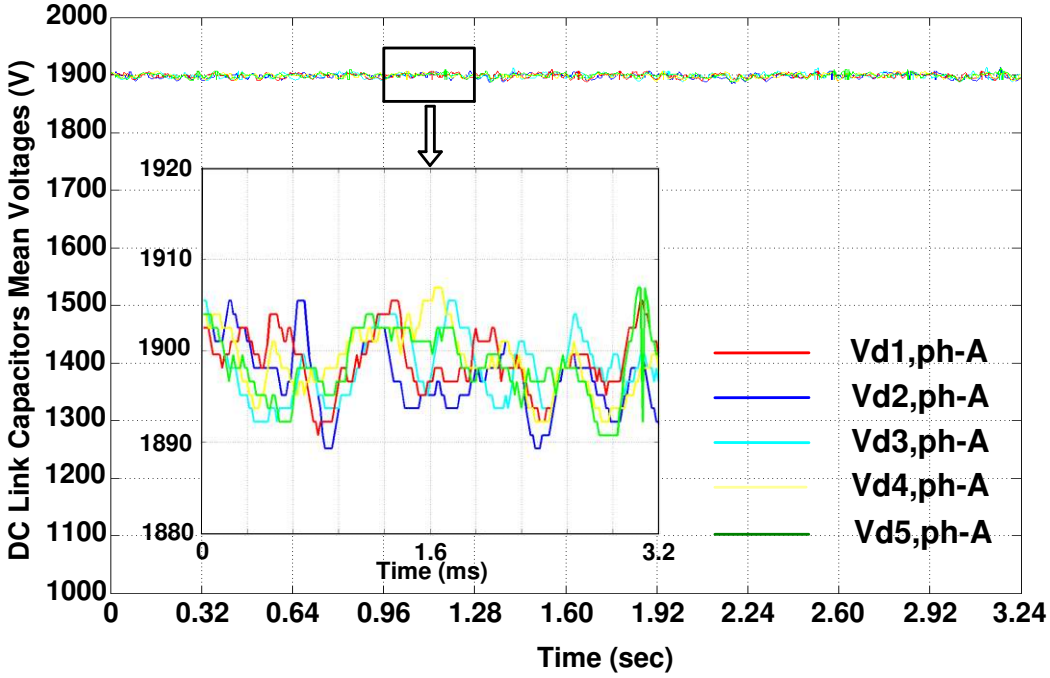
These results are summarized in Table 5.6. MSS algorithm reduces considerably both the instantaneous DC link voltage ripple and mean DC link voltage ripple at the

expense of higher switching losses for power semiconductors. It is not beneficial to reduce swapping period, Δt_s, considerably, i.e. below 400µs according to field test results given in Table 5.6. These values are consistent with those of simulation results given in Table 2.7 and -2.8 in Chapter-2.

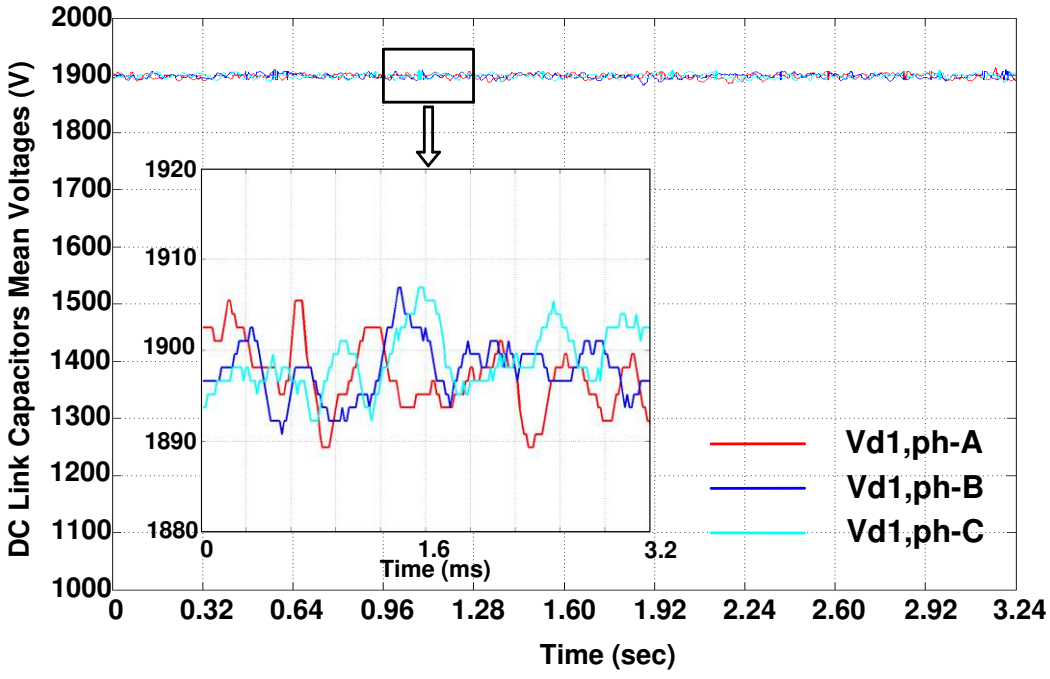
Table 5.6 Performance of selective swapping algorithms

Applied Method	**Inductive**			**Capacitive**		
	CSS	MSS with 400µs	MSS with 200µs	CSS	MSS with 400µs	MSS with 200µs
Instantaneous Voltage Ripple (peak-to-peak)	190V	145V	130V	205V	170V	190V
Mean Voltage Ripple (peak-to-peak)	30V	14V	16V	50V	23V	27V
Effective Switching Frequency	250Hz	500Hz	650Hz	200Hz	500Hz	700Hz

The variations in DC link capacitor voltages in one phase of any one of the five CMC modules are also recorded for full inductive operation mode. A typical record (120µs averaged data) is as shown in Figure 5.22. The instantaneous variations in the first H-bridge capacitors in all phases of the same CMC module are also recorded as shown in Figure 5.22. These results show that the modified selective swapping algorithm and its digital implementation balance the DC link capacitor voltages perfectly.



(a)



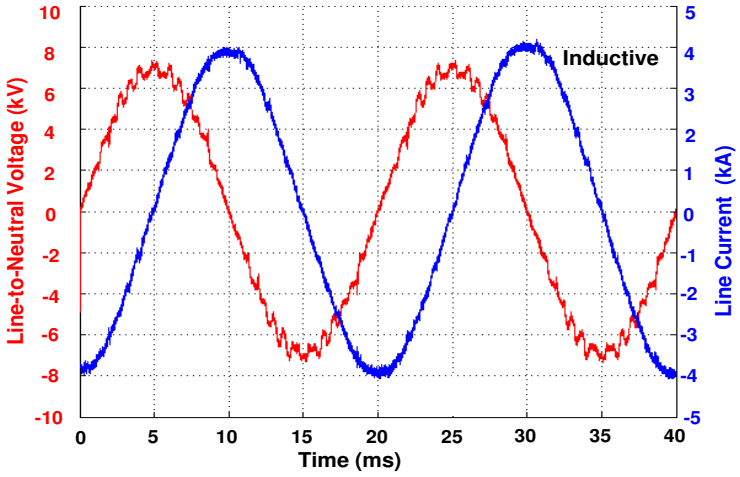
(b)

Figure 5.22 Variations in the DC link mean voltages of a CMC ((a) DC link voltages of HBs in phase-A; (b) DC link voltages of HB1s in three phases, Field data)

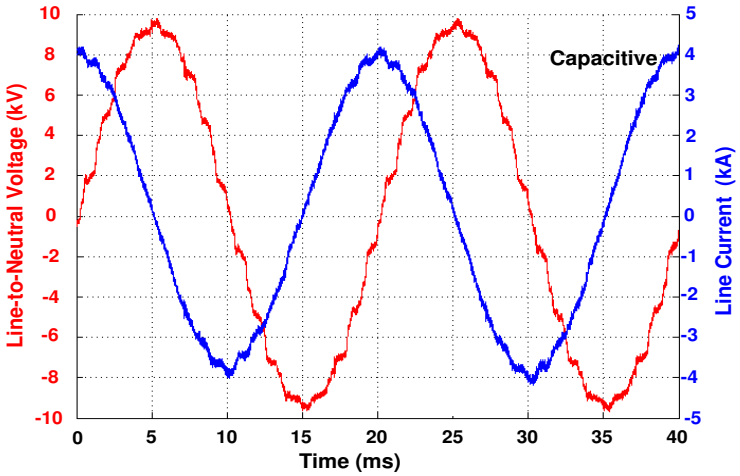
5.2.3 Field Performance of T-STATCOM System

5.2.3.1 Voltage and Current Waveforms at MV (10.5 kV) and HV (154 kV) sides

The voltage and current waveforms at PCC and AC side of CMCs are given in Figure 5.23 and Figure 5.24 while the T-STATCOM is generating ±50MVAr at PCC.

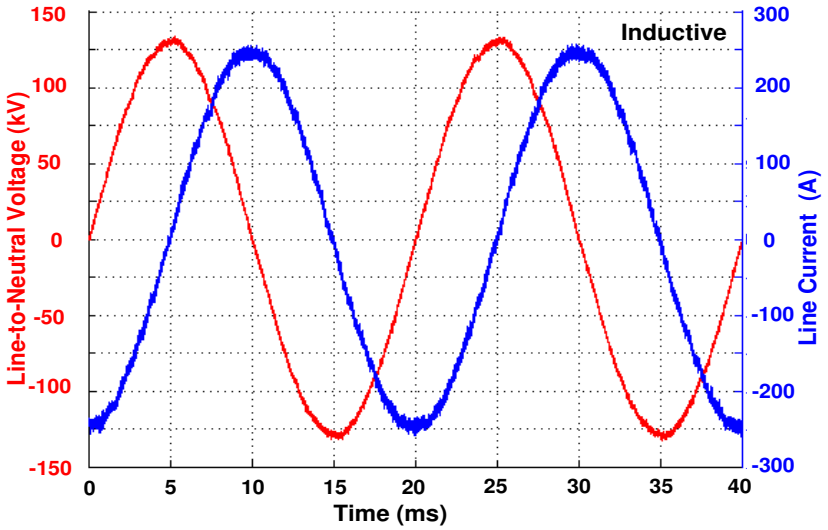


(a)

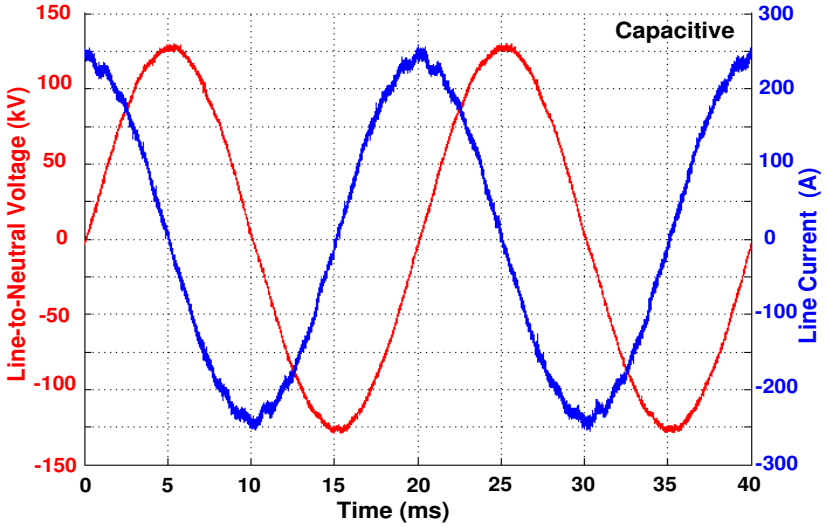


(b)

Figure 5.23 Line-to-neutral voltage and line current waveforms at MV side of T-STATCOM ((a) full inductive; (b) full capacitive, field data)



(a)



(b)

Figure 5.24 Line-to-neutral voltage and line current waveforms at HV side of T-STATCOM ((a) full inductive; (b) full capacitive, field data)

These waveforms have shown the success of digital implementation of the control system as well as the Q and P control, waveform synthesizing, SHEM, Selective Swapping and PLL techniques employed in the design and implementation of the overall system.

5.2.3.2 Voltage and Current Harmonics at PCC (154 kV)

Harmonic contents of the line-to-ground voltages at PCC with and without T-STATCOM are as given in Table 5.7. These values are deduced from the measurements of resistive-capacitive voltage transducers (RCVT by TRENCH). The RCVT has a frequency bandwidth of 1MHz and can measure low order harmonic components with unity gain. It is seen from Table 5.7 that the operation of T-STATCOM at its rated capacity in both capacitive and inductive operation modes does not affect the harmonic content of the PCC voltage.

Table 5.7 PCC line-to-ground voltage harmonicsmeasured by RCVT sensors

Harmonic Number	STATCOM Disconnected		Capacitive Mode		Inductive Mode		IEEE Std.519-1992 (%)
	$V_{b,g}$ (%)	$V_{c,g}$ (%)	$V_{b,g}$ (%)	$V_{c,g}$ (%)	$V_{b,g}$ (%)	$V_{c,g}$ (%)	
1	100	100	100	100	100	100	**100**
3	0.6	0.5	0.6	0.5	0.6	0.5	**1.0**
5	0.5	0.4	0.5	0.4	0.4	0.2	**1.0**
7	0.4	0.3	0.4	0.3	0.3	0.2	**1.0**
11	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
13	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
17	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
19	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
21	0.1	0.1	0.1	0.1	0.1	0.1	**1.0**
THD	**0.9**		**0.9**		**0.9**		**1.5**

Harmonic contents of the coupling transformer line current waveforms on the HV side (154 kV) are as given in Table 5.8. Both individual voltage and current harmonic values, and THD and TDD values comply with IEEE Std. 519-1992. The obtained field values are consistent with the desing values given in Chapter 3.

Table 5.8 154kV side current harmonics at rated power (I_L=188A, I_{SC}=20kA)

Harmonic Number	Capacitive Mode			Inductive Mode			IEEE Std.519-1992 (%)
	I_a (%)	I_b (%)	I_c (%)	I_a (%)	I_b (%)	I_c (%)	
1	100	100	100	100	100	100	**100**
3	0.2	0.2	0.2	0.2	0.2	0.2	**3.0**
5	0.4	0.4	0.4	0.4	0.4	0.4	**3.0**
7	0.2	0.2	0.2	0.2	0.2	0.2	**3.0**
11	0.1	0.1	0.1	0.1	0.1	0.1	**3.0**
13	0.1	0.1	0.1	0.1	0.1	0.1	**1.5**
17	0.5	0.5	0.5	0.5	0.5	0.5	**1.15**
19	0.3	0.3	0.3	0.3	0.3	0.3	**1.15**
21	0.1	0.1	0.1	0.1	0.1	0.1	**1.15**
TDD	**0.77**			**0.77**			**3.75**

5.2.3.3 Effects of Series Reactors on Voltage Harmonics

Harmonic contents of the line-to-ground and line-to-line voltage waveforms on the medium voltage side of the coupling transformer (after series connected input filter reactor) are as given in Table 5.9.

Table 5.9 10.5kV side voltage harmonics measured by RCVT sensors

Harmonic Number	Capacitive Mode			Inductive Mode		
	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)	$V_{a,g}$(%)	$V_{b,g}$(%)	$V_{c,g}$(%)
1	100	100	100	100	100	100
3	0.3	0.2	0.2	0.3	0.1	0.2
5	0.2	0.1	0.1	0.4	0.3	0.5
7	0.1	0.1	0.2	0.1	0.1	0.1
11	0.1	0.1	0.2	0.1	0.1	0.1
13	0.1	0.1	0.1	0.1	0.1	0.1
17	2.0	2.0	2.1	1.7	1.7	1.7
19	2.3	2.2	2.2	2.0	1.9	1.9
21	0.1	0.1	0.1	0.1	0.1	0.1

These results show that voltage harmonics are filtered out by the input filter reactor to a certain extent. Harmonic contents of the line current on the medium voltage side of the coupling transformer are given in Table 5.10. Their magnitudes are relatively low, as expected.

Table 5.10 CMC current harmonics at rated power

Harmonic Number	Capacitive Mode			Inductive Mode		
	I_a(%)	I_b(%)	I_c(%)	I_a(%)	I_b(%)	I_c(%)
1	100	100	100	100	100	100
3	1.2	1.2	1.2	2.0	2.0	2.0
5	0.5	0.5	0.5	0.4	0.4	0.4
7	0.6	0.6	0.6	0.2	0.2	0.2
11	0.3	0.3	0.3	0.1	0.1	0.1
13	0.2	0.2	0.2	0.1	0.1	0.1
17	0.8	0.8	0.8	0.5	0.5	0.5
19	0.9	0.9	0.9	0.2	0.2	0.2
21	0.1	0.1	0.1	0.1	0.1	0.1

5.2.3.4 Terminal Voltage Regulation (V-mode)

The 154 kV bus-bar to which the T-STATCOM is connected is a strong bus (5300 $MVA_{,SC}$). Therefore, the effect of T-STATCOM on bus-bar voltage in V-mode does not exceed ±1% depending upon the power demand of the loads supplied from the same bus. The performance of the T-STATCOM in V-mode is shown in Figure 5.25. These waveforms are constructed from 20ms averaged data. Line-to-line rms voltage at PCC in Figure 5.25 when T- STATCOM is in service is not a pure level voltage variation (0.5kV peak-to-peak max). These fluctuations are attributed to the facts that 1) Analog to digital converter introduces an error of ±0.5%, and 2) Sometimes the installed capacity of the T-STATCOM becomes insufficient to keep the terminal voltage precisely constant at the set value (159.5 kV) as can be understood from

Figure 5.25 shows that reactive power at PCC is fluctuating since it is not controlled in V-mode.

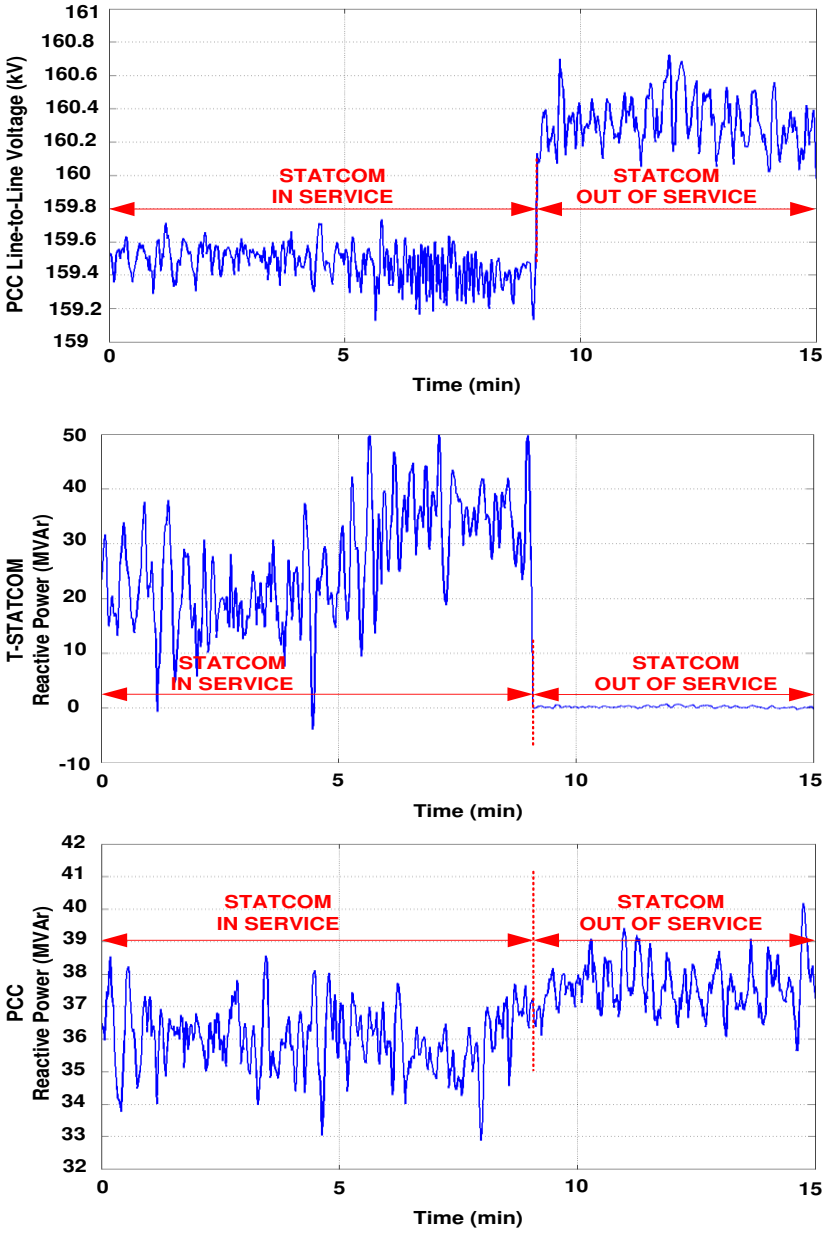


Figure 5.25 The performance of T-STATCOM in V-mode (Field data)

5.2.3.5 Reactive Power Compensation (Q-mode)

The records in Figure 5.26 (20ms averaged data) show the performance of the T-STATCOM in Q-mode. In the first 5-minute part of the record, the T-STATCOM brings the power factor to unity as viewed from the 154 kV side of the autotransformers. For this purpose, T-STATCOM produces nearly 45 MVAr-inductive. When T-STATCOM is operated in standby mode to produce 0 MVAr, nearly 27 MVAr-capacitive reactive power starts to flow to PCC via the autotransformers. This reactive power flow is not equal to the 45 MVAr inductive reactive power previously generated by T-STATCOM. This is attributed to the fact that the bus voltage at PCC increases nearly 2 kV, owing to the non-linear characteristics of power plants and loads connected to the same bus when T-STATCOM is operating in standby mode.

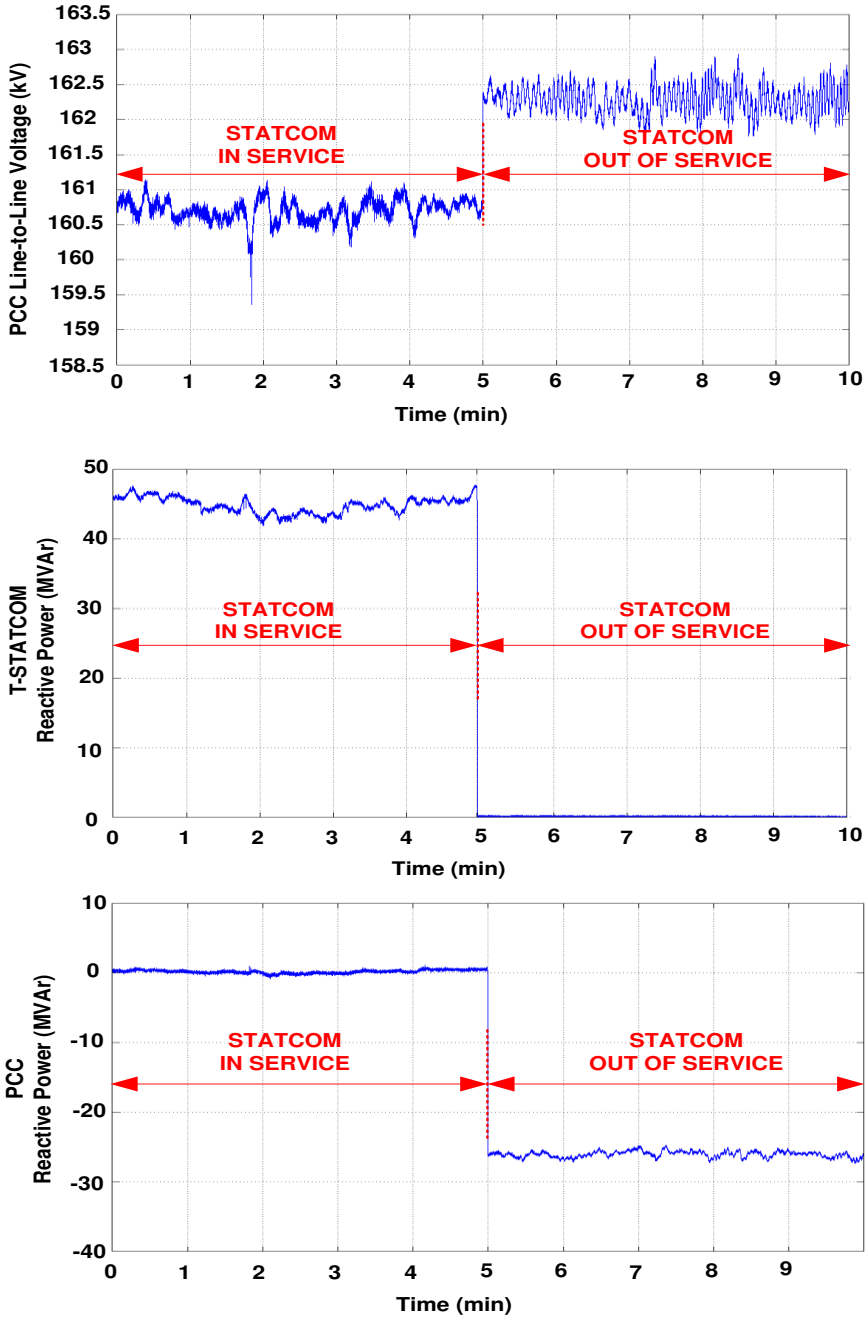
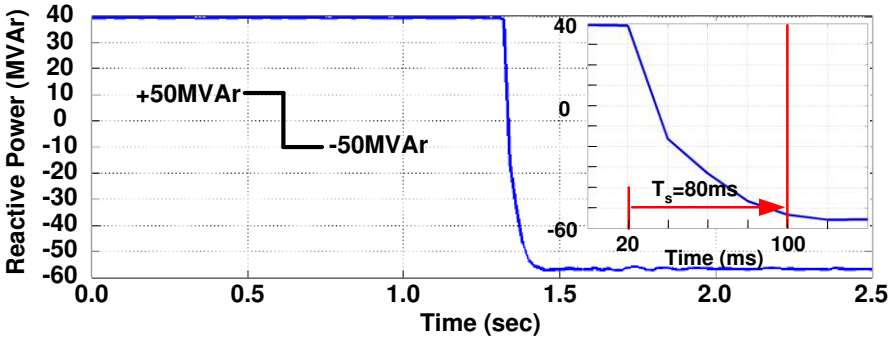


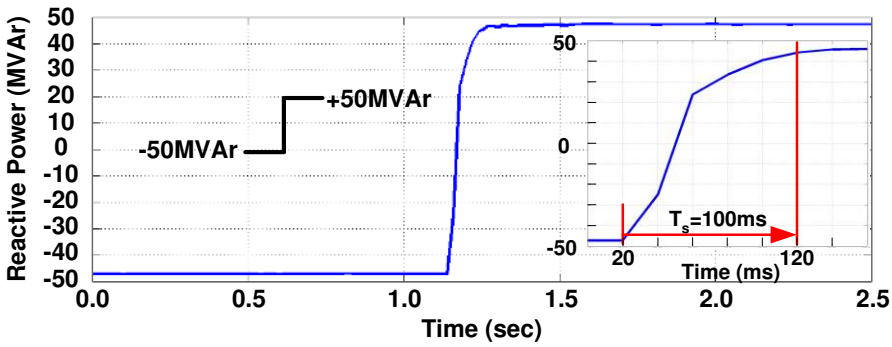
Figure 5.26 The performance of T-STATCOM in Q-mode (Field data)

5.2.3.6 Transitions Between Full Capacitive and Full Inductive Modes

The reactive power variations on the 10.5 kV side and 154 kV side of the coupling transformer are given when Q_{set} of T-STATCOM is varied from +50 MVAR (inductive) to -50 MVAr (capacitive) in Figure 5.27-a and Figure 5.27-b, respectively. There is a 10 MVAr (inductive) difference between the reactive power values of 154 kV and 10.5 kV sides which is the reactive power consumption of the coupling transformer.



(a)



(b)

Figure 5.27 Transition from a) from full inductive to full capacitive (10.5 kV side, field data) b) full capacitive to full inductive (154 kV side, field data)

As can be seen from these waveforms in Figure 5.27-a, the settling time of the closed loop control system is only 80ms. On the other hand, when Q_{set} is varied from -50 MVAr (capacitive) to +50 MVAr (inductive), the response of the closed loop control system will be as in Figure 5.27-b. For this case, the settling time is measured to be 100ms. It is worth to note that if the T-STATCOM were operated in open loop control mode, the settling time would not exceed 45ms.

The line-to-neutral voltage waveform and the associated line current waveform on the 10.5 kV side of the coupling transformer during transition from Q_{set} = +50 MVAr to -50 MVAr with the closed loop control system are given in Figure 5.28. The associated waveforms from Q_{set}= -50 MVAr to +50 MVAR are shown in Figure 5.29. The responses in Figure 5.28 and Figure 5.29 show the smooth and fast response of the control system against changes in Q_{set} from full inductive to full capacitive, or vice versa.

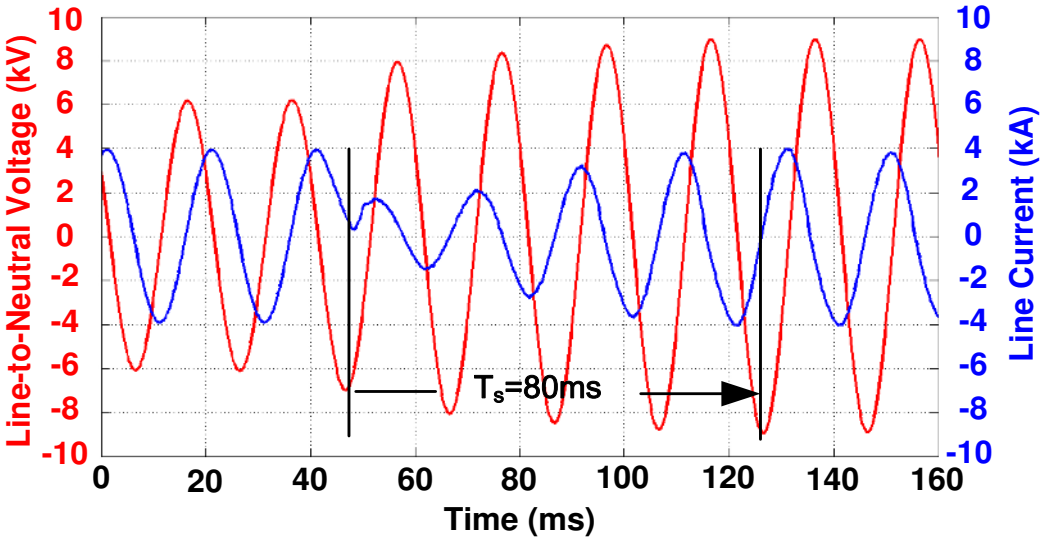


Figure 5.28 Variations in line-to-ground voltage and current during the transition from full inductive to full capacitive (10.5 kV side, field data)

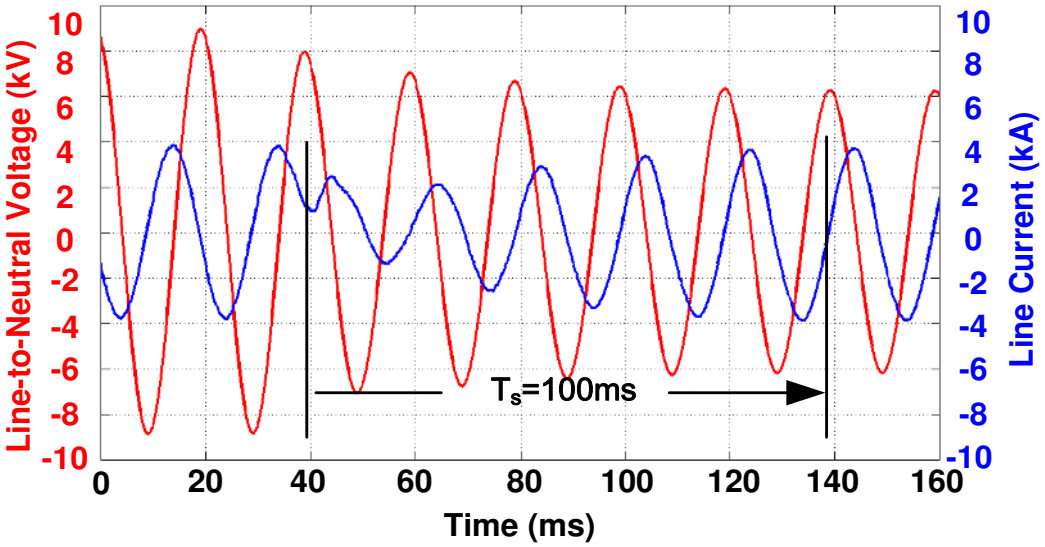


Figure 5.29 Variations in line-to-ground voltage and current during the transition from full capacitive to full inductive (10.5 kV side, field data)

CHAPTER 6

CONCLUSIONS

Nowadays, FACTS are being increasingly used in power systems, to enhance the system utilization and power transfer capacity as well as the stability, security, reliability and power quality of AC system interconnections. Among FACTS devices, the shunt controllers have shown feasibility in terms of in a wide range of problem-solving abilities from transmission to distribution levels. For decades, it has been realized that by manipulating the compensated reactive power, the transmittable active power through the interconnected networks can be increased without installing new transmission lines and the voltage profile of the buses can also be controlled easily by the shunt controllers.

As a shunt controller, Static Synchronous Compensator (STATCOM) systems are being installed for transmission and distribution levels. They are based on switching power converters employing turn-off capable semiconductor switches and hence they may operate under high switching frequency and provide faster response. Two-level, six-pulse bridge converters with relatively high switching frequencies and relatively low installed capacities are usually being the characteristics of Distribution type STATCOM (D-STATCOM) systems. These are usually connected to the Medium Voltage (MV) load bus via a step-up coupling transformer. However, Transmission type STATCOM (T-STATCOM) systems have much higher installed capacities and therefore the power semiconductors in their converter system/s should be switched at

lower frequencies. That is why in practical applications of T-STATCOM systems either multi-pulse converters or Multilevel Converter (MC)s are to be utilized. These systems are connected to the High Voltage (HV) or extra high voltage (EHV) buses of the transmission systems via coupling transformers.

Among the mature multilevel converter topologies, due to its modularity, flexibility and less number of power components, Cascaded Multilevel Converter (CMC) topology is the most promising alternative for T-STATCOM applications. It is possible to reach high voltage levels by the use of appropriate number of HBs connected in series for CMC topology. By it modular structure, the CMC can flexibly expand the output power capability if needed and is favorable to manufacturing. Moreover, redundancy can be easily applied in the CMC to enhance reliability for the entire system.

This research and technology development work deals with the sizing, system and power-stage designs of an HV IGBT based CMC for T-STATCOM applications. System design and the number of H-Bridge (HB)s in each phase of the Y-connected CMC are achieved in view of Total Harmonic Distortion (THD) at Point of Common Coupling (PCC), Total Demand Distortion (TDD) of the line currents and individual harmonic current limits recommended by IEEE Std.519-1992. A 12 kV, ±10 MVAr, 11-level CMC Module power stage with five HBs in each phase is designed and then implemented to deliver ±10MVAr to 154kV transmission bus (PCC) via a series filter reactor and 154/10.5kV coupling transformer. Therefore, the CMC module presented in this work constitutes a building block of large T-STATCOM systems. The Selective Harmonic Elimination Method (SHEM) is applied to synthesize T-STATCOM voltage waveforms at power frequency (50Hz) and the Modified Selective Swapping (MSS) Algorithm is exercised to balance the DC link capacitor voltages, perfectly at the expense of higher switching frequency, and hence switching losses. The power stage is carefully designed and its performance is optimized in view of the current HV IGBT technology.

A 154kV, ±50 MVAr, 11-level T-STATCOM system by the parallel use of five CMCs built in this work has been implemented in the field primarily for the purposes of reactive power compensation and terminal voltage regulation, and secondarily for power system stability. Since the operating voltage of CMC is chosen to be 10.5 kV (max.12 kV) line-to-line, it is connected to 154 kV line-to-line transmission bus through a specially designed 50/62.5 MVA Y-Y connected (YNyn vector group) coupling transformer and each CMC module is connected to secondary side of the coupling transformer via a series filter reactor bank. This is the first industry application of wire-bond HV IGBT based CMC in T-STATCOM applications. Five ±12 MVAr, 10.5 kV CMC modules are operated in parallel by the specially designed fully digital control system composed of DSP and FPGAs.

In the thesis, it is found that the number of HBs in series for CMC topology is not the only parameter on complying with THD and TDD limits specified in IEEE 519-1992. The series filter inductance value has also a great effect on THD and TDD limits. Therefore, choosing L_r value for CMC topology is a crucial issue when designing the system. As the value of series filter inductance rises, the THD and TDD values decrease for CMC topologies with three, five and seven HBs while the variations in AC input voltage of the CMC from full inductive operation to full capacitive operation becomes significantly high. Moreover, there is an optimum point of DC link voltage and M-range value for each CMC topology in view of complying with THD and TDD limits.

A Modified Selective Swapping (MSS) algorithm has been applied by the control system to reduce the instantaneous DC link voltage ripple of H-Bridges by an amount of 33%, and the mean DC link voltage ripple by an amount of 50%, as compared to the Conventional Selective Swapping (CSS) algorithm, thus resulting in perfect balancing of the H-bridge DC link voltages at the expense of higher semiconductor switching losses. The variations in instantaneous peak-to-peak and mean voltages decrease with MSS methods with low values of Δt_s while the effective

switching frequency of power semiconductors increases. Therefore, for practical applications, a compromise should be made between the instantaneous peak-to-peak voltage and the effective switching frequency. Beyond a Δt_s value such as Δt_s=1000μs, no difference exists between CSS and MSS methods for variations in DC link instantaneous peak-to-peak voltages.

In this work, the switching strategy chosen in the application of both CSS and MSS causes voltage spikes with magnitudes ±Vd, ±2Vd, ±3Vd and ±4Vd superimposed on the 11-level line-to-neutral voltage waveform. However, the voltage spikes arising from the application of MSS and CSS methods and superimposed on 11-level line-to-neutral voltage waveforms do not lead to an operational problem for the T-STATCOM and power system because they are successfully suppressed by the total series reactance as can be observed from line-to-neutral voltage waveforms at 154kV PCC. Also, the utilizations of the HV IGBTs used in each HB are not equal due to the use of a simple memoryless control system. However, the switching strategies to eliminate or decrease the duration of the superimposed voltage spikes and to equlize the utilizations of the HV IGBTs are shown to be possible in this work by using more complex control systems.

Moreover, a compromise is made between the turn-on and turn-off behaviors of the HV IGBTs. This is achieved by the followings:
a. Using laminated bus technology, Lstray is reduced to 75nH for each HB;
b. By modifying the standard IGBT driver circuit, turn-on time is prolonged to 2.5μs;
c.Using DC link capacitors with very low equivalent series inductances (Lself=50nH//50nH) and directly mounting them on the laminated bus to minimize the wiring inductance. For the purpose of the decreasing the I_{rr} and hence peak turn-on currents of the HV IGBT modules, the modification is made on the gate drive circuits by increasing the turn-on control resistance, Rg(on) from 2.0 Ω to 3.2 Ω. After modifying gate driver circuit, the turn-on time is found to be 2.5μs for HV IGBT modules. This reduces the reverse recovery current of anti-parallel diodes from

1500A to 1250A and hence decreases the peak turn-on current of IGBT2 from 2500A to 2250 A for the worst case in the transient state of the CMC operation. Therefore, after modification, the diode and IGBT parts of HV IGBT modules can be safely operated since their current and voltage magnitudes remain inside the related SOAs. However, after this modification, the reverse recovery loss, E_{rr} of the diode part decreases by a percentage of 10.11% and the turn-on loss, E_{on} of the IGBT part increases by a percentage of 17.30%.

Furthermore, owing to the application of the Selective Harmonic Elimination Method (SHEM), the 5^{th}, 7^{th}, 11^{th}, and 13^{th} voltage harmonics are successfully minimized. It has been shown by field tests that the total harmonic distortion (THD) of the line-to-neutral voltage waveform at the point of common coupling is as small as 0.9% with respect to the fundamental component. The total demand distortion (TDD) has been measured as 0.77%, in the 154 kV bus.

The transient response of the developed system is also found to be quite satisfactory. The settling time of the T-STATCOM at full-load from inductive mode to capacitive mode transition, and vice versa have been recorded as 80ms and 100ms, respectively in the field, with a transient free transition between modes. The modularity of H-Bridges for easy replacement in the case of a failure, and the mobility and flexibility of the overall T-STATCOM for easy relocation when necessary are being further advantages of the developed system.

Based on these operating principles described in this work, not only qualitative but also quantative design criteria for developing a CMC based T-STATCOM have been given. These are summarized in Table 6.1.

Table 6.1 Effect of main system parameters on cost and performance

System Parameter	Advantage	Disadvantage
Use of CMC instead of the other MC topologies	a. Modularity b. Flexibility c. Less number of components	a. Higher capacitance requirement in Farads b. Not applicable for HVDC back-to-back applications
Use of larger series filter inductance	a. Lower THD and TDD values b. Wider M-range and high resolution in VAr steps	a. High variation range of AC input voltage of CMC b. Higher power losses c. Higher cost d. Higher DC link voltage
Use of larger DC link capacitance value	a. Lower variations in peak-to-peak and mean voltages of DC link capacitor voltages b. Easy to balance DC link capacitor voltages	a. Higher cost b. Slower system transient response
Use of Modified Selective Swapping (MSS) method instead of Conventional Selective Swapping (CSS) method for the equalization of DC link capacitor voltages	a. Perfect balancing of DC link capacitor voltages c. The lower value variations in peak-to-peak and mean voltages of DC link capacitor voltages b. The use of lower capacitance values for DC link capacitors	a. Higher switching frequency b. Higher loss
Increase the number of HBs in series for each phase of CMC for given MVAr and voltage ratings	a. Minimization of THD and TDD values at PCC b. Lower DC link capacitor voltages of HBs c. Use of HV IGBTs with lower voltage ratings	a. The usage of higher number of components b. Lower reliability due to the usage of more components c. The complexity of power stage and control system

Table 6. 2 (Cont'd) Effect of main system parameters on cost and performance

System Parameter	Advantage	Disadvantage
Decrease Δt_s value in MSS method	a. Lower variation in peak-to-peak and mean voltages of DC link capacitor voltages	a. Higher switching frequency
Use of SHEM with off-line calculated switching angles	a. Easier to implement b. Lower switching frequency c. Diminish the low order harmonic components	a. Lower transient response b. Not possible to find optimum angles for some of the CMC topologies
Use of wire-bond HV IGBTs instead of press-pack IGBTs	a. Lower cost b. Availability in market c. Higher dissipation capability	a. Open-circuited when malfunctioned

Further Work

In this research work, CMC based T-STATCOM system is designed for reactive power compensation of balanced loads. A future work can be the modification of the T-STATCOM control system for reactive power compensation of unbalanced loads.

The developed T-STATCOM system can not safely operate during the faults of the power system at which it has been connected. Modifying the T-STATCOM system having Fault Ride Through capability is another interesting further topic for the application.

Implementing the proposed switching strategies in the thesis to eliminate or reduce the duration of the voltage spikes and to equalize the utilizations of the HV IGBTs with more powerfull DSP and FPGA circuits is another issue to be applied for the future.

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APPENDIX-A

SHEM EQUATIONS FOR 11-LEVEL CMC

The line-to-neutral waveform for 11-level CMC shown in Figure 2.7 of Chapter-2 can be expressed by:

$$f(t) = F_0 + \sum_{n=1}^{\infty}(a_n \cos(\text{hwt}) + b_n \sin(\text{hwt})) \quad \text{(A1.1)}$$

Since the output voltage is odd-quarter wave;

$$a_h = 0 \quad \text{(A1.2)}$$

and

$$b_h = \begin{cases} \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(\theta)\sin(h\theta)\ d\theta & for\ h = 1,3,5\ldots \\ 0\ for\ h = 2,4,6,\ldots \end{cases} \quad \text{(A1.3)}$$

Assuming DC link capacitor voltages are all balanced and equal to V_d;

$$b_h = \frac{4V_d}{\pi}[\cos(h\theta_1) + \cos(h\theta_2) + \cdots + \cos(h\theta_n)] \quad \text{(A1.4)}$$

The fundamental component is below as shown in (A1.5).

$$b_1 = \frac{4V_d}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_n)] \quad \text{(A1.5)}$$

To eliminate low order harmonics of 5th, 7th, 11th and 13th in the phase-to-neutral voltages of CMC by the switching angles of θ_1, θ_2,...., θ_5, the following equations are to be used:

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = M \quad \text{(A1.6)}$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \quad \text{(A1.7)}$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \quad \text{(A1.8)}$$

$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \quad \text{(A1.9)}$$

$$\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0 \quad \text{(A1.10)}$$

APPENDIX-B

PERMISSIBLE REGIONS FOR THD AND TDD RECOMMENDED BY IEEE STD.519-1992

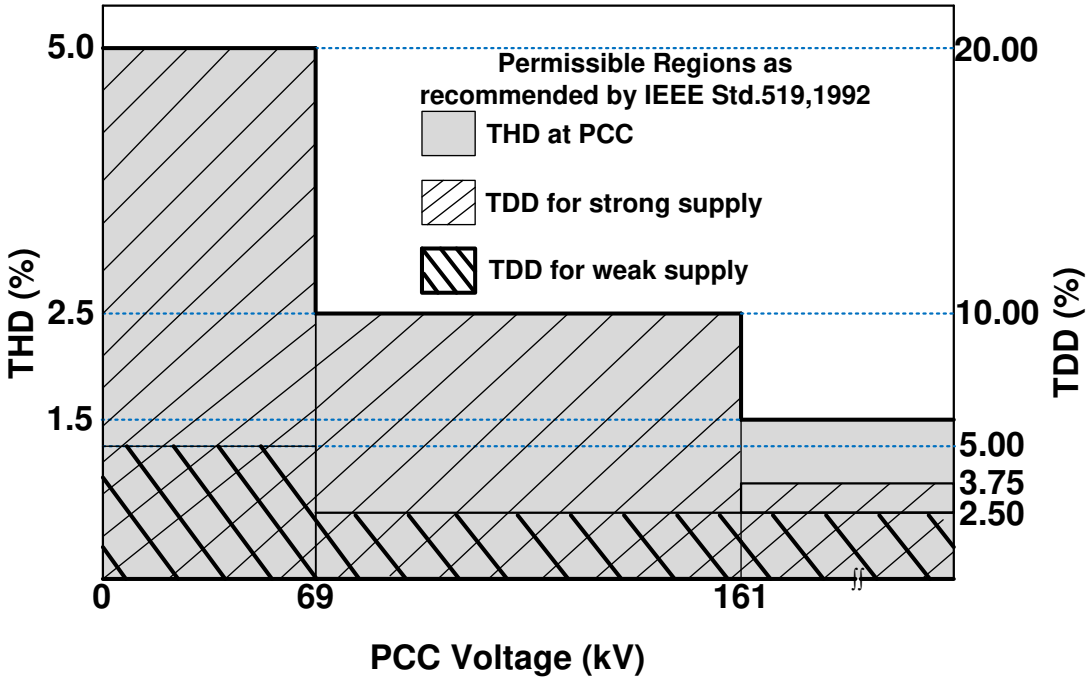

Figure B.1 Permissible regions for total harmonic distortion (THD) and total demand distortion (TDD) as a function of rated voltage at point of common coupling (PCC) as recommended by IEEE Std.519, 1992.

APPENDIX-C

RATINGS OF COMMERCIALLY AVAILABLE HV IGBTs

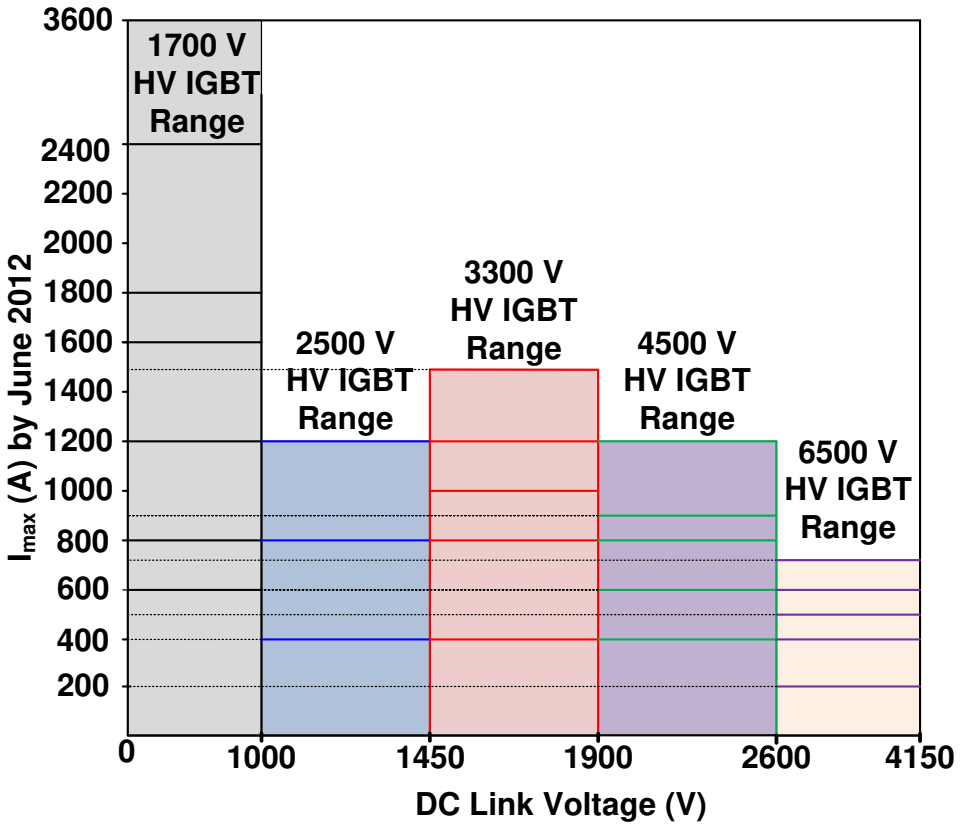

Figure C.1 Collector current and collector-emitter voltage ratings of commercially available High Voltage Insulated Gate Bipolar Transistors (HV IGBTs) by June 2012 with respect to DC link voltages of HB

APPENDIX-D

SOAs OF MITSUBISHI CM1200HC-66H HV IGBT MODULE

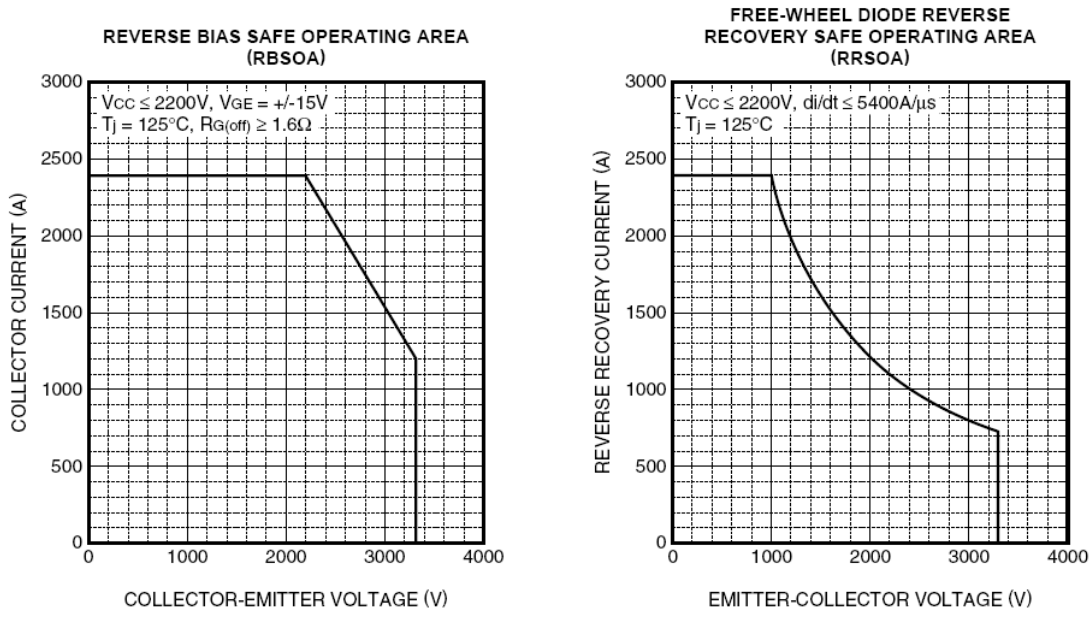

Figure D.1 Safe Operating Areas (SOA) of HV IGBT modules specified in datasheet of MITSUBISHI CM1200HC-66H

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FOREIGN LANGUAGES

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PUBLICATIONS

1. B. Gultekin, C.O. Gercek, etal, "Design and Implementation of a 154-kV, ±50-Mvar Transmission STATCOM Based on 21-Level Cascaded Multilevel Converter", *IEEE Trans. Ind. Appl.,* vol. 48 , no. 3, pp. 1030 – 1045, May/June 2012.
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