Cascaded Multilevel Inverter With Regeneration Capability and Reduced Number of Switches

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***Abstract*—Multilevel converters are a very interesting alternative for medium and high power drives. One of the more flexible topologies of this type is the cascaded multicell converter. This paper proposes the use of a single-phase reduced cell suitable for cascaded multilevel converters. This cell uses a reduced single-phase active rectifier at the input and an H-bridge inverter at the output side. This topology presents a very good performance, effectively controlling the waveform of the input current and of the output voltage and allowing operation in the motoring and regenerative mode. The results presented in this paper confirm that this medium voltage inverter effectively eliminates low frequency input current harmonics at the primary side of the transformer and operates without problems in regenerative mode.**

***Index Terms*—Multilevel systems, pulsewidth modulated power converters, regeneration capability.**

I. Introduction

In THE LAST few years, the necessity of increasing the power level in industry has sustained the continuous development of multilevel converters due to their capability of handling voltages up to 6.9 kV and power of several megawatts [1]–[3]. Among different topologies [4], the cascaded multicell [5], [6] inverter has received much attention.

The original converter proposed in [5] and [6] uses cells with diode rectifiers that does not allow a transfer of power from the load to the power supply (regeneration). Several loads such as laminators and downhill conveyors demand regeneration capability on the converter. This fact has motivated several researchers to seek alternatives of cascaded topologies with regeneration capability, which can be done by replacing the diode bridge with a pulsewidth modulation (PWM) active rectifier at the input side [7], obtaining single- and three-phase regenerative cells [8], [9].

The first part of this paper presents a general multicell converter and a review of different regenerative cells with their corresponding advantages and drawbacks, considering the number of switches, control issues and their overall performance. In Section III a new cell based on a half bridge single-phase rectifier [10], [11] and a three-level single-phase inverter (H-bridge) is presented. The standard control scheme [12], [13] is improved to guarantee a very high input power factor at the primary of the transformer and to prevent voltage imbalance on the capacitors of each cell. A multicell converter using the proposed regenerative cell is presented in Section IV and a special interconnection among the input transformers is used to ensure the cancellation of low order current harmonics.

Results for a seven-level converter using the proposed cell are included in Section V, showing good quality output signals while working with a very high input power factor in rectifying and regenerative mode.

Manuscript received December 18, 2006; revised November 23, 2007. This work was supported in part by the Chilean Research Fund (Fondecyt) through Grant 1060427, by the postgraduate program given by Fundación Andes under Grant C-14055, and by the Universidad Técnica Federico Santa María and the Millennium Nucleus on Industrial Electronics and Mechatronics P04048-F (MIDEPLAN).

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Digital Object Identifier 10.1109/TIE.2008.917095

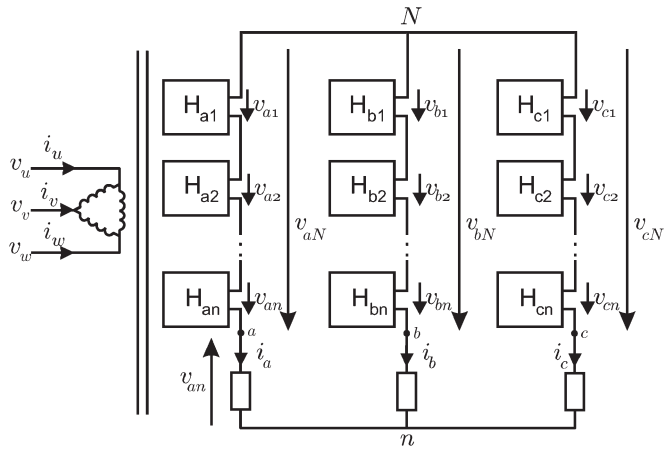

Fig. 1. Control scheme of the proposed cell.

II. Cascade Multicell Converter

The cascade multicell converter was introduced in the early 1990s in [5] and [6]; this topology is based in the series connection of units known as cells for each output phase, as shown in Fig. 1.

Each cell is a structure based on a rectifier fed by an isolated voltage source, a capacitive dc-link and an inverter structure. The series connection of the inverters of the cells produces a multilevel voltage (v_{xN} $x = a, b, c$), which corresponds to the addition of the output voltage of each cell

$$v_{xN} = \sum_{y=1}^{n} v_{xy}, \qquad x = a, b, c. \tag{1}$$

The cell structure proposed in [6] is based on a three-phase diode bridge, one dc-link capacitor and a single-phase

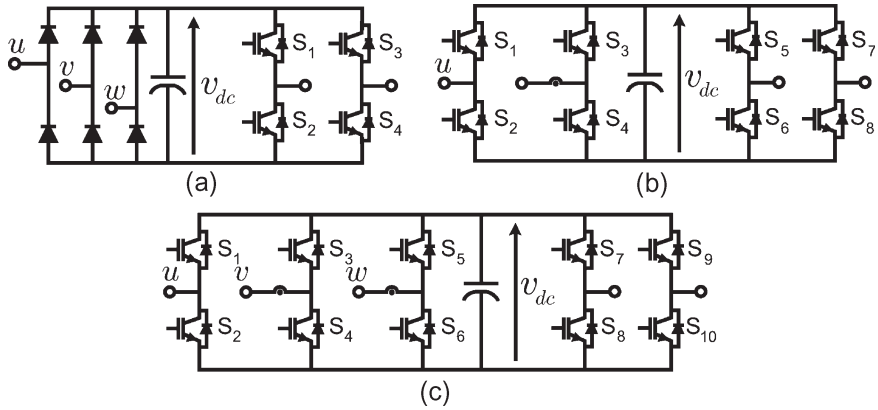

Fig. 2. Cell topologies: (a) Non-Regenerative; Regenerative with: (b) Single-phase PWM Rectifier; (c) three-phase PWM Rectifier.

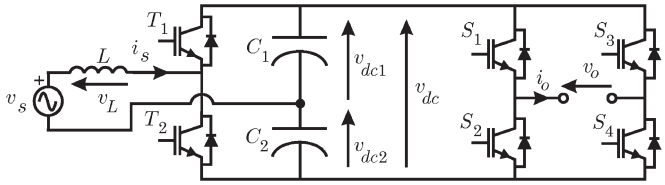

Fig. 3. Power circuit of the proposed cell.

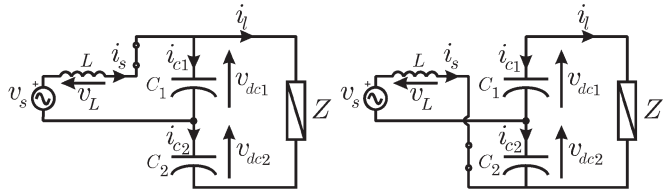

Fig. 4. Rectifier behavior when: (a) $T_1 = 1$; (b) $T_2 = 1$.

three-level inverter (or H-bridge) as shown in Fig. 2(a). This topology needs a complex input transformer to reduce low order harmonics and, due to the diode bridge, cannot reverse the power flux from the load to the supply.

In [8] the authors propose the use of PWM rectifiers as the front-end of the cells for applications that require regeneration capability, and a single-phase PWM-rectifier similar to that shown in Fig. 2(b) is used. This cell, known as an H-H cell, requires a simpler transformer than the one shown in Fig. 2(a) and can reach a very high power factor at the input with a proper input transformer connection. The main drawback of this cell is that the dc-link presents ripple at double the input voltage frequency $(2f_{\rm s})$. Since rotating coordinates also cannot be directly applied to control the input current [14], [15], it must be controlled in the stationary frame, where the reference for the control loop is in essence sinusoidal. Under this condition proportional–integrative (PI) controllers are not recommended since they do not have zero-steady state error [16], [17].

The cell presented in [9] uses a three-phase PWM rectifier as shown in Fig. 2(c) and requires ten semiconductors, an extra current sensor and a more complex transformer. However, it does not present pulsating power at double the input frequency, allowing a reduction in the size of the dc-link capacitor. Another important advantage is that the currents can be controlled in dq rotating frame.

III. Proposed Cell

A. Topology Description

The proposed cell, which is shown in Fig. 3, only requires two power semiconductors for the rectification stage and four for the classic H-bridge. Thus, the complete cell can be implemented in a standard six-pack inverter module.

Because the input rectifier topology naturally doubles the dc-link output voltage for a dc-link voltage of $v_{\rm dc}$, the input voltage source value must be lower than $v_{\rm dc}/2$ for a proper operation of the rectifier. If the proposed cell is compared with an H-H cell [8] with the same total dc-link voltage, the input current $i_{\rm s}$ must be doubled to maintain the same cell power rating. For this reason the insulated gate bipolar transistors (IGBTs) on the rectifier side must be rated at the same voltage $(v_{\rm dc})$, but at double the current that the IGBTs require for an H-bridge rectifier, while the IGBTs of the H-bridge inverter in both cells are exactly the same.

The dc-link has been separated in two dc-link capacitors, each working at $V_{\rm dc}/2$. However, as the capacitors are connected in series, their capacitance must be doubled if they are compared with the capacitance of a traditional H-H cell [8] to maintain the capacitance seen by the output H-bridge.

1) Rectifier Operation: From Fig. 3 it is easy to see that T_1 and T_2 must work in complementary mode, otherwise the dc-link would be short-circuited or the input inductance L would be open-circuited. Thus, only two conduction possibilities are allowed for the rectifier: $T_1 = 1$, $T_2 = 0$ or $T_1 = 0$, $T_2 = 1$. Both conduction states are shown in Fig. 4(a) and (b), respectively, where the Z impedance represents the effect of the H-bridge inverter.

Note that for a correct operation it is assumed that the dc-link voltage on each capacitor is always greater than the input voltage $v_{\rm s}$. Under this assumption the following expression can be obtained.

1) $T_1 = 1$: From Fig. 4(a) it can be seen that

$$v_{\rm L} = L\frac{di_{\rm s}}{dt} = v_{\rm s} - v_{\rm dc1}. \tag{2}$$

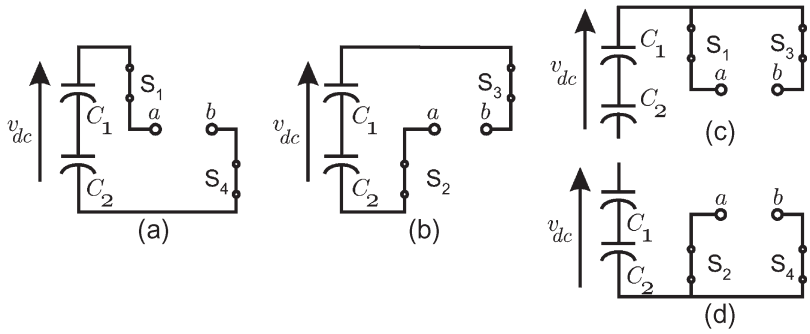

Fig. 5. H-bridge inverter output voltage: (a) $v_{\rm ab} = v_{\rm dc}$; (b) $v_{\rm ab} = -v_{\rm dc}$; (c) and (d) $v_{\rm ab} = 0$.

As $v_{\rm dc1} > v_{\rm s}$, (2) implies that $v_{\rm L}$ is always negative, so $i_{\rm s}$ decreases its value. Hence, the capacitor currents are

$$i_{\rm c1} = i_{\rm s} - i_{\rm l} \tag{3}$$

$$i_{\rm c2} = -i_{\rm l} \tag{4}$$

$$v_{\rm dc1} = \frac{1}{C_1}\int i_{\rm c1}(\tau)\, d\tau \tag{5}$$

$$v_{\rm dc2} = \frac{1}{C_2}\int i_{\rm c2}(\tau)\, d\tau \tag{6}$$

if $i_{\rm s} > 0$, C_1 can (depending on the value of $i_{\rm l}$) be charged by the mains, otherwise if $i_{\rm s} < 0$, the voltage in C_1 will decrease its value. The voltage in C_2 will depend exclusively on the load condition.

2) $T_1 = 0$: As seen in Fig. 4(b), (2) changes to

$$v_{\rm L} = L\frac{di_{\rm s}}{dt} = v_{\rm s} + v_{\rm dc2} \tag{7}$$

due to $v_{\rm dc2} > v_{\rm s}$, $v_{\rm L} > 0$ so $i_{\rm s}$ increases its value.

Under this condition, (3) and (4) change to

$$i_{\rm c1} = -i_{\rm l} \tag{8}$$

$$i_{\rm c2} = -i_{\rm s} - i_{\rm l}. \tag{9}$$

If $i_{\rm s} > 0$ the capacitor C_2 will be discharged, otherwise if $i_{\rm s} < 0$, the voltage in C_2 can increase its value. As in the previous section, the voltage in C_1 depends on the load condition.

The control scheme must adjust the duty cycle to keep the voltages $v_{\rm dc1}$ and $v_{\rm dc2}$ at their reference values.

2) Inverter Unit: Fig. 5 shows the four conduction states for an H-bridge inverter. Note that this topology generates up to three different output voltage levels based on the full dc-link voltage $v_{\rm dc} = v_{\rm dc1} + v_{\rm dc2}$, disregarding the rectifier topology.

B. Control Scheme

The control scheme for the rectifier side of this semireduced cell is shown in Fig. 6. This scheme uses a voltage controller $C_{\rm v}$ to control the entire dc-link voltage $v_{\rm dc}$ and a current controller $C_{\rm c}$ that enables a high input power factor. Typically $C_{\rm v}$ and $C_{\rm c}$ have been chosen as simple PI controllers. However, in this case a linear resonant controller at mains frequency $\omega_{\rm s} = 2\pi f_{\rm s}$

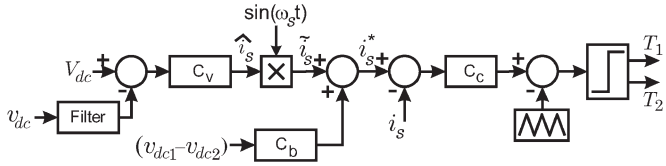

Fig. 6. Control scheme of the proposed cell.

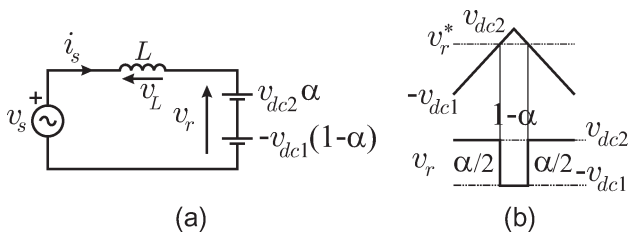

Fig. 7. Average model of the PWM rectifier: (a) Circuit; (b) PWM modulator.

is used for $C_{\rm c}$ to provide perfect phase tracking on the current loop at that frequency [16], [17].

In this way $C_{\rm v}$ and $C_{\rm c}$ structures are

$$C_{\rm v} = K_{\rm v}\frac{s + \alpha_{\rm v}}{s} \tag{10}$$

$$C_{\rm c} = K_{\rm c}\frac{s^2 + \alpha_{\rm c}s + \beta_{\rm c}}{s^2 - \omega_{\rm s}^2} \tag{11}$$

where $K_{\rm v}$, $\alpha_{\rm v}$, $K_{\rm c}$, $\alpha_{\rm c}$, and $\beta_{\rm c}$ are calculated depending on the desired bandwidth, overshoot and settling time.

Working with a sinusoidal input current of frequency $f_{\rm s}$ in phase with the input voltage has consequences in the dc-link capacitors voltages. A simple way to understand these effects is to use the average rectifier model proposed in [18] and shown in Fig. 7, and assume that the voltages are balanced. The following relations then hold, according to Fig. 7(b)

$$\alpha = \frac{1}{2} + \frac{v_{\rm r}^*}{V_{\rm dc}} \tag{12}$$

$$1 - \alpha = \frac{1}{2} - \frac{v_{\rm r}^*}{V_{\rm dc}}. \tag{13}$$

If the rectifier is working with unitary power factor, $v_{\rm r}^*$ must be a sinusoidal signal of frequency $f_{\rm s}$, and a magnitude and phase ($\hat{v}_{\rm r}$ and ϕ, respectively) depending on the load power

rating and the input impedance, so the instantaneous power on each capacitor are

$$\begin{aligned} p_{\mathrm{c1}} &= -v_{\mathrm{dc1}}(1-\alpha)i_{\mathrm{s}} \\ &= -v_{\mathrm{dc1}}\left(\frac{1}{2}-\frac{\hat{v}_{\mathrm{r}}^{*}\sin(\omega_{\mathrm{s}}t-\phi)}{V_{\mathrm{dc}}}\right)\left(\hat{i}_{\mathrm{s}}\sin(\omega_{\mathrm{s}}t)\right) \\ &= v_{\mathrm{dc1}}\left(\frac{\hat{v}_{\mathrm{r}}^{*}\hat{i}_{\mathrm{s}}}{2V_{\mathrm{dc}}}\left[\cos(\phi)-\cos(2\omega_{\mathrm{s}}t-\phi)\right]-\frac{\hat{i}_{\mathrm{s}}\sin(\omega_{\mathrm{s}}t)}{2}\right) \end{aligned} \tag{14}$$

$$\begin{aligned} p_{\mathrm{c2}} &= v_{\mathrm{dc2}}\alpha i_{\mathrm{s}} \\ &= v_{\mathrm{dc2}}\left(\frac{\hat{v}_{\mathrm{r}}^{*}\hat{i}_{\mathrm{s}}}{2V_{\mathrm{dc}}}\left[\cos(\phi)-\cos(2\omega_{\mathrm{s}}t-\phi)\right]+\frac{\hat{i}_{\mathrm{s}}\sin(\omega_{\mathrm{s}}t)}{2}\right). \end{aligned} \tag{15}$$

Since the main voltage harmonics are the same compared to the power harmonics in a capacitor, v_{c1} and v_{c2} have the same harmonics than p_{c1} and p_{c2}, respectively, then the entire dc-link voltage $v_{\mathrm{dc}} = v_{\mathrm{c1}} + v_{\mathrm{c2}}$ presents a ripple component at $2\omega_{\mathrm{s}}$ but not at ω_{s}. Since this ripple is a consequence of working with a high power factor, it cannot be compensated and must thus be ignored by the voltage controller. For this reason a band-stop filter at $2\omega_{\mathrm{s}}$ in the v_{dc} measurement is included.

Some research studies [12], [13], [19], have discussed a voltage imbalance phenomenon between both capacitors due to offsets on the control signals, initial conditions and asymmetry between both capacitances (typical tolerance is about 20%). These studies are focused on a rectifier side identical to the one proposed in this paper, but with a rather different inverter topology. In those works the problem is solved by introducing a dc offset in the current reference for the current loop, which allows movement of the dc-link neutral point to balance the capacitors voltage. As stated on the current literature, a simple proportional (P) controller should be enough to compensate the imbalance. However, according to (14) and (15), it can be noticed that strong components at f_{s} (in hertz) are present in v_{dc1} and v_{dc2}. Moreover, as the feedback control signal used is $\Delta v = v_{\mathrm{dc1}} - v_{\mathrm{dc2}}$, and the components at f_{s} (in hertz) in the capacitors are shifted in 180°, an amplified f_{s} (in hertz) component is present on the imbalance control path.

This component propagates through the P controller and will add spurious phase and magnitude components to $\tilde{i}_{\mathrm{s}}(t)$. Thus, the current loop will track $i_{\mathrm{s}}^{*}(t)$ instead of $\tilde{i}_{\mathrm{s}}(t)$, leading to an undesirable shifted phase input current that degrades the input power factor.

A simple solution to this issue is achieved by introducing a notch filter on the Δv measurement. The notch filter should provide a considerable attenuation at f_{s} (in hertz) to carry the input power factor near unity. Another well-known drawback of P controllers is that they cannot warrant zero steady-state error, even if the plant includes an integrator [20]; a PI controller for C_{b} is recommended. Note that if a low cutoff frequency PI controller is used, the notch filter can be omitted. Comparison results using the traditional P controller method and the new proposed notch-PI controller are shown in Fig. 8, demonstrating the effectiveness of the proposed scheme.

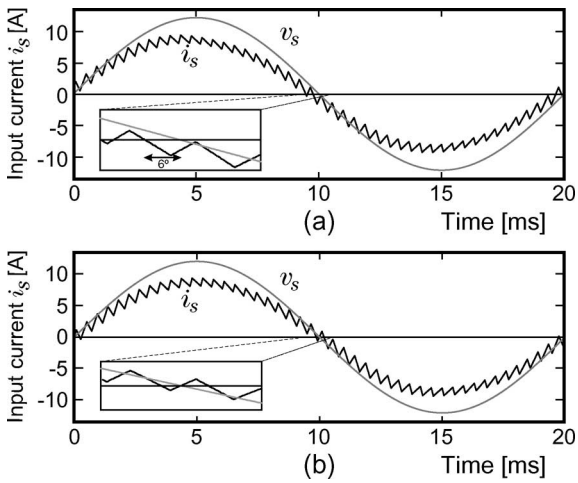

Fig. 8. Input current and grid voltage with: (a) P unbalance controller, (b) notch-PI unbalance controller.

IV. Multicell Converter With the Proposed Cell

Fig. 9 shows a seven-level multicell converter using the proposed cell.

Several input currents on each cell are present due to the H-bridge operation. This phenomenon is similar to the one described for an H-H cell in [21]. To obtain a proper cancellation of these harmonics components on the primary side of the transformer, the interconnection proposed in [21] is used.

According to Fig. 9 the following relationships holds for the secondary voltages:

$$v_{\mathrm{s1}} = v_{\mathrm{s4}} = v_{\mathrm{s7}} = k\sqrt{3}\hat{v}_{\mathrm{p}}\sin\left(2\pi f_{\mathrm{s}}t-\frac{\pi}{6}\right) \tag{16}$$

$$v_{\mathrm{s2}} = v_{\mathrm{s5}} = v_{\mathrm{s8}} = k\sqrt{3}\hat{v}_{\mathrm{p}}\sin\left(2\pi f_{\mathrm{s}}t-\frac{\pi}{6}+\frac{2\pi}{3}\right) \tag{17}$$

$$v_{\mathrm{s3}} = v_{\mathrm{s6}} = v_{\mathrm{s9}} = k\sqrt{3}\hat{v}_{\mathrm{p}}\sin\left(2\pi f_{\mathrm{s}}t-\frac{\pi}{6}-\frac{2\pi}{3}\right) \tag{18}$$

and for the primary currents

$$i_{\mathrm{u}} = \frac{1}{k}\left[(i_{\mathrm{s1}}+i_{\mathrm{s4}}+i_{\mathrm{s7}})-(i_{\mathrm{s3}}+i_{\mathrm{s6}}+i_{\mathrm{s9}})\right] \tag{19}$$

$$i_{\mathrm{v}} = \frac{1}{k}\left[(i_{\mathrm{s2}}+i_{\mathrm{s5}}+i_{\mathrm{s8}})-(i_{\mathrm{s1}}+i_{\mathrm{s4}}+i_{\mathrm{s7}})\right] \tag{20}$$

$$i_{\mathrm{w}} = \frac{1}{k}\left[(i_{\mathrm{s3}}+i_{\mathrm{s6}}+i_{\mathrm{s9}})-(i_{\mathrm{s2}}+i_{\mathrm{s5}}+i_{\mathrm{s8}})\right] \tag{21}$$

where k represents the turns ratio of the input transformer. For simplicity in this paper it is assumed that $k = 1$.

On the output side, assuming stationary states, the output voltages and currents are

$$v_{\mathrm{a}}(t) = \hat{i}\sin(\omega_{\mathrm{o}}t), \qquad i_{\mathrm{a}}(t) = \hat{i}\sin(\omega_{\mathrm{o}}t-\phi_{\mathrm{o}}) \tag{22}$$

$$v_{\mathrm{b}}(t) = \hat{i}\sin\left(\omega_{\mathrm{o}}t+120^{\circ}\right), \quad i_{\mathrm{b}}(t) = \hat{i}\sin\left(\omega_{\mathrm{o}}t-\phi_{\mathrm{o}}+120^{\circ}\right) \tag{23}$$

$$v_{\mathrm{c}}(t) = \hat{i}\sin\left(\omega_{\mathrm{o}}t-120^{\circ}\right), \quad i_{\mathrm{c}}(t) = \hat{i}\sin\left(\omega_{\mathrm{o}}t-\phi_{\mathrm{o}}-120^{\circ}\right) \tag{24}$$

where $\hat{i}$ and ϕ_{o} will depend on the output impedance.

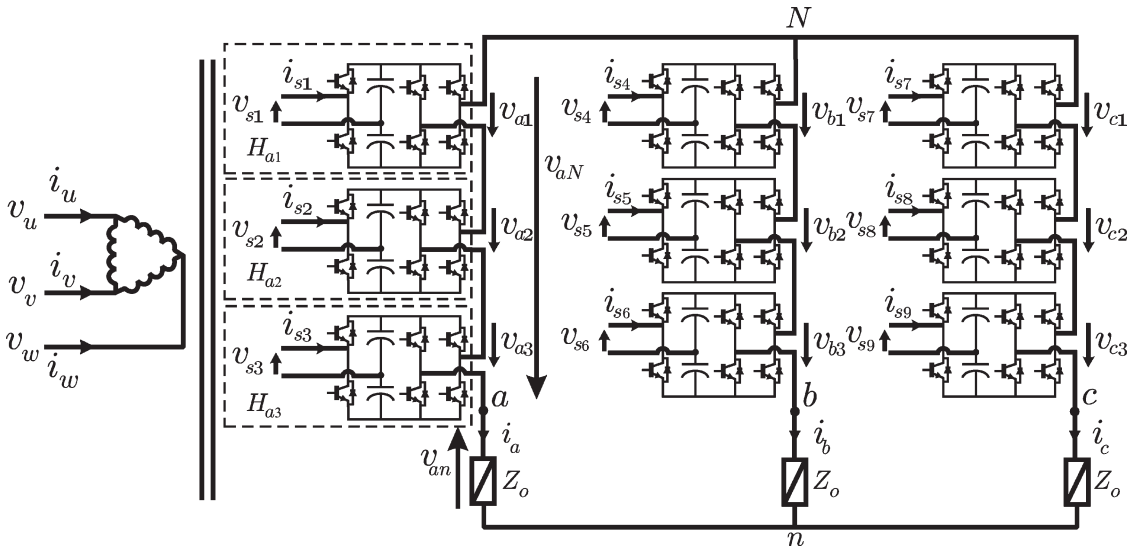

Fig. 9. Seven-level multicell converter with the proposed cell.

Under these conditions the output power of each cell can be calculated, e.g., for cell H_{a1}

$$p_{\mathrm{a1}}(t) = v_{\mathrm{a1}}(t) i_{\mathrm{a}}(t) = \frac{\hat{v}_{\mathrm{a1}} \hat{i}(t)}{2} \left[\cos(\phi_{\mathrm{o}}) - \cos(2\omega_{\mathrm{o}} t - \phi_{\mathrm{o}})\right]. \quad (25)$$

As cell H_{a1} is connected in series with cells H_{a2} and H_{a3}, the output current of these three cells are exactly the same. If a phase-shifted PWM modulation is then assumed, the fundamental output voltage and hence the instantaneous output power of these cells are the same.

Following the same procedure, the instantaneous output power for cells H_{b1}, H_{b2}, and H_{b3} is:

$$p_{\mathrm{b}x}(t) = v_{\mathrm{b}x}(t) i_{\mathrm{b}}(t) \qquad x = 1, 2, 3 = \frac{\hat{v}_{\mathrm{b}x} \hat{i}}{2} \left[\cos(\phi_{\mathrm{o}}) - \cos(2\omega_{\mathrm{o}} t - \phi_{\mathrm{o}} - 120^{\circ})\right] \quad (26)$$

and for cells H_{c1}, H_{c2} and H_{c3} is

$$p_{\mathrm{c}x}(t) = v_{\mathrm{c}x}(t) i_{\mathrm{c}}(t), \qquad x = 1, 2, 3 = \frac{\hat{v}_{\mathrm{c}x}\, \hat{i}}{2} \left[\cos(\phi_{\mathrm{o}}) - \cos(2\omega_{\mathrm{o}} t - \phi_{\mathrm{o}} + 120^{\circ})\right]. \quad (27)$$

Then the low frequency voltage ripple in the capacitors of cells H_{a1}, H_{b1}, and H_{c1}, due to the output currents, are phase shifted in 120°. As the voltage controllers will try to keep the capacitors voltage at V_{dc}, they will introduce harmonics in the input currents. These harmonics on the different cells will be phase-shifted in 120° as well. The same analysis can be done for $H_{\mathrm{a2}} - H_{\mathrm{b2}} - H_{\mathrm{c2}}$ and $H_{\mathrm{a3}} - H_{\mathrm{b3}} - H_{\mathrm{c3}}$, obtaining input current harmonics phase-shifted in 120° between the cells; by using the relationships (19)–(21) they are canceled in the input transformer, leading to an almost unitary input power factor. Although this harmonic cancellation is effective at any frequency, operation at very low frequencies can saturate the input transformer, affecting the process.

TABLE I
NET AND LOAD PARAMETERS

Param.	*Value*
Input resistance*	0.8[Ω]
Input inductance*	5.8[mH]
Input frequency	50 [Hz]
Primary voltage ($\hat{v}_p$)	190[V]
Transformer ratio (k)	19:4 (prim:sec)
Load resistance	80[Ω]
Load inductance	10[mH]

* seen from secondary side.

Note that as stated in [21], this cancellation process is only possible if the number of cells per phase is a multiple of three.

V. RESULTS

For the experimental results, the cells were built using IPM20CSJ060 six-pack modules and two dc-link capacitors of 3 mF. The control scheme was implemented in a digital platform based on a TMS320C6711 DSP, which resolves the control loops and the phase-locked loop (PLL) used for a correct synchronization with the net and a XC2S150 FPGA, from Xilinx, which manages the 29 A/D conversions and modulates the actuations calculated by the DSP. The calculation time for one control loop, including the A/D conversion, filters and PLL algorithm, was only 9 μs, so a PWM carrier of 2.9 kHz was used.

The net and load parameters are detailed in Table I.

The pulsating power generated by the output H-bridges increases its importance while the output frequency decreases. This can be seen in the simulated and experimental results of Figs. 10 and 11, respectively, where the converter is operated at $f_{\mathrm{o}} = 5$ Hz. The seven-level output voltages can be clearly identified, a low frequency distortion can be noted [Figs. 10(a) and 11(a)], and high quality output currents are still obtained [Figs. 10(b) and 11(b)]. The effect of the low output frequency is clear in the dc-link voltages of the cells as seen in Fig. 11(c),

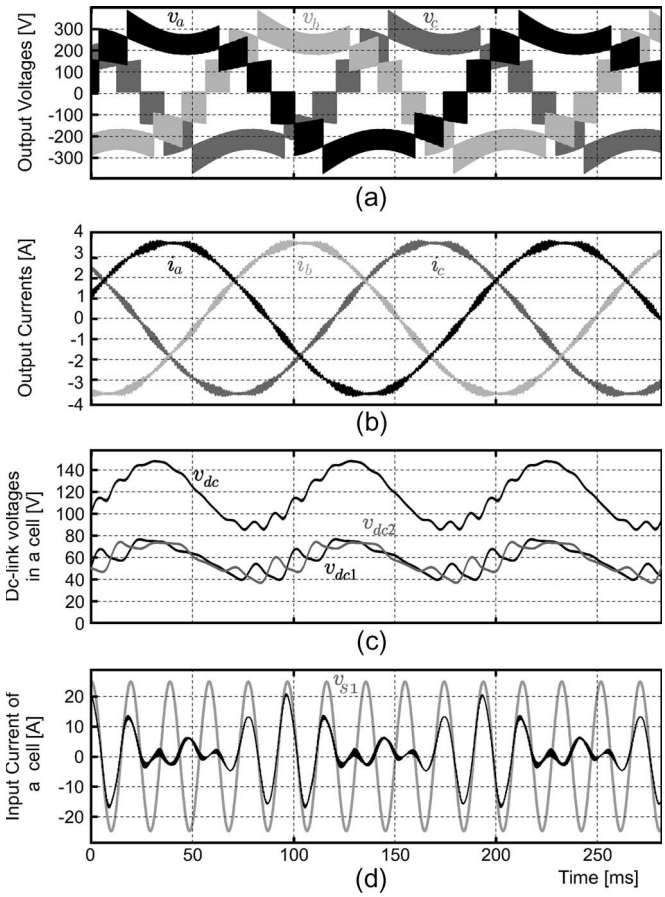

Fig. 10. Simulation results working with $f_{\rm o} = 5$ Hz: (a) Output voltages; (b) output currents; (c) total dc-link voltage $v_{\rm dc}$ and capacitors voltage $v_{\rm dc1}$ and $v_{\rm dc2}$; (d) input voltage and current of one cell.

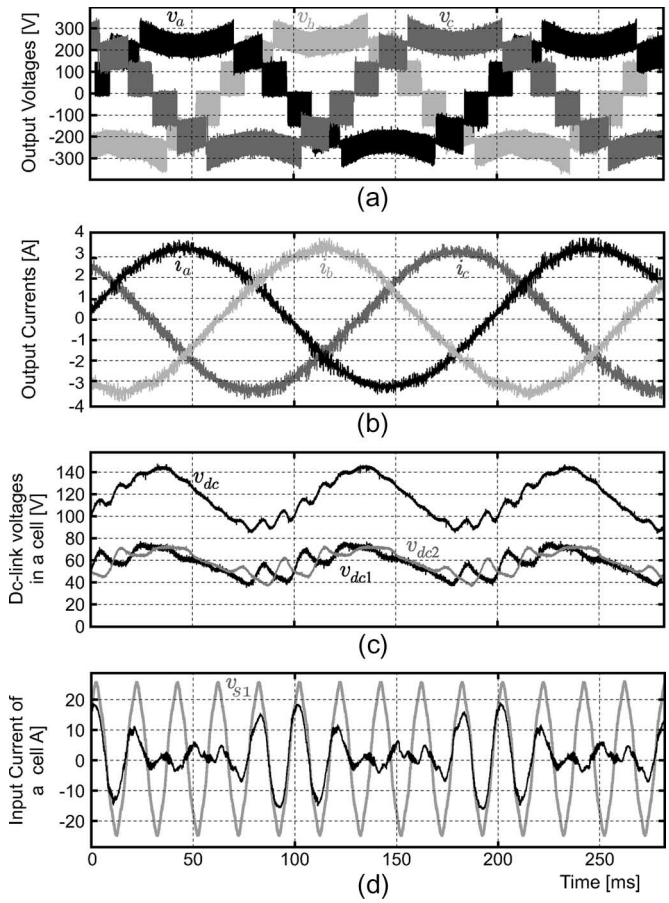

Fig. 11. Experimental results working with $f_{\rm o} = 5$ Hz: (a) Output voltages; (b) output currents; (c) total dc-link voltage $v_{\rm dc}$ and capacitors voltage $v_{\rm dc1}$ and $v_{\rm dc2}$; (d) input voltage and current of one cell.

by the presence of a low frequency $(2f_{\rm o})$ high amplitude harmonic component in the ripple. The input currents of the cell appear highly modulated due to the dc-link voltage ripple trying to compensate it, an effect shown in Figs. 10(d) and 11(d) Note however that the current keeps in phase with the input secondary voltage, even in those moments when the inverter operates in regenerative mode (i.e., at $t = 50$ [ms]) leading the dc-link voltage to its reference value. Also, note the presence of low order harmonics in the input voltage of the cells, which appear as additional perturbations to the inner current control loop.

Fig. 12(a)–(c) shows the input currents of cells $H_{\rm a1} - H_{\rm b1} - H_{\rm c1}$. It can be seen how the low order harmonics are phase-shifted in 120°, so by using the relationships (19)–(21), these harmonics can be dramatically reduced or even eliminated, as shown in Fig. 12(d).

This can be seen in a clearer way in Fig. 13, where the spectra of the input current at the secondary and primary are shown. Note that the cancellation is not perfect mainly due to two factors: tolerance of the capacitors on each cell and saturation and nonlinearities of the input transformer.

Fig. 14 shows the effect of the imbalance control in the behavior of the dc-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$. Note that if the imbalance control is off, the difference between the voltage in both capacitors reaches up to 40 V, which can lead to a

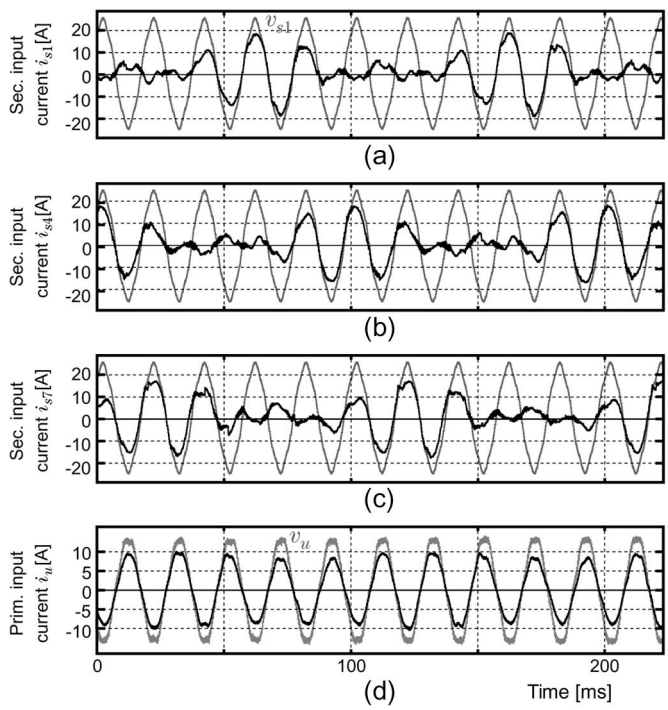

Fig. 12. Input currents: (a), (b), and (c) of cells with input voltages in phase; (d) at primary side.

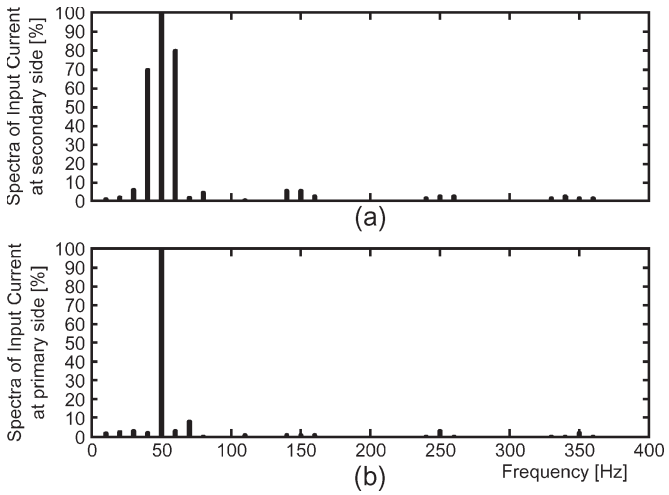

Fig. 13. Input current spectra: (a) At secondary side; (b) at primary side.

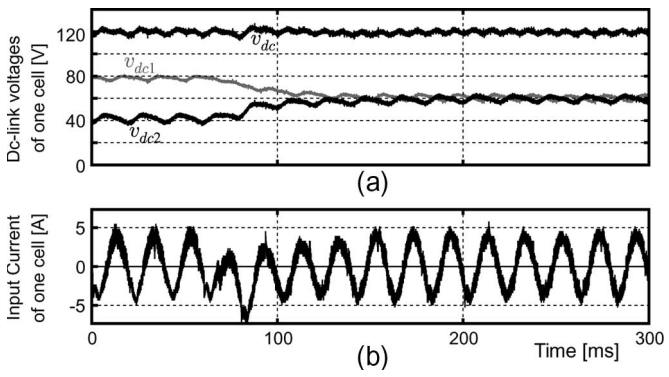

Fig. 14. Unbalance control at $f_{\rm o}$ 50 Hz when turned on: (a) Voltages of one cell; (b) input current of one cell.

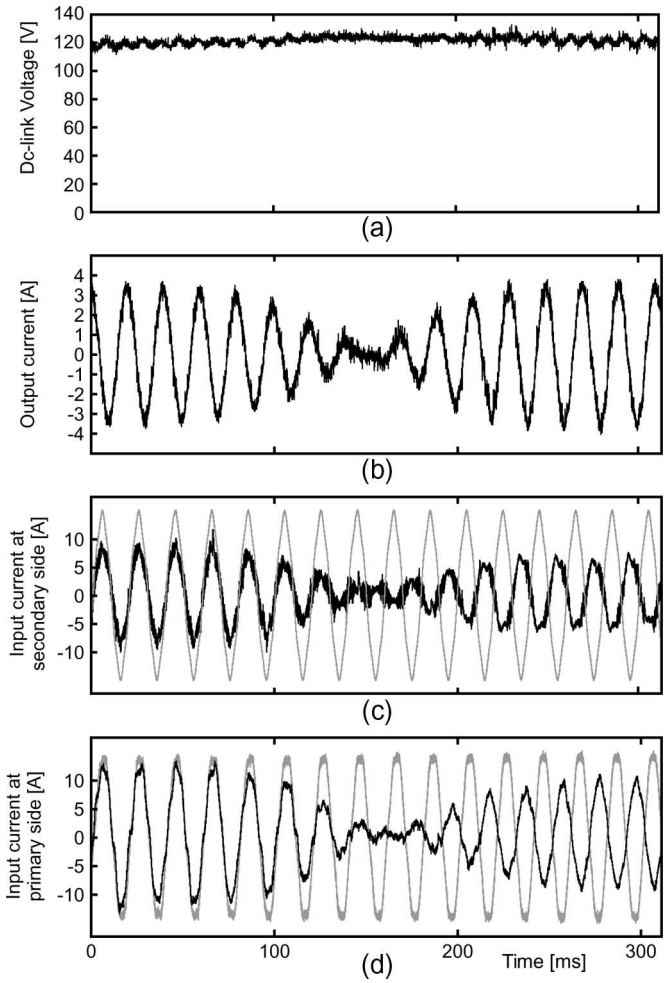

Fig. 15. Regeneration at $f_{\rm o} = 50$ Hz: (a) dc-link voltage in one cell; (b) output current; (c) input current and voltage at secondary side; (d) input voltage and current at primary side.

loss of control capability of the input current. This imbalance is quickly corrected when the imbalance controller is turned on. Note however that the entire dc-link voltage $v_{\rm dc}$ remains controlled at any time by the main voltage control loop.

Fig. 15 presents the transition from motoring to generating operation. From $t = 0$ to $t = 80$ ms the input current is sinusoidal and in phase with the ac voltage (Fig. 15(c) and (d), indicating that power is transferred from the three-phase power supply to the load. Starting at $t = 80$ [ms], an active load changes the polarity of the output current [Fig. 15(b)] and increases the dc-link voltage of the cell [Fig. 15(a)]. This forces the input current to change its polarity as well (180° out of phase with respect to the voltage, indicating a regeneration operation.

VI. Conclusion

The cell introduced in this paper has a reduced number of power switches at the cost of increasing the number of dc-link capacitors, but each one working with half of the voltage of the H-H cell. Also, note that losses in both converters are very similar, while the input current in the semireduced cell is twice that in the H-H cell, which has half the number of semiconductors.

An additional advantage is that a standard industrial six-semiconductor module, used for any conventional two-level inverter, can be used to build the entire cell.

In addition, the control strategy for the rectifier stage keeps the balance in the voltage of the dc-link capacitors without phase-shift between the input voltage and the fundamental frequency of the input current of each cell. The low frequency input current harmonics of each cell can be effectively eliminated at the primary side of the input transformer through a proper interconnection.

The authors believe that the proposed cell is a good compromise between cost and performance, allowing operation on any condition at a high input power factor.

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