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# Catalysis-Free Growth of III-V Core-Shell Nanowires on *p*-Si for Efficient Heterojunction Solar Cells with Optimized Window Layer

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**Abstract:** The growth of high-quality compound semiconductor materials on silicon substrates has long been studied to overcome the high price of compound semiconductor substrates. In this study, we successfully fabricated nanowire solar cells by utilizing high-quality hetero p-n junctions formed by growing n-type III-V nanowires on p-silicon substrates. The n-$InAs_{0.75}P_{0.25}$ nanowire array was grown by the Volmer–Weber mechanism, a three-dimensional island growth mode arising from a lattice mismatch between III-V and silicon. For the surface passivation of n-$InAs_{0.75}P_{0.25}$ core nanowires, a wide bandgap InP shell was formed. The nanowire solar cell was fabricated by benzocyclobutene (BCB) filling, exposure of nanowire tips by reactive-ion etching, electron-beam deposition of ITO window layer, and finally metal grid electrode process. In particular, the ITO window layer plays a key role in reducing light reflection as well as electrically connecting nanowires that are electrically separated from each other. The deposition angle was adjusted for conformal coating of ITO on the nanowire surface, and as a result, the lowest light reflectance and excellent electrical connectivity between the nanowires were confirmed at an oblique deposition angle of 40°. The solar cell based on the heterojunction between the n-$InAs_{0.75}P_{0.25}$/InP core-shell nanowire and *p*-Si exhibited a very high photoelectric conversion efficiency of 9.19% with a current density of 27.10 mA/cm$^2$, an open-circuit voltage of 484 mV, and a fill factor of 70.1%.

**Keywords:** heteroepitaxial growth; III-V; core-shell nanowire; indium tin oxide; oblique angle deposition; photo conversion efficiency



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## 1. Introduction

Heterostructures including nanocomposites or heterojunctions have also been highly attractive as building blocks for optoelectronic devices [1–5]. When two different semiconductors meet each other, band lineups occur at the interface in suitable combinations. Therefore, the carriers or electrons are transported or manipulated for applications. Among them, the combination of compound semiconductors which are mostly direct bandgaps gives more favorable optoelectronic properties than Si. Compound semiconductors which are mostly direct bandgaps give more favorable optoelectronic properties than Si [6,7]. However, the high cost associated with their raw materials such as gallium and arsenide and wafer manufacturing are a setback for expanding the compound semiconductors industry. Therefore, instead of using thick and single-crystalline wafers, the hetero-epitaxial growth of III-V compound semiconductors on Si has been highlighted for decades [8–13].

Nonetheless, III-V semiconductors and Si have a huge material dissimilarity including a large lattice mismatch and difference of thermal expansion coefficient which causes a high density of various defects during the growth of III-V on Si, deteriorating device performance [14–16]. One promising way to deal with these issues is to use bottom-up nanowires (NWs) grown by the vapor–liquid–solid (VLS) mechanism, in which lattice strain is elastically relieved at the nearby surface [17–19]. Among them, catalyst-free-, direct growth- NW array has been focused on due to their easy processing and prevention of the formation of the deep level defects by Au catalyst, enabling a superior level of hetero-interface which can be possibly utilized as high-performance electronic devices [20–24].

For most optoelectronic devices, the use of a transparent electrode is essential [2]. In order to fabricate an efficient optoelectronic device with III-V NW on Si substrate, typically transparent conductive oxide (TCO) such as indium tin oxide (ITO), zinc oxide (ZnO), aluminum-doped zinc oxide (AZO), and fluorine-doped zinc tine oxide (FZTO) etc. have been demonstrated. Among them, ITO has been exceptionally used as TCO window layers for various optoelectronic applications. Further, the ITO nanostructures, such as NWs, have also been used for anti-reflection coating (ARC), fully transparent conducting oxide (TCO) materials for light-emitting devices [25], 2-D [26–28], 3-D [29] nano branch ITO anode electrodes for PVs and infrared (IR) plasmonics devices [30]. The slanted ITO nanocolumns have been deposited onto the vertically aligned Si NWs to form the axial p-n junction for PV applications. The ITO nanocolumns antireflective coating has been reported to achieve an enhancement factor of 42% for photocurrents generated at wavelengths transparent to the window layer, demonstrating a viable efficiency-boosting strategy for GaAs solar cells [31].

Here, we successfully demonstrated n-InAsP/InP NW- p-Si heterojunction solar cells by catalyst-free and direct-growth of n-type III-V nanowires on p-Si substrates. The n-$InAs_{0.75}P_{0.25}$ NW array was grown on the p-Si by the Volmer–Weber mechanism as a three-dimensional island growth mode, which enables relaxation of lattice mismatch between III-V and silicon. Then, InP shell was deposited to form a surface passivation layer for core nanowires. Furthermore, for the device fabrication, the nanowire array was filled with BCB and the nanowire tip was exposed by RIE. After that, the ITO window layer is deposited by an E-beam evaporator, and finally, a metal grid electrode was deposited. Specifically, we investigated the effect of the ITO window layer playing an important role in reducing light reflection and electrically connecting the electrically isolated nanowires. When optimizing the deposition angle for conformal coating of the ITO layer, the lowest light reflectance and excellent electrical connectivity between the nanowires were achieved. Therefore, the n-$InAs_{0.75}P_{0.25}$/InP core-shell nanowire/p-Si heterojunction-based solar cell showed a short circuit current density ($J_{sc}$) of 27.10 mA/cm$^2$. Open circuit voltage ($V_{oc}$) of 484 mV and fil factor (FF) of 70.1%, resulting in a high PCE of 9.19%.

## 2. Experimental

Monocrystalline, *p*-type silicon wafers grown by the czochralski process are used for the growth of III-V NWs. The wafers have a resistivity of 1–10 Ω·cm with a diameter of 2 inches and a thickness of 375 μm. The wafers are cleaned using the RCA cleaning procedure and the native oxide is removed by the buffered oxide etchant (BOE) solution for 1 min. For the formation of a back-surface field (BSF) layer, a boron spin-on-dopant (SOD) solution (model B153, Filmtronics Inc., Butler, PA, USA) is spin-coated on the backside of the wafer at 3000 rpm and for 30 s. A soft baking is carried out at 220 °C for 25 min on a hot plate followed by a high-temperature diffusion process (1000 °C, 1 h) in the furnace with an atmosphere of 75% $N_2$ and 25% $O_2$ gases.

A metal-organic chemical vapor deposition (MOCVD, AIXTRON A200) system is used for the growth of $InAs_{0.75}P_{0.25}$/InP core-shell NWs.

For the wafer-scale uniform growth of III-V NWs, the 2-inch Si wafer is dipped in poly-L-lysine (PLL) solution (Sigma-Aldrich Inc., St. Louis, MO, USA) for 3 min then rinsed in DI water for 10 s. The PLL surface treatment is known to significantly increase

the uniformity and density of III-V NWs as demonstrated by our previous work [24]. Then, the Si wafer is immediately loaded into the MOCVD reactor. The reactor pressure is lowered to 50 mbar with a 15 L/min of $H_2$ gas flow and then the reactor is heated to growth temperatures from 580–630 °C. After temperature is stabilized, $AsH_3$ (99.99%, opto-grade, Air products, Yongin, Korea) gas flows into the reactor for 1 min and then TMIn (99.99%, opto-grade, Air products, Korea) and $PH_3$ (99.99%, opto-grade, Air products, Korea) gases are supplied to the reactor. The molar flow of TMIn, $AsH_3$, and $PH_3$ is $2 \times 10^{-5}$, $2.2 \times 10^{-4}$, and $8.4 \times 10^{-2}$ mol/min, respectively. After the growth of InAsP NW cores, the temperature is increased to 650 °C only with a supply of V (i.e., $AsH_3$ and $PH_3$) gases. After temperature is stabilized, the $AsH_3$ flow is stopped and the TMIn valve is opened to grow InP shell layers. The molar flow of disilane ($Si_2H_6$, 0.02% in $H_2$) gas is $4 \times 10^{-9}$ and $2 \times 10^{-8}$ mol/min for the lightly-doped *n*-type InAsP core and heavily-doped *n*-type InP shell, respectively. This flow corresponds to the doping concentration of mid-$10^{17}$ and low-$10^{18}$/cm$^3$ for planar InP film, respectively. The current density-voltage (*J-V*) characteristics are measured (Keithley 2635A) under the simulated AM1.5G radiation (calibrated to 1000 W/m$^2$, 1 sun) equipped with a high-quality optical fiber coupled to a xenon arc lamp. UV-Vis-NIR (Agilent, Santa Clara, CA, USA) is used for the reflectance measurement in the wavelength range of 300–1100 nm region.

## 3. Results and Discussion

Figure 1 illustrates the schematic representation of NW-SC fabrication process steps along with corresponding cross-sectional scanning electron microscope (SEM) (Hitachi-S4700) images. Figure 1a shows the *n*-type $InAs_{0.75}P_{0.25}$/InP core-shell NW array on a *p*-Si wafer with a BSF layer. The NWs are vertically well-aligned with an average height of 4 μm and thickness of 120 nm. The surface of III-V NWs is passivated by a 500 nm-thick $SiO_2$ layer, deposited by using a plasma-enhanced chemical vapor deposition (PECVD) technique. The passivated NW array is then planarized with benzocyclobutene (BCB) (3022-35 DOW Inc., Midland, MI, USA), which acts as a transparent (optical transparency in excess of 99%) electrical insulator for the top and bottom electrodes. The BCB layer was cured for 2 h at 250 °C in a $N_2$ atmosphere. After the formation of a BCB layer, the reactive ion etching (RIE) process is carried out with $CH_4/O_2$ gases in order to expose the top portion of the NWs (Figure 1b). After that, a 400-nm-thick ITO thin film as a window layer is deposited on the exposed NW tips by using an e-beam evaporator at an oblique angle deposition (OAD) configuration (Figure 1c). The structural and optical properties of the OAD-ITO thin films are further addressed in the details later. Figure 1d shows the fabricated NW SC of $10 \times 10$ mm$^2$ area with a top finger pattern of a Ti (20 nm)/Au (300 nm) multilayer, deposited by the e-beam evaporator using a stainless-steel shadow mask.

Figure 2a–i shows the optical and SEM images of *n*-type $InAs_{0.75}P_{0.25}$/InP core-shell NWs grown on *p*-type (111) Si wafers at different temperatures at 590 (a, d, and g), 600 (b, e and h) and 610 °C (c, f and i). One can see that the NWs are vertically aligned and very uniform over the entire 2-inch Si wafers with some micron-sized non-uniform features or 'chunks'. Different colors of the NW wafers suggest that the NW density and morphology vary with a growth temperature. The NW's density and morphology are well controlled for various densities from 1.0 to 9.0 $\times$ $10^7$ /cm$^2$ across the wafer. The average width of NWs increases from 40 to 300 nm and the height decreases from 7 to 2 μm. The high density of NWs is very much impelled to agglomeration as compared with low-density NWs (Figure 2j). When the $InAs_{0.75}P_{0.25}$ based NWs are hetero-epitaxially grown on Si via a catalyst-free or pattern-free growth method [6,23] III-V islands nucleate epitaxially on the surface of Si to alleviate the large strain arising from lattice mismatch at the interface between the Si and III-V semiconductor [32–35]. Once islands form on the Si surface, crystal growth can mostly proceed in the (111) direction due to the low surface energy in that direction [33]. In the meantime, hexagonal geometry of (111)B facets remains because surfaces of higher Miller-indices grow out quickly [36]. At the initial stage of growth, the size and density of islands can be controlled by the growth conditions. For example, the

adatom mobility is slower at a lower growth temperature, resulting in the decrease of a diffusion length, which is the average migration length of adatoms before incorporation. Therefore, the inter-NW distance becomes shorter at lower growth temperatures.

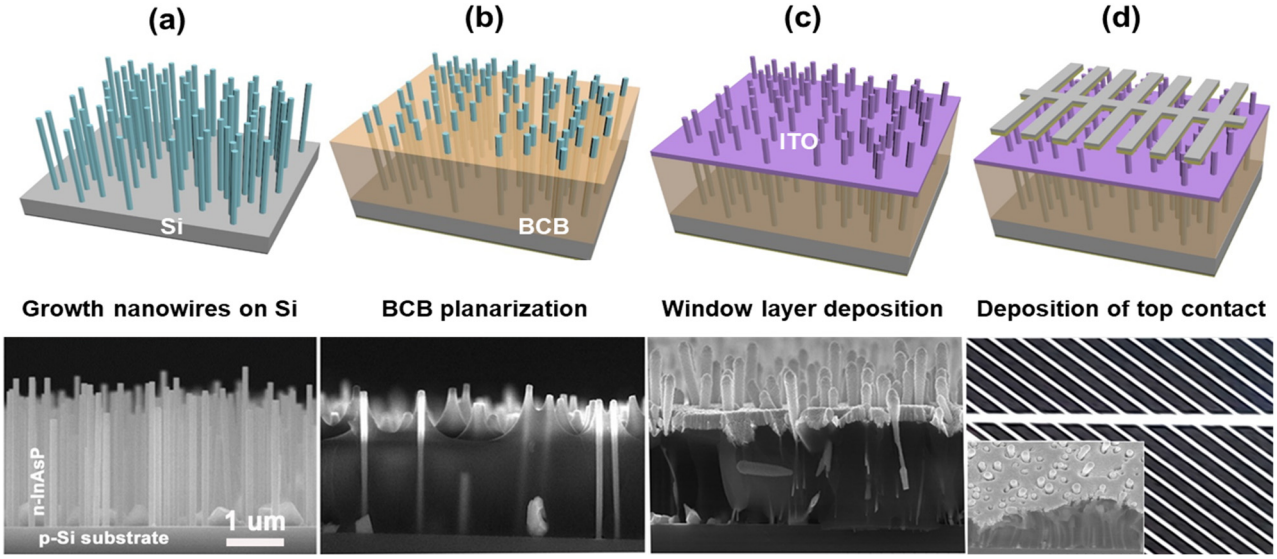


**Figure 1.** Schematic processing fabrication steps for solar cell fabrication with its corresponding cross-sectional SEM images below. (**a**) The growth of n-type $InAs_{0.75}P_{0.25}/n^{+}$-InP core-shell nanowires over 2-inch p-Si wafer after SOD processing, (**b**) The BCB planarization filling over nanowires, (**c**) ITO nanocolumns window layer deposition onto the nanowires tip after RIE, and (**d**) Finally, the deposition of the metal alloy Ti/Au top contact with finger pattern of is deposited over $10 \times 10$ $mm^2$ active area.

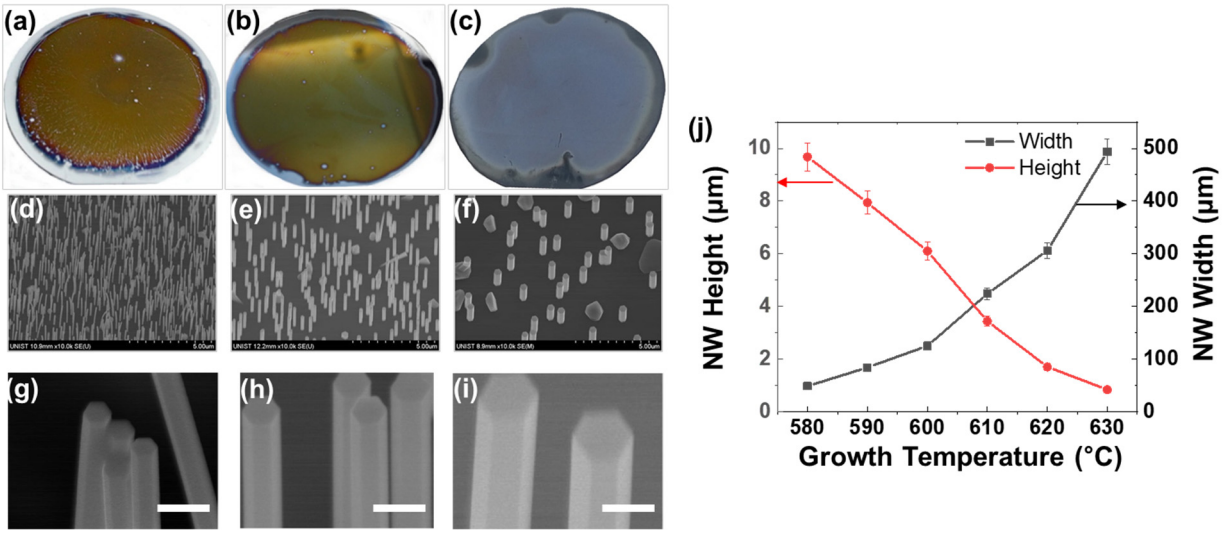


**Figure 2.** Nanowires density and design control over the 2-inch Si wafers with increasing temperature. (**a**–**c**) Optical microscope images of as-grown n-InAs0.75P0.25/n+-InP core-shell nanowires with various density and morphology with increasing temperature from 580 to 640 °C, the optical images of 2-inch wafer scale growth with uniform color distribution over the wafer from left to right, (**a**) grown at 590 °C, (**b**) 600 °C, and (**c**) 610 °C, (**d**–**f**) The corresponding SEM images with 30° tilted view at the center part of the each wafer, and (**g**–**i**) High magnification SEM images of each nanowire (scale bar: 200 nm) (**g**) The plot between nanowires design in terms of height and width with increasing growth temperature. (**j**) height and width of nanowire as function of growing temperature.

After the growth of $InAs_{0.75}P_{0.25}$ core NWs, InP shells are deposited at a higher temperature of 650 °C with increasing growth time from 4 to 30 nm in order to investigate the passivation effects of the shell thickness. Figure 3 illustrates photovoltaic performances of heterojunction core-shell NWs on Si as a function of increasing growth time of the InP passivated shell. Figure 3a displays the *J-V* characteristic under dark of an n-type $InAs_{0.75}P_{0.25}$/InP core-shell NWs. The data was plotted in semi-log axis to appropriately extrapolate the values such as reverse bias leakage current, ideality factor and rectification ratio. The low leakage current of ~$10^{-7}$ mA/cm$^2$ at −0.5 V and high rectification ratio of up ~$10^5$ (at ±0.5 V bias) are consistently measured for the sample with a 10-min-grown InP shell. A fitting curve in the diffusion current region reveals ideality factors of 1.52, which can be attributed due to two significant factors of non-catalyst and high-bandgap passivated shell growth, respectively [20,29,37,38]. Specifically, catalyst-free growth techniques such as the selected area epitaxy or Vomer–Weber approach require no catalysts [20] (for gold or copper) to initiate the growth, avoiding any metal incorporation within the GaAs crystal that has been reported to increase the reverse bias leakage current in NW-based devices [39]. Furthermore, the high-bandgap shells such as InGaP and InP can minimize the surface state density on the nanofacets that could partly deplete the n–p junction/interface. This is observed by the fact that the ideality factor is far below the space-charge-limited condition ($n \geq 2$). This is evidence that a high-quality p-n junction was formed between the $InAs_{0.75}P_{0.25}$/InP core-shell NWs and the p-Si substrate. Moreover, it is observed that the p-n junction quality improves with the increasing n-InP shell thickness over $InAs_{0.75}P_{0.25}$ core. InP shell acts as an effective passivation layer in this device with very low recombination velocity.

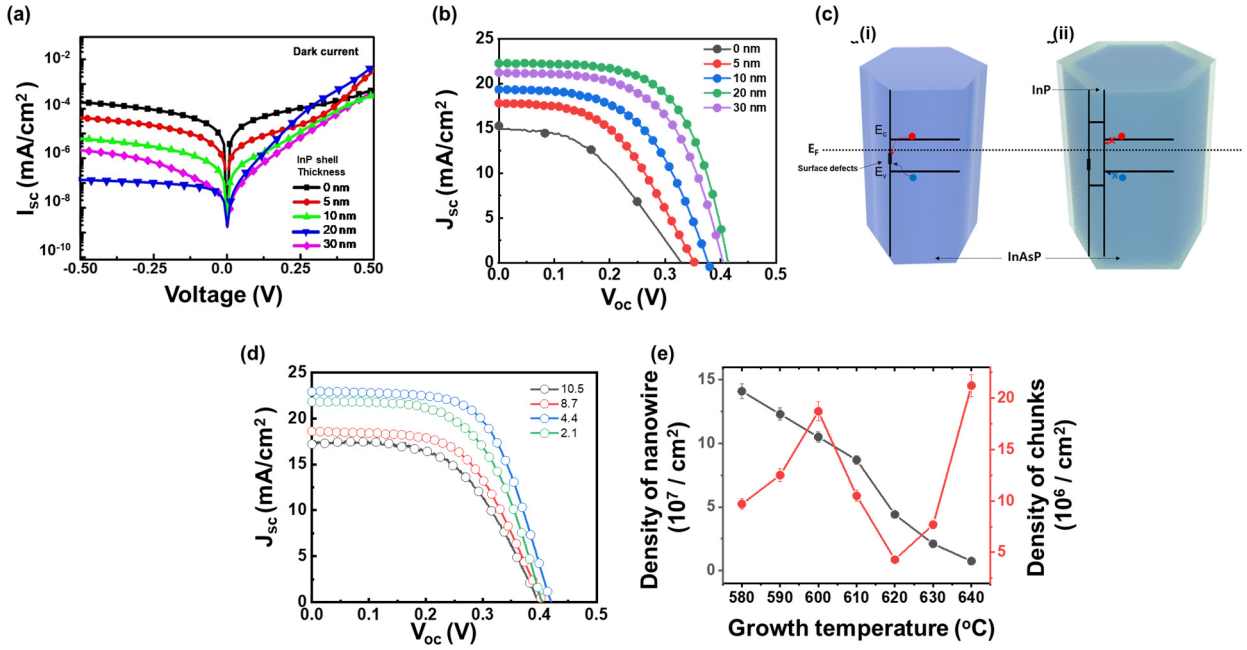


**Figure 3.** (**a**) D*ark J-V* characteristic for p-n junction with increasing growth thickness of InP shell from 5–30 nm, (**b**) *J-V* characteristics of solar cell devices with increasing $n^+$-InP shell thickness from 5–30 nm (**c**) Band diagram of InAsP/Si heterojunction (**i**) without InP and (**ii**) with InP layer. (**d**) *J-V* characteristics of solar cell devices with decreasing nanowire density from 10.5 to 2.1 × $10^7$ /cm$^2$ (**e**) The density of hexagonal nanowires and non-uniform micro scale chunks as function of growth temperature from 580 to 640 °C.

Figure 3b demonstrates the *J–V* characteristics under light for devices without and with in situ epitaxial growth of InP shell with increasing the thickness of the shell from 5, 10, 20 and 30 nm. The optimized InP shell with its high-bandgap (1.34 eV) minimalizes the surface

state density on the nanofacets that could partially deplete n-InAsP-core/$n^+$-InP-shell NW with p-Si. In a high-injection regime, a high series resistance is observed and hence the poor FF without passivation layer. For photovoltaic devices without InP shells (black lines), $V_{OC}$ of 325 mV and $J_{SC}$ of 15.43 mA/cm$^2$ with FF of 42.1% are observed. This translates into a poor photovoltaic efficiency of up to 2.11%. In the case of core–shell NWs junctions capped with InP shells, the photovoltaic properties are improved remarkably with increasing shell thickness from 4 to 20 nm; $V_{OC}$ = 423 mV, $J_{SC}$ = 22.25 mA/cm$^2$ and FF = 61.4%. This leads to a higher photoconversion efficiency of 5.70% for 10 min deposited InP shell. The InP shell layer has the role of reducing surface states as confirmed by high FF and $J_{SC}$. The $V_{OC}$ value is increased significantly compared with un-passivated devices since the offset between the InAs and InP conduction bands is ~0.52 eV. Such offset gives a strong confinement for the InAsP electrons in one-dimensional (1-D) NWs. Since the growth of InP is carried out continuously in the MOCVD chamber, which prevents InAsP from getting oxidized and results in a high-quality epitaxial growth. In the case of n-type $InAs_{0.75}P_{0.25}$ NW/ p-Si without InP passivation, there is an inevitable surface state at the surface of InAsP, which acts as a recombination center (Figure 3c,i). Therefore, $InAs_{0.75}P_{0.25}$ NW/ p-Si without InP passivation have bad diode characteristics. On the other hand, when the InP shell layer is deposited onto $InAs_{0.75}P_{0.25}$ NW, the surface is effectively passivated and reducing the defects at the surface of $InAs_{0.75}P_{0.25}$ NW (Figure 3c,ii). However, when the InP shell is too thick, light absorption within the shell cannot contribute to the photovoltaic parameter so short-circuit current, open-circuit voltage, and FF are reduced. The summary of photovoltaic performances without and with increasing InP-shell growth from 4 to 30 nm over InAsP-core is further shown in Table 1.

**Table 1.** The photovoltaic parameters of III-V core-shell nanowires grown/silicon heterojunction solar cell with and without InP-shell growth from 0 to 30 nm over InAsP-core.

| InP Thickness | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | Eff. (%) |
|---|---|---|---|---|
| 0 | 15.43 | 325 | 42.1 | 2.11 |
| 5 | 17.80 | 353 | 48.2 | 3.15 |
| 10 | 19.33 | 378 | 53.4 | 3.91 |
| 20 | 22.25 | 423 | 61.4 | 5.70 |
| 30 | 21.22 | 405 | 57.8 | 5.05 |

The *J-V* performance and summary of photovoltaic devices are optimization over NW density and design as shown in Figure 3d. With decreasing NW density from 8.7 to 4.4 × $10^7$ /cm$^2$ of exposed NWs, the photovoltaic efficiency is increased from 4.08 to 5.89% and then followed by reduction to 5.17% at 2.1 × $10^7$ /cm$^2$. Similarly, the $J_{SC}$ is increased from 18.58 to 22.90 mA/cm$^2$ with decreasing NW density from 8.7 to 4.4 × $10^7$ /cm$^2$ and further reduced to 21.80 mA/cm$^2$ at 2.1 × $10^7$ /cm$^2$. The $V_{OC}$ and FF also have the same behavior as $J_{SC}$. As shown in Figure 3d, photovoltaic parameters are highly dependent on the density of micro-sized chunks ($D_{chunk}$). The light absorption from the nanowires is enhanced when the nanowires are long and wide. Kim et al. [36] demonstrated that longer nanowires exhibited larger absorption. However, beyond a certain length, light absorption is saturated. Moreover, the shape [40] or arrangement [41] of nanowire also affects nanowire absorption. However, a large surface area of nanowire also acts as a recombination site for electronic devices including photovoltaic devices. Therefore, Yang et al. [38] claimed that there is a trade-off relation between performance and density or length of the nanowire. Likewise, devices with large densities of the nanowire (blue and red line in Figure 3d) have a large surface area so recombination losses are severe. Therefore, photovoltaic parameters are decreased. On the other hand, absorption capability in the sample with a low density of nanowire (green line in Figure 3d) is low so performance is slightly lower than devices with a medium density of nanowire (blue line in Figure 3d).

When the $D_{chunk}$ increases, the efficiency reduces significantly. All details are further listed in Table 2.

**Table 2.** The performance of photovoltaic devices depending on nanowires density ($D_{Nanowire}$).

| Density of Nanowire ($10^{-7}$/cm$^2$) | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | Eff. (%) |
|---|---|---|---|---|
| 10.5 | 16.95 | 398 | 50.8 | 3.39 |
| 8.7 | 18.58 | 406 | 56.0 | 4.08 |
| 4.4 | 22.90 | 420 | 61.6 | 5.89 |
| 2.1 | 21.80 | 404 | 58.2 | 5.17 |

Recent reports have also suggested that the NW's morphological control with diameter/width, height/length and pitch play a significant role in the photovoltaic performance [35,42,43]. It is observed that the NW agglomeration increases with increasing density. Hence, by controlling the NWs density, we are able to enhance the $J_{SC}$ significantly which has contributed to improving the photoconversion efficiency of the device. With optimized NW density at $4.0 \times 10^7$ /cm$^2$, a clear balance is observed with the number of absorbed photons at the p-n junction and the number of extracted/collected charge carriers without any recombination. We adopted an oblique angle deposition technique to uniformly deposit the ITO window layer on the top and side surfaces of the NWs. The ITO window layer plays dual roles of reducing light reflection as well as electrically connecting nanowires that are electrically separated from each other. With increasing oblique angles from 10 to 40°, 400-nm-thick ITO layers were deposited on the sample with a density of $4.0 \times 10^7$ /cm$^2$ at 240 °C. As shown in Figure 4a, SEM images demonstrate that the nanowire arrays are conformally coated with an increasing oblique angle. When deposited at a 40° oblique angle, the ITO layer is completely caped and covers (green color) the NWs as shown in the schematics. Therefore, the $J_{SC}$, $V_{OC}$, and FF are found to be increased continuously from 21.50 to 27.10 mA/cm$^2$, 433 to 484 mV and 62.4 to 70.1% respectively with increasing oblique angles from 10 to 40°, respectively (Figure 4b). Figure 4c shows the reflectance of the devices.

As shown in the dark J-V curves of photovoltaic devices with 0° and 40° angled deposited ITO layer (Figure 4d), this is in good agreement with the enhancement of photovoltaic parameters after angled deposition. The conformally coated ITO electrically connects the III-V nanowires more efficiently, and thus, it improved the diode characteristics with a low dark saturation current. The improvement of light absorption and electrical connection between these nanowires led to a continuous decrease in series resistance or an improvement in FF, achieving a record high efficiency of 9.19%. The detailed photovoltaic parameters are further summarized in Table 3.

**Table 3.** Summary of photovoltaic parameters with ITO transparent electrodes deposited at different OAD from 0 to 40°.

| Deposition Angle | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | Eff. (%) |
|---|---|---|---|---|
| 0 | 21.50 | 433 | 62.4 | 5.81 |
| 10 | 23.90 | 460 | 63.5 | 6.98 |
| 20 | 25.60 | 472 | 67.5 | 8.16 |
| 30 | 26.78 | 480 | 68.8 | 8.84 |
| 40 | 27.10 | 484 | 70.1 | 9.19 |

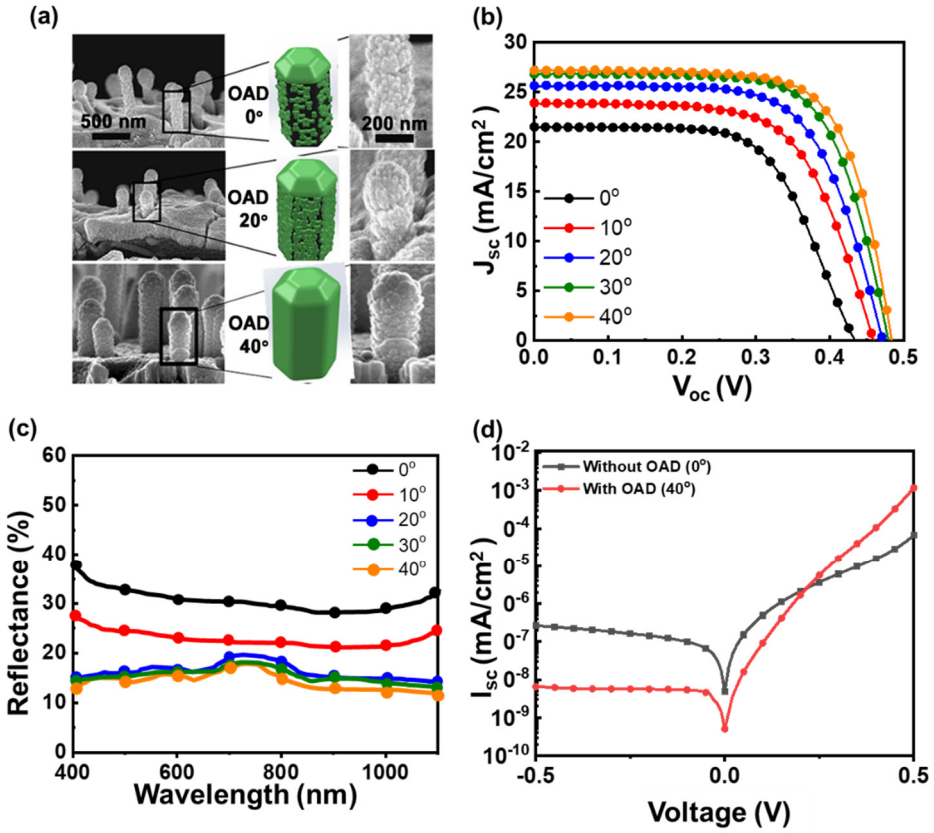


**Figure 4.** (**a**) SEM images of ITO coated III-V core-shell nanowires grown on silicon (**b**) *J-V* performance with increasing ITO oblique angle from 0 to 40° (**c**) The reflectance spectra with increasing ITO oblique angle deposition from 0° to 40° (**d**) Dark J-V curves of photovoltaic devices with 0° and 40° angled deposited ITO layer.

## 4. Conclusions

In summary, we fabricated the wafer scale growth of n-type $InAs_{0.75}P_{0.25}/n^{+}$-InP core-shell NWs over 2-inch p-Si. The heteroepitaxial was grown n-$InAs_{0.75}P_{0.25}$ NW onto the Si as a three-dimensional island growth followed by the Volmer–Weber mechanism. Moreover, a wide bandgap of InP shell effectively reduced recombination and demonstrated an excellent diode rectification ratio greater than $10^4$ at $\pm$1 V bias with 1.52 ideality factors. Moreover, 400 nm thick ITO nanocolumns deposited at 40° oblique angle onto the NWs have been able to suppress the reflectance gradually towards 12% over the 300–1100 nm wavelength range and connect isolated nanowires. As a result, $InAs_{0.75}P_{0.25}$/InP core-shell nanowire and p-Si heterojuction solar cells exhibited $J_{SC}$ of 27.10 mA/cm$^2$, $V_{OC}$ of 484 mV and 70.1% of FF, corresponding to PCE of 9.19%. This heteroepitaxial growth of III-V nanowire arrays on p-type Si substrate enables high-performance optoelectronic devices at a low cost. Thus, this work can open up the possibility of the III-V nanowire arrays-based electronic devices with new techniques in an inexpensive and simple way beyond traditional photovoltaics.

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