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Epitaxial cubic silicon carbide on silicon is of high potential technological relevance for the integration of a wide range of applications and materials with silicon technologies, such as micro electro mechanical systems, wide-bandgap electronics, and graphene. The hetero-epitaxial system engenders mechanical stresses at least up to a GPa, pressures making it extremely challenging to maintain the integrity of the silicon carbide/silicon interface. In this work, we investigate the stability of said interface and we find that high temperature annealing leads to a loss of integrity. High–resolution transmission electron microscopy analysis shows a morphologically degraded SiC/Si interface, while mechanical stress measurements indicate considerable relaxation of the interfacial stress. From an electrical point of view, the diode behaviour of the initial p-Si/n-SiC junction is catastrophically lost due to considerable inter-diffusion of atoms and charges across the interface upon annealing. Temperature dependent transport measurements confirm a severe electrical shorting of the epitaxial silicon carbide to the underlying substrate, indicating vast predominance of the silicon carriers in lateral transport above 25 K. This finding has crucial consequences on the integration of epitaxial silicon carbide on silicon and its potential applications. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4955453]

Epitaxial cubic silicon carbide (SiC) films on silicon have attracted extensive interest in many semiconductor device applications such as high-voltage, high-frequency diodes, hetero-junction bi-polar transistors and micro electro mechanical systems (MEMS).[1,2] This is because they offer access to the electrical and mechanical properties of the SiC material such as its wide band gap, high thermal conductivity, and chemical stability, in addition to a large tuneable tensile stress.[1,3] However, the large lattice and thermal mismatches between the SiC film and silicon result in a high density of defects[4] and a sharp residual stress gradient at the SiC/Si interface.[5] Consequently, non-ideal diode characteristics have been observed for the common n-SiC/p-Si electronic junction, which poses concerns for the reliability of 3C-SiC devices.[1,4,6–9]

Tanner *et al*. have characterized the as-grown n-3C-SiC/p-Si hetero-junctions and have demonstrated a strong interface with reverse bias breakdown voltages exceeding 200 V, and ±1 V rectification ratio of 200 000 at room temperature.[1] However, the stability of the interface at higher temperatures, which is relevant for the synthesis of graphene on 3C-SiC/Si,[10] GaN on SiC/Si[11] and for harsh-environment applications of the SiC/Si[12] has not yet been investigated to-date.

In this work, we evaluate the stability of the SiC/Si hetero-junction at high temperatures by performing stress, electronic transport measurements, and high-resolution microscopy of the SiC/Si interface. We show that high temperatures have catastrophic consequences on the SiC/Si junction.

Unintentionally *n*-type doped epitaxial 3C-SiC films with thickness of 250 nm were grown in-house at 1000 °C on low-doped 6″ wafers of *p*-type Si(100) and Si(111) with thickness of 680 ± 25 μm in a hot-wall horizontal Low-Pressure Chemical Vapour Deposition (LPCVD) system using an alternate supply of SiH_4 and carbon source gas, described in previous reports.[4,13] The carbonisation was performed at 950 °C using C_2H_2.

For the electrical characterization, SiC/Si wafers were diced into 1 × 1 cm^2 fragments. For measurements with setup 1 (Griffith University), 150 nm nickel contacts were sputtered on the four corners of the aforementioned samples. The electrical properties such as the carrier concentration, carrier mobility, and sheet resistance were estimated at room temperature by performing Hall measurements in a van der Pauw configuration on the as-grown SiC(100) films, with electrical probes directly connected with the metal contacts and sweeping the DC input current of 0 to 10 mA using a HP4145B semiconductor parameter analyser.[10] Analogous SiC(100) films were annealed at 1100 °C using a Carbolite High Temperature Furnace at 10^{-4} mbar for 1 hr, and the electrical measurements were repeated at room temperature on the annealed SiC films. Complementary measurements were also carried out on the 1 × 1 cm^2 fragments of the bare silicon substrate. Additionally, equivalent electrical measurements at room temperature were performed on 1 × 1 cm^2 fragments of commercially available, unintentionally *n*-type doped NOVASiC SiC(100) grown at 1350 °C after a carbonisation step at 1100 °C.[14]

The temperature-dependent transport measurements of the as-grown and the annealed in-house SiC(100) films were performed with a Quantum Design PPMS (subsequently referred to as "setup 2"). 1 × 1 cm^2 fragments of SiC wafers with (5/50 nm) Ti/Au contacts on the four corners in the van

der Pauw geometry were used. In instances of poor wire bond adhesion, silver epoxy was used to make electrical connection to the samples. Two probe current-voltage curves were measured to ensure ohmic contact. The measurements were carried out as a function of temperature in the range between 5 K and 300 K. Hall carrier density values were measured by sweeping the magnetic field ±0.1 T, symmetrizing the measured R_{xy} response and fitting the linear slope to extract the carrier density. The temperature-dependent resistivity is used to estimate the ionization energy of dopants in the samples (see below). High-resolution transmission electron microscopy (HRTEM) was performed to characterize the SiC/Si interface of the as-grown and the annealed SiC(100) and SiC(111) films using a FEI Tecnai F30 system operating at 200 keV.[4] Sample foils for transmission electron microscopy were prepared via a focused ion beam (FIB) lift-out technique using a FEI Strata DB235 FIB/SEM with a Ga^+ ion source. The foils were excavated from the bulk samples and thinned to about 500 nm. Subsequently, Ar^+ ion milling was conducted in a Fiscione NanoMill^{TM} to remove Ga^+ ion damage. A 2 μm thick Pt/Au protective layer was deposited on the samples prior to FIB milling.

We also conducted a residual in-plane stress analysis on the as-grown and annealed in-house SiC films via full wafer curvature measurement. 3C-SiC(100) and 3C-SiC(111) films grown with different thicknesses on full 6″ silicon wafers were used for the study. A Tencor Flexus 2320 system was used for measuring the wafer curvature of the Si substrate and the substrate-film composite at room temperature.[4] The residual in-plane stress for the SiC film was calculated using the modified Stoney's equation with appropriate elastic moduli (E) and Poisson's ratio (ν) values: 130 GPa and 170 GPa, 0.28 and 0.26 for Si(100) and Si(111), respectively.[4,5] Subsequently, the as-grown films were subjected to thermal annealing in N_2 at different temperatures of 1100 °C, 1180 °C, and 1250 °C for 2 hrs. This was done in a Hi-Tech Furnace Systems (UK) LPCVD system at sub-atmospheric pressure of 10–1000 Pa.[5] From the residual stress values of the as-grown and the annealed film, the absolute stress difference (MPa) between them was assessed.

Table I shows the room temperature van der Pauw measurement results of the as-grown and the annealed SiC(100) samples obtained with setup 1. The as-grown SiC(100) indicates *n*-type conduction with sheet carrier concentration (n_s), carrier mobility (μ_s), and sheet resistance (R_s) of $3.3(\pm0.2)\times10^{14}$ cm^{-2}, 14(±10) cm^2/V s, and 1354 ± 1 Ω/□, respectively.

Upon annealing, the sample shows an abrupt switch to *p*-type conduction with a n_s ~3 times larger than that of the as-grown sample. In addition, the mobility increases significantly from 14 cm^2/V s to 273 cm^2/V s, accompanied by a drastic decrease of the R_s of the sample down to 24 Ω/□. These room temperature values are in good agreement with those obtained from setup 2, at Monash University.

TABLE I. Electrical characteristics measured at room temperature for in-house SiC/Si(100) samples as-grown and after annealing at 1100 °C (data acquired with setup 1).

	As-grown	Annealed
Carrier type	Electrons	Holes
Sheet carrier concentration, n_s (cm^{-2})	$3.3(\pm0.2)\times10^{14}$	$9.5(\pm0.2)\times10^{14}$
Mobility, μ_s (cm^2/V s)	14(±10)	273(±10)
Sheet resistance, R_s (Ω/□)	1354 ± 1	24 ± 1

Complementary room temperature measurements of the bare silicon substrate indicate *p*-type conduction with a sheet carrier concentration of $\sim9\times10^{13}$ cm^{-2}, from which a bulk carrier concentration of $\sim1.3\times10^{15}$ cm^{-3} is estimated, and a mobility of ~341 cm^2/V s.

We thus hypothesize that the switch to *p*-type carriers, increase in mobility, and drop in sheet resistance are due to a shorting of the SiC film to the substrate upon annealing with consequent dominance of the carriers in the thick silicon substrate, with relatively high mobility. If we considered the annealed SiC sample in Table I as an electrically shorted substrate plus film composite, we would estimate a bulk sheet carrier concentration of 1.5×10^{16} cm^{-3}. This is an order of magnitude higher than the bulk carrier concentration directly measured on the silicon substrate, which is plausible as a result of the combined carrier contributions from both silicon substrate and the silicon carbide.[15]

Further corroborating this hypothesis, the as-grown unintentionally doped (thus *n-type*) commercial NovaSiC SiC films on p-type Si(100) show the unexpected *p-type* conduction already when measured at room temperature, with n_s, μ_s, and R_s of 1×10^{14} cm^{-2}, 272 cm^2/V s, and 180 Ω/□, respectively. When grown on *n*-type substrates instead, these films always show *n*-type conduction. This indicates that the transport characteristics of the commercial samples may be dominated by the substrate already as-grown. Note that such samples are grown at a much higher temperature of 1350 °C.[14]

The low-temperature transport measurements were performed on the SiC films grown in-house for a more detailed analysis. Figure 1 illustrates the low temperature behaviour of the sheet resistance of the as-grown and the annealed SiC(100) as a function of temperature in the range between

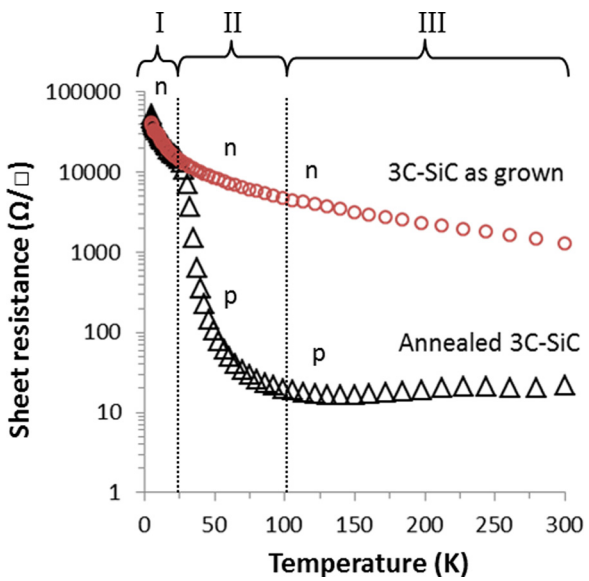

FIG. 1. Sheet resistance of the 250 nm thick as-grown SiC(100) and the vacuum annealed SiC(100) at 1100 °C for 1 hr as a function of temperature in the range between 5 K and 300 K.

5 K and 300 K. The sheet resistance of the as-grown SiC film decreases monotonically with temperature. From basic solid state theory, the resistivity of a semiconductor versus temperature would decrease according to an Arrhenius type behaviour[16,17] such as

$$\rho \propto T^{3/2} \exp\left(\frac{E_a}{2k_B T}\right), \quad (1)$$

where ρ is the resistivity, k_B is the Boltzmann constant, T is the absolute temperature, and E_a is the activation energy of the semiconductor. In particular, for k_BT far below the bandgap of the semiconductor, the activation energy dominating the resistivity behaviour is the donor (for *n*-type) or acceptor (for *p*-type) energy level for the specific dopant.

In hetero-epitaxial SiC on silicon, it is notoriously hard to identify a specific dopant level as the resistivity is affected by a combination of different unintentional defects, including N incorporation.[18] Indeed, by fitting the as-grown SiC resistance behaviour, we confirmed the presence of different donor contributions with energy levels approximately varying from 2 meV to 52 meV (extracted using Equation (1)) over the studied temperature range as reported in the literature.[18]

On the other hand, the annealed SiC(100) indicates a more complex behaviour within the same temperature range. For temperatures below ~25 K (zone I), its behaviour matches with that of the as-grown SiC, including the presence of a majority of *n*-type carriers. However, just above ~25 K, a change in majority carriers to *p*-type is observed, concomitant with a sharp decrease in sheet resistance of several orders of magnitude (zone II). In zone II, this sample shows the typical decreasing resistance behaviour versus temperature expected for a semiconductor with different donor/acceptor characteristics. Above ~150–200 K (zone III), the annealed sample shows an increase in resistivity, associated with a predominance of phonon scattering, while continuing to exhibit prevalent *p*-type conduction.

Fig. 2 shows the fitted resistivity for the annealed SiC as a function of temperature in the range from 30 K to 100 K (zone II), with slope = 0.11. The extracted acceptor energy level using Equation (1) is about 44 meV, which is consistent with the boron acceptor energy level in silicon (46 meV).[19] Note that this was calculated through an approximated expression of Eq. (1) where the power dependence of the temperature was neglected, an adequate approximation for low temperatures.

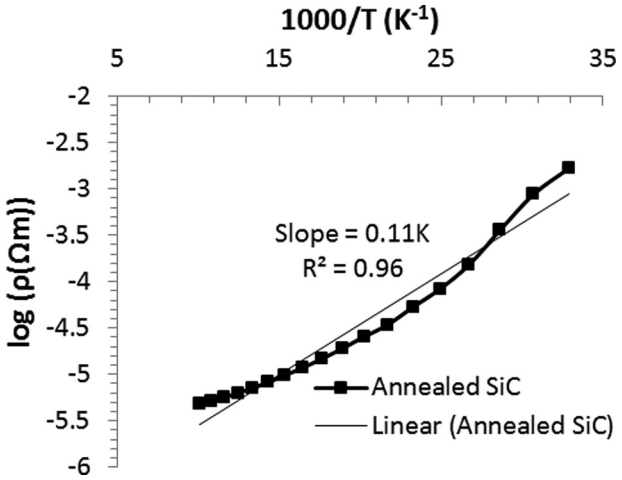

FIG. 2. Resistivity versus temperature for the annealed SiC(100). Activation energy of 44 meV is obtained by fitting the data over 30 K to 100 K (zone II).

The data in Fig. 1 indicate that while the resistivity of the as-grown SiC/Si(100) matches what is expected for an *n*-type 3C-SiC semiconductor film, the behaviour of the annealed SiC/Si(100) matches with that of 3C-SiC only for temperatures below 25 K. Above 25 K, (zone II) the resistance behaviour closely resembles the one expected from silicon (see the extracted energy level). The fact that above 25 K the majority carrier type conduction switches abruptly from *n*- to *p*-type is a further strong indication that the silicon substrate dominates the conduction in the annealed SiC/Si in zones II and III, including room temperature. This all would indeed point to a system in which the conduction of the thin film SiC and that of the silicon substrate are highly intermixed, appearing electrically shorted. The *p*-type conduction within the thick silicon substrate clearly dominates until between 50 K and 25 K where a substantial freeze-out of the boron dopants in the silicon matrix is reached.[20] Note that the total number of carriers in the silicon substrate and in the SiC film are comparable, but the *p*-type carriers in the silicon show much higher mobility, so they dominate the system above the B dopant freeze-out temperature. Therefore, we find that the *n*-type conduction of the SiC film is the prevalent measured signal only below 25 K.

If the carbonisation layer, which serves as the sealing layer for the out-diffusion of silicon, develops substantial discontinuities, this would allow for extensive charge diffusion at the SiC/Si interface with consequent loss of the *n-p* junction.

If this were the case, the degradation of the interface would likely be accompanied by a relaxation of interfacial stress. Table II shows residual mean stress (MPa) and absolute stress differences (MPa) of SiC(100) and SiC(111) films of thickness ranging between 50 nm and 1 μm, before and after annealing at different temperatures above the SiC growth temperature.

We have already reported[5] that the as-grown 3C-SiC films on Si show tensile mean residual stress due to the lattice and thermal mismatches. From Table II, we can observe that, when the thin films of SiC are thermally annealed, the stresses tend to become more compressive. The extent of the change upon annealing is given by the absolute stress difference (MPa) in Fig. 3, and it appears to be strongly dependent on the film thickness. In particular, the largest difference is found for the thinnest films, for both SiC(100) and SiC(111).

In addition, Table II shows that, not surprisingly, the extent of stress change also depends on the annealing temperature: higher annealing temperatures lead to a larger change. For example, the 49 nm thick SiC(100) data shown led to an absolute stress difference of 532 MPa when annealed at 1180 °C while annealing at 1250 °C caused a larger stress difference of 762 MPa. The absolute stress differences between the as-grown and annealed samples as a function of the film thickness is plotted in Fig. 3. All the samples shown here are annealed at 1180 °C in N_2 for 2 hrs.

TABLE II. Residual mean stresses (σ) for the as-grown and annealed SiC (100) and SiC(111) films and the absolute stress differences between them. The films are of different thicknesses and annealed in N_2 for 2 hrs at different temperatures of 1100 °C, 1180 °C, and 1250 °C.

			σ_{anneal} (MPa)			
Sample no.	Thickness (nm ± 2 nm)	$\sigma_{as\text{-}grown}$ (MPa)	1100 °C	1180 °C	1250 °C	Absolute stress differences (MPa)
SiC(100)						
1	49	424		−108		532
2	49	363			−399	762
3	66	302	129			173
4	67	288		−28		315
5	67	322			−208	530
6	92	323		133		190
7	92	291			−15	306
8	270	187		147		39
9	300	305		273		31
10	348	308		297		11
11	994	151		153		−3
SiC(111)						
1	50	423		−462		885
2	53	616			−563	1179
3	69	856	735			121
4	70	1034	891			143
5	69	467		−120		586
6	70	840		439		401
7	71	590			−203	794
8	90	458		100		358
9	95	644			90	554
10	238	524		442		82
11	300	915		852		63
12	945	679		672		7

These data indicate that the absolute stress differences after annealing for SiC(100) and SiC(111) are of a similar magnitude. Furthermore, the thickness dependence clearly indicates suppression of the stress change with increasing thickness, with samples on the order of 1 μm showing virtually no change with annealing. The strong reduction in stress change when moving away from the interface indicates that this is an interfacial stress dominated phenomenon. Note that as a result of this stress relaxation at the SiC/Si interface, we observed plastic relaxation of the substrate after annealing, leading to a change in the bare substrate wafer curvature to more convex. The values of σ_{anneal} in Table II were not corrected for this change, so that the stress changes in Fig. 3 are in fact a measure of the overall SiC/Si interface relaxation. Finally, we note that that the occurrence of plastic deformation of the silicon substrate was reported by Zielinski *et al.*, when growing SiC at high temperatures.[22]

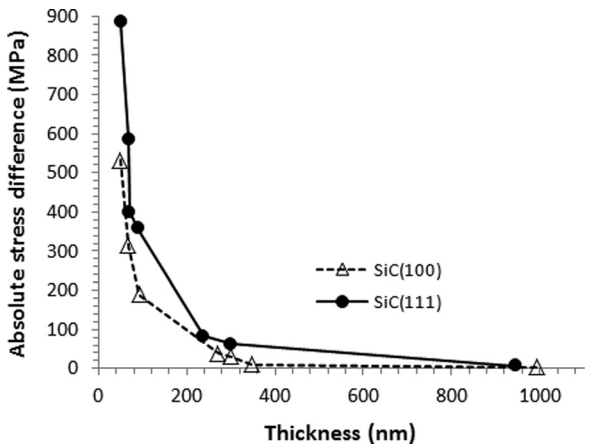

FIG. 3. Absolute stress difference of the epitaxial SiC(100) and SiC(111) films before and after annealing at 1180 °C versus film thickness. Each point represents the absolute difference of the average stress for the as-grown and the annealed films. The difference indicates in all cases a transition towards a more compressive stress state with decreasing thickness. Note that the exponential suppression of the stress difference with increasing thickness indicates the interfacial nature of the stress change.

Cross sectional transmission electron microscopy focusing on comparing the SiC/Si interface of as-grown and SiC films annealed at 1100 °C should likely indicate morphological changes.

Fig. 4 shows that both the as-grown 3C-SiC(100) and SiC(111) films possesses a very thin, well defined ∼1 nm thick carbonisation layer at the interface. On the other hand, it is evident that, after annealing, the SiC/Si interface degraded, appearing inhomogeneous in the TEM image.

All of these data indicate a substantial degradation of the interface as failure *mode*, a consequence of the combination of high temperatures and high stresses at the SiC/Si interface. A substantial amount of stress is relaxed at the SiC/Si interface by allowing substantial atomic interdiffusion between the SiC and the silicon substrate. Here, we indicate that the carbonisation barrier can already break down at temperatures roughly above 1000–1100 °C, although the exact temperature may slightly shift depending on the carbonisation processes. This effect is so prominent that the insulating n-SiC/p-Si junction is destroyed and the

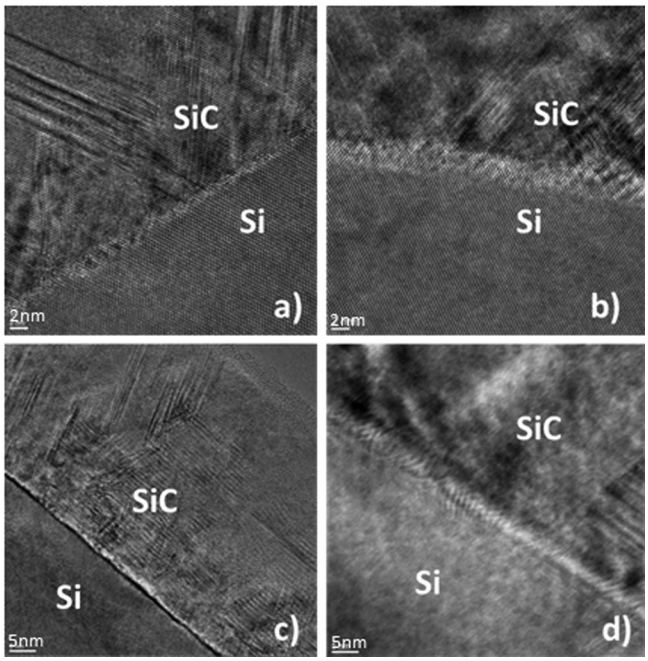

FIG. 4. High-resolution TEM micrographs of the SiC-Si interface of the 250 nm-thick SiC(100) and SiC(111) films (a) as-grown SiC(100) film (b) SiC(100) film annealed in vacuum at 1100 °C, for 1 hr (c) as-grown SiC(111) film (d) SiC(111) film annealed in vacuum at 1100 °C, for 1 hr. The SiC/Si interface of both the as-grown SiC films appears to be well-defined, whereas the interface of the annealed SiC films appears inhomogeneous.

layer-substrate system becomes electrically shorted to the substrate.

Such fatal failure can occur both upon film growth at high temperature (NovaSiC) and annealing at high temperature (in-house films). The detailed description of the failure mechanisms will be strongly dependent on the specific sample preparation. Here, we suggest some plausible root causes. The interface layer of the in-house SiC films on silicon possesses about a GPa of compressive stress.[5] That alone could lead to failure at high temperatures because of enhanced creep effects.[21] For the commercial samples, this is potentially compounded by the additional compressive thermal stress[23] of the thin carbonisation layer when brought to 1350 °C for the SiC growth and increased Si out-diffusion at such temperature, only ~60 °C lower than the silicon melting temperature. The silicon out-diffusion from silicon substrate to the silicon carbide at high temperatures in the absence of an efficient diffusion barrier is a well-known issue.[24,25] The occurrence of creep via atomic diffusion at the SiC/Si interface was likely already observed earlier.[22]

The SiC/Si interface instability has crucial consequences on applications where the silicon carbide on silicon is exposed to high temperatures. In particular, this affects not only the use of SiC on silicon for harsh environments, but also the use of SiC on silicon as pseudo-substrate for the growth of III-N and graphene on silicon, as those materials are currently grown at temperatures above 1000 °C. Therefore, we indicate a compelling need to identify a more robust barrier at the SiC/Si interface able to insulate the silicon carbide from the silicon substrate at high temperatures.[24]

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