# CDF run IIb silicon: Design and testing

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***Abstract*—The various generations of Silicon Vertex Detectors (SVX, SVX', SVXII) for Collider Detector at Fermilab (CDF) at the Fermilab Tevatron have been fundamental tools for heavy-flavor tagging via secondary vertex detection. The CDF Run IIb Silicon Vertex Detector (SVXIIb) has been designed to be a radiation-tolerant replacement for the currently installed SVXII because SVXII was not expected to survive the Tevatron luminosity anticipated for Run IIb. One major change in the new design is the use of a single mechanical and electrical element throughout the array. This element, called a *stave*, carries six single-sided silicon sensors on each side and is built using carbon fiber skins with a high thermal conductivity on a foam core with a built-in cooling channel. A Kapton bus cable carries power, data and control signals underneath the silicon sensors on each side of the stave. Sensors are read out in pairs via a ceramic hybrid glued on one of the sensors and equipped with four SVX4 readout chips. This new design concept leads to a very compact mechanical and electrical unit, allowing streamlined production and ease of testing and installation. A description of the design and mechanical performance of the stave is given. Results on the electrical performance obtained using prototype staves are also presented.**

***Index Terms*—Collider Detector at Fermilab (CDF) Run IIb, performance, silicon strip detector, stave design, SVX4.**

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## I. Introduction

THE Collider Detector at Fermilab CDF Run IIb silicon detector (SVXIIb) [1], [2] is designed to be a radiation-tolerant replacement for the current five-layer SVXII [3] and beampipe layer (L00) [4] detectors. The design of SVXIIb is optimized for Higgs and new-particle searches while also being affordable, reliable, and simple to construct and operate. To minimize the development time, the design of SVXIIb makes use of existing technologies and specific CDF infrastructure to the greatest extent possible.

The new detector is divided into two barrels covering a total of about 1.2 m along the beam direction (the CDF luminous region is about 70 cm long), with six active layers (each with full phi coverage) with radii between 2.1 cmand 18 cm from the beam line. Staves fill up layers 1 through 5 for a total of 180 for two barrels, while the innermost layer (layer 0) [5] is constructed of components using smaller sensors and support structures, and follows the design of the previous L00. The layout of SVXIIb is shown in Fig. 1.

A radiation-hard readout chip, called SVX4 [6], [7], has been designed in 0.25 $\mu$m complementary metal-oxide-semiconductor (CMOS) technology, and production quality wafers

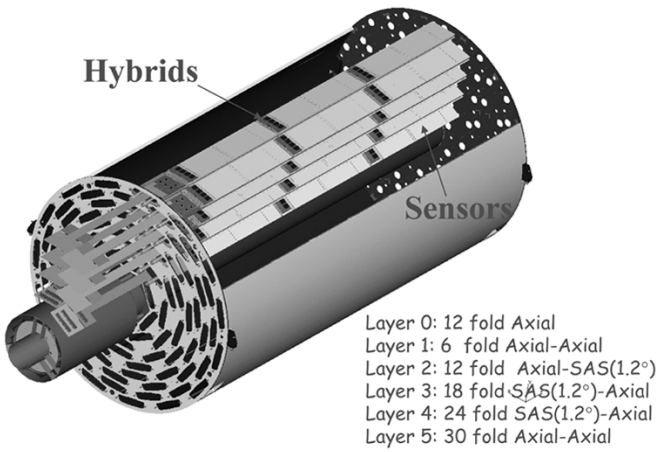


Fig. 1. Three-dimensional layout of one barrel shows population of 90 staves in a SVXIIb barrel volume.

have been fabricated at Taiwan Semiconductor Manufacturing Company (TSMC).

There are only two designs of single-sided silicon microstrip sensors for the outer five layers: axial and stereo. The strips on the stereo sensors are tilted at an angle of 1.2° with respect to the axial direction. The silicon sensors are made at Hamamatsu Photonics (HPK) on P-type $6''$, 320 $\mu$m thick wafers with a strip pitch of 75 $\mu$m for the axial sensors and 80 $\mu$m for the stereo sensors. The sensors are designed for high-voltage operation (up to 1 kV) due to the expected radiation dose. The designs are based upon multiguard concepts developed for use at the large hadron collider (LHC) experiments. The dimensions of the axial sensors are 96.4 mm in length and 40.6 mm in width; the stereo sensors have the same length but their width is 41.1 mm. The bias resistance is typically 1.5 $M\Omega$ with 12 pF of strip capacitance and the initial depletion voltage is in the range of 100–200 V. Studies of sensor performance after irradiation have confirmed stable operation [2] up to $1.4 \times 10^{14}$ neutrons/cm$^2$, a dose equivalent to 30 fb$^{-1}$ of data collected at the Tevatron.

The SVXIIB works in conjunction with two other outer tracking systems. The first, intermediate silicon layers (ISLs) [8], is an existing array of one (two) layers of double-sided silicon at a radius of 22 cm (20–28 cm), between a pseudorapidity $\eta$ of $|\eta| < 1.0 (1 < |\eta| < 2)$. The second is a large cylindrical drift chamber system, central outer tracker (COT) [9], which has an inner radius of 44 cm and an outer radius of 132 cm and covers the pseudorapidity range of $|\eta| < 1.0$. The combination of these three detectors provides excellent track reconstruction efficiency and purity in the very dense track environment expected in high-luminosity operation during Run IIb at the Tevatron.

## II. Stave Design Overview

The new and unique aspect of the stave design is that the active silicon, the power distribution, the data and control lines, and the cooling are integrated with the mechanical support structure. Using the same stave design for over 90% of the detector volume has the advantage of minimizing the number of

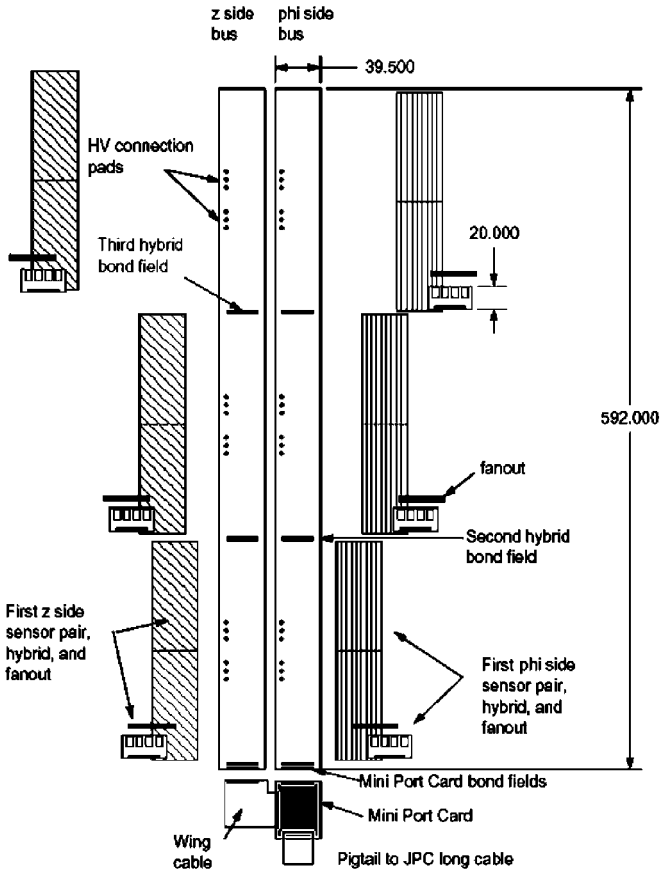


Fig. 2. Components and structure of a stave.

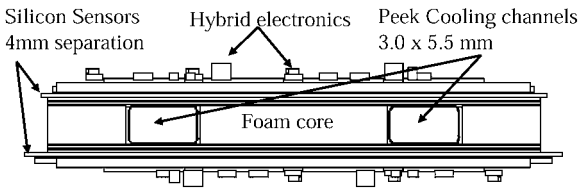


Fig. 3. View of cross-section on stave structure and material.

different components and construction fixtures, and of streamlining the production processes, reducing the construction time and also the design, construction and testing costs.

Fig. 2 shows an exploded view of the stave components. Six axial sensors are mounted on bus cable of one side of stave core and six axial or stereo sensors are mounted on the other side. The innermost and outermost layers are instrumented with staves with axial sensors on both sides, which improve the efficiency and purity of algorithms which associate silicon hits to tracks found in the outer trackers. The three intermediate axial/stereo layers provide three-dimensional track information for vertex reconstruction and standalone tracking (especially important in the forward region where there is no COT coverage).

Each stave has three modules on each side. A module consists of two silicon sensors paired together. Data are read out by a hybrid which is glued on top of one of the sensors, as shown in Fig. 3. A flat bus cable is mounted beneath the sensors on both sides and distributes power, control signals and data. At the end of the stave is a data transmission card called the mini port card (MPC), which serves the entire stave. The phi-side bus cable is

bonded on the MPC substrate directly while the z-side bus cable signals are carried through a flexible cable around the side of the stave to the MPC.

## III. Mechanical Overview of the Stave Design

The total length of a stave is 66 cm. The core of a stave consists of a foam core with a built-in cooling tube and two carbon-fiber composite skins [1] attached to it. Carbon-fiber skins have a high thermal conductivity. The structure is light and rigid. Two copper-on-Kapton bus cables (190 $\mu$m thick), used for data, controls and power distribution, are further laminated on the carbon-fiber skins. The MPC and six silicon modules are precisely glued to the core assembly. Electrical connections are made to the bus cable with wirebonds. A gap of 3 mm between modules and openings in the bus cable shield expose wirebonding pads for connection to the hybrids and to the MPC.

### A. Mechanical Support

The staves are mounted in precise positions using holes and slots in aluminum inserts glued into each end of the stave core. These fit on precisely located pins protruding from the inner and outer bulkheads. With this design, an average angular deviation of the modules with respect to the stave axis of 20 $\mu$rad has been achieved. The total alignment precision within a barrel is expected to be better than 150 $\mu$rad.

The gravitational sag over the total length of the stave is less than 150 $\mu$m, in agreement with a finite element analysis, as shown in Fig. 4(a). The radial deviations within the modules are more important for track reconstruction; the achieved average is 100 $\mu$m.

### B. Stave Cooling

To prolong the lifetime of the detector in the high-radiation environment, the silicon sensors are required to operate at temperatures below room temperature. The innermost layers are expected to receive the largest radiation dose and thus have the lowest temperature specification ($-5$ °C at Layer 1) while the outermost layer could operate up to 15 °C, as the radiation dose scales as $\sim r^{-1.5}$ in the CDF environment [10]. Good thermal coupling between the sensors and the cooling system is important to achieve these values. The expected heat generated by a stave is about 18 W from the 24 SVX4 readout chips, bus-cable resistance, MPC and leakage current assuming a dose equivalent to an integrated luminosity of 30 fb$^{-1}$.

The core of a stave contains a built-in U-shaped cooling tube. The cooling channel is formed using a polyetheretherketone (PEEK) plastic tube with walls 0.1 mm thick, selected for its radiation tolerance. A finite-element thermal model has been developed to study temperature trends on the stave. Assuming a coolant temperature of $-15$ °C[2], the location with the highest temperature on the silicon is underneath the readout hybrid and has a temperature of $-2.9$ °C, as shown in Fig. 4(b). The maximum strip temperature (averaged over the strip volume) is about $-10$ °C on the axial side and $-4$ °C on the stereo side.

[1]Four plies of K13C2U oriented 0/90/90/0 for a total thickness of 250 $\mu$m

[2]43% by weight of ethylene glycol in water.

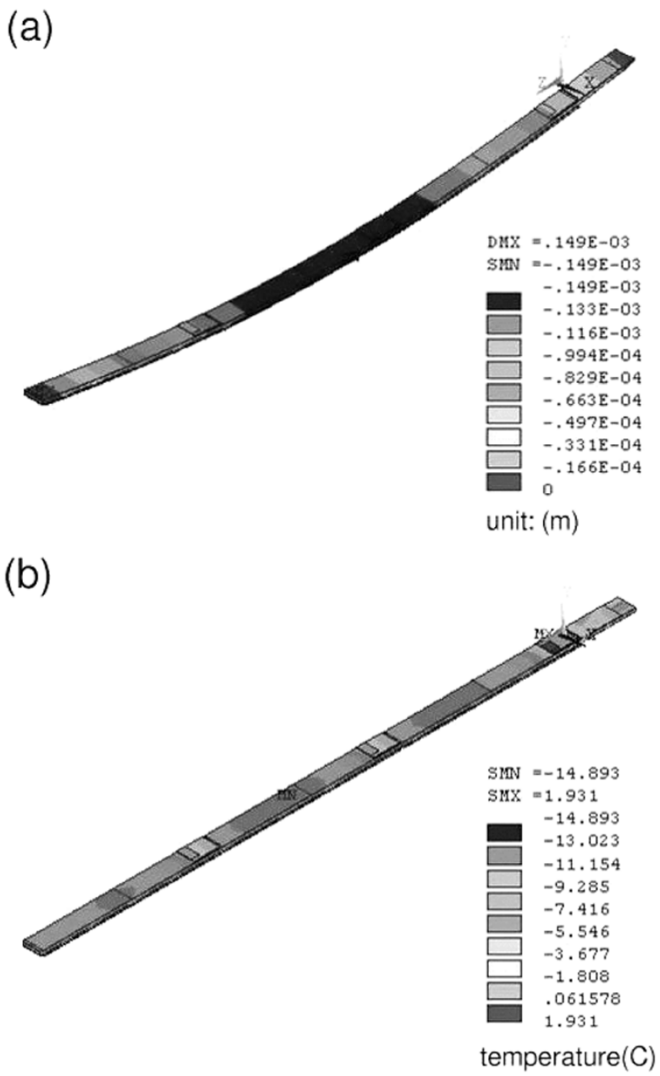


Fig. 4. (a) Finite-element analysis of stave structure under gravity. (b) Stave temperature distribution assuming coolant temperature of $-15$ °C.

The cooling system will be operating below atmospheric pressure in the detector region to avoid leaking coolant into the active volume. A gas system is designed to provide continuously-flowing, cooled, dry nitrogen at a pressure of slightly more than one atmosphere in order to prevent water condensation.

### C. Stave Material

In order to minimize multiple-scattering and nuclear interactions of particles with the stave material, special attention has been given to minimize the amount of stave material. The stave design achieves a total of 1.95% radiation length $(X_0)$ on average for perpendicular tracks. Contributions to the total come from: 37% $(0.0072X_0)$ silicon sensors, 16% $(0.0031X_0)$ hybrids, 16% $(0.0031X_0)$ bus cables, and 31% $(0.0060X_0)$ support structure and cooling. This achievement is especially significant when compared to the SVXII total material, which is approximately the same in spite of the employment of double-sided silicon sensors in SVXII and the higher level of radiation tolerance of SVXIIb. The extra silicon material (from the use of single-sided sensors) and the added cooling capability in

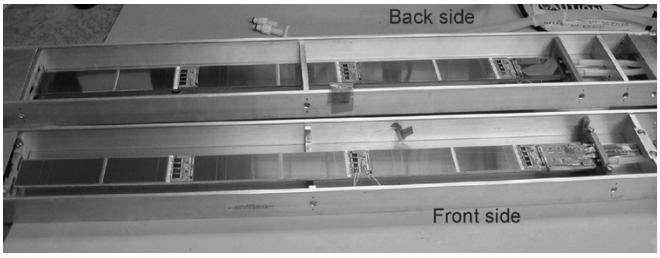


Fig. 5. Picture of two staves, showing both front and back sides.

SVXIIb are compensated by a smaller hybrid, the positioning of the MPC and the service cables and pipes at the end of the stave, outside of the tracking volume.

## IV. Stave Readout Electronics

Each stave constitutes a single readout unit. Data are read serially along the stave starting with the module farthest from the MPC on the axial side and ending with the one closest to the MPC on the opposite side. Fig. 5 shows both front and back sides of staves. The MPC at the end of stave connects bus cables on both sides for power distribution, readout processing and bidirectional data control. An important feature of the readout scheme (common to all CDF silicon readout chips) is the capability to read out only channels above a programmable pedestal value (sparse readout) and optionally their neighbors, considerably reducing the readout time and data size.

In the SVXIIb, data may be acquired and read out simultaneously. This deadtime-less operation presents challenges, since the bus cable runs directly underneath the active sensors and is at all times carrying active control, clock and data signals serving the SVX4 chips and the MPC.

### A. SVX4 Chip

The SVX4 chip is designed and fabricated in a 0.25 $\mu$m CMOS process with custom layout rules for radiation tolerance. It contains 128 parallel charge-integration channels, each with an analog pipeline and an integrated 8-b ADC. The chip is designed to run in a deadtime-less mode: the front-end (analog) part can run in parallel with the back-end (digital) part. For each channel, there are 46 pipeline cells to store the data. The pipeline depth covers the CDF Level 1 trigger latency and allows up to four physics events to be held for later digitization and readout. It is capable to operate with very little deadtime for Level 1 trigger rate up to 50 kHz. The chip operates at +2.5 V. Other important features of the SVX4 chip are [6], [7]:

1) minimum time between triggerable events is 132 ns;
2) chip inputs are optimized for capacitive loads between 10 and 40 pF;
3) preamplifiers may be calibrated on a channel-by-channel basis using a built-in charge injection circuit;
4) there are three modes of channel readout: all channels, channels above a programmable threshold, and channels above threshold with neighbors;
5) programmable shunt circuit allows inputs from individual faulty strips to be disabled, preventing them from saturating the preamp and affecting adjacent strips;
6) common-mode noise is effectively eliminated with a real-time event-by-event pedestal subtraction circuit;
7) equivalent noise charge is about $(400 + 40 * \text{pF})$;
8) dynamic range of the preamplifier is 200 fC.

All of these features have been tested in prototypes and preproduction units and have been found to work perfectly. From an operational point of view, the programmable shunt circuit for each channel, a new feature of the SVX4 chip, is especially important.

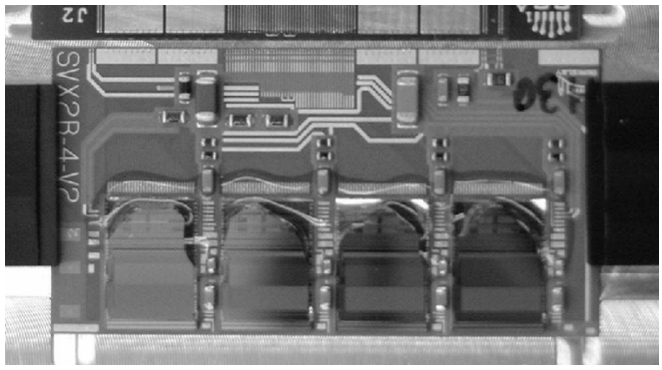


Fig. 6. BeO hybrid carries 4 SVX4 chips. All wirebonds are encapsulated for protection except for the SVX4 chip inputs. Note the presence of the testing PCB on the top of the figure and the multiple wirebonding pads.

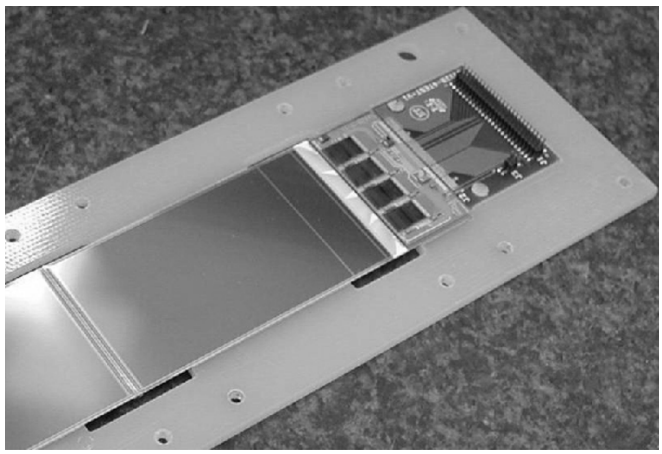

Fig. 7. Picture of module. Two silicon sensors are wire bonded and held by a G10 frame. One side of the sensor is bonded to a pitch adapter which connects to the SVX4 chips on hybrid.

### B. Hybrid

The SVXIIb hybrid used on the stave is a Beryllium Oxide (BeO) substrate circuit board with gold conductors. There is one hybrid design for all staves. Each carries four SVX4 chips. The BeO substrate has the advantages of low mass and good thermal conductivity. By using 100/100 $\mu$m trace/space and 125 $\mu$m via technology, the hybrid size, $38 \times 20 \times 0.38$ $\text{mm}^3$, was reduced considerably with respect to the previous version used in the SVXII. Ceramic pitch adapters are used to match the bond field of the chips to the wider pitch sensors. Hybrids are extensively tested and burned-in before being used on modules. Since there is no readout cable on the hybrid, multiple bondable pads are provided for use with a small PCB for testing purposes (Figs. 6 and 7).

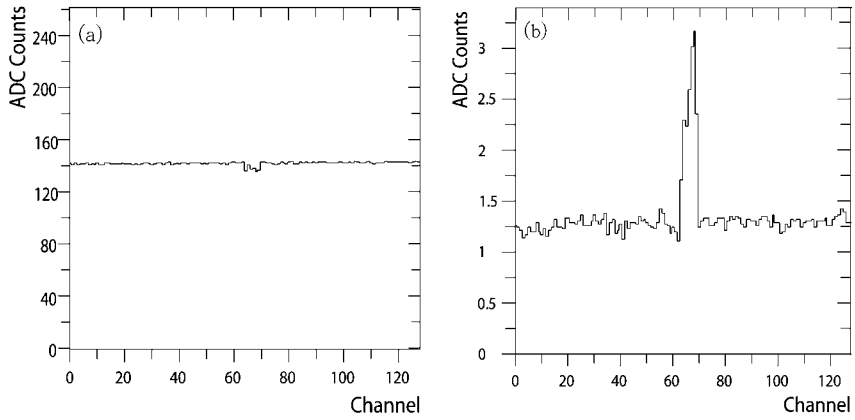


Fig. 8. (a) Pedestal and (b) noise distribution of a single SVX4 chip. Higher noise values for selected channels are due to different capacitive loads.

### C. MPC

The MPC also uses a BeO substrate. There are five transceiver chips and bypassing and termination components mounted on the MPC. The transceiver chip is a custom 0.25 $\mu$m CMOS, radiation-tolerant integrated circuit with separate drivers and receivers. Two flexible cables are used to connect the MPC to the Data Acquisition (DAQ) system, one for data and control signals and one for power. An additional flexible cable is bent around the side of the stave and glued on to the carbon fiber opposite to the MPC. This flexible cable (called the wing) is used to connect MPC with the bus cable on the back side of the stave.

All the communication signals, such as clock and control signals, from the DAQ use the low voltage differential signal (LVDS) standard, while MPC outputs to the DAQ system are pseudo-LVDS. All signals are regenerated at the MPC and sent to the chips on the hybrids. Some signals will be transformed from LVDS to single-ended signals for the chips. Some of the data bus lines are bi-directional, and the differential drivers on the MPC regenerate the signal in both directions.

### D. Bus Cable

The bus cable is a flexible etched laminate of Kapton, copper traces and aluminum foil. The cables are laminated to the carbon fiber surface of the stave. The single-sided silicon sensors are glued on top of the cable. Bus traces are 75 $\mu$m wide with a 100 $\mu$m space between the edges of neighboring traces. Traces are paired if they are used for differential signal transmission. Each pair is separated by a 150 $\mu$m gap. Power and ground traces are wider to reduce the voltage drop.

A 25 $\mu$m thick aluminum shield separates the bus traces from the sensor backplane. This shield is crucial to avoid pickup noise in the sensors. The best ground configuration is found to be a direct low-impedance connection from the shield to the analog ground of the nearest hybrid. The impedance of the bus depends on the geometry and the thicknesses of the Kapton between the bus lines and the carbon fiber below and between the bus lines and the aluminum shield above. The measured value is 75 $\Omega$.

## V. Stave Electrical Testing

All components undergo a thorough testing before installation on a stave. Sensors are individually tested at the manufacturer, HPK, and are retested on a sample basis; SVX4 chips are probed on their wafers before dicing; hybrids are electrically tested and then are burned-in for at least three days before integration into modules. Quality assurance and control on individual components has been considered in the design process to ensure good performance of the final product [11].

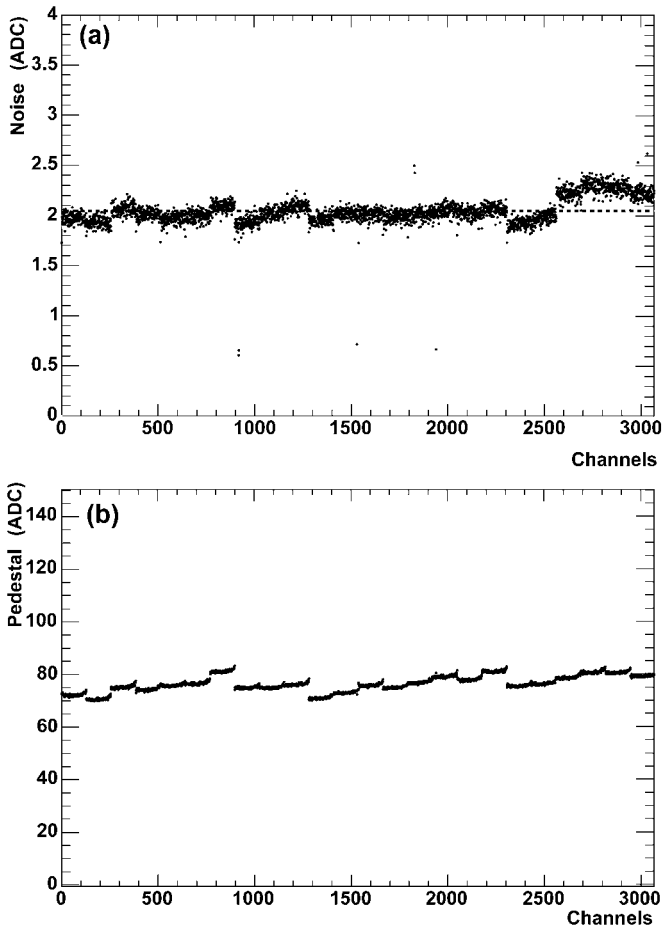


Fig. 9. (a) Noise (dot points) and average dnoise (dashed line) and (b) pedestal distribution for a full stave. A total of 3072 channels are read out. Noise and dnoise coincide (i.e., the common-mode noise is very small) with a value of $\sim$ 1000 electrons.

### A. Chips/Hybrids/Modules Testing

Pedestal, noise, and differential noise (dnoise, i.e., the noise in the difference between the data from two adjacent channels,

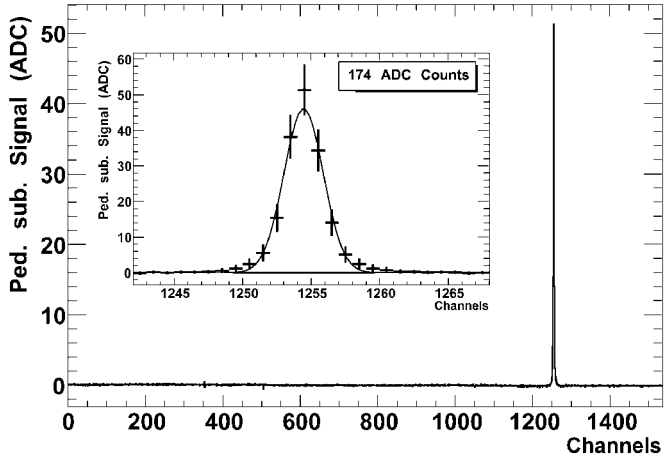


Fig. 10. Pedestal-subtracted laser data. A clear signal is seen around channel 1255, which is in the area illuminated by the laser.

which suppresses common mode contributions) distributions are the primary tools to assess the quality of chips, hybrids and modules. Fig. 8(a) and (b) show the pedestal and noise distributions for a single SVX4 chip, respectively with several different capacitors connected to different input channels. The increased noise with input capacitive load is as expected. Other common testing tools, such as gain scans, bandwidth scans, pipeline-cell noise and pedestal scans, are routinely performed.

### B. Stave Testing

Extensive studies on proper grounding of the bus cable shield, the carbon-fiber support structure, and the sensors' high-voltage reference have been performed before reaching a final configuration on the stave. The best performance is obtained when the sensor high voltage line is referenced to the analog ground connection on the hybrid, when the bus cable shield is broken under each module and connected separately to the same hybrid analog ground directly above, and when the carbon-fiber structure is grounded to the MPC at one end of the stave. Fig. 9(a) shows noise distribution (dot points) and average differential noise (dash line) for a full stave, and Fig. 9(b) shows the pedestal distribution. The noise on the stave is around 1000 electrons and the typical gain for the SVX4 chip is about 500 electrons per ADC count. Deadtime-less performance is a key issue for stave operation at CDF. Studies to date indicate acceptable performance [12].

### C. Laser Run on Stave

The stave performance was also studied using a 1064 nm focused laser signal. The offline pedestal subtracted data, as shown in the Fig. 10, has a clear, clean laser signal covering a few strips.

## VI. Conclusion and Plan

Although the construction of the SVXIIb detector has been recently canceled due to the revised Tevatron luminosity plans, the development phase of the project will proceed to conclusion as silicon sensors, SVX4 chips and hybrids are already available in preproduction quantities. About 15 staves and four L0 modules will be built and installed on a prototype barrel and a L0 carbon fiber support structure, respectively. The L0 support structure will be inserted into the barrel and system testing will be performed using this configuration to demonstrate the feasibility of the SVXIIb design. Final results will be documented and published.

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