CDF Run IIb silicon detector: The innermost layer

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Abstract—The innermost layer (L00) of the Run IIa silicon detector of CDF was planned to be replaced for the high luminosity Tevatron upgrade of Run IIb. This new silicon layer (L0) is designed to be a radiation tolerant replacement for the otherwise very similar L00 from Run IIa. The data are read out via long, fine-pitch, low-mass cables allowing the hybrids with the chips to sit at higher $z(\sim 70 \text{ cm})$, outside of the tracking volume. The design and first results from the prototyping phase are presented. Special focus is placed on the amount and the structure of induced noise as well as signal-to-noise values.

Index Terms—CDF Run IIb, noise, performance, silicon strip detector.

I. INTRODUCTION

THE design of the Run IIb upgrade of the CDF silicon detector [1] consists of six silicon layers. A critical part of the new design is the innermost layer, L0. This layer is essential for successful vertexing, tracking and for the second level displaced track trigger (SVT [2]). To minimize the scattering material in the first measurement layer, L0 follows the design of the Run IIa L00 detector. L0 sits at a radius of 2.1 cm. The main constraints for this innermost layer, close to the interaction region, are radiation hardness and low mass of the device. These lead to the development of a radiation hard readout chip (the SVX4 chip [3]) and to the usage of long, light-weight signal cables. These cables connect the sensors to the hybrids so that the hybrids with the chips and the associated cooling are outside of the tracking volume. A concern with these long cables is noise pick-up, and increased input capacitance, both potentially degrading the system performance. While offline algorithms can correct for the pick-up noise, this is not possible in the online data, feeding the displaced vertex trigger.

Despite the cancellation of the CDF Run IIb silicon upgrade project, an understanding of the performance, especially the noise pick-up, of the innermost layer is important. In view of the observed limitations during operation, as well as physics data taking of the similar L00, and of the planned Run IIb upgrade of the D0 silicon detector with a very similar innermost layer [4], we present the results of the L0 prototype studies in this article.

II. L0 LAYOUT

L0 consists of two mechanically and electrically independent parts that are concentric to the Tevatron beams, one at positive, the other at negative z (the z axis pointing along the beam direction with $z = 0$ cm being the center of the CDF interaction region). A schematic view of the L0 layout is shown in Fig. 1. L0 is a 12-fold symmetric axial layer. The silicon sensors are single sided with a strip pitch of 25 μm. Alternating strips are read out

Fig. 1.   Layout of the innermost layer L0.

Fig. 2.   View of one of the DYCONEX prototype cables taken with a microscope.

resulting in an effective pitch of 50 μm. Sensors are 14.85 mm in width and 78.5 mm in length for a total of 256 readout strips. They are made at HPK [5] and are identical to the L00 sensors used in Run IIa. Two sensors are ganged together and read out by one hybrid, housing two SVX4 readout chips. This assembly is called a module. Modules are mounted on a castellated carbon fiber (CF) structure with an aluminum/Kapton shield laminated to it. The CF structure consists of a ~ 0.5 mm CF skin and is built with a precision of ~ 50 μm. Highly thermally conductive and extra stiff CF was used. The structure will be supported by the outer layers' barrel and is therefore independent of the beampipe it is surrounding. Three modules are glued to the CF structure along z for each of the twelve ϕ segments. The cables from lower-z modules run on top of higher-z modules. The wire bonds of the higher-z module are protected by a small G10 bridge that is glued to the sensors. The length of L0 is six modules plus gaps inbetween for a total coverage of approximately 96 cm. In order to assure radiation hardness, the silicon sensors need to be actively cooled. This is achieved by embedded cooling tubes in the CF structure. The tubes run underneath the entire length of the sensors, cooling them to a temperature below -5 °C.

A. Fine-Pitch Cables

To minimize scattering material in the first measurement layer, the frontend electronics (hybrids and readout chips) and the associated cooling are located just outside of the tracking region ($|z| > 70$ cm) and flare out to slightly larger radii (~ 4 cm) to reduce additional scattering. The hybrids are connected to the sensors via light-weight fine-pitch cables. The longest of the cables is 60-cm long. These cables supply the high voltage and ground to the sensors and send the analog signals from the sensors to the chips.

Two different cable designs were pursued by two different vendors, KEYCOM [6] and DYCONEX [7]. KEYCOM fabricated prototype cables on 50-μm thick Upilex substrate with a trace pitch of 100 μm over most of the length, necking down to 47 μm near both ends for bonding to the sensors and the chips. The achieved trace width is rather wide (~ 35 μm), which leads to a high cable capacitance. The extremely fine pitch at the end of the cables proved difficult to fabricate. One half of each sensor is bonded to a cable which is bonded to a single chip on the hybrid. At the sensor and the hybrid ends, the two cables of one module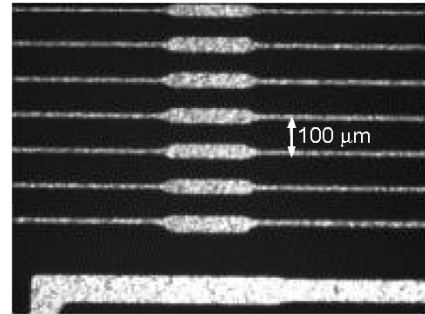 are side-by-side while in the wide sections (100-μm pitch) they are on top of each other. DYCONEX, on the other hand, produced prototype cables with a 100-μm pitch over the full length. Narrow trace widths were achieved (~ 15 μm), leading to low capacitance cables (roughly 25% less than the KEYCOM cables). A zoom-in view of one of the prototype cables is shown in Fig. 2. The two cables of one module are in this case overlapped and staggered by 50 μm with respect to each other, giving an effective 50-μm pitch to match that of the chips and the sensors. Consequently, alternating channels are bonded to the top and bottom cables (all odd channels to one cable and all even channels to the other cable). This bonding scheme is mechanically more challenging, but the coarser pitch proved easier to fabricate.

III. PROTOTYPE PERFORMANCE

Two prototype modules were built, one with a KEYCOM cable and the other with a pair of DYCONEX cables. Both modules were mounted on a prototype CF structure and installed inside an Aluminum box as a means to protect the setup from external light and noise sources. Between the CF and the silicon modules a $\sim 0.5 -$ cm wide Aluminum strip and a $\sim 1.5 -$ cm wide Kapton strip were glued. The two modules were mounted such that the cables of the DYCONEX module run on top of the KEYCOM module. The KEYCOM module has only one cable bonded between sensors and readout chip, while the DYCONEX module has a full set of two cables that are bonded to the silicon and the two readout chips. In order to study the effect of the capacitive load of the sensors and the cables separately, some channels on the DYCONEX module were only bonded to the cable plus one sensor, or to the cable only, without any silicon. DYCONEX cables were chosen for the prototyping phase of this detector upgrade due to their high quality, although they require a more challenging bonding scheme. Therefore, only the performance of the DYCONEX module is studied in greater detail here, while the KEYCOM module is only used to evaluate the influence of another module that is read out simultaneously. For all results shown here, the silicon was biased to $V_{\text{bias}} = 140$ V, which corresponds to the depletion voltage of the sensors.

A. Signal-to-Noise Ratio

As a first test, the signal-to-noise ratio was measured as a function of the preamplifier bandwidth setting of the SVX4 chip. The bandwidth setting (in binary units) is used to adjust the
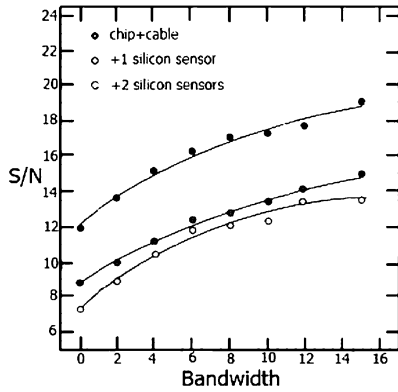
Fig. 3.   Signal-to-noise ratio for the DYCONEX module as a function of bandwidth (or charge integration time) for three different capacitive loads.
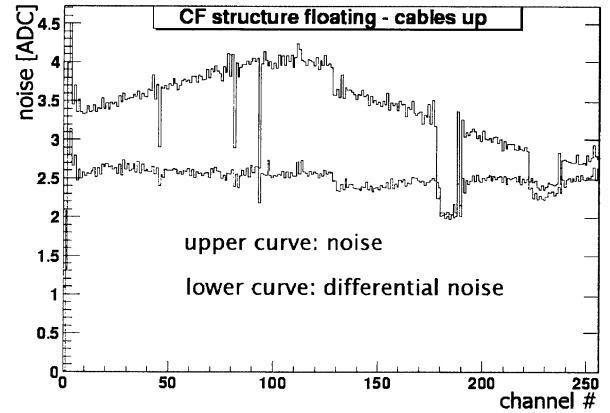

Fig. 4.   (Upper curve) Noise and (lower curve) differential noise are shown versus channel number; the CF structure is floating.

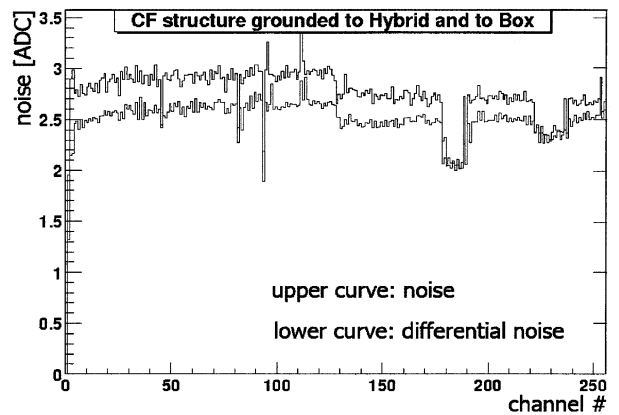Fig. 5.   (Upper curve) Noise and (lower curve) differential noise are shown versus channel number; the CF structure is grounded.

risetime of the preamp in the SVX4 chip by adjusting one of the capacitors attached to the preamp. The signal integration is fast and therefore relatively stable for different bandwidth settings, however, the integrated noise increases if the risetime is fast (corresponding to small bandwidth values). One ADC count corresponds to about 500 electrons in our system, and the signal is about 23 000 electrons. The signal was produced by the means of charge from an external voltage source injected into selected channels, the gain was then measured both in "signal" as well as in "noise" channels as a function of the bandwidth setting in the chip. The result of this study is shown in Fig. 3 for three different capacitive loads to the input channel of the readout chip: only the cable is bonded to the chip (upper curve), the cable plus one silicon sensor are bonded (center curve), and the cable plus both sensors are connected (lower curve). The qualitative result is as expected and as seen from the outer layers' measurements, that use the same readout chip [8], the signal-to-noise ratio increases monotonously with bandwidth and decreases with a larger capacitive load. Despite the long cable length (59.5 cm) a signal-to-noise of about 13 can still be reached, which is found to allow for quality physics data taking. A conservative limit of the life span of this device can be drawn from studies of radiation damage in the Run IIa detector, which indicate that the signal-to-noise in the innermost layer L00 will be reduced to about 6 after 8 fb^{-1}. Note, that we estimate the silicon trigger to work efficiently down to signal-to-noise values of 8 and the b-tagging algorithm to be efficient down to 6.

B. Noise Pick-Up

Of special importance is the study of the noise behavior of the L0 modules. The long cables could act as an antenna. Running on top of adjacent modules, both the silicon as well as the cables, they could pick up environmental noise. As long as this extra noise is uniform across a chip, it can be subtracted at run time by the real time pedestal subtraction (RTPS) feature of the SVX4 chip. In the currently installed Run IIa L00 detector, a nonuniform pick-up noise is observed, where higher noise is seen toward the edges of individual chips. The nature of this pick-up noise was studied and will be discussed briefly in Section IV. In this section, the noise behavior of the L0 prototypes is presented.

In Fig. 4, the noise and differential noise (i.e., common-mode subtracted noise) versus channel number are shown for the DY-

CONEX module. The difference between the two is a measure of the excess noise in the system. In this case, the CF structure was left floating. As expected, nonuniform excess noise can be seen, with larger noise toward the center of the module, where the floating Aluminum strip is located. The channels with IDs around 180 are only connected to the readout cables and no silicon, while the channels with IDs around 230 are connected to the cables plus one silicon sensor. All other channels have the full load of cables and both sensors. Since no significant excess noise is measured in the partially connected channels, we can conclude that the noise pick-up takes place over the full length of the silicon sensors.

Fig. 5 shows a similar plot with the CF grounded, via the Aluminum strip, to both the Aluminum box and the analog ground on the hybrid of the DYCONEX module. The amount of excess noise is largely reduced and is nearly uniform across the module.

Fig. 6 shows a plot with the same configuration as in Fig. 5 but with the RTPS feature activated, which subtracts event-by-event a pedestal offset. The excess noise is reduced (especially for the second chip, channels 128 to 255), but there is still small excess noise visible toward the edges of the first chip (channels 0 to 127). The amount of this noise is small and tolerable.

In addition to these grounding studies, we also varied the proximity of the cables to the walls of the Aluminum box, to the carbon fiber structure and to each other, and varied the shielding
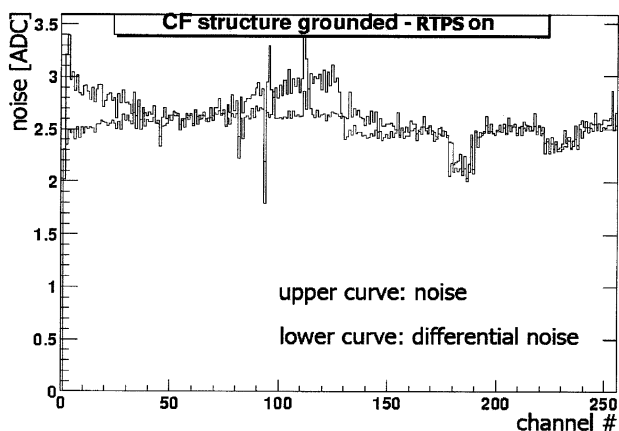
Fig. 6. (Upper curve) Noise and (lower curve) differential noise are shown versus channel number; the CF structure is well grounded and RTPS is activated.

of the assembly by shielding the cables from each other, or from the Aluminum box. We see a clear dependence of excess noise on the chosen configuration of the assembly.

Since we failed to account for these effects in the current L00 detector, resulting in operational obstacles, we want to stress the obvious, namely that special care needs to be taken when dressing the final device. The state of the KEYCOM module, whether it was powered up and reading out or not during data taking of the DYCONEX module, did not have any effect on the performance of the DYCONEX module itself, nor on the value and shape of the excess noise in any of the configurations we tested. This leads us to the conclusion that, in the CDF detector, the source of the noise which is subsequently picked up by the carbon fiber structure and/or the long signal cables, is not the neighboring modules, but outside components, like the outer silicon layers, the silicon detector readout electronics, or even nonsilicon detector components in the environment.

IV. COMPARISON WITH L00 STUDIES

In the currently installed Run IIa L00 detector [9] a nonuniform pick-up noise is observed, where large excess noise is seen toward the edges of individual chips. For this reason, all channels of this layer have to be read out as opposed to the sparsification that is used for the outer layers. This leads to a large data volume and a long readout time. Furthermore, L00 can not currently be included in the second level silicon trigger that finds displaced tracks. This nonuniform noise is subtracted offline by fitting Chebychev polynomials to the raw data of every single chip in every event, thus making L00 data available for offline analyzes. The nature and origin of this pick-up noise was studied with a spare module on the bench.

In Fig. 7, the noise and differential noise are shown versus channel number for this L00 test module. The nonuniform excess noise, that can be seen especially on the first chip, was induced by placing a wire underneath sensors, cables and the hybrid. The wire was connected to a waveform generator. As a comparison, data from the same module are shown in Fig. 8, but shielded from the wire by an Aluminum foil. In this case, no difference between noise and differential noise and therefore no excess noise is observed. The overall higher noise and even differential noise levels compared to the Run IIb L0 device is
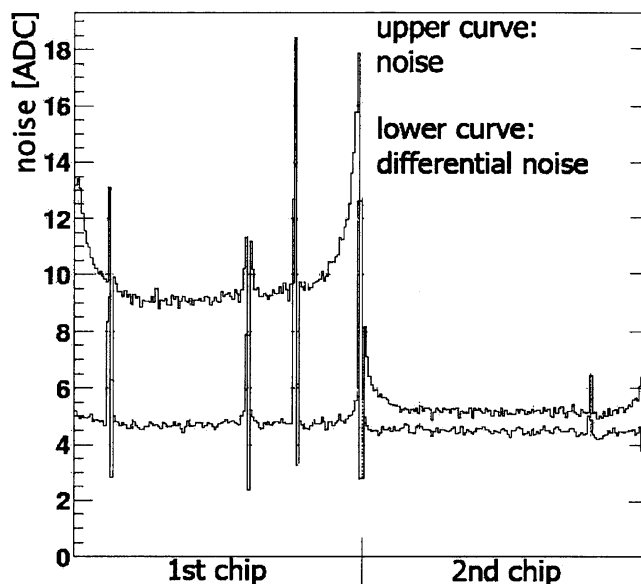

Fig. 7. (Upper curve) Noise and (lower curve) differential noise are shown versus channel number; a wire was introduced as an external noise source; no shielding of the device from the noise source was attempted.
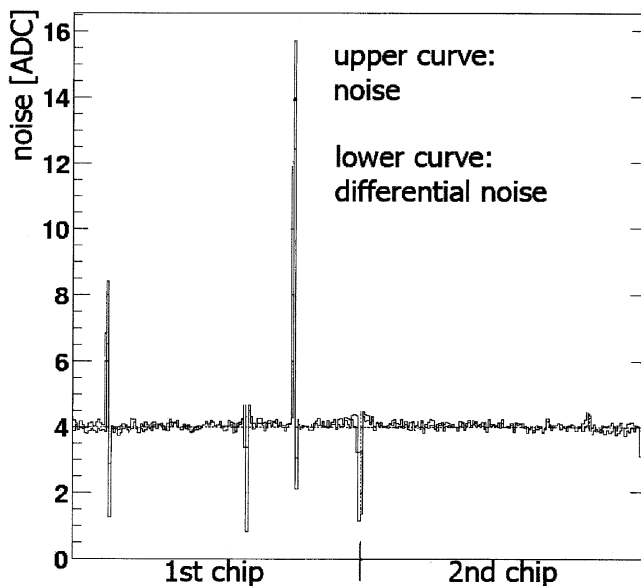

Fig. 8. (Upper curve) Noise and (lower curve) differential noise are shown versus channel number; a wire was introduced as an external noise source; the device was shielded from the noise.

due to less noisy readout chips and cables in Run IIb compared to the components used in Run IIa.

The dependence of the noise on the frequency of the injected signal from the waveform generator was studied. Between 0 and 500 kHz, no large noise contributions were observed, but between 1 and 2.5 MHz, a significant increase in excess noise was seen. However, the noise showed the same shape across individual chips for all frequencies. As a reference, the frequency used in Figs. 7 and 8 was 2.4 MHz. Finally, moving the wire from below the module to the top, the behavior of the two chips flips, i.e., the second chip shows a higher noise, as expected.

In summary, the observed nonuniform excess noise in the Run IIa L00 detector can be reproduced on the bench using a spare

module, when introducing an external noise source. No excess noise is detected when shielding the assembly from the environment.

V. CONCLUSION

First, prototypes of the innermost layer of the CDF Run IIb silicon upgrade were tested on a prototype carbon fiber structure. The achieved signal-to-noise values are as designed and are comparable to the outer layers' results. A study of nonuniform noise as well as grounding and shielding issues was performed. The results were similar to those from a previous study using a Run IIa L00 module. From these tests, we conclude that the new innermost layer of CDF would work as designed in the CDF environment, provided that special care for grounding and shielding of the device, both internally and externally, is taken.

Furthermore, we hope that these studies provide useful for similar detectors built elsewhere in the future.

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