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Cell Capacitor Sizing in Multilevel Converters: Cases of the MMC and AAC

Michaël M. C. Merlin, Tim C. Green

Abstract

Multilevel converters, such as the Modular Multilevel Converter (MMC) or the Alternate Arm Converter (AAC), rely on charged capacitors in their cells to generate their AC voltage waveform. Since the cell capacitors are physically large and occupy approximately half the cell volume, their capacitance must be kept minimal while limiting the voltage fluctuation caused by the current passing periodically through these capacitors. This paper proposes a mathematical model which estimates the energy deviation for the stacks of both the MMC and the AAC during steady-state operation under any power factor and for AC voltage magnitude fluctuation of up to $\pm 10\%$. The analysis is then used to calculate the minimum size for the cell capacitors in order to keep their voltage fluctuation within set boundaries for both topologies. The results show that the MMC requires 39 kJ/MVA of capacitive energy storage under sinusoidal modulation but this reduces with triplen injection modulation. The AAC has a lower requirement for storage in its cells of 11 kJ/MVA but the AAC has a 6-pulse DC current ripple which requires a filter estimated to have a further 33% capacitive storage.

Index Terms

AC-DC power converters, HVDC transmission, HVDC converters, Capacitors, Energy storage.

I. INTRODUCTION

Multilevel converters such as the Modular Multilevel Converter (MMC) [1], [2] represent a new generation of Voltage Source Converter (VSC) as they have brought significant improvements over the classic 2- or 3-level VSC [3], [4] such as the Neutral Point Clamped converter (NPC). Thanks to their large number of voltage levels, these multilevel converters are able to generate staircase voltage waveform with relatively small steps. The voltage waveform across the AC reactor is thus improved and its current becomes much less distorted. The gain is twofold [5]: (i) bulky AC filters are no longer required, thus reducing the footprint of the converter station, and (ii) the IGBTs in the converter can be operated close to the fundamental frequency without compromising the quality of the current waveform, thus increasing significantly the power efficiency of the converter.

Another promising multilevel converter topology is the Alternate Arm Converter (AAC) [6]–[8], shown in Fig. 2. This topology utilises alternatively its arms to generate its voltage waveform and conduct the AC current. This

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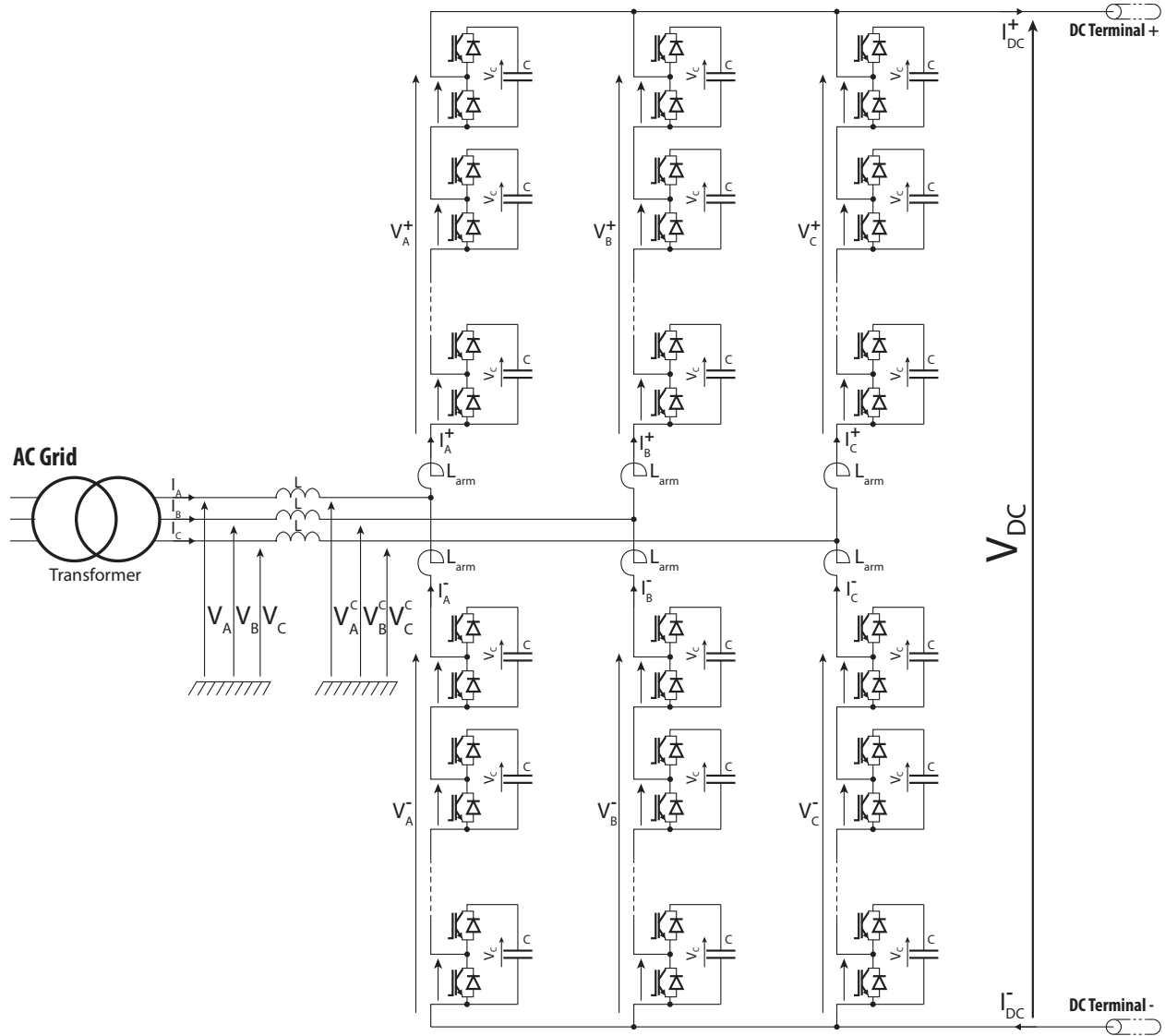


Fig. 1: Schematic of the half-bridge MMC.

mechanism allows the AAC to reduce the number cells in its stacks by almost a factor two while keeping both the low current distortion characteristic and the high power efficiency of the half-bridge MMC. Besides, the AAC is capable of blocking the flow of current from the AC-side to the DC-side during a DC-side fault thanks to its stacks of full bridge cells and can even be operated as a STATCOM [9] during an outage of the DC bus. A reduced dynamic model of the AAC is presented in [10]. The AAC has also been used in DC-DC converter arrangements [11], [12] and it has been shown [13] that the AAC exhibits better thermal balance between its IGBT modules than the MMC. However, the AAC works best when operated at its sweet-spot which corresponds to an operating point where complete energy exchange is achieved between the AC and the DC grids and is defined by a linear relationship between their respective voltage magnitudes as stated in (1).

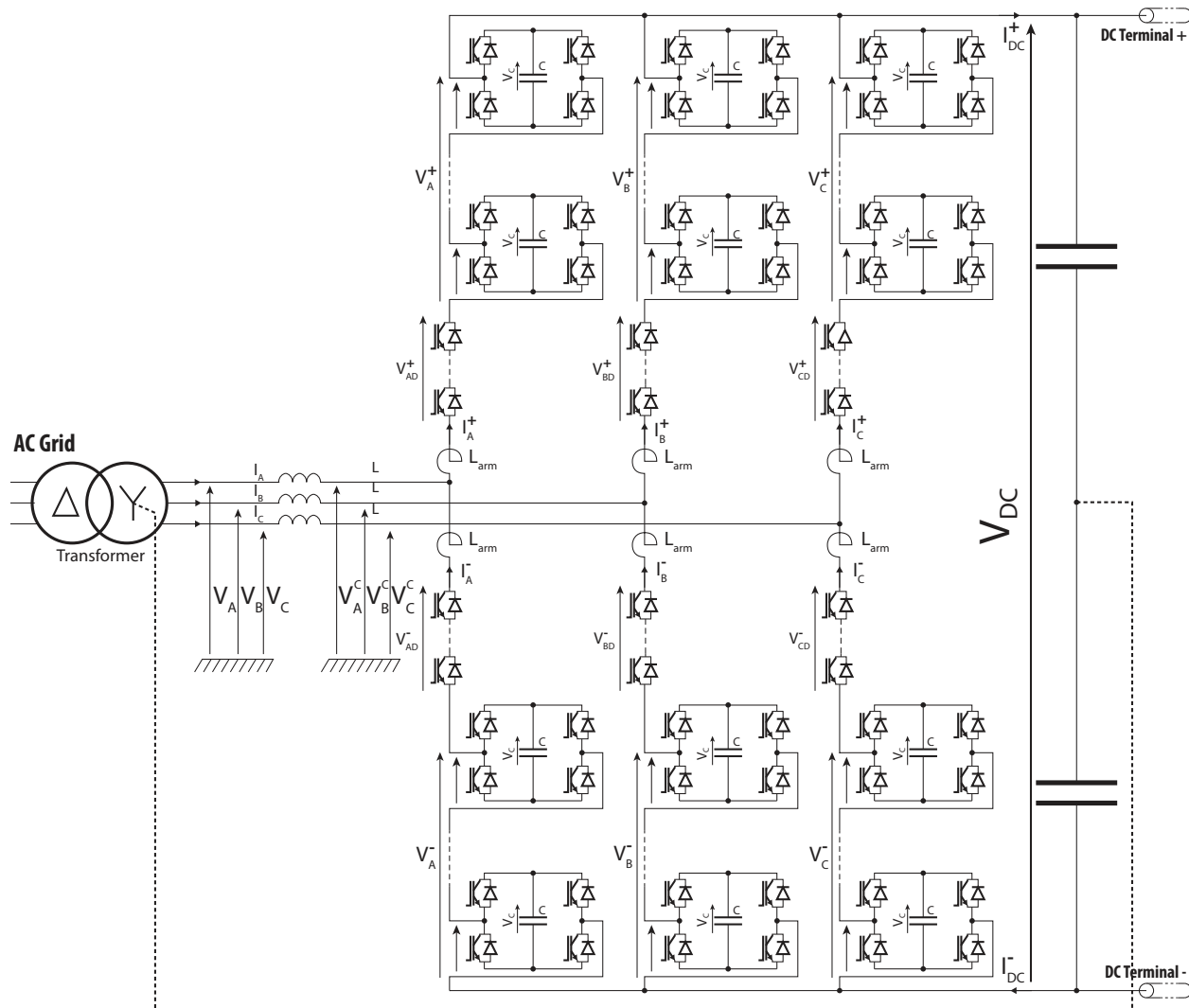


Fig. 2: Schematic of the AAC.

$$\hat{V}_{AC_{nom}} = \frac{2}{\pi} V_{DC} \quad (1)$$

In most of the recently proposed multilevel topologies [2], [6]–[8], [11], [12], [14], [15], stacks of H-bridge cells are used and these cells contain charged capacitors which can be connected in or out of the conduction path in order to generate a controllable voltage across the whole stack. These cells are generally of the half-bridge or full bridge types and this choice defines the number semiconductor devices in the conduction path and the ability or not to generate a negative voltage from the charged capacitor. Some cell variants exist, such as the Double Clamped Submodule (DCS) [16], which offer compromises between power losses, device count and negative voltage generation capability. The modularity of these stacks is also a strong advantage because additional modules can be included [17] in order to increase the reliability of the whole converter without affecting significantly its

performance.

Regardless of the cell type used in the stacks, the cell capacitors have to remain charged around their reference value in order to ensure proper operation of the converter. Overcharging these capacitors means risking their failure [18] or accelerated fatigue with cascading effects on the all other components. In the opposite condition, running them undercharged reduces the maximum voltage capability of the stack leading potentially to the instability of the whole converter due to loss of control of the arm currents. Each converter topology has its own specific energy balancing mechanism to ensure that the average energy in their stacks is kept constant over each cycle, as described in [14], [19] for the MMC and [6], [8] and the AAC.

Such high voltage capacitors are often of the film technology or gas-impregnated [18], [20] as this technology has the advantage of being energy-dense, having low ESR values, the ability to withstand high voltage and current peaks and are generally considered reliable over the lifetime of an HVDC station. However, even after the average energy management of the stacks has been appropriately managed, the fact remains that these cell capacitors are connected in to the current path during each cycle and inevitably see their voltage fluctuating around their reference value with a magnitude defined by the size of the capacitors. The bigger the capacitors, the smaller their voltage deviation but, at the same time, the stacks become larger in volume and cost with little to no improvement on the overall performance of the converter. Voltage and energy deviation of the cell capacitors has already been analysed in [1], [21]–[26], specifically for the MMC. Methods consisting of adding harmonic circulating currents have also been suggested in [27], [28] in order to reduce the cell capacitor voltage deviation but at the expense of both high conduction and switching losses. A thorough study of the energy requirements of the MMC has recently been published in [26] where triplen harmonic voltage injection was used. The results of this study show that the MMC with such triplen harmonic voltage injection requires a minimum of 21 kJ/MVA of total energy storage to operate under normal conditions. This paper addresses the issue of finding the minimum size of these capacitors for two multilevel converter topologies, namely the MMC and the AAC. This minimal size is set such that the average voltage of these cell capacitors does not exceed a defined fluctuation boundary under operation at any power factor and for normal tolerance of the AC voltage magnitude about its nominal value.

II. FRAMEWORK OF THE STUDY

This study finds the bare minimum size of cell capacitors to meet the desired maximum voltage deviation and do not take into account any additional margin that a manufacturer may incorporate to meet some situations, such as transients, faults, component degradation or redundancy. Therefore, this paper establishes the base case limits for steady-state as it is considered to be a useful step in comparing types of modular VSC. In [26], the energy requirement for the MMC using triplen harmonic injection is calculated as energy per power rating units (e.g. kJ/MVA) and the cell capacitors are obtained consequently to the resulting total energy storage required in the stacks.

A. Assumptions of the model

In order to achieve simplicity in the results of this study without compromising accuracy, a number of assumptions have been used in the mathematical model of the studied topologies. First, only the theoretical voltage and current waveforms during steady state operation are considered. This implies that the voltage of the stacks does not present the staircase shape which is characteristic of the multilevel converters but is rather assumed to be smooth and as close as possible to its ideal waveform.

Second, the energy stored in the various inductors of these converters is neglected. Indeed, in transmission applications, these components are usually sized small (e.g. 0.1 pu) and their stored energy is negligible compared to the energy stored in the cell capacitors, e.g. often between 1 and 3 orders of magnitude smaller. Therefore their inclusion would have a marginal affect on the final numerical figures but a complex influence on the mathematical model developed in this study.

Third, the mathematical model developed for this study assumes that the duty of the cells is perfectly distributed between them, meaning that all the cell capacitors in a stack present the same voltage. Voltage deviation between the cell capacitors is not discussed in this study and is the topic of cell rotation or modulation algorithms, discussed elsewhere [21], [29].

Fourth, the stacks of cells analysed under the load convention: a positive power denotes power going into the stacks, hence its energy will be positive and the cell capacitors will exhibit higher voltage magnitudes, and vice-versa.

B. Cell Capacitor Voltage and Stack Energy Deviations

Despite being primarily interested in the cell voltage deviation, the switching pattern of the individual cells makes it difficult to predict their voltage fluctuation. However, by looking at the total energy stored in the stack, a model can be constructed and studied. Equation (2) defines how to move from the energy to the voltage, using N_{cell} as the number of cells per stack, C_{cell} as the capacitance of a cell capacitor and $V_{cell}(t)$ as the real-time average value of the cell voltages in a stack.

$$E_{stack}(t) = N_{cell} \frac{C_{cell}}{2} V_{cell}^2(t) \quad (2)$$

In the following equations, ΔV represents the maximum relative voltage deviation in p.u. (e.g. 0.2) around the nominal cell voltage $V_{cell,nominal}$ when a stack reaches respectively its maximum energy deviation $\Delta \hat{E}_{stack}$ (3a) and its minimum energy deviation $\Delta \check{E}_{stack}$ (3b) from its initial energy state $E_{stack}(0)$ defined at the beginning of each fundamental cycle.

$$N_{cell} \frac{C_{cell}}{2} (V_{cell,nominal} (1 + \Delta V))^2 = E_{stack}(0) + \Delta \hat{E}_{stack} \quad (3a)$$

$$N_{cell} \frac{C_{cell}}{2} (V_{cell,nominal} (1 - \Delta V))^2 = E_{stack}(0) + \Delta \check{E}_{stack} \quad (3b)$$

Equations (3a) and (3b) have been defined such that the maximum voltage deviation of the cells has a value opposite to their minimum voltage deviation, thus centered around the nominal cell voltage value. This method ensures that the capacitors are sized to manage equally both the maximum and minimum voltage deviation and assumes that the energy controller of the converter moves the initial energy state of the stacks in reference to (4a), formed by dividing (3a) and (3b), yielding the optimal value for E_0 in (4b).

$$0 = \frac{E_{stack}(0) + \Delta\hat{E}_{stack}}{(1 + \Delta V)^2} - \frac{E_{stack}(0) + \Delta\check{E}_{stack}}{(1 - \Delta V)^2} \quad (4a)$$

$$E_{stack}(0) = \frac{-\Delta\check{E}_{stack} (1 + \Delta V)^2 + \Delta\hat{E}_{stack} (1 - \Delta V)^2}{4 \Delta V} \quad (4b)$$

The peak to peak energy deviation is defined by the difference between the maximum and the minimum energy deviations, as stated in (5a), and becomes an important factor when combining (4b) into (3a) in order to obtain the nominal amount of energy storage per stack (5b) similarly as in [1]. From this quantity, the minimal cell capacitance can be extracted, as shown in (5c).

$$\Delta E_{stack} = \Delta\hat{E}_{stack} - \Delta\check{E}_{stack} \quad (5a)$$

$$E_{stack_{nominal}} = \frac{\Delta E_{stack}}{4 \Delta V} \quad (5b)$$

$$C_{cell} = \frac{\Delta E_{stack}}{2 N_{cell} V_{cell_{nominal}}^2 \Delta V} \quad (5c)$$

III. STACK ENERGY DEVIATION

Equation (5c) shows that the size of the cell capacitors should be chosen proportionally to the peak to peak energy deviation. This section details how to quantify this characteristic for both the MMC and the AAC, under different operating conditions. In all the equations below, the AC grid voltage and current functions are defined as in (6a) and (6b) respectively.

$$V_{AC}(t) = k_{AC} \hat{V}_{AC_{nom}} \sin(\omega t) \quad (6a)$$

$$I_{AC}(t) = \frac{\hat{I}_{AC}}{k_{AC}} \sin(\omega t + \phi) \quad (6b)$$

The angle ϕ specifies the angle difference between the voltage and the current and will be used throughout this paper to describe the energy deviation as a function of the relative amount of active and reactive power. The parameter k_{AC} represents the variation of the AC grid voltage magnitude under normal conditions. In this study, this parameter will vary between 0.9 and 1.1 in order to represent a $\pm 10\%$ variation as this is usually the requirements set by network operators [30], [31]. The design of the converters will also reflect this voltage magnitude fluctuation as they have to cope with the additional voltage requirement that this AC voltage variation may imply. Besides, the

apparent power of a converter is given by (7a) and the active power by (7b) used to express the DC current I_{DC} as a function of the voltage and current quantities in (7c).

$$|\overline{S}| = 3 \frac{\hat{V}_{ACnom} \hat{I}_{AC}}{2} \quad (7a)$$

$$P = 3 \frac{\hat{V}_{ACnom} \hat{I}_{AC}}{2} \cos(\phi) = V_{DC} I_{DC} \quad (7b)$$

$$I_{DC} = \frac{3 \hat{V}_{ACnom} \hat{I}_{AC}}{2 V_{DC}} \cos(\phi) \quad (7c)$$

A. Case of the MMC

The MMC is the first multilevel VSC to achieve a high number of voltage levels without any compromise on the complexity of its topology and has thus a truly modular structure, as illustrated in Fig.1. The cells are usually of the half-bridge type in order to minimize the power losses. This also implies that the MMC can only under-modulate, i.e. $k_{AC} \hat{V}_{ACnom} \leq \frac{V_{DC}}{2}$, otherwise it would force the stacks to generate negative voltage during part of the cycle. This leads to (8) which specifies the nominal AC voltage magnitude as a function of the DC voltage magnitude and the maximum AC voltage variation \hat{k}_{AC} . Typically, as in this paper, the variable \hat{k}_{AC} is set to 1.1 if a $\pm 10\%$ variation of the AC voltage magnitude is needed.

$$\hat{V}_{ACnom} = \frac{1}{\hat{k}_{AC}} \frac{V_{DC}}{2} \quad (8)$$

The stacks of cells need to be able to generate a voltage from 0 up to V_{DC} , resulting in the number of cells per stack being defined as in (9).

$$N_{cellMMC} = \frac{V_{DC}}{V_{cellnominal}} \quad (9)$$

In the MMC, the AC current is split evenly between the top and bottom arms while an equal share of the DC current runs through each leg converter. In many studies [32]–[35], additional circulating currents have been reported, mainly consisting of second harmonic currents. This issue can be fixed by including harmonic suppressing functions in the controller of the MMC as presented in [35]. This study assumes that the controller has been designed according to such design criteria and thus no harmonic current is circulating in the arms. The power exchanged with the top stack can be thus written as in (10).

$$P_{Stack}^+(t) = V^+(t) (-I^+(t)) \quad (10a)$$

$$\begin{aligned} &= - \left(\frac{V_{DC}}{2} - V_{AC}(t) \right) \left(\frac{I_{AC}(t)}{2} + \frac{I_{DC}}{3} \right) \\ &= -\hat{V}_{ACnom} \hat{I}_{AC} \left(\hat{k}_{AC} - k_{AC} \sin(\omega t) \right) \left(\frac{\sin(\omega t + \phi)}{2 k_{AC}} + \frac{\cos(\phi)}{4 \hat{k}_{AC}} \right) \\ &= \frac{|\overline{S}|}{3} \frac{\hat{k}_{AC}}{2 k_{AC}} \left(\frac{k_{AC}}{\hat{k}_{AC}} \sin(\omega t) - 1 \right) \left(\frac{k_{AC}}{\hat{k}_{AC}} \cos(\phi) + 2 \sin(\omega t + \phi) \right) \end{aligned} \quad (10b)$$

From the power equation (10b), the energy deviation of the positive arm can be derived (11).

$$\Delta E_{Stack}^+(t) = \int_0^t P_{Stack}^+(x) dx \quad (11a)$$

$$= \frac{|\bar{S}|}{3\omega} \frac{\hat{k}_{AC}}{4\hat{k}_{AC}} \left(- \left(\frac{k_{AC}}{\hat{k}_{AC}} \right)^2 \cos(\omega t - \phi) - \cos(\omega t + \phi) \dots \right. \\ \left. \left(\left(\frac{k_{AC}}{\hat{k}_{AC}} \right)^2 + 2 \frac{k_{AC}}{\hat{k}_{AC}} \sin(\omega t) - 4 \right) + 2 \left(\left(\frac{k_{AC}}{\hat{k}_{AC}} \right)^2 - 2 \right) \cos(\phi) \right) \quad (11b)$$

The power of the negative arm can be found by changing some signs in (10) and this yields (12a), which is a time-mirrored version of (10a). This shows that the power functions for the upper and lower arms are similar under all operating points.

$$P_{Stack}^-(t) = V^-(t) (-I^-(t)) \quad (12a)$$

$$= \left(\frac{V_{DC}}{2} + V_{AC}(t) \right) \left(-\frac{I_{AC}(t)}{2} + \frac{I_{DC}}{3} \right) \\ = \left(\frac{V_{DC}}{2} - V_{AC}(-t) \right) \left(\frac{I_{AC}(-t)}{2} + \frac{I_{DC}}{3} \right) \\ = V^+(-t) (-I^+(-t))$$

$$P_{Stack}^-(t) = P_{Stack}^+(-t) \quad (12b)$$

When (12b) is integrated in order to find the energy deviation of the negative arm, the resulting equation (13b) is both the sign-opposite and time-reversed version of the energy deviation (11b).

$$\Delta E_{Stack}^-(t) = \int_0^t P_{Stack}^-(x) dx \quad (13a)$$

$$= \int_0^t P_{Stack}^+(-x) dx \\ = - \int_0^{-t} P_{Stack}^+(y) dy$$

$$\Delta E_{Stack}^-(t) = -\Delta E_{Stack}^+(-t) \quad (13b)$$

Since this study focuses on the peak to peak energy deviation of the arms within a cycle, these sign differences will not influence the results and only the equations from the positive arm will be considered. Figure 3 shows the energy deviation within a cycle of an MMC arm under different operating conditions. The graph shows that the energy deviation is indeed influenced by the AC voltage magnitude but essentially keeps the same shape but a different magnitude.

B. Case of the AAC

The AAC is an hybrid VSC between the MMC and the two-level converter. As the MMC, it uses its stacks of cells to generate staircase voltage waveforms but also uses its arms alternately to conduct the AC current, similarly to

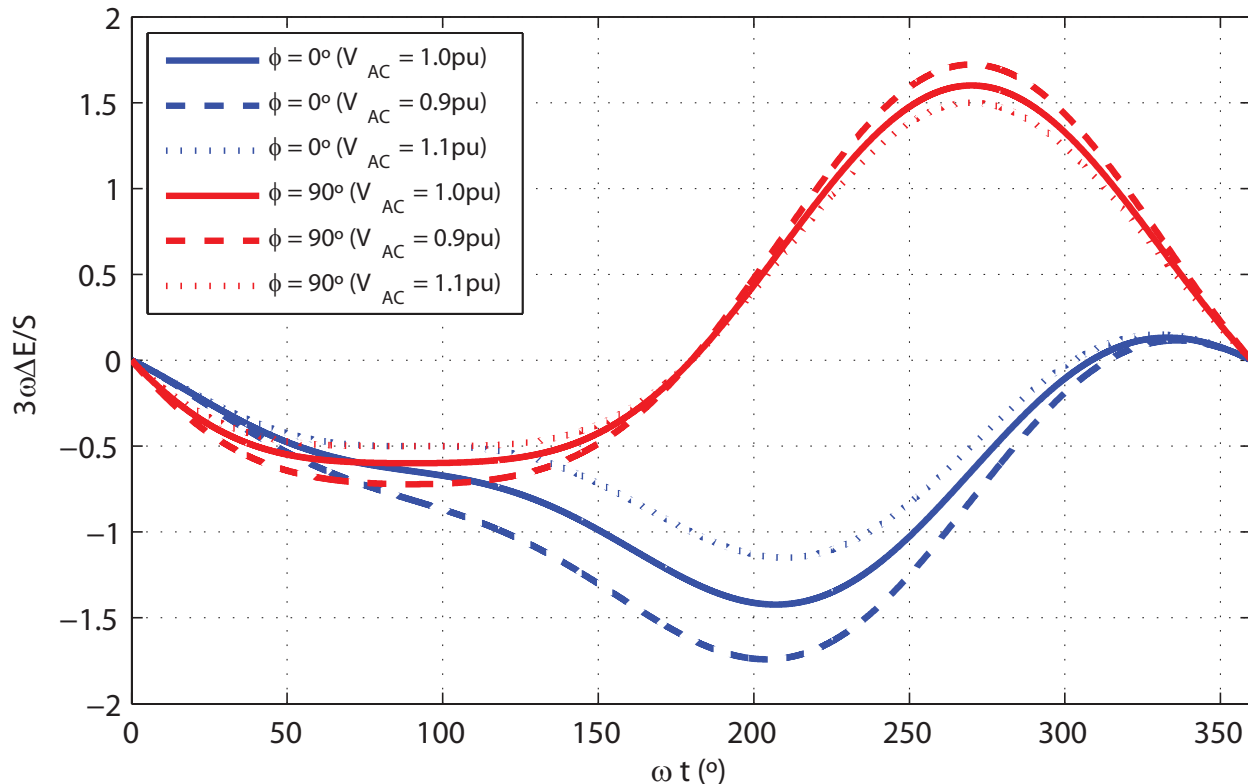


Fig. 3: Energy deviation of the positive arm of an MMC for real power only (blue) and reactive power only (red) operation.

the 2-level converter. However, in contrast to the MMC, the AAC generates a DC current waveform with a 6-pulse ripple, inherent to the direct rectification of the 3-phase AC current. This fact implies that some DC filtering might be required depending on the requirements set by the DC network operator and this filter may include significant capacitance. This study focuses on the cell capacitors and will provide any sizing figures for the DC bus capacitor in the final results. Furthermore, it is assumed that the operating method consists of using the top arm only to construct the positive part of the converter voltage waveform and vice versa with the bottom arm. The consequences of this method are twofold. First, the maximum voltage of the stacks is reduced. Series-connected IGBTs, called director switches, are used to isolate the arm which is not conducting and provide the difference in voltage between the maximum stack voltage and the converter AC voltage.

Second, the DC current is obtained directly by rectification of the AC current which creates a dependency in energy between the AC and DC sides. The study of the AAC in [6], [8] has shown that there is a single operating point, called sweet-spot which allows all the energy coming from one side to pass to the other side without any energy left in the stacks. The sweet-spot is defined by a linear relationship between the AC peak voltage and the DC bus voltage as expressed in (1). However, the AC voltage magnitude may fluctuate around its nominal value, thus the AC voltage needs to vary and is defined by (14).

$$\hat{V}_{AC_{nom}} = \frac{2}{\pi} V_{DC} = \frac{4}{\pi} V_{DC_{terminal}} \quad (14)$$

The sweet-spot defines a nominal AC voltage magnitude higher than the DC terminal voltage ($V_{DC_{terminal}} = \frac{V_{DC}}{2}$), which implies that the AAC needs to over-modulate to operate correctly. When the AAC is operated away from its sweet spot, a fraction of the energy transferred through the converter is in fact left inside the stacks, leading to a steady drift in their energy levels. Operation away from the sweet spot is still possible, thanks to the existence of the overlap periods (twice per cycle) happening during the handover from one arm at the end of its working period to the other arm at the beginning of its own working period. These periods can be extended and used to exchange to the DC side the remaining extra energy left during the conversion process.

Since the DC fault blocking is a desirable feature of the AAC, the stacks have to be able to withstand the full AC voltage despite the absence of the DC bus voltage. Therefore, the number of H-bridge cells in a stack is thus defined as in (15a). This equation becomes (15b) when taking the AC voltage magnitude (14) into account. The factor k_{AC} represents again the fluctuation (e.g. $\pm 10\%$) of the AC voltage magnitude around its nominal value, i.e. the sweet-spot (14).

$$N_{cell_{AAC}} = \frac{\hat{k}_{AC} \hat{V}_{AC_{nom}}}{V_{cell_{nominal}}} \quad (15a)$$

$$= \hat{k}_{AC} \frac{2}{\pi} \frac{V_{DC}}{V_{cell_{nominal}}} \quad (15b)$$

From this description, the power function of the positive arm in an AAC can be expressed as in (16).

$$P_{Stack}^+(t) = V^+(t) (-I^+(t)) \quad (16a)$$

$$\begin{aligned} &= - \left(\frac{V_{DC}}{2} - V_{AC}(t) \right) I_{AC}(t) \\ &= - \left(\frac{\pi}{4} \frac{\hat{V}_{AC_{nom}}}{k_{AC}} - k_{AC} \hat{V}_{AC_{nom}} \sin(\omega t) \right) \frac{\hat{I}_{AC}}{k_{AC}} \sin(\omega t + \phi) \\ &= \frac{|\bar{S}|}{3} \left(\cos(\phi) - \cos(2\omega t + \phi) - \frac{\pi}{2 k_{AC}} \sin(\omega t + \phi) \right) \end{aligned} \quad (16b)$$

The resulting energy deviation of the positive arm becomes thus (17).

$$\Delta E_{Stack}^+(t) = \int_0^T P_{Stack}^+(x) dx \quad (17a)$$

$$\begin{aligned} &= \frac{|\bar{S}|}{3\omega} \frac{1}{2 k_{AC}} (\cos(\omega t + \phi) (\pi - 2 k_{AC} \sin(\omega t)) \dots \\ &\quad - \cos(\phi) (\pi - 2 k_{AC} \omega t)) \end{aligned} \quad (17b)$$

Since the two arms are working alternately during the two opposite parts of the cycle, they share the same power and energy equations with the only difference being a time delay. Equations (18) and (18c) represent respectively

the power and energy functions of the negative arm, expressed through the respective functions of the positive arm. Therefore, the study will focus also on the positive arm as the results will be the same as for the negative arm.

$$P_{Stack}^-(t) = V^-(t)(-I^-(t)) \quad (18a)$$

$$\begin{aligned} &= \left(\frac{V_{DC}}{2} + V_{AC}(t) \right) I_{AC}(t) \\ &= - \left(\frac{V_{DC}}{2} - V_{AC} \left(t + \frac{T}{2} \right) \right) I_{AC} \left(t + \frac{T}{2} \right) \end{aligned}$$

$$P_{Stack}^-(t) = P_{Stack}^+ \left(t + \frac{T}{2} \right) \quad (18b)$$

$$E_{Stack}^-(t) = E_{Stack}^+ \left(t + \frac{T}{2} \right) \quad (18c)$$

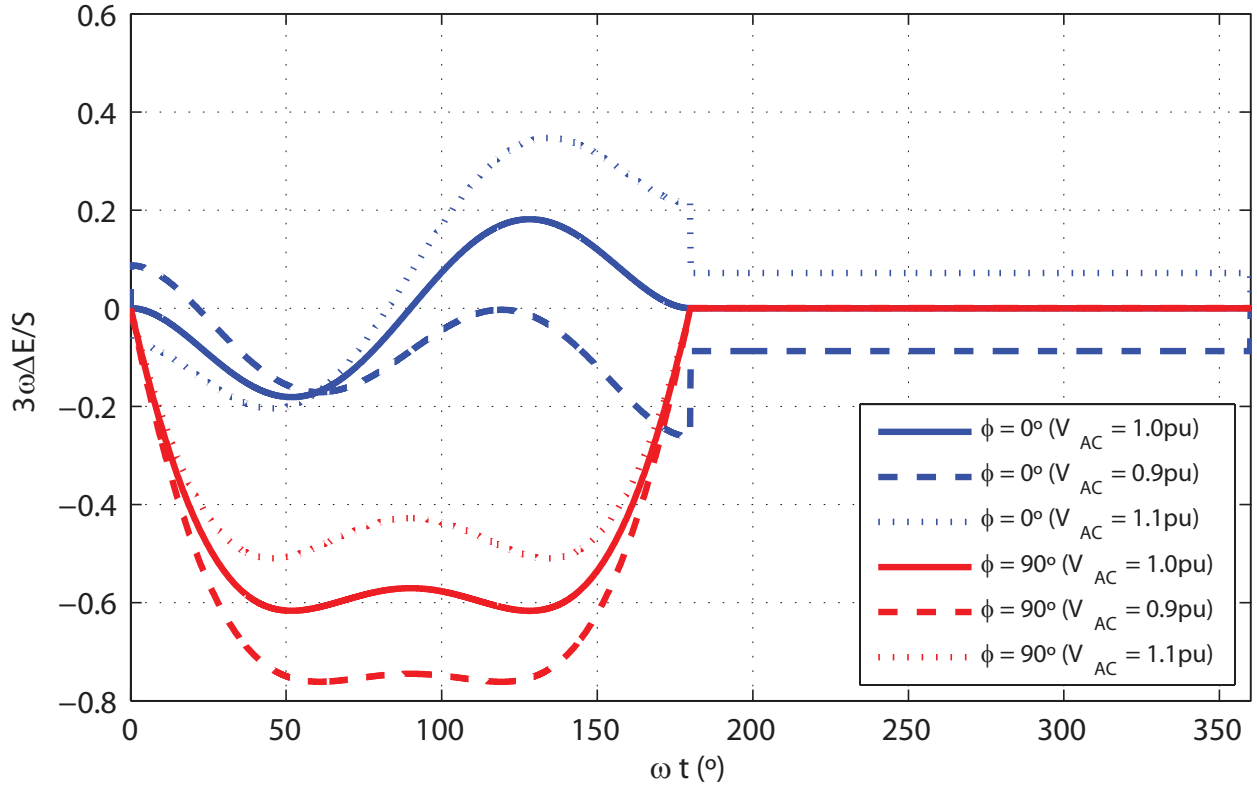


Fig. 4: Energy deviation of the positive arm of an AAC for real power only (blue) and reactive power only (red) operation.

Figure 4 shows the energy deviation of the positive arm of an AAC under different operating conditions. The graph shows that the arm comes back to its initial condition at the end of the cycle, i.e. $\Delta E(T) = \Delta E(0) = 0$ even when the AC grid has moved away from the sweet spot, i.e. $V_{AC} \neq 1.0pu$. Drifts in the arm energy can be observed in these cases but suppressed at the end of the cycle thanks to the bursts of energy provided during the

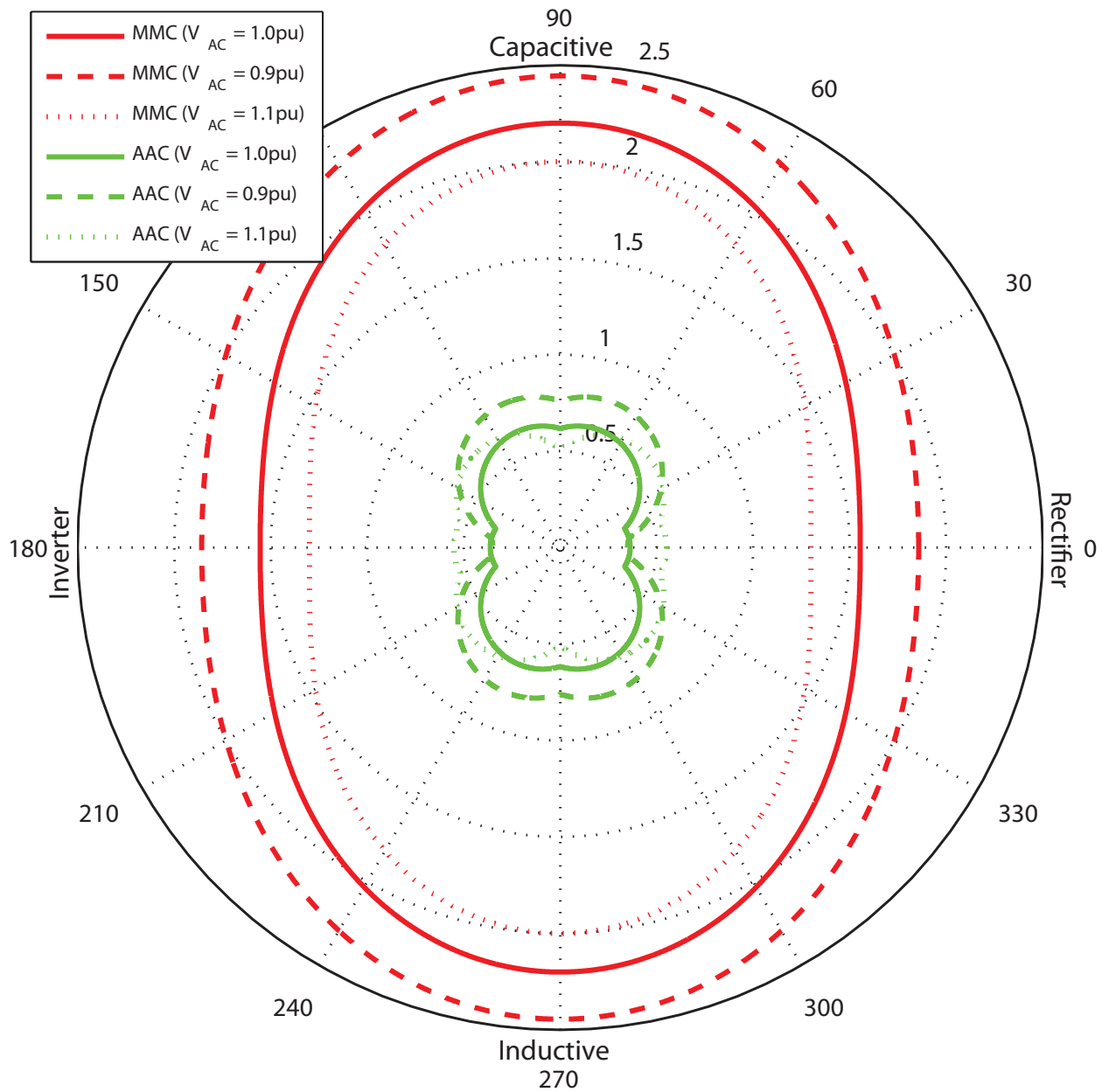


Fig. 5: Normalised peak to peak energy deviation for the MMC (red) and AAC (green) under different operating conditions.

overlap periods (at the beginning, middle and end points of the graphs).

IV. PEAK TO PEAK ENERGY DEVIATION

As explained in section II-B, the sizing of the cell capacitors depends mainly on the peak to peak energy deviation. The energy functions (11b) and (17b) are nonlinear and finding a symbolic solution would be too complex, but numeric values can be easily computed with an acceptable degree of precision for the nonlinear parts over the full range of ωt and ϕ . Figure 5 shows the peak to peak energy deviation across a cycle as a function of the current angle ϕ and for a $\pm 10\%$ AC voltage magnitude fluctuation. These results are scalable in power and frequency as they only represent the numerical solution to the nonlinear part in (11b) and (17b), leaving a factor $\frac{|\bar{S}|}{3\omega}$.

It can be observed in this graph that the peak to peak energy deviation is symmetrical along the active ($\phi = 0^\circ$) and reactive ($\phi = 90^\circ$) power axis. For both the MMC and the AAC, the energy deviation increases with reactive power and decreases significantly when moving close to the operating points with active power only. The MMC sees its energy deviation increasing when its modulation index decreases, denoting longer conduction periods of its cell capacitors while the current magnitude is increased to compensate for the smaller AC voltage magnitude. On the other hand, higher modulation index improves the situation by reducing the energy deviation but is limited by the half-bridge cells which prevent the MMC from generating a peak AC voltage higher than the DC terminal voltages. The AAC presents a lower energy deviation than the MMC in all cases but the best cases are when the converter is operated at its sweet spot. When operated away from this point (either higher or lower in AC voltage), the arms start drifting before being pushed back to their initial value by the balancing techniques during the overlap periods.

According to these results, the highest energy deviation for an MMC stack happens when the AC grid voltage is at $0.9pu$ and $\phi = 90^\circ$, i.e. reactive power only. The peak to peak energy deviation at this point is equal to $2.44 \frac{|\bar{S}|}{3\omega}$. Using this value, the minimum size for the cell capacitors in an MMC can be derived as (19a) and re-expressed as (19b) if the number of cells has been defined according to (9). At a fundamental frequency of 50 Hz and 10% cell capacitor voltage deviation, the total amount of energy stored in an MMC with sinusoidal modulation is equal to 39 kJ/MVA. This compared with the 21 kJ/MVA quoted in [26] when the MMC is using triplen harmonic voltage injection.

$$C_{Cell_{MMC}} \geq \frac{2.44 |\bar{S}|}{3\omega 2 N_{Cell} V_{cell}^2 \Delta V} \quad (19a)$$

$$\geq \frac{1.22 |\bar{S}|}{3\omega V_{DC} V_{cell} \Delta V} \quad (19b)$$

Concerning the AAC, the highest energy deviation for a stack occurs when the AC grid voltage is also at $0.9pu$ and $\phi = 71^\circ$, i.e. a power factor of 0.32. At this point, the peak to peak energy deviation is equal to $0.80 \frac{|\bar{S}|}{3\omega}$, giving a minimum size for the cell capacitors in an AAC of (20a) and ultimately (20b) when taking the number of cells (15) into account. At a fundamental frequency of 50 Hz and 10% cell capacitor voltage deviation, the total amount of energy stored in an AAC with sinusoidal modulation is equal to 11 kJ/MVA which is almost a third of the energy requirement of the MMC under sinusoidal voltage modulation (39 kJ/MVA) and slightly over half the

requirement of the MMC with triplen harmonic voltage injection (21 kJ/MVA) [26].

$$C_{Cell_{AAC}} \geq \frac{0.80 |\bar{S}|}{3\omega 2 N_{Cell} V_{cell}^2 \Delta V} \quad (20a)$$

$$\geq \frac{0.57 |\bar{S}|}{3\omega V_{DC} V_{cell} \Delta V} \quad (20b)$$

V. NUMERICAL EXAMPLES

In order to picture what the equations (19b) and (20b) imply in terms of actual cell capacitor size and total capacitor volume, numerical examples are given in Table I for two different power ratings. The choice was made to set the maximum voltage deviation at $\pm 10\%$ of the nominal cell voltage as an acceptable compromise between capacitor size and controllability of the stack voltages.

TABLE I: Numerical examples for MMC and AAC

Topology	MMC	AAC	MMC	AAC
Power rating	20 MW	20 MW	600 MW	600 MW
DC bus voltage	± 10 kV	± 10 kV	± 300 kV	± 300 kV
AC line voltage (RMS)	11.0 kV	15.6 kV	331 kV	467 kV
Nominal cell voltage	1.5 kV	1.5 kV	1.5 kV	1.5 kV
Number of cells per stack	14	10	400	281
Maximum cell voltage deviation	10%	10%	10%	10%
Cell capacitor	8.3 mF	3.8 mF	8.65 mF	4.0 mF
Total stored energy across all 6 arms	778 kJ	255 kJ	23.3 MJ	7.7 MJ
DC bus capacitor	Negligible	441 μF	Negligible	15 μF
Energy stored in the DC bus capacitor	Negligible	88 kJ	Negligible	2.6 MJ

The results from Table I show that the AAC can be designed with smaller cell capacitors which, added to the smaller number of cells, results in a much smaller amount of energy storage across all of its 6 arms, hence a smaller volume. When compared to the MMC, the cell capacitor of the AAC is slightly less than half the size and the total energy storage in the converter station is about a third of that of the MMC. However this advantage of the AAC over the MMC is reduced by its requirement for a large DC bus capacitor (which could be in the hundreds of μ F as used in [8]) in order to reduce significantly the effects of the 6-pulse ripples present in the DC current generated by the AAC. A quick calculation of the minimal DC bus capacitor size can be obtained by computing the maximum charge fluctuation as in (21b) assuming that (i) all the DC current ripples will flow through this capacitor, (ii) the

phase angle is kept small and (iii) the power rating of the converter is proportional to the DC bus voltage using both (7a) and (14). According to (22b), for an desired DC voltage fluctuation of $\Delta V_{DC} = 5\%$, the AAC requires a 441 μF DC bus capacitor at 20 kV DC or, more generally, an extra 4.4 kJ/MVA of energy stored in the DC bus capacitor which is equivalent in energy storage to two additional stacks of cells as indicated in Table II when 10% cell voltage deviation is allowed.

$$\hat{Q} = 2 \int_{I_{DC}(t) = \langle I_{DC} \rangle}^{t = \frac{\pi}{\omega}} \hat{I}_{AC} \sin(\omega t + \phi) - I_{DC} dt \quad (21a)$$

$$= C_{DC} \Delta V_{DC} V_{DC} \approx \frac{0.1324}{\omega} \hat{I}_{AC} \quad (21b)$$

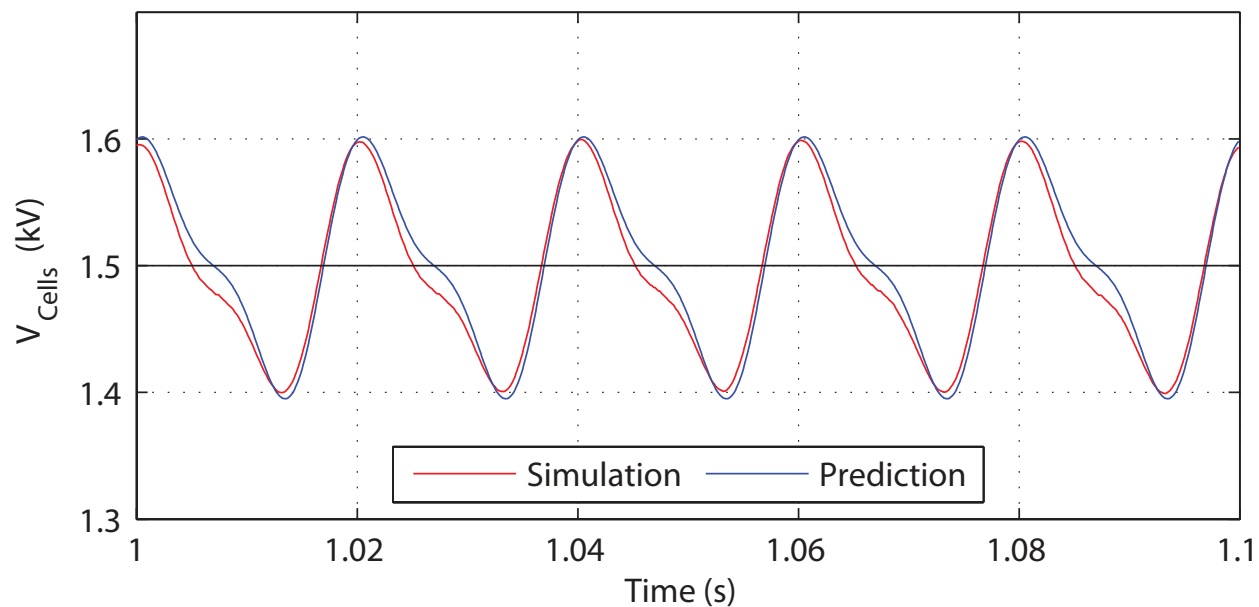
$$E_{DC} = \frac{C_{DC}}{2} V_{DC}^2 \quad (22a)$$

$$= \frac{0.208}{\Delta V_{DC}} \frac{|\bar{S}|}{3\omega} \quad (22b)$$

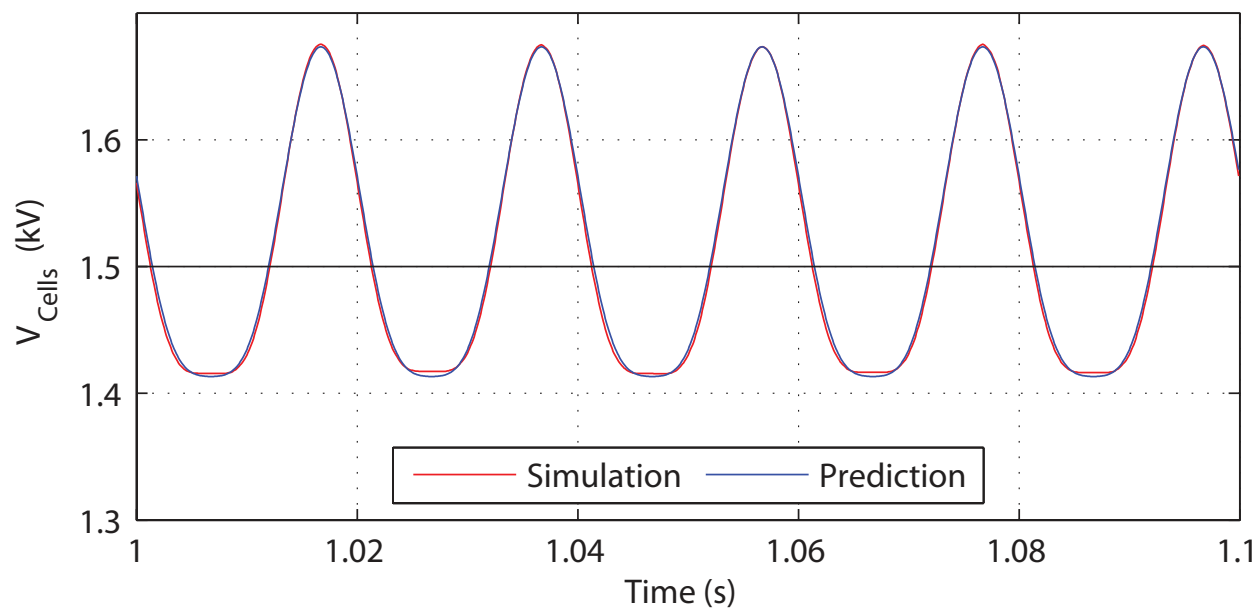
VI. SIMULATION RESULTS

In order to confirm the validity of the mathematical model, component-level models of both the MMC and the AAC have been simulated using the 20 MW case presented in Table I. Figures 6a and 6b show the average voltage of the cells in the positive arm in leg A of a half-bridge MMC for $\phi = 0^\circ$ (i.e. rectifier mode) and $\phi = 90^\circ$ (i.e. capacitive reactive power mode) respectively, with the AC grid voltage fixed at 1.0 pu. Figures 7a and 7b show the average voltage of the cells in the positive arm in leg A of an AAC under the same conditions. All the prediction curves come from the mathematical model developed in section III. The energy levels of the arm inductors have been measured in simulation and confirmed the assumption that the inductors store an insignificant amount of energy compared to the stack of cells. In fact, in this 20 MW simulation models, the arm inductors are 2 mH big with a peak arm current of 1 kA thus totalling a maximum of 6 kJ which is at least 1 order of magnitude smaller than the total energy stored in the stack (≥ 100 kJ). In higher power rating, e.g. 600 MW, the voltage levels are scaled up but not the current magnitudes, making this difference in stored energy even more strikingly big.

The prediction curves fit closely with the simulation results in all four simulated cases. There are still some minor discrepancies between the simulation results and the prediction curves but again these are likely because of the stored energy inductors not being taken into account in the mathematical model. Nonetheless, the simulation results confirm that the choice of cell capacitor sizes (8.3 mF for the MMC compared to 3.8 mF for the AAC) gives the desired maximum peak to peak voltage deviation specified (i.e. $\Delta V = \pm 10\%$) for both converters at this particular power rating (20 MW), despite the difference in the number of cells (10 cells per stack for the AAC and 14 cells per stack for the MMC). Furthermore, both the MMC and the AAC exhibit higher voltage deviations when in reactive power mode ($\phi = 90^\circ$) compared to active power mode ($\phi = 0^\circ$), as it can be observed in Figure 5. This indicates that both converters will benefit in terms of total energy deviation, hence cell capacitor size, from



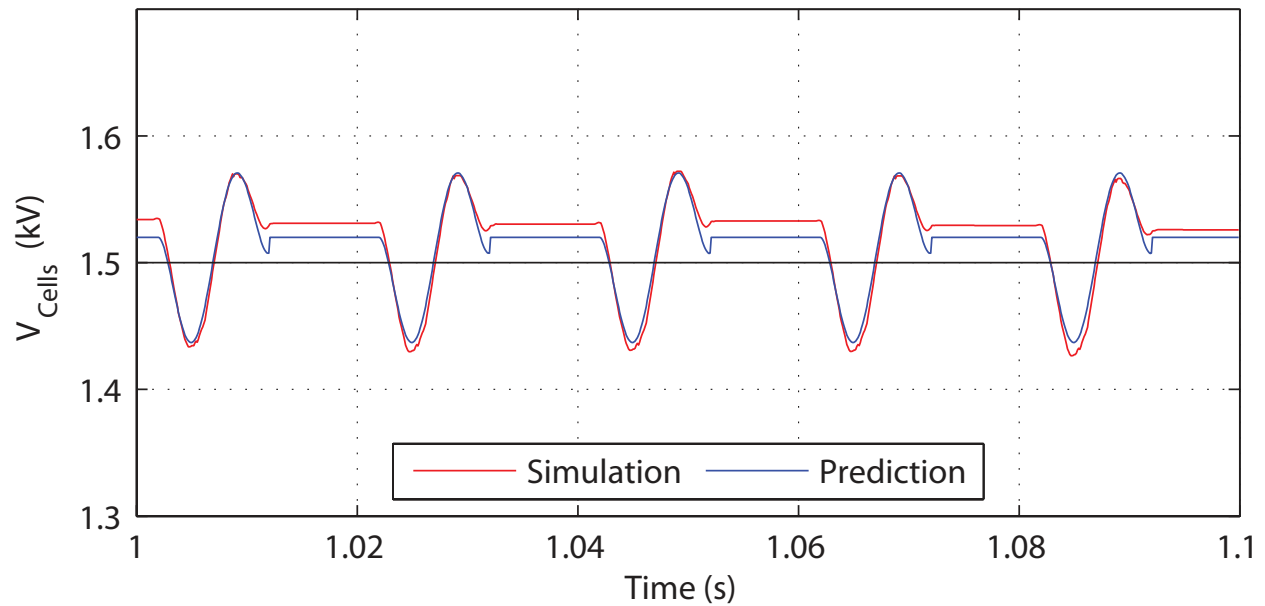
(a) Rectifier mode.



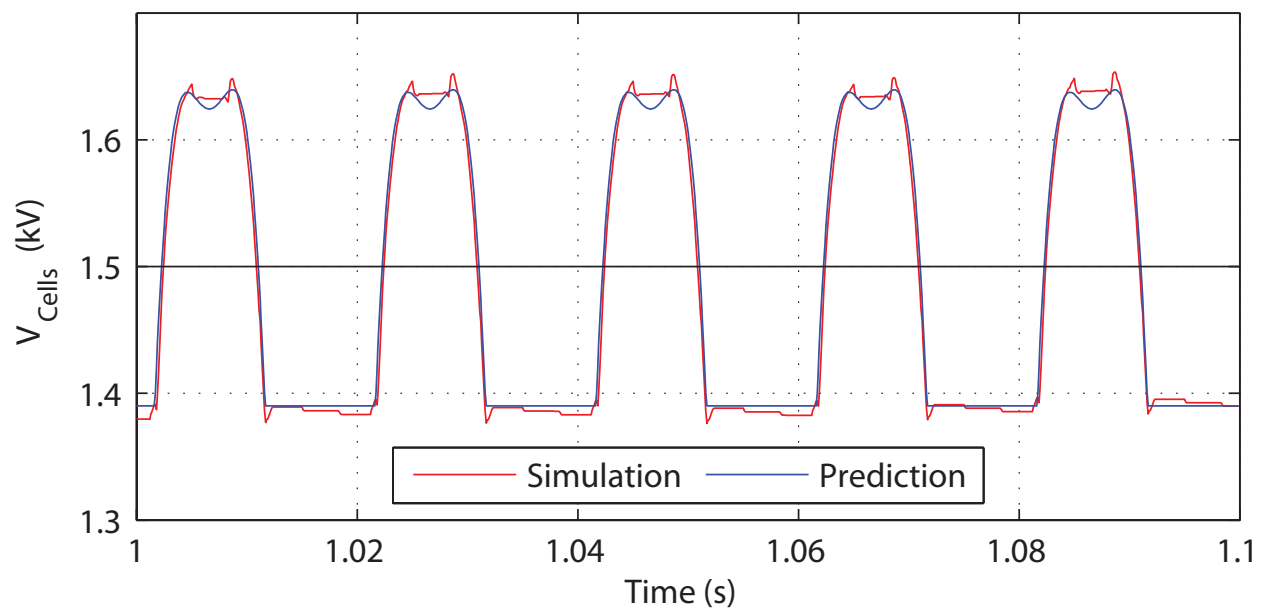
(b) Capacitive reactive power mode

Fig. 6: Average cell voltage in an MMC at $V_{AC} = 1.0pu$

constraining their maximum reactive power rating, although the AAC gains slightly more than the MMC if the reactive power specification is reduced.



(a) Rectifier mode.



(b) Capacitive reactive power mode

Fig. 7: Average cell voltage in an AAC at $V_{AC} = 1.0pu$

VII. CONCLUSION

An assessment of the intra-cycle energy deviation of the cell stacks of two multilevel VSC topologies, namely the MMC and the AAC, has been performed, primarily motivated as a means to compare the physical volume of capacitance required by each topology under various operating conditions. Keeping this volume to a minimum is

TABLE II: Design formulae for the MMC and AAC (for a $\pm 10\%$ AC voltage fluctuation)

Topology	MMC	AAC
Nominal AC peak voltage	$\frac{1}{1.1} \frac{V_{DC}}{2}$	$\frac{2}{\pi} V_{DC}$
Number of cells per stack	$\frac{V_{DC}}{V_{cell}}$	$1.1 \frac{2}{\pi} \frac{V_{DC}}{V_{cell}}$
Minimal Cell capacitor	$\frac{1.22}{V_{DC} V_{cell} \Delta V} \frac{ S }{3\omega}$	$\frac{0.57}{V_{DC} V_{cell} \Delta V} \frac{ S }{3\omega}$
Total stored energy across all 6 arms	$\frac{3.66}{\Delta V} \frac{ S }{3\omega}$	$\frac{1.20}{\Delta V} \frac{ S }{3\omega}$
Total cell energy requirement at 50 Hz and 10% cell voltage deviation	39 kJ/MVA	11 kJ/MVA
DC bus capacitor	Negligible	$\frac{0.416}{\Delta V_{DC} V_{DC}} \frac{ S }{3\omega}$
DC energy requirement at 50 Hz and 5% DC voltage deviation	Negligible	4.4 kJ/MVA

generally desired but is particularly important for converters to be placed on off-shore platforms. The peak-to-peak energy deviation of a stack was analyzed from first principles and the mathematical model was verified against a component-level simulation of example power converters at 20 MW. Example capacitor sizes were calculated for this converter and one at 600 MW to illustrate the use of the model. The results are summarized in Table I.

The analysis shows that the stack energy deviation is proportional to the apparent power processed by the converters, inversely proportional to the frequency and is a non-linear function of the relative AC voltage magnitude and phase angle of the current. The energy deviation is symmetrical about both the active and reactive power axes (when ignoring the reactive power of the phase reactors). Both topologies exhibit generally higher levels of energy deviation when generating reactive power, with the MMC exhibiting its highest energy deviation when acting solely as a STATCOM. The minimum energy deviations are, in both cases, obtained at unity power factor operation (i.e. only active power). Since the cell capacitors have to be sized to accommodate the highest energy deviation across the expected operating envelope, it can be advantageous to constrain the maximum reactive power, even at times of ample current rating (i.e. low active power transfer).

The energy deviation in the MMC is smallest when it operates at its maximum AC voltage capability (the limit imposed by the DC bus voltage) and the deviation increases as the modulation index decreases. If the AC voltage magnitude is expected to vary by $\pm 10\%$ around a nominal value then the worst case normal operating point corresponds to a modulation index of 0.8 for the MMC and this point will define the energy deviation for which the cell capacitors must be chosen. Table II summarises the capacitor sizing formulae and the energy requirement for both the MMC and AAC.

In the case of the AAC, the energy deviations are at their smallest (mostly) when the converter is operated at its sweet-spot and this would normally be arranged to correspond to the nominal AC voltage. The energy deviation in the AAC worsen (in most cases) when the AC voltage magnitude diverges from the sweet-spot value in either

direction. If the AC voltage is expected to vary by $\pm 10\%$ then these points will define the energy deviation for which the cell capacitors must be sized. A further consideration is that operation away from the sweet-spot relies on balancing mechanisms which may limit the AC voltage range if, for instance, a limit on balancing current is reached.

Comparing the MMC and the AAC, it is found that the AAC has the smaller magnitude of energy deviation per cell (for any power factor) by a factor of up to 2. This implies that the cell capacitors in the AAC can be designed to be almost half the size of those in the MMC. Furthermore, because the AAC requires fewer cells, the total volume of cell capacitors in the AAC is approximately 3 times smaller than the volume required by the MMC (for the same power rating, P-Q envelope and AC voltage deviation from nominal). However, the AAC produces a six-pulse DC current (in contrast to the essential constant current of the MMC) and thus is likely to require a capacitive filter on the DC-side which is significant compared to a stack and removes some of the advantage.

When considering $\pm 10\%$ maximum cell voltage deviation and $\pm 5\%$ DC bus voltage maximum ripples, the results show that the MMC requires 39 kJ/MVA of capacitive energy storage under sinusoidal modulation but this reduces with triplen injection modulation as shown in [26]. The AAC has a lower requirement for storage in its cells of 11 kJ/MVA but the AAC has a 6-pulse DC current ripple which requires a filter estimated to have an additional 4.4 kJ/MVA for the DC bus capacitor which is equivalent to a further 33% capacitive storage.

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