Challenge: Variability Characterization and Modeling for 65- to 90-nm Processes

Hiroo Masuda, Shin-ichi Ohkawa, Atsushi Kurokawa and Masakazu Aoki*
Semiconductor Technology Academic Research Center (STARC)
3-17-2, Shin-Yokohama, Kohoku-ku, Yokohama, 222-0033 Japan
* Electronic Systems Engineering, Tokyo University of Science, Suwa, Nagano, 391-0292 Japan

Abstract- In sub-100-nm processes, many physical phenomena have become critical issues in the development of processes, devices, and circuits. To achieve reasonable compromise in ASIC design, device- and process-level characterization of physical designs is a fundamental requirement. In this paper, we address topics regarding "design for variability", which are increasingly important in the 65- to 90-nm technology era. We have developed a new test-structure to precisely measure the on-chip variation of key LSI components (MOST, R, C, and circuit-delay). Statistical analysis of the experimental results revealed that the 3σ variation of MOS drive-current within a chip was 30%, which led to equal variation in the circuit propagation delay (Tpd). We found that variation can be suppressed due to its randomness features in multi-stage circuitry and high-performance, large-gate-area driver CMOS devices.

1. INTRODUCTION

In scaled LSIs below the 100-nm technology node, physical problems have once again become of major interest to circuit designers. Signal integrity problems due to capacitive crosstalk[1] and power-line bounce noise[2] are known to degrade design quality. Inductive crosstalk and noise[3] may limit circuits operating at gigahertz speeds even on a chip. Another emerging issue is increasing variability problems, which are amplified by the required low power and low Vdd operation. Traditionally, to cope with variability (process, environmental, and time-dependent variation), we have used techniques such as guard-banding (worst-casing) and setting design margins. Figure 1 illustrates the widely expected performance crisis regarding 65- to 90-nm technologies[4]. First, the performance improvement achievable through scaled technology will level off since the MOS driving capability will be limited because of low Vdd and carrier velocity saturation, and interconnect signal propagation will be degraded by narrow and densely pitched interconnect structures. Second, relative critical dimension (CD) control will be reduced and on-chip variation significantly increased due to photolithographic problems (e.g., concerning optical proximity control (OPC) and phase-shift mask (PSM)), CMP dummy problems, and impurity and line-edge fluctuations. These problems were predicted in ITRS 2003 (Fig. 2). Gate CD variation and line edge roughness (LER) will be difficult to control for below-65-nm technology. This will lead to a sharp increase in CMOS Vth variation (Fig. 3)[5] and drive current variation within the die distribution.

In this paper, we describe our activities aimed at suppressing variability in 65- to 90-nm process technologies. First, we look at ways to precisely measure the variation within a die. We introduce a sophisticated test structure (DMA-TEG) and show that it provides reliable regarding MOS Ids, C, and R variation[6-7]. Second, we derive a robust analysis methodology which categorizes measurement data into systematic and random components[8]. We have applied this methodology to various cases of characterization and modeling to determine the actual features of variation in 90-nm devices. We also assess the propagation delay (Tpd) variability by measuring the frequency variation of ring-oscillator circuits implemented in the DMA-TEG. We have found that the relative Tpd variation can be reduced with number of stages which form the ring-oscillators.

2. MEASURING VARIABILITY

A. Test structure

Variation is hard to measure with reliable precision within a reasonable time. Special care must be taken concerning the test structure and measurement jig to obtain meaningful variation data. We have developed a special purpose test-structure, the device matrix array-test element group (DMA-TEG), which features on-chip measurement circuits and matrix unit decoder access. A chip photograph is shown in Fig. 4. The die size is 5 x 5 mm, and the 4.2 x 4.4 mm DMA-TEG is located at the upper-right of the die. Individual CMOS devices, the R and C of metal layers, and so on can be measured using test-structures laid out at the upper-left on the chip. The DMA design architecture is shown in Fig. 5. The basic idea of the architecture is to use 16 x 16 matrix array

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units (MAUs) to measure the on-chip variation of circuit components. As shown in the MAU cell details, in the MAU densely packed CMOS and interconnect components are manually designed and on-chip measurement circuits for R, C, and the down-countered frequency with low leakage bus lines are carefully designed. Figure 6 shows the main features of the DMA-TEG and compares the second-generation 90-nm DMA to the first-generation DMA designed for 130-nm technology. Key improvements are (1) 1.3X MAU size, (2) a 140% increase in the number of components, and (3) additional 90° rotated patterns. The on-chip measurement circuits and test jig were carefully studied in terms of measurement precision and time. The results are listed in Fig. 7, and compared with those for the 130-nm DMA. As shown, minimal error in the measurement system was achieved with regard to R, C, Ids (Vth), and ring oscillator frequency. The measurement time of the DMA was 2.5 hr/chip (since improved to 1.0 hr/chip). Several on-chip circuits contribute to this highly precise measurement:

R measurement: Kelvin circuit
C measurement: CBCM circuit
Ids measurement: leakage control circuit
Frequency measurement: down-counter

Based on these techniques, we have been able to conduct within die variability measurements in a reliable manner for the first time.

B. Measurement results

The test system automatically measures the DMA-TEG using a special PC controlled test-program. Collected data are displayed as a chip-map, wafer-map, correlation-map, and histogram. Basic characteristic quantities, such as mean (μ) and standard deviation (σ), are calculated after outliers are detected and eliminated. Figure 8 shows an example of experimental data showing within-die variation: experimental within-die variation is shown as chip-maps for two types of ring-oscillator frequency, N and PMOS drain current, contact resistance on the N+ diffusion layer, via resistance between metal 2 and 3, and the interconnect wire resistance and capacitance of narrow-pitch metal 2. The relative on-chip variation of the N and PMOS drain current is dominant, whereas there is much less fluctuation in the interconnect wire resistance and capacitance. Figure 9 shows an example of the die-to-die distribution of the NMOS Ids variability (a systematic component). Note that the on-chip variation within a wafer does not show a uniform tendency; e.g., some chips have a negative slope in the horizontal direction while others have a positive slope in the vertical direction. In Fig. 10, we summarized the relative variation (σ as a percentage) for typical components used in 90-nm process technology. The on-chip variation was the average for the 71 dies/wafer. The Ids variation of smaller scale N and PMOS technologies will clearly be crucial, and will have to be carefully considered in process and design development.

Estimation of the variation (σ) is the most important task in the measurement. If we assume the variation is normally distributed (usually a valid assumption), the values obtained from the DMA-TEG will be within a 10% error with a 98% level of confidence. This also depends on the number of MAUs, though, and accurate assessment of within-die variation needs over 200 MAUs per chip [9].

3. VARIABILITY ANALYSIS

On-chip variation is a problem which increasingly arises in 65- to 90-nm technologies. It can be characterized as having two components – systematic and random [10] – and we need to reliably decompose measurement data into these two components. A technique developed for such decomposition is shown in Fig. 11. To extract systematic components, the raw data is fitted with a fourth-order polynomial in a two-dimensional space (x,y). The extracted 2D polynomial equation is assumed to exhibit a curved surface for the systematic component of on-chip variation. Residual amounts (equal to the raw data less the 2D polynomial value) show the effective random component of on-chip variation. In this way, the raw data are divided into systematic and random components.

We tested the validity of this algorithm by applying it to NMOS Vth and Ids variation data (Fig. 12). The extracted random component showed how random the variation was. The random component histogram in Fig. 12 shows +/- 4σ accuracy in fitting to a normal distribution. Therefore, the extracted random component appears to be purely random in nature.

The systematic component can be characterized by its correlation length. This metric represents the distance along which the on-chip slope is correlated. Figure 13 shows a correlation length histogram for an on-chip NMOS Ids systematic component. This histogram shows that the correlation length was close to normal in its distribution, with a range of 1.2 to 3.0 mm. In other words, NMOSs closely laid out (within 1 mm in distance) are well correlated with respect to systematic component variation.

Figures 14 and 15 show Pelgrom plots [11] of the Vth and Ids on-chip variation (σ) for NMOS devices with various length and width (L&W) dimensions. As expected, on-chip variation was linearly related to the square root of the MOS gate-area. The interconnect

resistance of the metal wire was also dependent on the width and length, which reflects the LER and metal-dishing effect of the CMP process. Figure 16 shows experimental data regarding the effect of L&W dimensions on the variability of M2 wire resistance in NMOS devices. Again smaller dimensions led to greater on-chip variation.

A simple question regarding the MOS Vth variability is what happens when the technology generation changes? Figure 17 compares experimental data on 90-nm and 130-nm Ids on-chip variation presented as Pelgrom plots. (Circles show the minimum-dimension MOS used in a standard cell library.) This data shows that the Ids variation doubled for each technology node enhancement below 100-nm processes. The data for Vth variation versus the technology node curve (Fig. 3) showed a similarly increasing trend.

4. DELAY VARIABILITY

We can use ring-oscillators in DMA-TEG to evaluate the circuit-delay variability. Various types of ring-oscillator circuit are implemented in the DMA (Fig. 18). We can use inverter, 2NAND, 2NOR, 3NAND, and 3NOR circuit components. Oscillators have a seven-stage circuit chain. To evaluate the output loading effect of each circuit, we used a fan-out 1 and 4 and M2 and 3 interconnect loading with Capacitance and Resistance. The resulting 3σ variation of the propagation delay (Tpd/stage) ranged from 11 to 22%. We measured the maximum variability with an inverter-type ring-oscillator with minimum-size transistors. Output loading lowered on-chip variation, but did not significantly reduce Tpd variation. This is because both the on-chip variation and the performance of the oscillators are determined solely by the N and PMOS Ids and its variation. Note that if we used 10X gate-width devices in the inverter circuit, the Tpd variation would be significantly improved, as has been shown experimentally. The physical reason for this result is clear from the Ids-variation vs. gate-area relationship shown in Fig. 17. As explained, good correlation between the Tpd variation and Ids variation has been found experimentally. This was confirmed by the correlation between the on-chip Ids and the ring-oscillator frequency data (Fig. 19). Figure 20 shows the gate-area effect on the Tpd variation; up to a three-fold improvement was realized by using a larger (10X) gate-area CMOS in the oscillator.

In addition, the large random variation in MOS Ids and Vth can be suppressed through the well known multi-stage effect.

CONCLUSION

The "design for variability" approach is increasingly important in the 65- to 90-nm technology era. Accordingly, we have developed the DMA-TEG test-structure which enables precise measurement of on-chip variation in key LSI components (MOST, R, C, and circuit-delay). Statistical analysis of experimental data has revealed that the 3σ variation of the MOS drive-current reaches 30% within a chip, and this leads to significant variation in a circuit's per-stage Tpd. We confirmed that the variation can be suppressed due to its randomness features in multi-stage circuitry and high-performance, large-gate-area driver CMOS devices.

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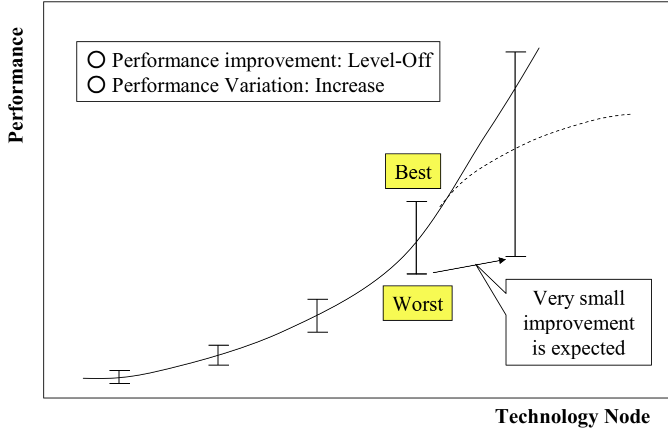


Fig. 1 Performance crisis in 65- to 90-nm technologies

Year	2003	2004	2005	2007	2010	2013	2016
DRAM ½ pitch (nm)	100	90	80	65	45	32	22
Total gate 3s (nm)	4.5	3.75	3.15	2.5	1.8	1.3	0.9
Lithography 3s (nm)	4.0	3.35	2.8	2.2	1.6	1.15	0.8
LER 3s (nm)	3.6	3.0	2.6	2.0	1.4	1.0	0.7
Gate Etch 3s (nm)	2.0	1.7	1.4	1.1	0.8	0.6	0.4

ITRS 2003

- Manufacturable solutions are known
- Interim solutions are known
- Manufacturable solutions are NOT known

Fig. 2 ITRS 2003 on gate CD variation and line edge roughness (LER) control

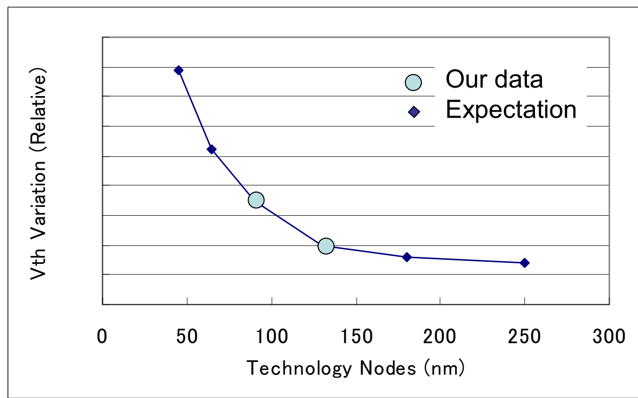


Fig. 3 Technology trend of CMOS Vth variation with experimental data for 130-nm and 90-nm technologies

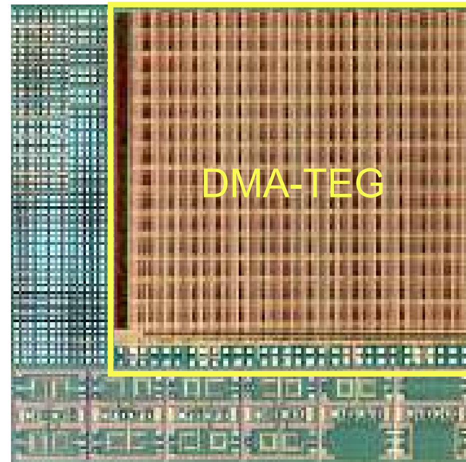


Fig. 4 Chip photograph of 90-nm DMA-TEG

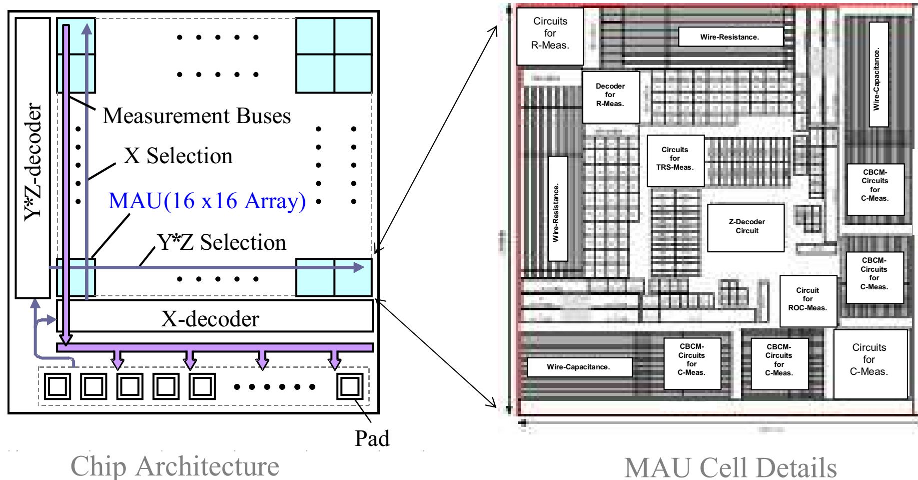


Fig. 5 DMA design architecture: 16x16 MAU array and decoders

Items	90nm DMA chip	130nm DMA chip
Chip size	5.0mmx5.0mm	←
DMA area	4.2mmx4.4mm	4.0mmx4.0mm
MAU size	240μmx240μm	←
Array size	16x16	14x14
Samples/chip	256	196
Devices/MAU	350*1, *2	148*1
Total # devices/chip	89600	29008

*1 Including size-variation

Components	90nm DMA Chip	130nm DMA Chip
C-measure structures	41x2*2	30
R-measure structures	62x2*2	51
NMOS structures	26x2*2	26
PMOS structures	26x2*2	26
Ring OSC types	20x2*2	15
Total	350	148

*2 0/90 degree dependency

Fig. 6 Main features of the DMA-TEG: comparison of the second-generation 90-nm DMA and the first-generation 130-nm DMA technology

Items		90nm DMA CKT & Jig*	130nm DMA CKT & Jig*
R-measure.		3458A (Wait time 20ms)	←
	･Time ･Error	53ms/dut、28min/chip σ =4.0 m Ohm	95ms/dut、16min/chip σ =3.6 m Ohm
C-measure.		E5270(Wait time 2.88ms)	4156B(Wait time20ms)
	･Time ･Error	62ms/dut、22min/chip σ =4.8 aF	80ms/dut、8min/chip σ =8.5 aF
MOS –measure.		E5270 (Wait time 640us)	4156B(Wait time 1.92ms)
	･Time ･Error	170ms/dut、75min/chip σ <500pA (ΔVt=1.07mV)	640ms/dut、107min/chip σ <1.0nA (ΔVt=0.34mV)
ROS –measure.		52132A(Gate time 10ms)	52132A(Gate time 1.0ms)
	･Time ･Error	200ms/dut、34min/chip Δ=0.3%	500ms/dut、25min/chip Δ=0.3%
Total Time		159min./chip (Devices: 89600)	156min./chip (Devices: 29008)

Fig. 7 DMA-TEG measurement precision and measurement time

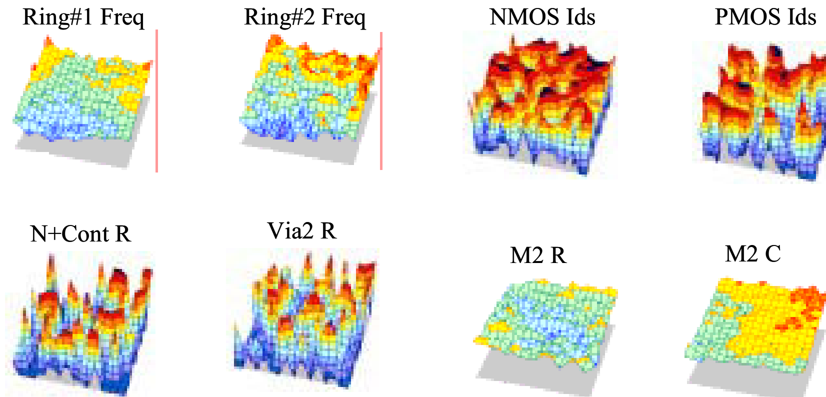


Fig. 8 Examples of experimental data showing within-die variation

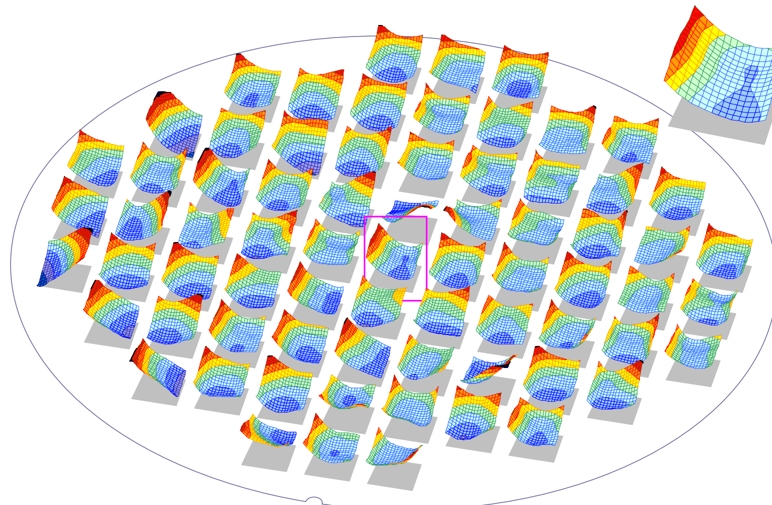


Fig. 9 An example of the die-to-die distribution of NMOS Ids variability (systematic component)

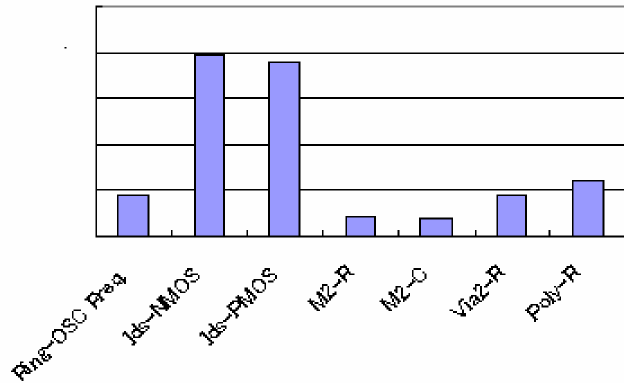


Fig. 10 Summary of relative variation (σ in %) for typical components used in a 90-nm process technology

◆ Application of a 4th-order polynomial fitting for date decomposition.

$$z(x,y) = a_0 + a_1 x + a_2 y + a_3 x^2 + a_4 xy + a_5 y^2 + a_6 x^3 + a_7 x^2 y + a_8 x y^2 + a_9 y^3 + a_{10} x^4 + a_{11} x^3 y + a_{12} x^2 y^2 + a_{13} x y^3 + a_{14} y^4 .$$

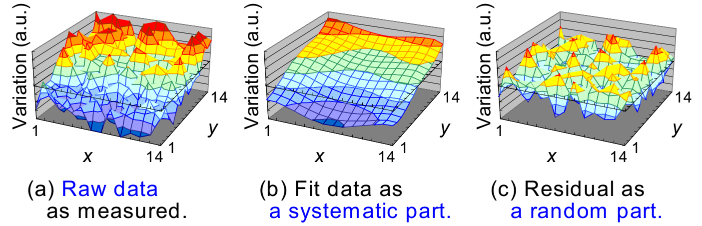


Fig. 11 A new technique for decomposing systematic and random components [NOTE: In the top line, change 'date' to 'data'.]

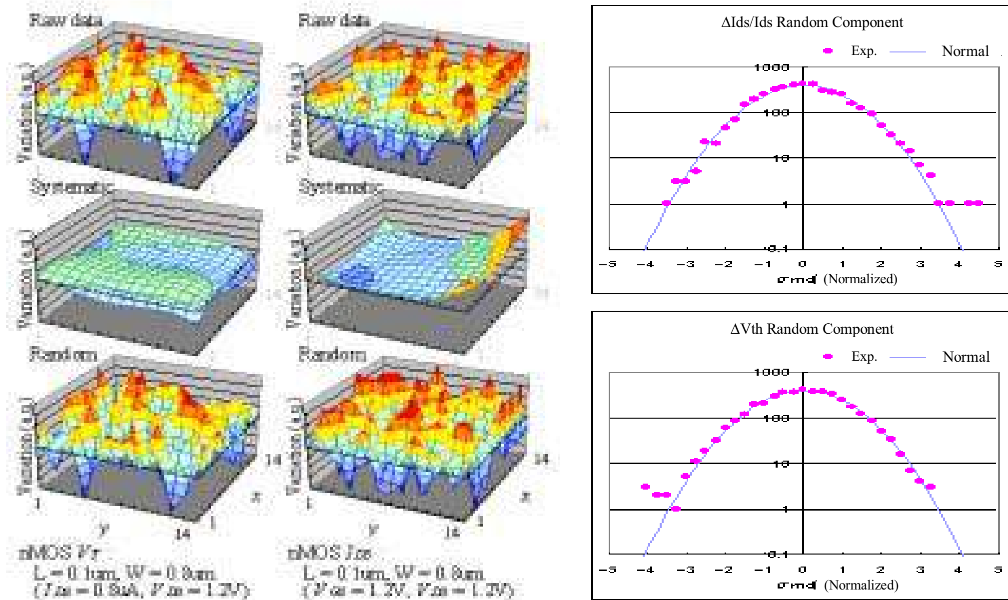


Fig. 12 Application of the developed decomposition algorithm to NMOS Vth and Ids variation

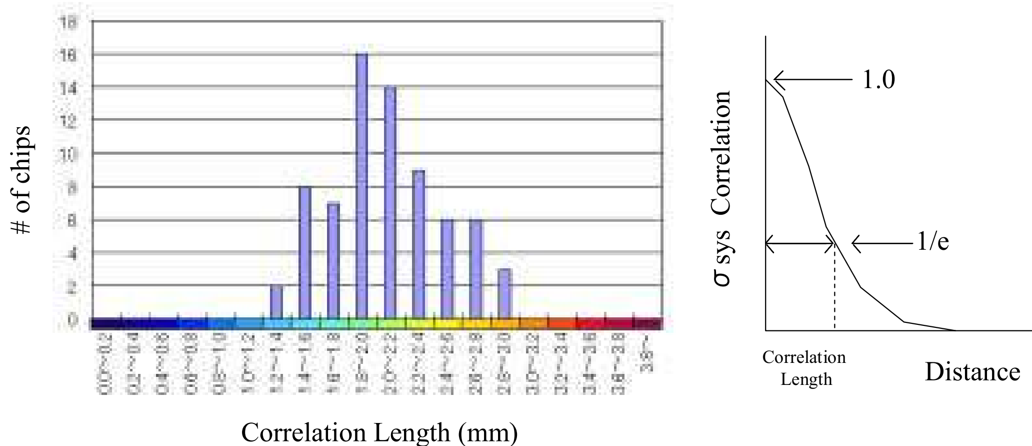


Fig. 13 Correlation-length histogram for the on-chip NMOS Ids systematic component

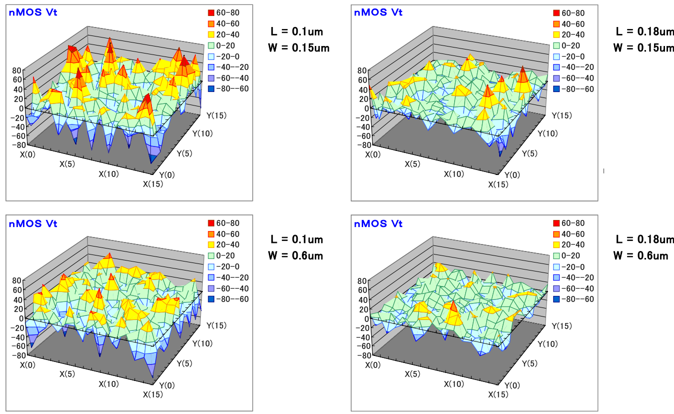


Fig. 14 Experimental data showing the dimension effect on NMOS Vth variability

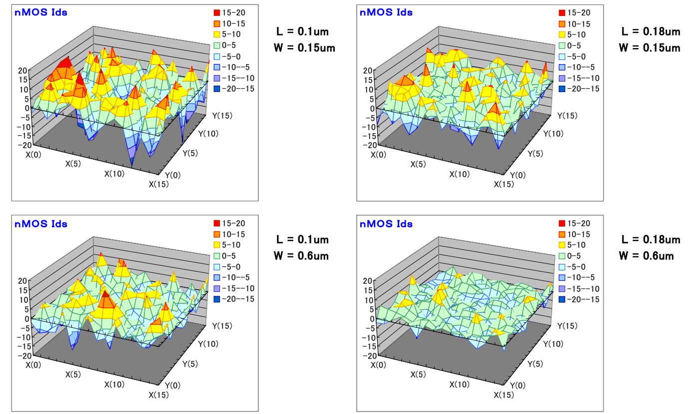


Fig. 15 Experimental data showing the dimension effect on NMOS Ids variability

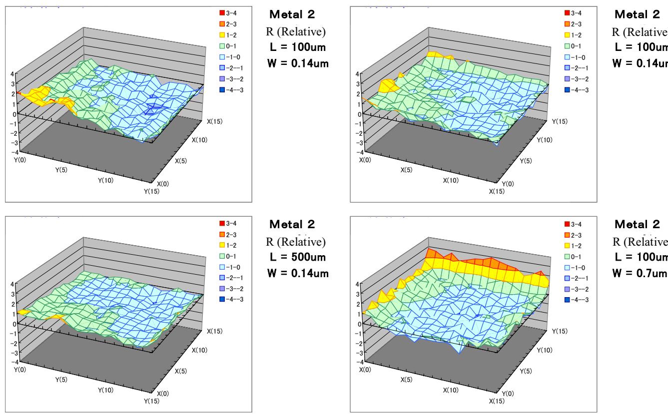


Fig. 16 Experimental data showing the dimension effect on the variability of M2 wire resistance

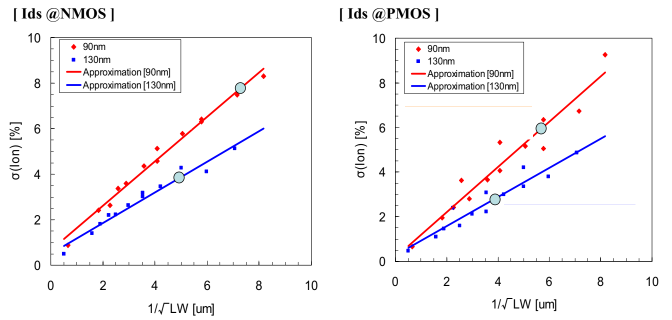


Fig.17 Experimental data for 90-nm and 130-nm Ids on-chip variation in the form of Pelgrom plots

<u>Type</u>: Inv, 2NAND, 2NOR, 3NAND, 3NOR
<u>Loading</u>: FO=1&4, M2&M3 Wires (FO=4 level)

(1) Tpd/Stage (Within Die) Variation:
- σ =3.74 - 7.48%, (3σ=11-22%)

(2) Other measurement results:
- N/PMOS size (gate area) dependency: large area → smaller Tpd σ
- Loading effects (@M2、FO=4): change is negligible

Fig. 18 Various types of ring-oscillator circuit are implemented in the DMA

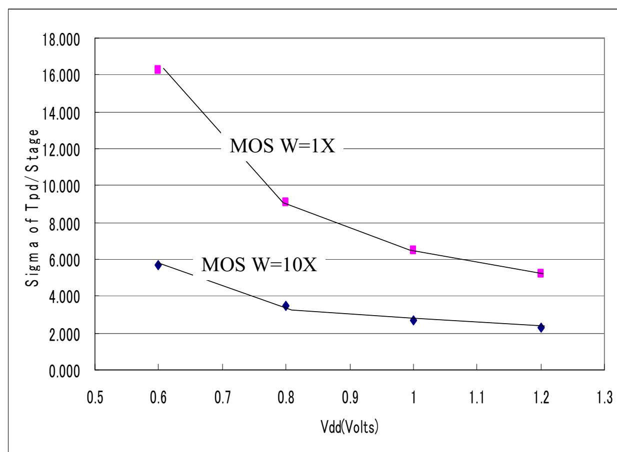
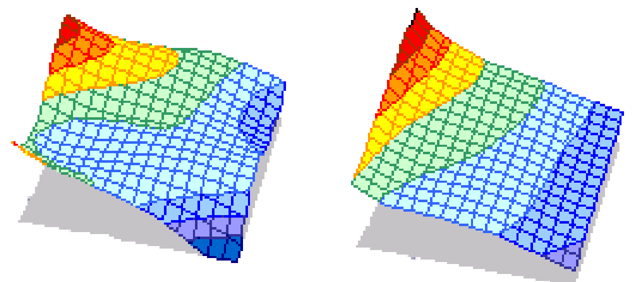


Fig. 20 Gate-area effect on Tpd variation: three-fold improvement was achieved by using a larger (10X) gate-area CMOS in the oscillator



NMOS Ids (WID) Variation　　Ring-osc1 Freq. (WID) Variation

Fig. 19 On-chip correlation data between Ids and ring-oscillator frequency