Challenges for a new integrated Ultra-wideband (UWB) source

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Abstract ---- **This paper presents a description of a new method to generate a short impulse based on a counter designed on BiCMOS SiGe technology. This architecture includes a new method to modify the PRF (pulse repetition frequency) by changing the counter division ratio and an easy way to control the impulse frequency center. A pseudo-noise sequence prescaler modulates the impulses with specific modulation schemes, such as pulse position, bi-phase modulation or a combination of both. The total power consumption is 65 mA at 7GHz.**

I. INTRODUCTION

Since February 2002, the Federal Communication Commission (FCC) has conditionally allocated 7.5GHz of spectrum for unlicensed types of ultra-wideband (UWB) wireless systems in the 3.1 to 10.6 GHz frequency band. The UWB technologies are developed to be used for super-high-speed communication, geolocation and highly-accurate sensing, low cost RF tagging, and so forth. UWB differs from other RF technologies: instead of using a narrowband frequency carrier to transmit data, it sends impulses of energy across a spectrum of frequencies. Most radio technologies in use today use the modulation of a carrier, but at the beginning of the last century, physics and radio engineers used a spark gap to generate ultra wideband signals for transmission of data before sinusoidal carriers were invented. However, the generation of impulses and their adequate control for effective communication purposes were extremely difficult to master until recently. In the recent past, creative methods have been proposed to implement the impulse waveform generator (step recovery diodes [1-2] etc.). In our solution, we propose an integrated waveform generator based on the original use of counters and a PN sequence prescaler.

Our paper is presented as follows. In the first part, we describe the circuit principle in which we distinguish the waveform generator and the PN sequence prescaler. The second part is dedicated to the design description and simulation results for the various blocks.

II. CIRCUITS DESCRIPTION

The pulse generator is composed of a waveform generator that delivers a short pulse and a PN sequence prescaler used to modulate the pulse with a code [3].

II.1 Waveform generator

Today, the integration of a low cost and reproducible impulse generator with short duration sub-nanosecond pulses (~ 150ps) implies a lot of constraints. The concept is to use common blocks to achieve this function. The theoretical impulse is similar to one cycle of a sine wave as shown in Figure 1. These signals correspond to ultra-wideband signals in the frequency domain (see. Figure 2).

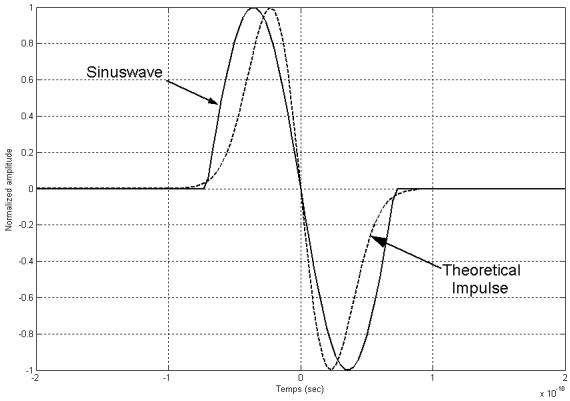

Figure 1: Comparison between a sinusoidal and a derivative gaussian monocycle in the time domain

An architecture using the mixing of a sinusoidal signal provided by a VCO (Voltage Controlled Oscillator) with this same signal divided by 2 is capable of printing the monocycle. The block diagram and the chronogram are presented in Figure 3. The main advantage of this system is its simplicity. Moreover, all the system is synchronized by one VCO and the pulse width is directly dependent on the source frequency.

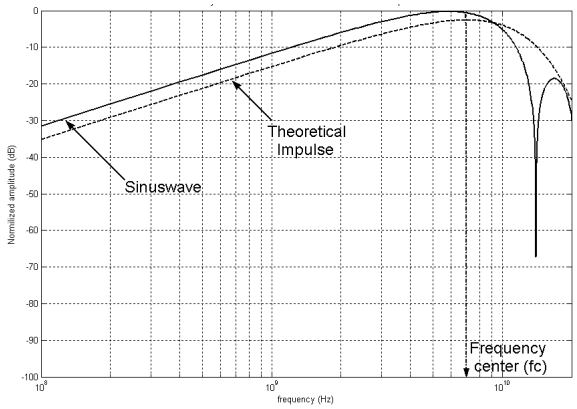

Figure 2: Comparison between a sinusoidal and a derivative gaussian monocycle in the frequency domain

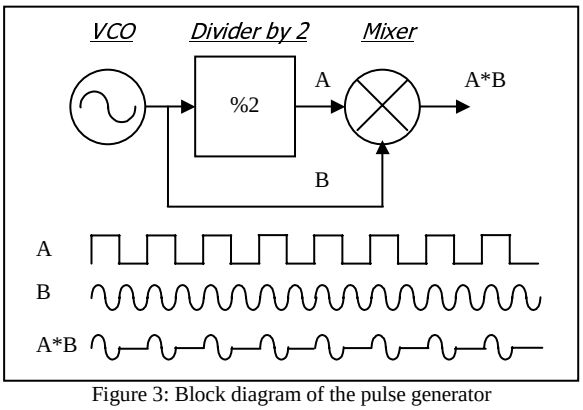

Figure 3: Block diagram of the pulse generator

However, with such a system the PRF (Pulse Repetition Frequency), i.e. the distance between impulses is fixed. We propose a solution to control this distance which consists in replacing the "divider by 2" by a counter as shown in Figure 4. The Hit signal delivered by the counter is used to select the pulse. The division ratio is set with the bits of control.

II.2 PN sequence prescaler

Before transmitting the information, the technique of spread spectrum modulation is used [4]. Not only this technique has the advantage to smooth the power spectral density of the signal but it can also give the signal a noise-like appearance for the other (unauthorized) receivers. Thus multiple user transmissions can simultaneously occupy the same frequency band with guaranteed message privacy, provided that each user's signal has been spread using a unique pseudo-random code, also referred to as pseudo-noise (PN) sequence. The second challenge for this kind of system is to synchronize the PN sequence code with the transmitted impulses. The PN sequence prescaler is presented in Figure 5. The code is loaded in parallel 16 by 16 bits from a ROM and is transmitted in serial at the MUX output.

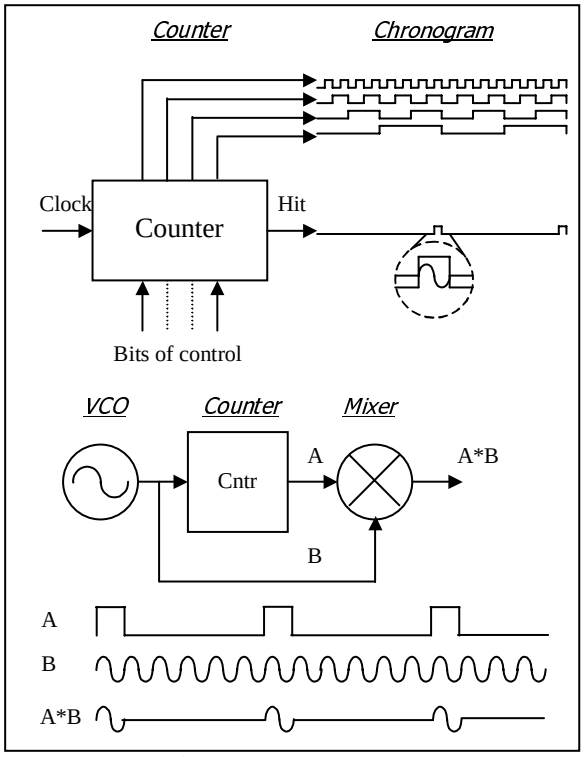

Figure 4: New waveform generator block diagram with the counter

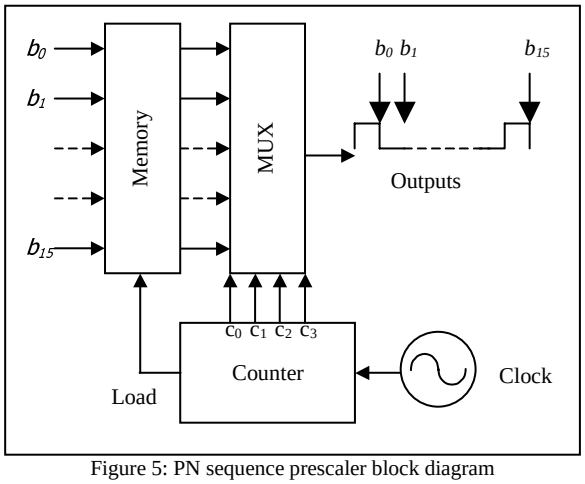

Figure 5: PN sequence prescaler block diagram

To simplify the synchronization for all the system, the clock is replaced by the Hit signal delivered by the waveform generator counter.

For each rise time of the counter, the multiplexer selects one code value from b0 to b15, then a signal "load" is emitted to load the next 16 code values in memory. The chronogram of the PN sequence prescaler is presented in Figure 6. Note that the clock signal has been replaced by the "hit" signal of the waveform generator counter.

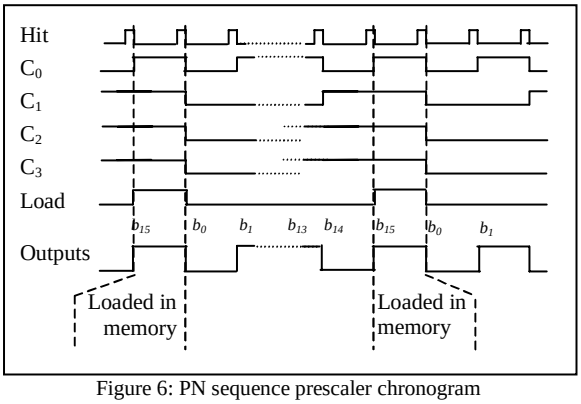

Figure 6: PN sequence prescaler chronogram

II-3 Pulse generator: waveform generator & PN sequence prescaler

The information can be encoded in a UWB signal in a variety of methods. The most popular modulation schemes developed to date for UWB are pulse-position modulation (PPM), pulse-amplitude modulation (PAM), on–off keying (OOK), and binary phase-shift keying (BPSK), also called bi-phase. The original feature of this design is to make it possible to manage various types of modulations: bi-phase and PPM independently from code or data.

a) Pulse generator configuration with the bi-phase modulation

In bi-phase modulation, the information is encoded with the phase (0 or 180°) of the impulses. The phase of the impulses is switched to encode a 0 or a 1. To achieve this function, the code transmitted in serial and the information (data) are first multiplied together, and then multiplied again by impulses as illustrated in Figure 7.

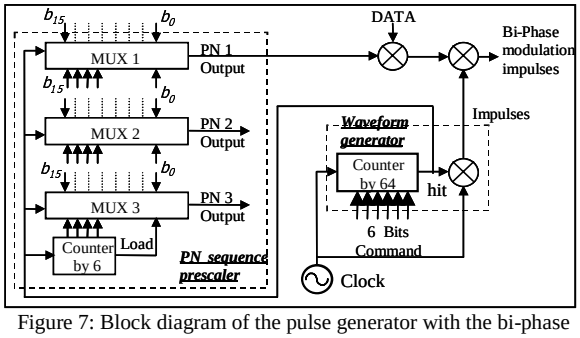

Figure 7: Block diagram of the pulse generator with the bi-phase modulation

At the output of the system we obtain bi-phase modulation impulses. As explained before, the PN sequence prescaler is synchronized by the output waveform generator counter. This architecture requires only one clock to synchronize all the system. The impulse frequency center (fc) is fixed by the clock frequency and the PRF by 6 bits command counter. Thus, the ratio between central frequency and PRF could be 64 max.

The chronogram presented in Figure 8 shows all the principal outputs of the pulse generator with the bi-phase modulation. In this configuration, the bi-phase modulation is controled by the PN1 code and the PN2 and PN3 outputs are disabled.

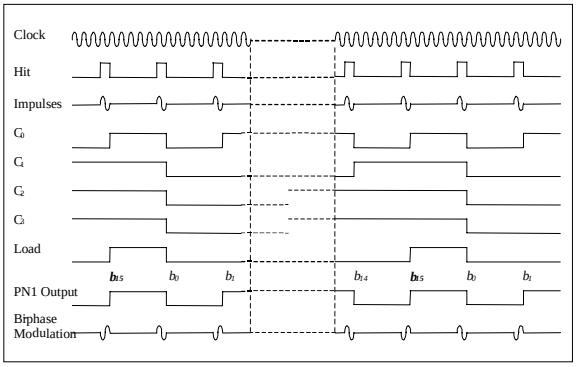

Figure 8: Pulse generator with bi-phase modulation chronograms

b) Pulse generator configuration with PPM modulation

PPM modulation is based on the principle of encoding information with two positions in time, referred to the nominal pulse position. The block diagram is presented in Figure 9.

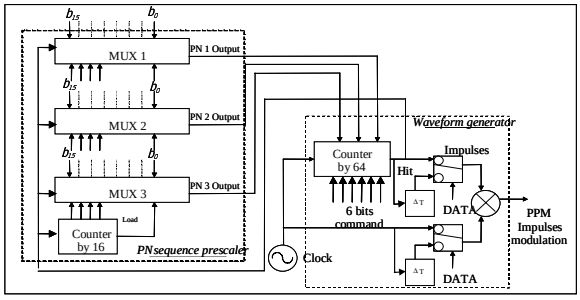

Figure 9: Pulse generator block diagram with the pulse position modulation

A pulse transmitted at the nominal position represents a 0, and a pulse transmitted after the nominal position represents a 1. In this design, one bit is encoded in one impulse, but, in general, additional positions can be used to provide more bits per symbol. The time delay between positions is typically a fraction of a nanosecond, while the time between nominal positions is typically much longer to avoid any interference between impulses. The principle used in this modulation is to change the division ratio dependent on each code values. This ratio will define the time between impulses, and thus, their position in the frame. In this design only 3 inputs are used to define the time interval between the impulses. This

implies a division ratio of N=16 so the maximum interval time is defined by: N*1/fc (for fc=7GHz and N=16 ⇒ max. interval time is 2.28ns). The data modulation is achieve by fixing a delay at the same time on the clock and the counter output. On this design, the delay is equal to one quarter of the clock period.

III. DESIGN DESCRIPTION & RESULTS

The design has been developed with a 0.18 um BiCMOS SiGe JAZZ technology featuring a 75 GHz f_T and a 90 GHz fmax. The simulations have been made for an input frequency of 7GHz and a supply voltage of 2.7V. The power consumption is 100mA. Note that 35 mA is used for buffers to perform the measurement onto a 50 ohms load.

III-1 Counter by 64 design and simulated results

This counter uses 6 JK flip flop and a few AND blocks integrated in one block. It also contains other blocks used to manage current consumption according to the division ratio. The Figure 10 and 11 show respectively the architecture of the 6 bits synchronous waveform generator's counter and the simulated chronograms. On Figure 11, we see that the b_0 to b_5 bits counter output features the desired division ratio. We also verify that the hit signal appears after 64 clock cycle.

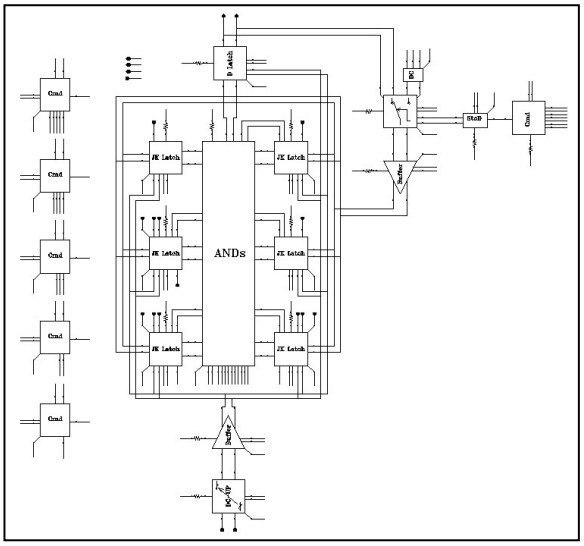

Figure 10: Simulated counter circuit

III-2 PN sequence prescaler design and simulated results

The architecture of the PN sequence's multiplexer is presented in Figure 12. On this figure we can discern four block families: buffers, memory, switches and D latch. The simulated results are shown in Figure 13. The C_0 to C_3 bits counter also features the counter by 16 division ratio to control the MUX. We also verify that the load signal appears after 16 clock cycles. Thus, the PN sequence outputs correspond to the loaded code.

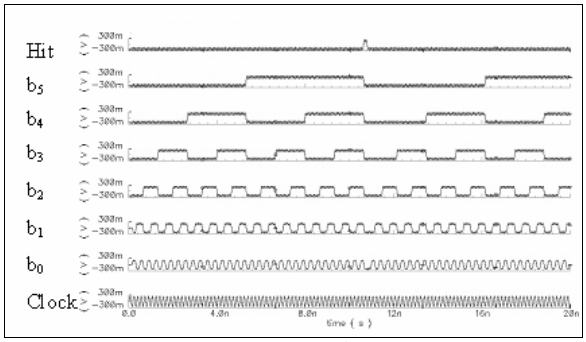

Figure 11: Simulated results of the counter by 64

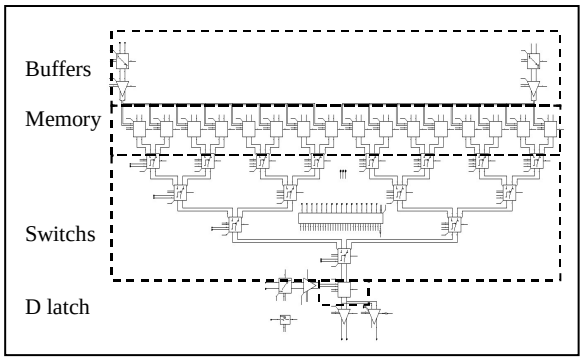

Figure 12: MUX circuit description

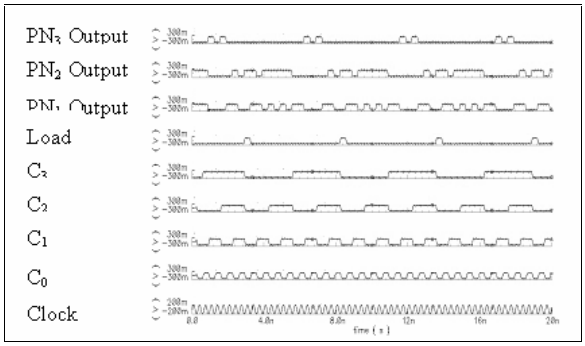

Figure 13: PN sequence prescaler simulated results

III-3 Pulse generator results with Bi-phase modulation

In Figure 14, we have plotted the simulated results of the pulse generator output for a bi-phase modulation. The output impulse features a width of 165ps with a 400 mV peak. As shown on this plot, the PN1 code modulates the impulses phase by 0 or 180°. The output spectrum corresponding to the short impulse is

presented in Figure 15. We get a wide spectrum up to 10 GHz. These results show the good functionality of the proposed pulse generator.

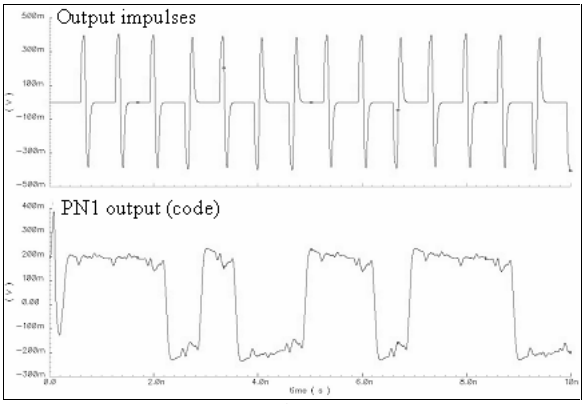

Figure 14: Simulated results of the pulse generator with the bi-phase modulation

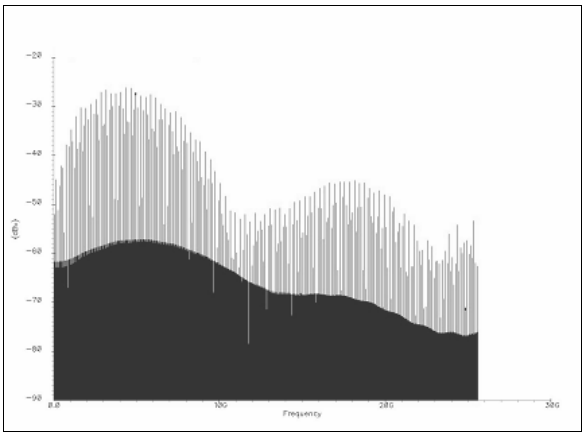

Figure 15: Ultrawide band spectrum for the bi-phase modulation

III-4 Pulse generator results with PPM modulation

We have also illustrated in Figure 16 the output pulse generator for a PPM modulation. In this configuration, the three PN sequences are enabled and modulate the impulses. The figure illustrates clearly that the division ratio is modulated by the code which imposes the pulse position in the frame. The achieved results show the validity of the developed configuration for the PPM modulation. In the same way, we have been able to verify that the data impose the pulse position in the slot.

IV. CONCLUSION

In this paper, we have presented the design of an integrated pulse generator. We have included in the same circuit the pulse generator function with the bi-phase and PPM modulation currently used in UWB systems. These interesting features allow the use of different configuration (PRF modifications, modulation type, pulse width …). The simulated results show very interesting performances as well as the feasibility of such a circuit on silicon. The implementation is on going (The counter by 64 layout is presented in Figure 17). Measurement results should be available by the end of the second semester of 2003.

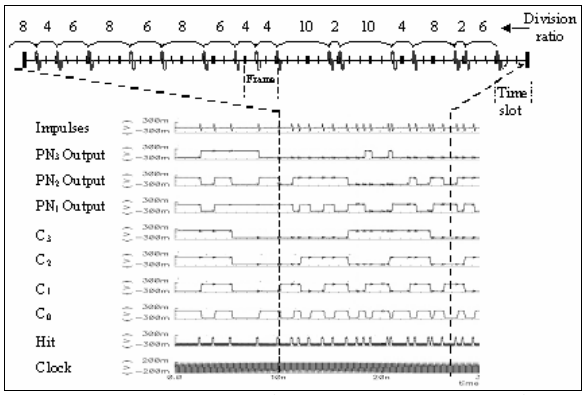

Figure 16: Simulated results of the pulse generator with thef PPM modulation

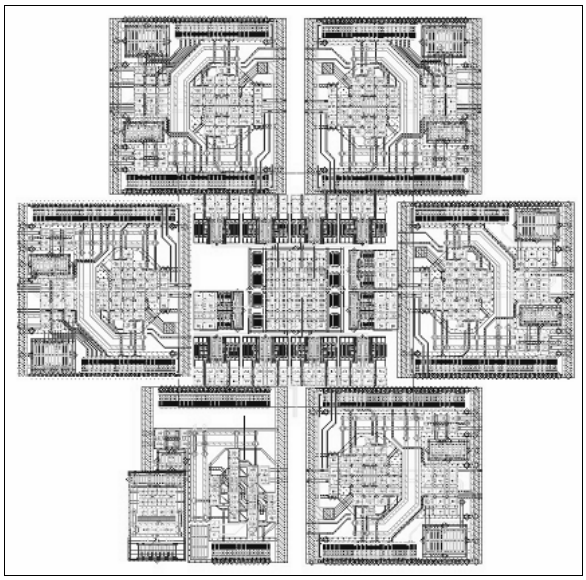

Figure 17: Counter by 64 layout

V. REFERENCES

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