Challenges in Hardening Technologies Using Shallow-Trench Isolation

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ABSTRACT

Challenges related to radiation hardening CMOS technologies with shallow-trench isolation are explored. Results show that trench hardening can be more difficult than simply replacing the trench isolation oxide with a hardened field oxide.

DISCLAIMER

I. Introduction

In the past, commercial technologies have often employed local oxidation of silicon (LOCOS) for transistor isolation. Commercial LOCOS oxides are inherently soft to ionizing radiation due to positive charge buildup in the oxide. Figure 1 shows the cross section of a transistor with LOCOS isolation illustrating positive charge buildup near the SiO_2/Si interface in the bird's beak regions. Because of its radiation sensitivity, manufacturers of radiation-hardened CMOS ICs have typically avoided LOCOS isolation and normally use specially designed hardened field oxides for transistor isolation.

In recent years, many commercial CMOS IC suppliers have replaced their LOCOS isolation with shallow-trench isolation for advanced submicron technologies. This is because trench isolation is more compatible with planarization techniques and high-density circuits. Figure 1 shows a typical layout for trench isolation. At first glance, it appears that one might be able to retrofit a commercial IC process using trench isolation for radiation hardness by replacing the trench insulator with a hardened field oxide.

In this work, we discuss issues associated with developing radiation-hardened trench isolation. We show that this can be more difficult than simply replacing the non-hardened trench isolation with traditional hardened field oxides and planarizing the surface by chemical/mechanical polishing. Results using the three-dimensional device simulator DAVINCI [1] are used to illustrate potential problems with hardening the trench and to provide insight into process and design changes that could be made to develop a radiation-hardened shallow-trench process.

II. Experimental Details

All devices were fabricated in Sandia's Microelectronics Development Laboratory in a half-micron CMOS technology using shallow-trench isolation. The original version of this 5V technology (CMOS6) was unhardened and used LOCOS isolation. Initial development efforts to convert this technology to a shallow-trench isolation technology focused primarily on replacing the LOCOS field isolation with 500-nm deep trench isolation etched into the silicon between active devices. The gate-oxide thickness for the technology is 12.5 nm, n-channel transistors are fabricated on p-type epitaxial substrates (1.5×10^{16} acceptors/cm^3); and p-channel transistors are fabricated in n-wells with a surface concentration of $\sim 10^{17}$ donors/cm^3. Data are also presented for metal-gate capacitors with standard hardened field oxide structures.

Both transistors and capacitors were irradiated using a 10-keV x-ray source at room temperature. Radiation-induced threshold-voltage shifts, ΔV_{th}, as well as components due to oxide- and interface-trap charge, ΔV_{ot} and ΔV_{it}, were estimated from transistor current-voltage measurements at room temperature using the midgap charge-separation technique [2]. The n- and p-channel transistor threshold voltages were extrapolated from linear least-squares fits to the square-root of the drain-to-source current versus gate-to-source voltage curve in the saturation region at $\pm$ 5 V. For the capacitors, high frequency (1-MHz) C-V traces were recorded by sweeping the gate from inversion to accumulation. ΔV_{ot} and ΔV_{it} were estimated from midgap voltage shifts and midgap-to-flatband stretchout, respectively [2].

III. Results

We first illustrate the total-dose hardness of transistors processed with the straightforward approach of forming a traditional hardened field oxide in the shallow-trench isolation. Simple capacitor test structures (silicon/hardened field oxide/metal gate) fabricated using this same hardened field oxide show little charge buildup after irradiation at 5V to total doses above 1 Mrad(SiO_2). Thus, it might be expected that transistors and ICs fabricated with this hardened field oxide would be hard to at least 1 Mrad(SiO_2), consistent with previous IC data using a comparable planar field oxide [3]. Figure 2 is a series of subthreshold current-voltage (I-V) curves measured on 0.75 x 20-µm n-channel transistors irradiated in steps to 1 Mrad(SiO_2) at a dose rate of 167 rad(SiO_2)/s using a 10-keV x ray source. The I-V curves were taken less than 1 minute following exposure. The gate-to-source bias during irradiation was 5V. The data exhibit excess leakage current due to radiation-induced charge buildup in the field oxide [4] at total dose levels greater than 20 krad(SiO_2). At only 100 krad(SiO_2), the drain-to-source leakage current at 0V gate-to-source bias exceeds 1 µA. These results are similar to those obtained for the *unhardened* CMOS6 technology using LOCOS isolation. (Data for the unhardened process will be presented in the full paper).

High leakage currents at relatively low total doses were also observed for identically processed ICs. 16K-bit SRAMs

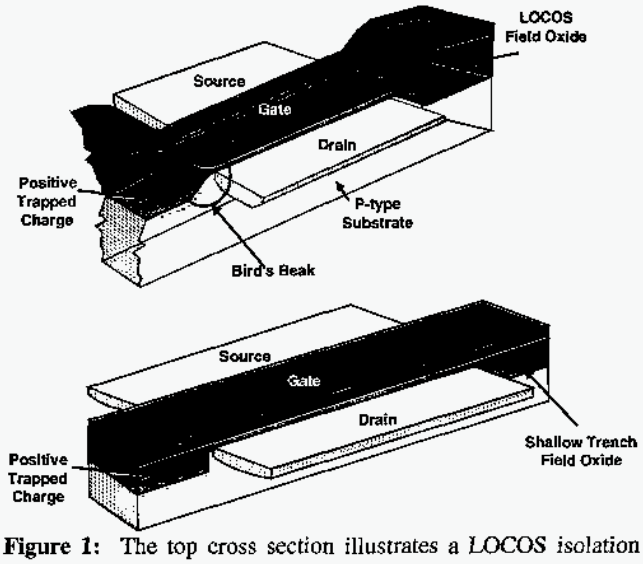

Figure 1: The top cross section illustrates a *LOCOS isolation* that is commonly used for commercial CMOS technologies. The bottom cross section illustrates shallow-trench isolation.

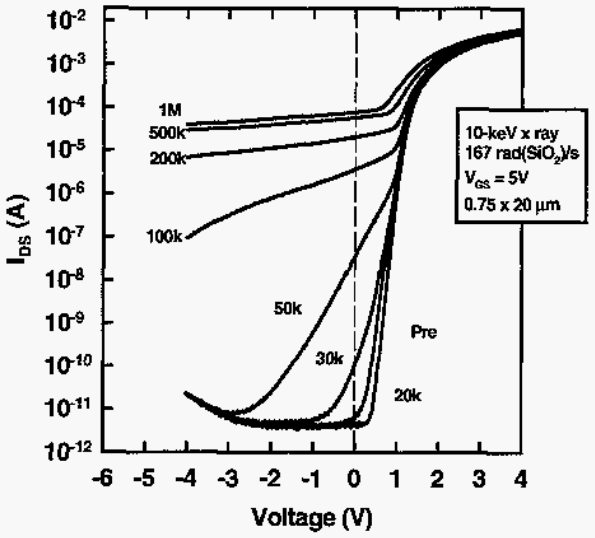

Figure 2: I-V curves for n-channel transistors irradiated in steps to 1 Mrad(SiO_2) using 10 keV x-rays.

failed functionally at total dose levels from 80 to 100 krad(SiO_2). Edge leakage was identified as the primary failure mechanism. As expected [5,6], there is a good correlation between n-channel transistor I_{DS} (V_{GS}=0V) and 16K-bit SRAM static leakage current (I_{DD}) as illustrated in Figure 3. Thus, these data suggest that we cannot simply harden the trench isolation in this technology by using the traditional hardened field oxide [3] as the trench insulator.

Figure 4 is a cross-section of a trench isolated transistor illustrating two possible leakage paths caused by parasitic field-oxide transistors in parallel with the gate-oxide transistor. The sidewall leakage path from source to drain in the n-channel transistor has been determined to be the primary leakage path for the devices examined in this work. Leakage from n+ to n-well beneath the trench has been eliminated in the n-channel transistor test structure used to obtain the data in

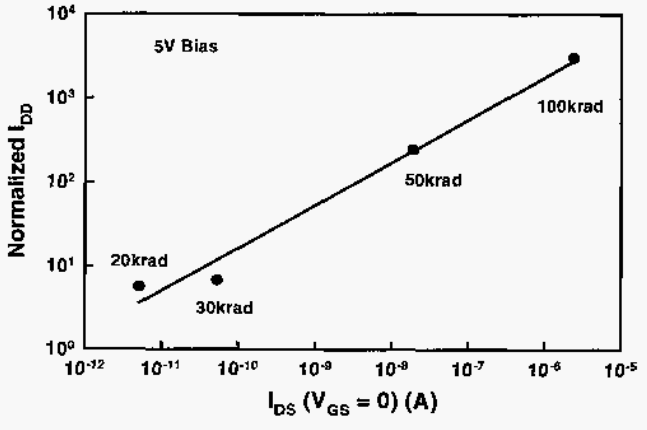

Figure 3: The change in 16K-bit SRAM static power supply leakage current normalized to its preirradiation value versus transistor I_{DS}(V_{GS}=0). Transistors and SRAMs were biased at 5 V during irradiation.

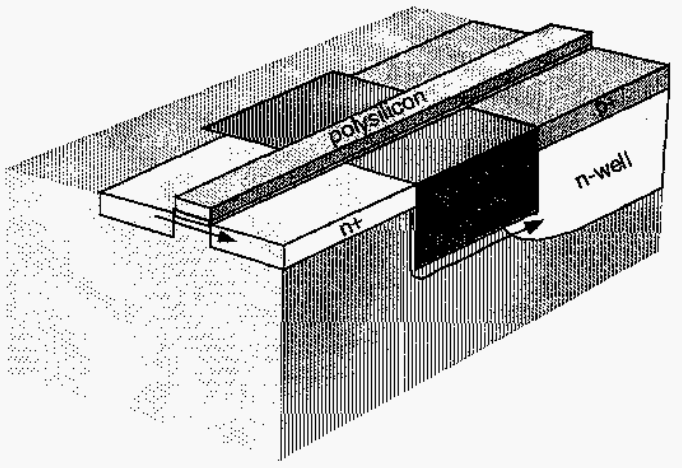

Figure 4: Arrows indicate two possible parasitic leakage paths in a shallow trench technology.

Figure 2 because there is no n-well near this test structure.

Because of the inherent design of the shallow-trench isolation, the effective insulator thickness between the polysilicon gate electrode contact and the trench sidewall varies throughout the field oxide region. As a result, the electrostatic potential throughout the field oxide isolation region can vary significantly. A contour plot of the electrostatic potential throughout a trench region as simulated by DAVINCI is illustrated in Fig. 5. The simulation assumes the trench isolation is even with the gate oxide such that the surface is level (it is difficult, if not impossible, to ensure the trench insulator extends above the trench edge and is level [7]). The electrostatic potential was simulated with the n+, p+, and p-epi/substrate regions biased at 0V. The polysilicon gate across the top of the structure (not shown) and n-well were biased at 5V. In the top part of the figure, we show a magnified view of the electric field magnitude in the region where the source-to-drain n-channel sidewall leakage path exists. The electric field exceeds 4.5 MV/cm at the Si corner. In fact, the electric field near the p+ region (not shown) exceeds 6 MV/cm. The larger electric field by the p+ region is attributed to the work function difference between the two regions [8]. As shown below, the high electric fields in the corners can help to explain the increased transistor leakage current for the case where the trench regions were processed using a typical hardened field oxide (Fig. 2). It is also of interest to point out that these corner regions have been shown to reduce gate oxide integrity [9] and cause anomalous humps in the subthreshold I-V characteristics [7,9-11]. This problem is enhanced if the trench isolation is recessed below the trench corner and the gate oxide is permitted to wrap around the corner.

A higher electric field can lead to increased threshold voltage shifts for traditional field oxides. Figure 6 is a plot of flatband, oxide-trap charge, and interface-trap charge voltage shifts versus applied field for capacitors irradiated to 10 krad(SiO_2). The capacitors were fabricated using the same hardened field oxide as that used in the trenches. For electric

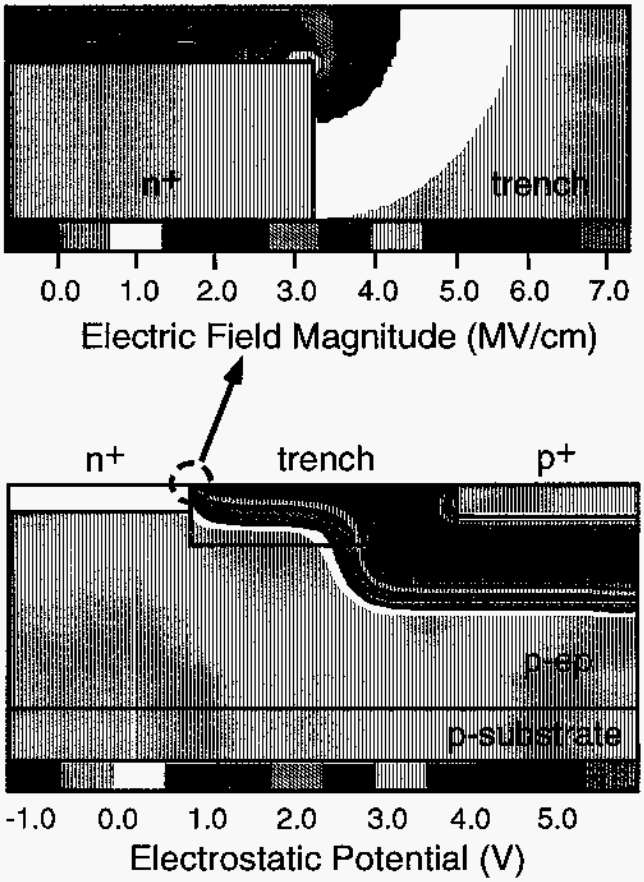

Figure 5: Electrostatic potential in the trench region is shown in the bottom cross section with n+, p+, and p-epi biased at 0V. The polysilicon gate (not shown) and n-well are biased at 5V. The top cross section illustrates the electric field magnitude near the corner of the trench.

fields greater than ~0.7 MV/cm, there is a rapid increase in ΔV_{fb} and ΔV_{ot} with applied field. As a result, high hardness levels are achieved at the low electric fields typical of conventional planer hardened field oxides. However, as indicated in Figure 5, for trench isolation, very high fields (and poor hardness levels) can be obtained at the edges of the trench under normal operating conditions. Thus, the increases

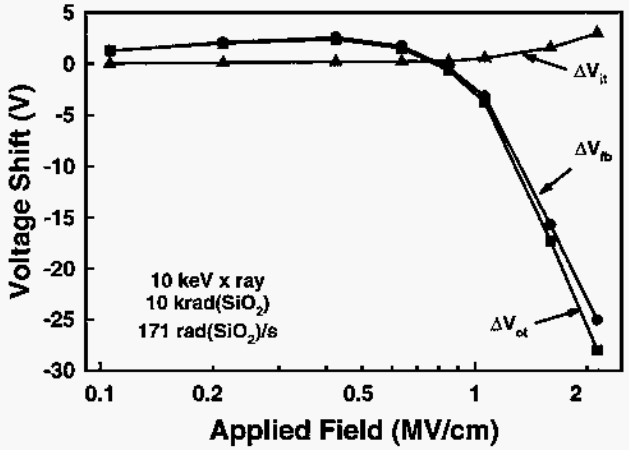

Figure 6: Voltage shift versus applied electric field for hardened field oxide capacitors irradiated to 10 krad(SiO_2).

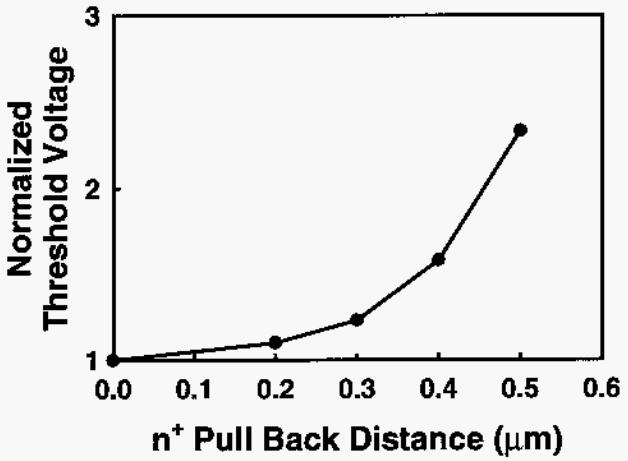

Figure 7: DAVINCI simulation of the change in parasitic field oxide transistor threshold voltage normalized to its initial value before the pull back versus the distance the n+ regions are pulled back from the trench side wall.

in ΔV_{fb} and ΔV_{ot} in Figure 6 at high electric fields are consistent with the high transistor leakage current data shown in Figure 2.

There are numerous methods that can be envisioned to reduce the electric fields near the trench edges. One logical method is to increase the oxide thickness at the corners of trenches. However, this method likely will include increased processing steps with additional mask levels. If high fields must be tolerated, it may be necessary to (1) develop field insulators that are not significantly affected by high-field irradiation, or (2) reduce the effect of charge buildup in the field oxide by increasing the threshold voltage of the parasitic field oxide transistors. The field threshold voltage can be increased by pulling back the source and drain regions (n+ implants) from the trench edges and/or increasing the sidewall doping (p+ implant) [10,12,13]. (This is similar to the approach of forming guardbands that was used in early radiation hardened CMOS technologies.) The disadvantage to the pullback approach is that chip area must be sacrificed. However, even if the n+ implants are pulled back for trench isolation, it is possible that the final device area can still be made less than it would be for LOCOS isolation with its birds beak. We have simulated the increase in the n-channel parasitic field oxide transistor threshold voltage that might be obtained by pulling back the n^+ source/drain implants from the trench edge. These simulations did not take into account an increase in sidewall doping that could also be implemented. Figure 7 is a plot of the simulated normalized threshold voltage in the edge region versus the distance that the n+ region is pulled back from the trench. As the pullback distance increases, there is a rapid increase in threshold voltage. With a 0.5-μm pull back, the threshold voltage is increased by more than a factor of 2, which can significantly improve the radiation response of the technology.

While the data presented above suggest that hardening shallow-trench isolation may be more difficult to achieve than using traditional hardened field oxides, the task is achievable.

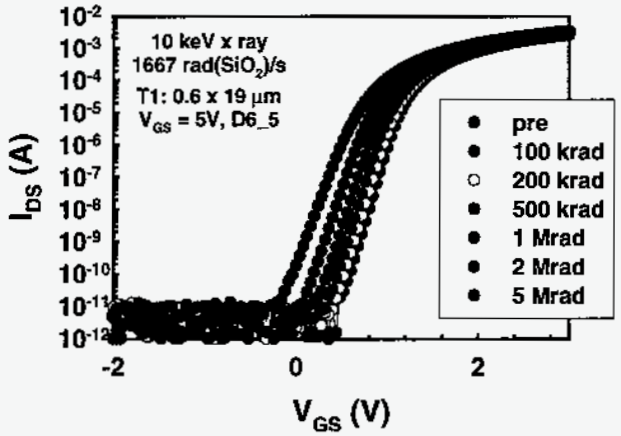

Figure 8: I-V curves for n-channel transistors irradiated in steps to 1 Mrad(SiO_2) using 10 keV x-rays.

In fact, Sandia has successfully developed a radiation-hardened half-micron CMOS shallow-trench technology that is referred to as CMOS6r. The technology also uses feedback resistors for single event upset immunity [14]. Transistors from this technology show no indication of field oxide leakage for total doses up to 5 Mrad(SiO_2) in contrast to the devices of Figure 2. I-V characteristics measured on n-channel transistors from this technology irradiated in steps to 5 Mrad(SiO_2) using 10-keV x rays are shown in Figure 8. In addition, 16K-bit SRAMs have also been irradiated to 5 Mrad(SiO_2) using 10-keV x rays at 5V bias. No functional failures were observed. IC parametric degradation will be shown in the full paper.

IV. Summary

Retrofitting a commercial CMOS process using trench isolation is more complex than simply replacing the trench insulator with a traditional hardened field oxide. High electric fields at the edges of the trench may limit the total dose radiation hardness. We have used device simulations to illustrate one technique (n+ pullback) for reducing the impact of high electric fields at the corner of the trenches. In addition, other techniques can be used to reduce the electric field in the oxide at the trench edges or to increase the threshold voltage of the parasitic trench field oxide transistors (e.g., doping of side walls).

Acknowledgments

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