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Challenges in the Packaging of MEMS

Ajay P. Malshe
High Density Electronics Center (HiDEC)
Department of Mechanical Engineering
204 Mechanical Engineering Building
University of Arkansas
Fayetteville, AR 72701-1201
Phone: (501) 575-6561
Fax: (501) 575-6982
e-mail: apm2@engr.uark.edu

Chad O'Neal
High Density Electronics Center (HiDEC)
Department of Mechanical Engineering
204 Mechanical Engineering Building
University of Arkansas
Fayetteville, AR 72701-1201
Phone: (501) 575-5303
Fax: (501) 575-6982
e-mail: nco@engr.uark.edu

Sushila B. Singh
High Density Electronics Center (HiDEC)
Department of Mechanical Engineering
204 Mechanical Engineering Building
University of Arkansas
Fayetteville, AR 72701-1201
Phone: (501) 575-6561
Fax: (501) 575-6982
e-mail: ss22@engr.uark.edu

William D. Brown
High Density Electronics Center (HiDEC)
Department of Electrical Engineering
3217 Bell Engineering Center
University of Arkansas
Fayetteville, AR 72701-1201
Phone: (501) 575-6045
Fax: (501) 575-7967
e-mail: wdb@engr.uark.edu

William P. Eaton
Reliability Physics Department
Sandia National Laboratories
PO Box 5800
Albuquerque, NM 87185-1081
Phone: (505) 845-8209
Fax: (505) 844-2991
e-mail: weaton@sandia.gov

William M. Miller
Reliability Physics Department
Sandia National Laboratories
PO Box 5800
Albuquerque, NM 87185-1081
Phone: (505) 844-7161
Fax: (505) 844-2991
email: millerwm@sandia.gov

Abstract

The packaging of Micro-Electro-Mechanical Systems (MEMS) is a field of great importance to anyone using or manufacturing sensors, consumer products, or military applications. Currently much work has been done in the design and fabrication of MEMS devices but insufficient research and few publications have been completed on the packaging of these devices. This is despite the fact that packaging is a very large percentage of the total cost of MEMS devices. The main difference between IC packaging and MEMS packaging is that MEMS packaging is almost always application specific and greatly affected by its environment and packaging techniques such as die handling, die attach processes, and lid sealing. Many of these aspects are directly related to the materials used in the packaging processes. MEMS devices that are functional in wafer form can be rendered inoperable after packaging. MEMS dies must be handled only from the chip sides so features on the top surface are not damaged. This eliminates most current die pick-and-place fixtures. Die attach materials are key to MEMS packaging. Using hard die attach solders can create high stresses in the MEMS devices, which can affect their operation greatly. Low-stress epoxies can be high-outgassing, which can also affect device performance. Also, a low modulus die attach can allow the die to move during ultrasonic wirebonding resulting to low wirebond strength. Another source of residual stress is the lid sealing process. Most MEMS based sensors and devices require a hermetically sealed package. This can be done by parallel seam welding the package lid, but at the cost of further induced stress on the die. Another issue of MEMS packaging is the *media compatibility* of the packaged device. MEMS unlike ICs often interface with their environment, which could be high pressure or corrosive. The main conclusion we can

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draw about MEMS packaging is that the package affects the performance and reliability of the MEMS devices. There is a gross lack of understanding between the package materials, induced stress, and the device performance. The material properties of these packaging materials are not well defined or understood. Modeling of these materials and processes is far from maturity. Current post-package yields are too low for commercial feasibility, and consumer operating environment reliability and compatibility are often difficult to simulate. With further understanding of the materials properties and behavior of the packaging materials, MEMS applications can be fully realized and integrated into countless commercial and military applications.

Introduction

Microelectromechanical Systems (MEMS) consist of mechanical devices and machine components ranging in size from a few microns to a few hundred microns. They can be the mechanical interconnects of microsystems, and are categorized as either sensors or actuators. These devices generally integrate signals from one physical domain to another, such as mechanical-to-electrical, electrical-to- mechanical, electrical-to-chemical, etc.

MEMS sensors are devices such as pressure sensors, accelerometers, and gyrometers that perceive an aspect of their environment and produce a corresponding output signal. Actuators are devices that are given a specific input signal on which to act and a specific motion or action is produced. Some examples of MEMS actuators are: microengines, microlocks, and discriminators. Sensors can be thought of as being passive, waiting on a signal from the environment to elicit a response, while actuators are activated by the user. The sources of motion for MEMS elements such as gears or microlocks are usually electrostatics, thermoactuation, wobble motors, and with limited success, even microsteam engines [1]. These "motors" provide the mechanical input required to activate the actuators and can be used with a gear train to raise or lower a micromirror for a digital light processing application. As well, these microengines produce the motion of a linear actuator or activate a weapon safety system which requires motion of the mechanical locking elements [2], [3], [4].

In the state-of-the-art manufacturing, MEMS are fabricated using manufacturing processes and tools borrowed from the microelectronics industry. Many of these processes and tools are used directly, while others have been modified to meet the specific needs of MEMS [5]. The devices are either produced using successive deposition and selective etching of polysilicon layers on top of the silicon substrate (surface micromachining), by etching into the silicon substrate using anisotropic etchants and heavily doped etch stops (bulk micromachining), or high aspect ratio micromachining (HARM). Surface micromachining currently uses up to 5 layers of polysilicon for device design [1]. Geartrain structures, microengines, microsteam engines, and micromirrors for digital light processing are just some of the devices that can be fabricated using surface micromachining [1]. Bulk micromachining is used to fabricate structures like cantilevers, bridges, or channels, as well as many more complicated devices [1]. HARM includes processes such as LIthographie, Galvanoformung, and Abformung, (i.e. lithography, electroplating and molding), (LIGA) and deep silicon reactive ion etching (RIE) [1], [6], [7]. LIGA is a German acronym for a micromolding process and is one method of creating high aspect ration microstructures. These HARM processes are able to create free standing structures up to a few hundred microns in height [1].

MEMS fabrication also differs from integrated circuit (IC) fabrication in other ways. For instance, MEMS do not currently follow the very large scale integration (VLSI) paradigm. The development cycle is long and often several design cycles are required to comply with design specifications [8]. This is because often the products, as well as the technologies are being developed simultaneously. MEMS design and fabrication is more like that of application specific integrated circuits (ASICs). There are currently relatively few generic parts that can be rearranged to create any one of thousands of different devices in the manner that resistors, transistors, and capacitors can be arranged in IC design [8]. Research laboratories like Sandia National Laboratories in Albuquerque, New Mexico and MCNC in Research Triangle Park, North Carolina are developing libraries of different parts that can be reassembled in various configurations [9], [10]. This allows faster design times, and increased modularity of the devices. There are so many different fields of application for MEMS that we may never see the level of modularity that ICs have.

Although fabrication techniques can be carried over from IC to MEMS technology, the requirements of MEMS packaging are different from those of IC packaging. Unlike IC die packaging, MEMS dice need to interface with the environment for sensing, interconnection, and/or actuation [11]. MEMS packaging is application specific and the package allows the physical interface of the MEMS device to the environment [11]. In the case of a fluid mass flow control sensor, the medium flows into and out of the package. Harsh environments may create different challenges for the packaging of MEMS [11]. These types of packaging are referred to as media compatible

packaging. In addition to challenges related to the environment of the MEMS chip and interfacing it with the environment, challenges also exist inside the MEMS package with the die handling, die attach, interfacial stress, and outgassing [12]. These new challenges in the field of MEMS packaging need immediate research and development efforts.

To date, most of what is known about MEMS packaging remains proprietary and published literature is scarce. The challenges of MEMS packaging have been known for some time, but little open research has been done to collect data and work toward meeting these challenges [12]. A disproportionality exists between the resources spent on the packaging of MEMS and the time spent researching MEMS packaging. Currently, the cost of MEMS packaging typically accounts for 75% or more of the sale price of the device [13].

The motivation for overcoming the challenges associated with MEMS packaging is the low cost and the ubiquitous applications of MEMS. MEMS could be used to create *smart* systems in almost any existing application one could imagine, as well as many new applications never before possible. Everything from tire pressure sensors, to undefeatable weapon system locks, space applications, and surgical procedures are possible [1]. MEMS packaging is already far behind the capabilities of MEMS designers, and it is the purpose of this paper to share the challenges of MEMS packaging and create an awareness of and an interest in MEMS packaging within the packaging community.

Challenges in MEMS *System* integration

There is a philosophical difference between the motivation for packaging ICs and packaging MEMS. The goal of IC packaging is to provide physical support for the chip, provide an electrical interface to active chip(s) in the system, supply signal, power, and ground interconnections, and allow heat dissipation [14]. Also, a package must effectively isolate the chip physically from its environment. MEMS devices, on the other hand, often are intimately interfaced with their environment [11]. Figure 1 shows a comparison between a typical DIP IC package and a MEMS pressure sensor package, which has an opening to sense pressure variation. Another issue is the media compatibility of the MEMS package. MEMS devices may need to operate in diverse environments or media such as under automobile hoods, with intense vibrations, and in salt water, strong acids, alkaline or organic solutions [11]. In conclusion, the package, while performing detection or actuation, must be able to withstand the environment(s) [11].

Another challenge in MEMS packaging is the effect that packaging parameters have on reliability. The package is part of the complete system and all aspects must function together and must be compatible with each other. This determines which materials and what design considerations and limitations become important. One of the main scientific challenges of MEMS is the issue of material properties. The properties of the materials depend on how they are used, processed, the heat treatments to which the materials are subjected, and even the specific pieces of equipment used during fabrication. Not all the materials used react in the same way to these parameters, so compromises must be made. Some materials may be hard to obtain with R&D production run numbers. Low quantities of materials are used, and suppliers are reluctant to sell small quantities or develop new products for limited markets [12]. One good point about the materials used in microsystems is that the material properties generally get better at the microscale. This is due to a decrease in the number of defects encountered in the materials. The defect density remains about the same as in the macroscale, but since the MEMS devices are so small, the chance of a killer defect occurring in a device is reduced.

Packaging of MEMS dice is application specific, and hence, desired process steps could vary significantly. Thus, it is important to classify MEMS dice by their packaging requirements and then develop the packaging standards and related knowledge base. The device and the package should be designed concurrently with the application and the environment in mind from the project conception.

Table 1 summarizes the different techniques that can be used to meet the various packaging parameter challenges. These solutions are not complete or foolproof, but are techniques that have been exercised and that provide direction for further research.

Release and Stiction

Releasing of the MEMS dice is an important step in MEMS packaging. Typically, the polysilicon features are surrounded by silicon dioxide which protect the features and prevents them from becoming damaged or contaminated. This oxide must be etched away, freeing the devices before they are operational. This is done using

an HF etch, which is selective between SiO_2 and Si [1]. The dilemma on this issue is when it should be done. It is most economically done in wafer form as a batch process, but this leads to almost certainty that contamination of the devices and damage during the dicing of the released wafer will occur. The cooling fluid will obliterate the tiny mechanical devices. The most inefficient time is after dicing since each chip must be released individually rather than the entire wafer at once. The MEMS features, however, do remain protected throughout the potentially lethal dicing stage.

There is also a risk of stiction during and after the release. Stiction occurs from the capillary action of the evaporating rinse solution in the crevices between elements, like cantilevers and the substrate[1]. This stiction can render the MEMS devices useless after all the resources have already been invested in them. An example of stiction is shown is Figure 2. The beam-type element has been pulled down to the substrate by the capillary forces. Preventing stiction from occurring after release is also a major challenge to be dealt with. Some methods that are effective are freeze drying and supercritical CO_2 drying [1]. These methods remove the liquid surface tension from the drying process, preventing stiction from occurring. This, however, does not prevent stiction throughout the lifetime of the device. For this, the surface should be roughened to minimize contact area, or non-stick coatings can be applied to the device surfaces. Stiction can also be reduced in the design process by using dimples in regions of the device where stiction may be a problem [1], [15]. These small protrusions on the bottom on an element can greatly reduce the contact area between the MEMS device element and the substrate. Figure 3 shows a cantilever beam with dimples on the bottom surface.

Dicing

Another challenge in MEMS packaging is dicing the wafer into individual dice. Dicing is typically done with a diamond saw a few mils thick. This requires that coolant flow over the surface of the very sensitive dice along with silicon and diamond particles that are generated during sawing, which is deadly to these devices. These particles, combined with the coolant, can contaminate or even destroy the devices. The fluid can simply wash the features off the surface of the wafer. Contaminants can get into the crevices of the features, causing the devices to fail [1]. An alternative to dicing is wafer cleaving. Wafer cleaving is commonly done in III-V semiconductor lasers and has applications in MEMS [16]. Cleaving does not require coolant and does not generate nearly as many particles as sawing. Laser sawing and wafer-level encapsulation are two other methods that can decrease the hazards of dicing, but increase the cost of the processing and assembly. When considering higher cost processing technologies such as these, it is important to remember to consider the cost for the entire process of manufacturing a part.

Die Handling

Die handling is another area of MEMS system fabrication and assembly which is currently not meeting the requirements of MEMS. Because of the delicate surface features of MEMS, these chips cannot be moved using vacuum pick-up heads as in traditional IC die assembly. The MEMS dice must be picked up and handled by the edges, which will require new infrastructure for the automated handling of MEMS. Handling chips by the edges is more difficult than by the top surface because of greatly reduced surface area and increased dexterity requirements of the pick-and-place equipment. These MEMS die handling fixtures could be fingers or clamps that delicately handle the MEMS dice by their edges, or collets that fit existing pick-and-place equipment. In order to handle the high volumes of MEMS chips, die handling fixtures and methods that handle the chips by the edges will become commonplace in intermediate to high volume MEMS packaging houses.

Wafer Level Encapsulation

Wafer level encapsulation eliminates the need for special die handling fixtures. With wafer level encapsulation, a capping wafer is bonded to the top of a device wafer and when diced, each MEMS chip has a protective lid attached to it. These wafers can be bonded in a vacuum to produce a permanent vacuum inside each device chip. The wafer bonding can be done using direct bonding, but the required temperature is about 1000° C [17]. Glass frit or anodic bonding is more commonly used because the processing temperature is between 450 and 500° C [12]. However, the glass frit may cause stress in the die if the glass is not chosen with a coefficient of thermal expansion (CTE) close to that of silicon. Anodic bonding requires high voltage, which can also be a

disadvantage for integrated systems combining MEMS and IC devices on a single chip [1]. Wafer level encapsulation is not the cure-all for die handling incompatibilities. However, it is unique to semiconductor sensor packaging and adds considerable cost to the sensor die because of the added fabrication steps and increased die area required.

Stress

When polysilicon is deposited, a great deal of stress is created in the films. Most of this stress can be annealed out at a temperature of around 1000° C, and is most effective if the polysilicon is deposited amorphously and then annealed to form a polycrystalline structure [18]. This creates the lowest stress arrangement with the fewest defects in polysilicon. The second source of stress results from the die attach material at the interface between the MEMS die and the package substrate. Depending on the die attach material and CTE mismatch between the package and the chip, interfacial stress can develop within a MEMS package [19].

A major drop in reliability can be caused by excess stress in the package. This stress can be caused by stress inducing fabrication processes, CTE mismatch in the die attach, lid sealing, or shrinkage during the attach curing. The results of stress are that the devices may deform, gear teeth may become misaligned, tensile stress may cause the resonant frequency to increase and result in device breakage, and excessive compressive stress causes long beam elements to buckle. Packaging stresses can induce both offset and scale factor shifts in sensors. The use of hard solders like AuSn or AuSi can put excessive stress on the delicate components and cause the features, as well as the die itself, to warp or fail [20], [21].

Stress effects also worsen as chip sizes increase. MEMS chip sizes may be larger than many IC chips since the feature sizes are larger and the devices typically require more die area. This stress can be reduced by using lower modulus die attach materials that deform as the chip and package expand and contract [20]. These low modulus die attach materials may also allow creep over time. Stress relaxation can be very bad in die attach materials because a change in the stress state will lead to changes in device performance (resonant frequency, offset, scale factor shifts). Although high stress may be undesirable, it is also undesirable for the stress state to change over time [22].

Outgassing

When epoxies or cyanate esters are used for die attach, they outgas as they cure [23]. The water and organic vapors may then redeposit on the features, in crevices, and on bond pads. This leads to device stiction and corrosion. Die attach materials with a low Young's Modulus, like epoxies, also allow the chip to move during ultrasonic wirebonding, resulting in low bond strength, which has been documented in certain pressure sensors [9]. Possible solutions to outgassing challenges include very low outgassing die attach materials and the removal of outgassing vapors during die attach curing.

Testing

Testing these devices is also an issue. No one wants to package a bad chip, it is too expensive and too time consuming. However, currently this is the only way to implement certain tests on MEMS devices. All testing that can be accomplished from wafer-level probing should be done at the wafer level, and finish testing with cost effective, specially modified test systems that test the devices after packaging.

State-of-the-Art in MEMS Packaging

The present state-of-the-art in MEMS is combining MEMS with ICs and utilizing advanced packaging techniques to create complex MEMS systems. One application is to put CMOS and MEMS on one chip. The challenge is that the processing steps for CMOS and MEMS are not compatible. For instance, the high temperature anneal destroys the diffusion profiles and aluminum interconnects used in the CMOS devices. There are three main methods that have been used to create the monolithic integration of CMOS and MEMS: (1) Electronics First (University of California, Berkeley), (2) MEMS in the Middle (Analog Systems), and (3) MEMS First (Sandia National Laboratories) [1].

One of the most recent efforts of monolithic integration has been Sandia's MEMS First effort in which the

MEMS are first fabricated in an etched trench then covered with a sacrificial oxide. After the trench is filled completely with SiO_2, the surface is planarized [1]. This flat surface serves as the starting material for the CMOS foundry. The sacrificial oxide covering the MEMS is removed after the CMOS devices are fabricated. This protects the MEMS devices from the CMOS processing steps [1], [24]. Figure 4 is a schematic of Sandia's MEMS First approach to monolithic integration. An alternative approach to monolithic integration is the use of Multi-chip Modules (MCM) [25]. IC and a MEMS dice can be placed in the same package, eliminating these processing incompatibilities.

Advanced packaging techniques like MCM and flip chip are being actively pursued for use with MEMS [26]. The idea of MCM is that several different MEMS sensors and actuators, or a combination, can be combined into a single package forming complex systems that can perform several functions or subfunctions of a larger process. These MCM systems should be modular and any number of them could be constructed from the available MEMS sensors and actuators [25]. This opens the already nearly limitless range of applications for systems of much greater complexity.

A downside to MCM use is signal loss and apparent added packaging expense. This signal loss is especially noticable with some capacitive devices. For some of these devices, the capacitance changes being sensed are less than a femtofarad. A single 100 micron by 100 micron bond pad can add a picofarad of capacitance, thereby swamping the desired signal change [27]. In these applications, one may put detection circuitry right next to the MEMS device in order to decrease the effects of parasitic capacitance. The apparently greater cost of packaging is due to the issue of known good die (KGD), or pretested dice, that are known to work before being placed into the MCM. MCMs also have larger packages sizes that do cost more than a single chip package. Also depending on the MCM requirements, the substrate can be a major part of the packaging costs if it requires multiple layers and high density signal lines. Stress can also be increased from the larger package dimensions [14]. The disposibility of MCM packaged systems becomes much less palatable, and the cost of rework more acceptable.

Surface micromachining is categorized by the number of active layers in the process. The layers simply stack on top of each other as the number of levels increases. The more levels, the more design potential and the more complex the device can become. Sandia National Laboratories recently unveiled their state-of-the-art 5 layer process with several new, more complex devices. These surface micro-machined devices can now be up to 12 microns tall and much stronger and more robust than with the previous four layer technology [9].

The next state-of-the-art process is the idea of lab-on-chip. This is the concept of several sensors and actuators on a single chip, or in the same package using MCM technology, forming a mixed signal system that will fulfill a function or group of functions. Mixed signal in this sense refers to input and/or output signals that can be mechanical, electrical, magnetic, optical, biological, acoustical, chemical, etc. There are several directions researchers are going with the concept of lab-on-chip. There are applications involving chem-lab-on-chip where the object is to create several sophisticated chemical sensors on a single chip [27]. Another application is an optical bench on a chip which utilizes semiconductor lasers, beam splitters, movable mirrors, lenses, etc., to make a miniaturized version of an optical bench [28]. Also, efforts have been made toward a DNA lab on a chip where the polymerase chain reaction (PCR) is carried out to amplify DNA and then various separation techniques are used to analyze the DNA [29].

Due to the size of MEMS devices, it is best to have non-contact signal interfaces with the environment. Some microdevices can be destroyed by macrosize forces, however, others can survive amazingly high force levels [30]. Mechanical signal interfaces between MEMS devices, such as geartrains, however, are commonplace. The lab-on-chip concept capitalizes on the many possibilities and advantages of MEMS. It is conceivable that an entire control panel of sensors could be reduced to hand-held size. This would have tremendous value in spacecraft and fighter jets where space and weight considerations are critical [26]. On a space expedition like the Pathfinder mission, many more experiments and observations could be made because of the increased number of sensors and instruments that would fit on board.

Summary

The role of packaging is to provide a compact housing, as well as an interface between a device and the outside world. It should protect the chip, while letting it perform its intended function cleanly with very little attenuation or distortion of the *signals*, such as electrical and/or mechanical and/or optical, etc., in the given environment, and do so at a low cost. The packaging and assembly, as well as the materials used, are integral parts of a microsystem. The total cost of processing and assembly must be taken into account when designing and

fabricating a device. Packaging is a significant portion of the total cost of a MEMS device, unlike IC packaging. Traditional front-end and back-end packaging become blurred and united in the development of the system. MEMS packaging breaks the paradigms of traditional packaging, and is an exciting field ready for additional wide-spread research and development of new applications. Currently, there is scattered research being performed related to MEMS packaging, for example, in the areas of die attach and outgassing. However, focused efforts are essential for reliable implementation of the technology.

Future Directions

In the future, the field of packaging and integration will be required to consider, not only the packaging of individual devices, but also the seamless integration of electrical (ICs) and/or mechanical (MEMS) and/or optical (integrated optics) and/or chemical, etc. devices. The advanced packaging and integration concepts need to address the packaging of individual devices as well as multi-domain devices for synergistic response in the desired environment. In particular, for MEMS devices, based on the current knowledge base, we believe that the packaging and integration could be realized in three ways:

- hybrid thick film,
- multichip module (MCM), and
- monolithic integration.

The usage of these would be guided by the application and the associated cost.

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About the Authors

Ajay P. Malshe, Ph.D. (1992), is an Assistant Professor at the Department of Mechanical Engineering and an adjunct faculty at the High Density Electronics Center (HiDEC), Department of Electrical Engineering, University of Arkansas, Fayetteville, AR. His background is materials science and engineering, and has authored more than 60

publications and holds three patents. His two distinct fields of research interest are electronic packaging, and materials and manufacturing. The electronic packaging related subjects of his interest are nano and micro systems packaging and integration, and high-density electronics packaging. He is active in IMAPS, ASME and other related professional societies.

Chad B. O'Neal received his B.S. from the Department of Mechanical Engineering at the University of Arkansas in 1998 and is currently pursuing his M.S. in mechanical engineering at the High Density Electronic Center (HiDEC) located at the University of Arkansas, Fayetteville. Mr. O'Neal is currently studying the area of MEMS packaging, specifically the effects of die attachment stress induced onto the devices and the functionality of the MEMS devices after packaging. His research of MEMS packaging is in collaboration with Sandia National Laboratories. He currently has two publications.

Sushila Singh received Ph.D. from Department of Electronic Science, University of Poona, Pune, India, in 1996. After Ph.D. she worked as a Project Associate for Optoelectronics, a Division of the Society for Applied Microwave Electronics Engineering Research (SAMEER), Department of Electronics, Government of India. Presently she is a visiting research assistant professor at the Department of Physics, University of Arkansas, Fayetteville, AR. Her three distinct fields of research interest are electronic packaging of MEMS, optical interconnects for electronic packaging and optoelectronic devices for communication and computation. She has authored over 20 publications.

William D. Brown received the B.S. degree in Electrical Engineering from the University of Arkansas, Fayetteville, in 1969, the M.S. degree from Pennsylvania State University, University Park, in 1970; and the Ph.D. degree from the University of New Mexico, Albuquerque, in 1975. From 1969 to 1977, he was a Member of the Technical Staff at Sandia National Laboratories in Albuquerque, NM. In 1977, he joined the faculty of the Electrical Engineering Department at the University of Arkansas where he presently holds the rank of University Professor and serves as the Associate Dean for Research in the College of Engineering. His research interests include microelectronic materials and devices, and solid-state and semiconductor physics. Dr. Brown's research has resulted in 96 technical journal publications, 186 conference/workshop presentations, 83 technical conference proceedings articles, and 16 educational conference proceedings articles. He has contributed to and edited the books, Electronic Manufacturing Processes published by Prentice Hall, and Nonvolatile Semiconductor Memory Technology and Advanced Electronic Packaging: With Emphasis On Multichip Modules, both published by the IEEE PRESS. He presently serves on the Executive Committee of the Board of Directors of the Electrochemical Society. He is a registered Professional Engineer in the State of Arkansas and holds memberships in IEEE, IMAPS, ECS, MRS, AVS, the Arkansas Academy of Science, and the American Society of Engineering Educators (ASEE).

William P Eaton received the M.S. degree in Materials Science from the University of California at Davis in 1993, and the Ph.D. degree in Electrical Engineering from the University of New Mexico, Albuquerque, in 1997. He is currently in the Reliability Physics department at Sandia National Laboratories, Albuquerque, NM, working on MEMS reliability. He has been actively doing MEMS research since 1990, working on projects in wafer bonding, bulk micromachining, surface-micromachined pressure sensors, release etch modeling, reliability, device characterization, and packaging.

William M. Miller manages the Reliability Physics Department at Sandia National Laboratories. He received his B.S. (1979) in physics from the University of Washington and his M.S. (1980) and Ph.D. (1984) in physics from the University of Illinois. He has been employed by Sandia since 1984, working on silicon nitride non-volatile memories, silicon-on-insulator (SOI) technology and metallization processes. Since 1989 he has worked on IC reliability issues, with an emphasis on dielectric breakdown and MicroElectroMechanical Systems (MEMS). He became the manager of Sandia's Reliability Physics Department in 1992. During his career he has published 17 technical papers and has mad scores of presentations on a wide range of topics. He currently holds one US patent and has another pending in the area of MEMS.

Packaging Parameters	**Challenges**	**Possible Solutions**
Release etch and dry	Stiction of devices	Freeze drying, supercritical CO_2 drying, roughening of contact surfaces, non-stick coatings
Dicing/Cleaving	Contamination risks, elimination of particles generated	Release dice after dicing, cleaving of wafers, laser sawing, wafer level encapsulation
Die handling	Device failure, top die face is very sensitive to contact	Fixtures that hold MEMS dice by sides rather than top face
Stress	Performance degradation and resonant frequency shifts	Low modulus die attach, annealing, compatible CTE match-ups
Outgassing	Stiction, corrosion	Low outgassing epoxies, cyanate esters, low modulus solders, new die attach materials, removal of outgassing vapors
Testing	Applying non-electric stimuli to devices	Test all that is possible using wafer-scale probing, and finish with cost effective, specially modified test systems

Table 1

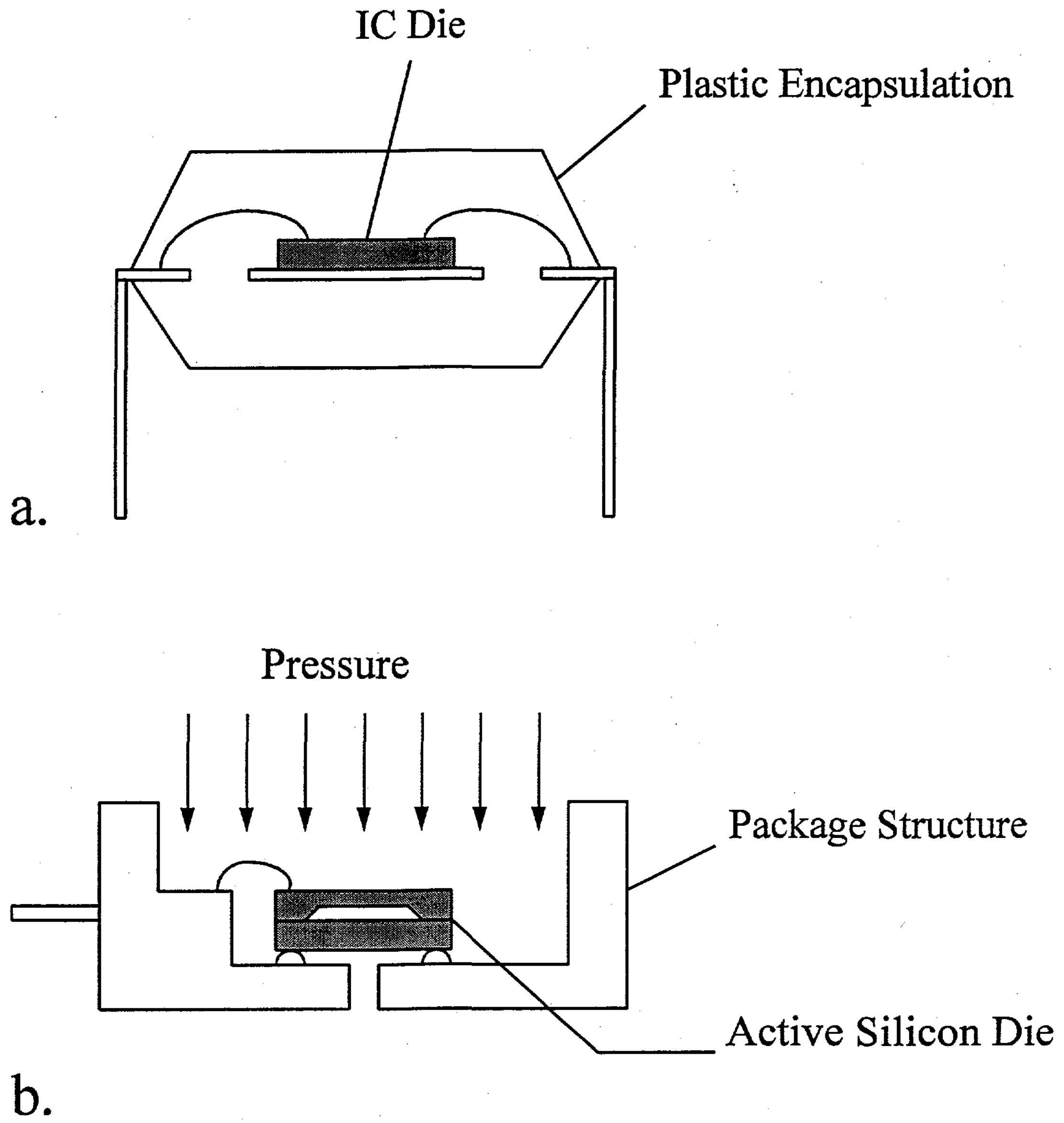

Figure 1

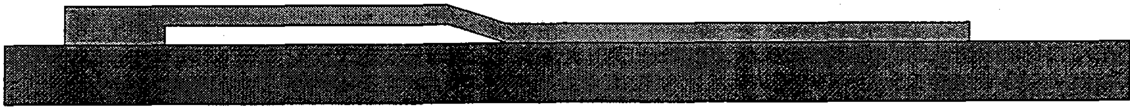

Figure 2

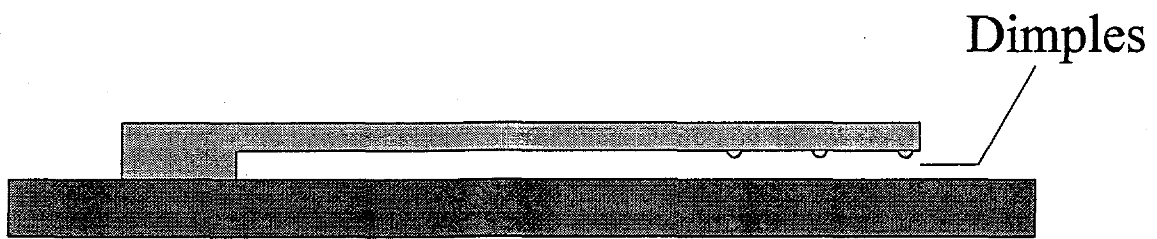

Figure 3

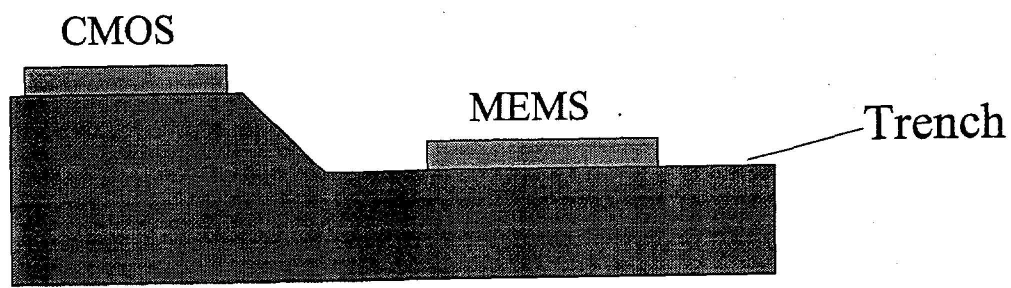

Figure 4

Table 1. Current packaging parameters, challenges, and suggested possible solutions for MEMS.

Figure 1. Schematic of an IC package (A) [14] and a MEMS pressure sensor package (B) [12].

Figure 2. Beam-type element displaying the effect of stiction.

Figure 3. An example of dimples used to prevent stiction.

Figure 4. Cross-sectional schematic of Sandia's *MEMS First* approach to monolithic integration [1], [24].