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# Channel formation in single-monolayer pentacene thin film transistors

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**Abstract**
The geometrical arrangement of single-molecule-high islands and the contact between them have large roles in determining the electrical properties of field effect transistors (FETs) based on monolayer-scale pentacene thin films. As the pentacene coverage increases through the submonolayer regime there is a percolation transition where islands come into contact and a simultaneous rapid onset of current. At coverages just above the percolation threshold, the electrical properties vary with geometrical changes in the contacts between the pentacene islands. At higher coverages, the FET mobility is much lower than the mobility measured by the van der Pauw method because of high contact resistances in monolayer-scale pentacene film devices. An increase in the van der Pauw mobility of holes as a function of pentacene coverage shows that second layer islands take part in charge transport.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

Interfaces in organic electronics, such as thin film field effect transistors (FETs) and organic light emitting diodes, are unavoidable and play a crucial role in determining the performance of these devices [1, 2]. The operation of organic devices involves charge injection through metal–organic interfaces and charge transport in organic layers, processes which often appear in series in device properties [3, 4]. The electrical properties of the semiconducting layer in organic thin film FETs, for example, depend both on the electronic interface between the gate dielectric and organic layer and on the properties of contacts [5, 6]. The properties of these interfaces are in turn linked to intrinsic electronic effects, such as the formation of Schottky barriers as well as to the structure of the organic thin film near the interface. Here we separate the contributions of these phenomena using monolayer-scale pentacene thin films.

Charge transport at the gate dielectric interface of an organic FET involves an accumulation layer with a thickness on the order of only several times the spacing between molecular layers. Estimates based on classical continuum electrostatics give thicknesses of only a few nanometres [7]. More refined calculations take into account the band structure of the organic layer, but give essentially the same result [8]. The small scale of the layer in which the charge transport occurs, given either estimate, suggests that the structure at the very earliest stages of the growth of thin films is most relevant to the electronic properties of the layers. Pentacene thin films have been used to develop FETs in which hole mobilities of up to 1 $cm^2\ V^{-1}s^{-1}$ have been reported [9, 10]. In these devices, however, the thicknesses of the pentacene layers are hundreds of nanometres. It is thus difficult to understand the connection between the interfaces formed during growth and the electrical properties [11–13].

In a few cases, monolayer-scale devices have been used to address the connection between the structural properties of the first few molecular layers and charge transport. For example, Granstrom *et al* used two-contact structures to probe the electrical properties of single grains of sexithiophene only a few molecules thick [14]. The charge carrier mobility in these grains was orders of magnitude lower than typical thick film devices and the observed mobility was not a function of the thickness of the grain. Similarly, Dinelli *et al* showed that the

  

mobility saturated after forming the second layer of sexithienyl thin films [15]. For top contact FETs on few-monolayer pentacene films, the efficiency of the electrical contact to the channel layer depended on the thickness of the portion of the pentacene film separating the contacts from the accumulation layer [16, 17]. It is highly desirable to extend the range and precision with which trends in the electrical properties of devices as a function of small changes in the total amount of pentacene on the surface can be understood.

In a series of measurements varying the pentacene coverage through the single molecular layer regime, we have found that the evolution of the electrical properties of pentacene thin films is linked to the formation of connections between pentacene islands. As the pentacene coverage increases, islands come into contact at a percolation threshold and result in a sudden onset of current and a rapid increase in current with increasing pentacene coverage. In thicker films, contact resistance dominates the properties of two-terminal devices. Four-terminal electrical measurements show that the effective mobility of charges in the pentacene film increases rapidly as the pentacene layer increases in thickness.

## 2. Transistor formation

The electrical studies were conducted using both two-contact FET devices and four-contact van der Pauw geometry structures. For both types of samples, the substrate was a highly doped silicon wafer which acted as the gate in the electrical measurements. A 200 nm thermally grown silicon dioxide layer with a capacitance of $1.7 \times 10^{-8}\,\mathrm{F\,cm^{-2}}$ was used as the gate dielectric. The source and drain electrodes of FET devices were photolithographically defined and consisted of a 60 nm Au film on a 10 nm Cr adhesion layer on the silicon dioxide. The channel length and width were 10 $\mu$m and 1 mm, respectively. The four-contact devices consisted of 500 $\mu$m square electrodes at the corners of a square 2 mm on an edge. Pentacene films were grown on the pre-patterned contact structures by thermal evaporation under vacuum at $10^{-6}$ torr. The deposition rate was determined by measuring the area covered by pentacene islands in atomic force microscopy (AFM) images at a number of deposition times. The substrate was at room temperature during both the pentacene growth and the electrical measurements.

An *in situ* electrical measurement technique was developed to probe the formation of transistor devices during the deposition of the pentacene layer. Throughout the time of the deposition, a constant voltage, $V_{ds}$, was applied between source and drain electrodes and the gate voltage, $V_{gs}$, was scanned periodically. The gate voltage scans were similar to the conventional measurement of device transfer characteristics. The duration of each cycle of the gate voltage scan was adjusted for each experiment and varied from 30 to 90 s, depending on the scan range. In addition to these continuous measurements, electrical measurements were also made during pauses in the deposition. The transistor parameters of the two-contact FET devices were obtained by interpreting the current–voltage characteristics of the transistors using MOSFET theory [18]. For each gate voltage scan, the saturation mobility and threshold voltage were determined from a linear fit to the square root of the drain current as a function of gate voltage [18].

Measurements of the sheet conductance of monolayer-scale films using the van der Pauw method allowed contact resistance effects to be eliminated [19]. The van der Pauw technique averages a series of voltage measurements, each of which is made with a fixed probe current. For these samples, a current of several nA produced voltages of less than 1.5 V at all the terminals. These low voltages ensured that, at the gate voltages of interest, the film was biased into the linear rather than saturation regime. To measure the electrical properties as a function of carrier concentration, the gate voltage was scanned through a range of values and a van der Pauw measurement of the sheet conductance was made at each value of $V_{gs}$. The mobility can be found from the sheet conductance by assuming that all the charge carriers induced in the pentacene by gate voltages larger than the threshold voltage are mobile. The two-dimensional carrier density $p$ in the pentacene layer is then given by $p = C_i(V_{gs} - V_T)/e$, where $C_i$ is the capacitance per unit area of the gate dielectric layer and $e$ is the electronic charge. If all carriers have the same mobility $\mu_{eff}$, the sheet conductance $\sigma$ is given by $\sigma = pe\mu_{eff}$. Values of $\mu_{eff}$ can be found by measuring differential changes in the sheet conductance as a function of the gate voltage, so that $\mu_{eff} = (1/C_i)/(\partial\sigma/\partial V_{gs})$. The derivative can be computed numerically or found using a linear fit to a plot of $\sigma$ as a function of $V_{gs}$. We have used a notation in which $\mu_{eff}$ represents the mobility determined using the van der Pauw sheet conductance to differentiate it from the mobility found in conventional two-contact devices, $\mu_{FET}$.

## 3. Monolayer electrical and structural properties

The growth and geometric arrangement of islands is central to the electrical properties of submonolayer thin films. Figure 1 is a plot of the drain current measured at points with $V_{gs} = -100$ V in continuous sweeps of the gate voltage during pentacene deposition at a rate of 0.17 ML $\mathrm{min^{-1}}$. Here 1 ML corresponds to the area density of molecules required to complete one molecular layer. The drain–source voltage was fixed at $V_{ds} = -50$ V for these measurements. At coverages below 0.77 ML the drain current was less than 25 pA, comparable to the gate leakage current before depositing pentacene. Current began to flow through the channel between the source and drain when the pentacene coverage reached 0.77 ML. In a number of experiments, the coverage at which current exceeds the initial value was distributed between 0.69 and 1.3 ML. We attribute this range in our observations of the initial flow of current to the high threshold voltage of these transistors, which will be discussed below.

The sudden onset of current and its rapid increase after the threshold coverage can be interpreted in terms of the geometric percolation of the single-layer pentacene islands. The percolation threshold for a continuous two-dimensional system occurs when the coverage of islands reaches an area fraction of 0.67 [20]. This threshold value varies only slightly with changes in the distribution of island sizes and deviations in shape away from circular islands [21]. In terms of the electronic properties of the transistor, the current path between the source and drain is formed at the percolation

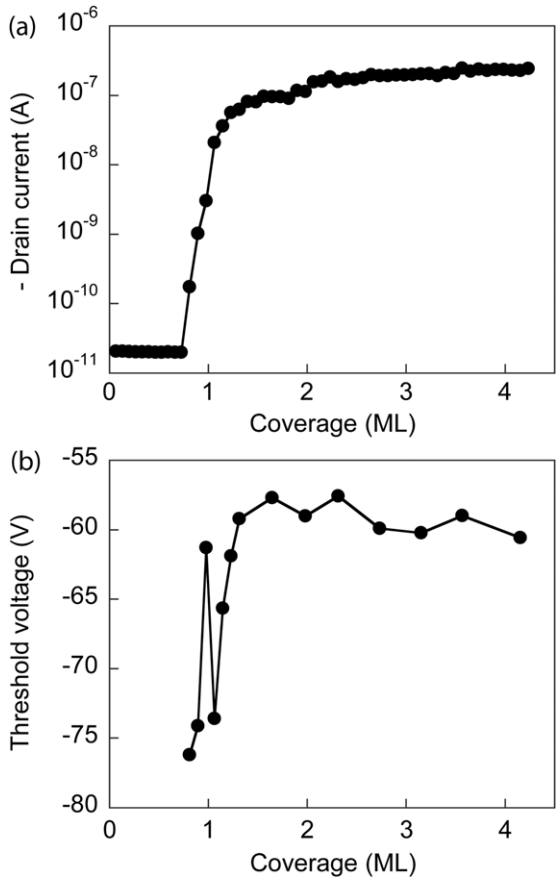


**Figure 1.** Drain current (*a*) and threshold voltage (*b*), as a function of pentacene coverage during the formation of a bottom-contact pentacene FET. The current in part (*a*) are the values measured at $V_{gs} = -100$ V during a series of gate voltage scans from −70 to −100 V with the source–drain voltage held at −50 V.

threshold. Similar phenomena have been observed in the growth of metal clusters on $SiO_2$ and in the formation of rubrene thin film transistors [22, 23]. In both of these cases, however, the formation of three-dimensional islands at low coverages complicates the geometric description of the percolation transition.

The rapid increase in current immediately following the percolation threshold can be explained geometrically. The improved connection between pentacene islands with increasing coverage is illustrated in figure 2 in AFM images of pentacene at coverages from 0.3 to 1.24 ML. When the coverage is small only isolated pentacene islands exist and between 0.3 and 0.6 ML the islands size simply increased laterally. With 0.6 ML pentacene, the islands are still not connected. Once the coverage exceeds the percolation threshold, the number of spanning clusters increases and eventually a two-dimensional uniform pentacene layer is completed. AFM images with 0.75 and 0.92 ML in figure 2 show the progressive filling in of the first layer without forming the second layer. The islands heights of 1.58 ± 0.06 nm in these images are in agreement with the interpretation of the islands as consisting of a single layer of pentacene molecules slightly inclined with respect to the surface normal of the substrate.

The electrical properties of the pentacene film were also analysed during pauses in the pentacene deposition at two submonolayer coverages. Figure 3(*a*) shows the drain current as a function of pentacene coverage during this experiment. The drain current at each coverage is plotted for the point in the gate voltage scan at which $V_{gs} = -80$ V. The measurements were made at a fixed drain voltage of −50 V. Transistor characteristic curves measured at 0.72 and 0.9 ML are shown in figures 3(*b*) and (*c*). In the electrical measurements shown in figure 3, more negative gate voltages produced higher currents at the same drain voltage. As in a typical p-type FET, the charges accumulated by negative gate voltages above the threshold voltage are confined to the pentacene islands. At submonolayer coverages, the pentacene submonolayer can be thought of as being in a charge transport limited regime, which is sensitive to geometrical change in pentacene islands but not to the contacts. AFM images in the inset show increasing contact between islands commensurate with the large increase in current between these two coverages. The effective mobility for the 0.9 ML transistor (figure 3(*c*)) was $9.8 \times 10^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$.

Although the physical coalescence of islands improves the electrical connections among them, the improvement in the electrical conduction due to the increased contact area between pentacene islands saturates after the first monolayer is completed. At coverages near 1 ML, for example, as in figure 2(*e*) with 1.15 ML of pentacene, a closed or nearly closed first pentacene layer coexists with second layer nuclei. The shapes of second layer islands visible in figures 2(*e*) and (*f*) are dendrites rather than the roughly circular islands of the first layer. Third and higher layer islands form almost immediately, consistent with previous observations that the kinetic processes governing pentacene island growth are quite different when islands are grown on top of pentacene islands. The Ehrlich–Schwoebel barrier for molecules descending from the first layer to $SiO_2$ is significantly lower than to descend from the second to the first pentacene layers [24, 25]. Because the third layer islands nucleate almost immediately, the second layer of islands does not percolate as easily as the first monolayer.

The pentacene islands also have a geometric effect in determining the threshold voltage of the FET devices. In figures 3(*b*) and (*c*), the magnitude of the threshold voltage at two submonolayer coverages was much larger than that of typical thick films [26, 27]. Through our continuous electrical measurements we observed that as the pentacene coverage increases from the percolation threshold to 1 ML, the threshold voltage decreases rapidly (figure 1(*b*)). The threshold voltage for this device rapidly was −70 V immediately following the connection of the islands and decreased in magnitude to −60 V as the first layer was completed.

These p-type organic transistors are operated in accumulation mode, in which the threshold voltage is conventionally thought to be the flat band voltage [18]. In the simplest view, a high threshold voltage arises from a large trap density of traps [28]. In these monolayer films, isolated pentacene islands with specific trap densities come into contact, with potentially locally higher threshold voltages at the contact between islands. The plateau of the threshold voltage observed with coverage above 1 ML reflects the microstructure of the pentacene film that forms two-dimensional channel. Once the first layer was completed, the contact between islands was no longer improved by adding pentacene, and the threshold voltage remained constant.

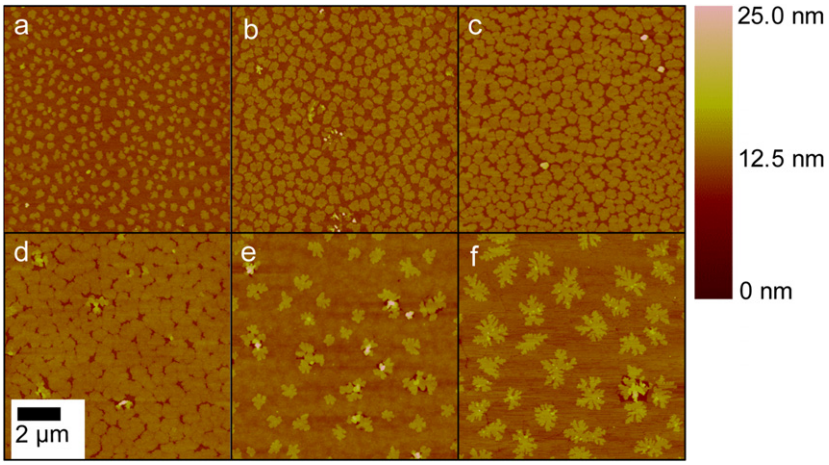


**Figure 2.** Atomic force microscope images of pentacene islands on $SiO_2$ substrates at pentacene coverages of (*a*) 0.30 ML, (*b*) 0.60 ML, (*c*) 0.75 ML, (*d*) 0.92 ML, (*e*) 1.15 ML and (*f*) 1.24 ML.

The values of the FET mobility in our submonolayer transistors, less than $10^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$ based on the measurements in figure 3(*c*), were far below those of transistors using films with thicknesses at the 100 nm-scale. Similar values have been found in monolayer transistors studied by other groups. The low values are somewhat puzzling since it is expected that most charge transport occurs in the first few molecular layers close to the gate dielectric. One possibility is that the barriers to carrier injection at interfaces with the source and drain electrodes, which can affect the mobility measured in two-terminal devices are responsible for the poor device performance. The barriers in thicker films have been investigated using scanning Kelvin probe microscopy and four-contact methods [29–31]. It was shown in these studies with thicker films that a significant fraction of the total voltage between the drain and source appears across the metal–semiconductor contacts. Interpreting this electrical phenomenon microscopically is challenging because the area of the contact between single-molecule-high pentacene islands and the metal electrodes can be structurally different from the bulk. This is especially important in these bottom-contact devices because the presence of the electrodes can modify the kinetic processes of thin film growth.

The van der Pauw measurements in figure 4(*a*) on a transistor with a 1.4 ML pentacene film eliminate the contact resistance and provide the opportunity to electrically probe the pentacene monolayer rather than the contacts. These measurements were performed without removing the sample from the deposition chamber. The mobility measured using the slope of the plot in figure 4(*a*) was $\mu_{\rm eff} = 0.085$ cm$^2$ V$^{-1}$s$^{-1}$. The effective mobility is approximately two orders of magnitude larger than the mobility value determined using two-contact FET structures.

The large contact resistance in FET devices suggests that the measurements of electrical parameters on monolayer-scale devices span two regimes. At very low coverages, in the submonolayer regime, the contact between islands is important and improvements in the contact can lead to changes in the current and threshold voltage. In the higher coverage regime, after completing the first molecular layer, the contact resistance becomes important. At these higher coverages, the two-terminal devices are not able to probe the electrical properties of the pentacene layer and instead reflect the properties of the contact.

The elimination of the contact resistance provides the opportunity to study the mobility of charge carriers in pentacene thin films as a function of the pentacene coverage. We deposited pentacene onto three van der Pauw geometry devices at the same time with each different thickness. After deposition we removed these samples from the vacuum chamber and, after wiring them in air, measured the sheet resistance as a function of gate voltage under vacuum in the deposition chamber. The probe current for the sheet conductance measurements in figure 5 was 4.2 nA. The mobility of a 0.99 ML pentacene layer was 0.016 cm$^2$ V$^{-1}$s$^{-1}$. At this coverage, vacant sites between pentacene islands are still being filled by additional pentacene, since second layer islands are visible on top of the first layer.

At higher coverages, as more pentacene molecules were added, the vacant sites between islands were almost completely filled and second layer islands grew laterally. For a 1.32 ML film, the mobility doubled with respect to the lower coverage sample, even though the pentacene coverage had only increased by 30%. With 1.6 ML the second layer islands were larger, with the beginnings of the third layer on top of them. The change in mobility across the range of coverage for these three samples was striking, with $\mu_{\rm eff}$ increasing from 0.016 cm$^2$ V$^{-1}$s$^{-1}$ with 0.99 ML to 0.15 cm$^2$ V$^{-1}$s$^{-1}$ at 1.6 ML. A summary of the mobilities for two-and four-contact devices appears in table 1. The deposition rate for the 1.4 ML film shown in figure 4 was 0.09 ML min$^{-1}$. Because the deposition rate for the 0.99 ML, 1.32 ML, and 1.6 ML films shown in figure 5 was higher, 0.7 ML min$^{-1}$, it may be most useful to use only those three films when considering trends in the mobility with increasing coverage.

The differences between the measurements with two-contact FETs and the four-contact van der Pauw geometry structures can be used to estimate the resistance at the contacts between the metal electrodes and the pentacene monolayers. The large difference between the mobilities observed with two and four terminals suggests that a detailed estimate of the contact resistance is not necessary. At the coverages for which we have made the four-terminal measurements, the

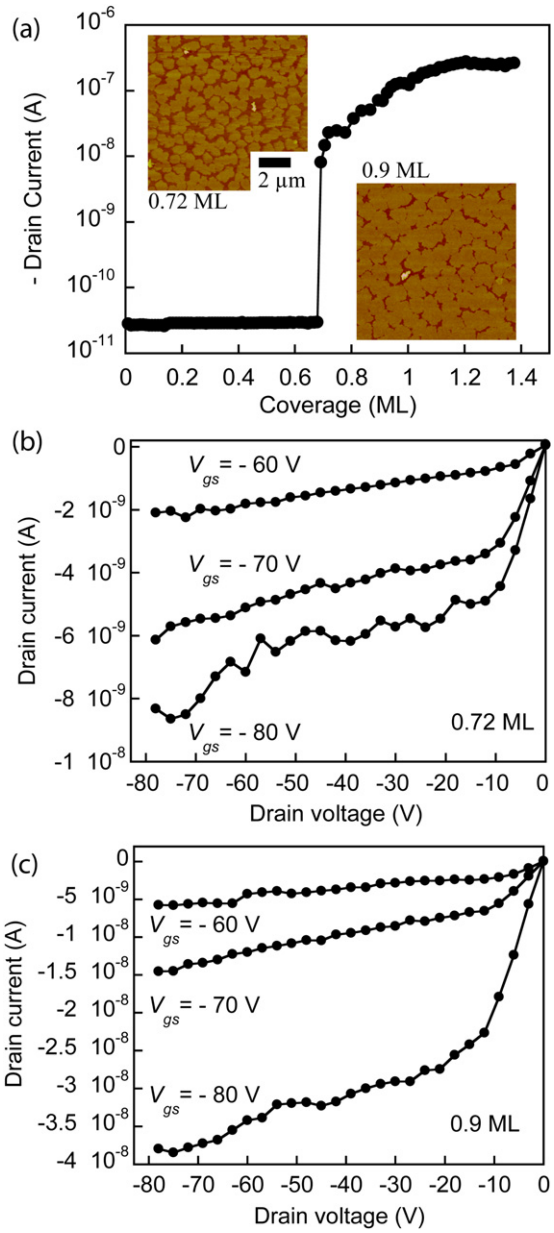


**Figure 3.** (*a*) Drain current as a function of pentacene coverage during an experiment in which the deposition was paused at 0.72 and 0.9 ML. The inset shows AFM images at 0.72 and 0.9 ML. Transistor output characteristic curves at (*b*) 0.72 ML and (*c*) 0.9 ML.

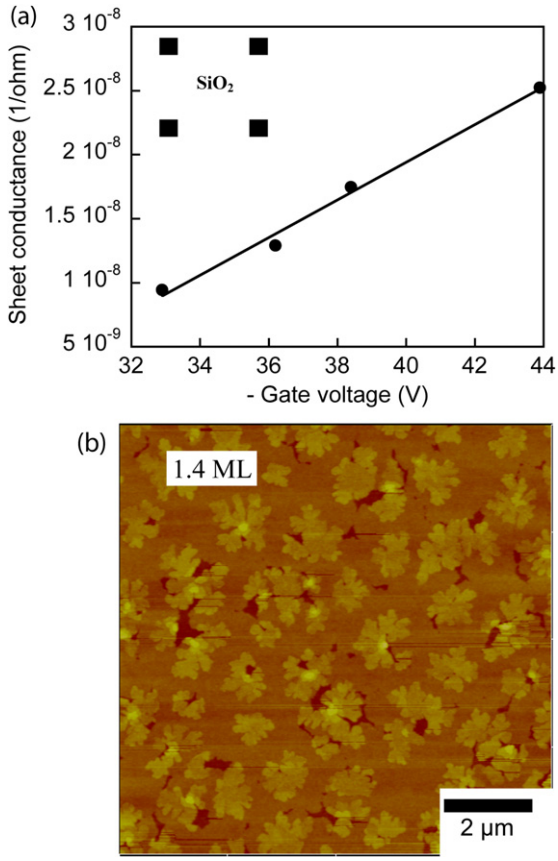


**Figure 4.** (*a*) Sheet conductance as a function of gate voltage for a 1.4 ML. The inset shows the schematic of the van der Pauw geometry device (top view). (*b*) AFM image of this thin film.

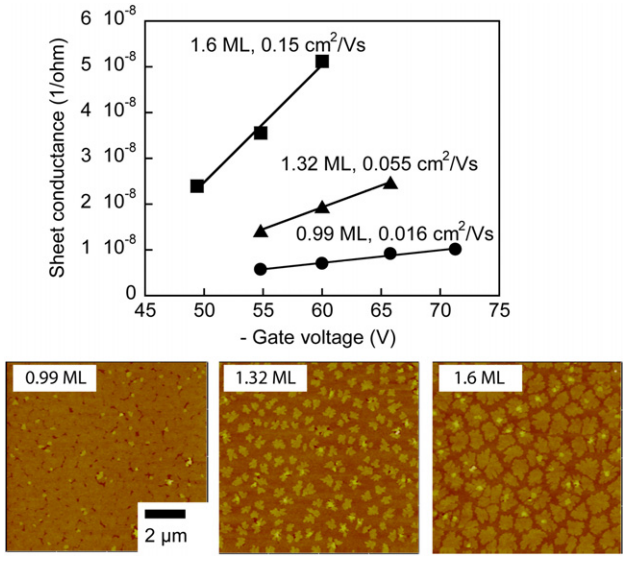


**Figure 5.** Sheet conductance as a function of gate voltage at pentacene coverages of 0.99, 1.32 and 1.6 ML. AFM images of the three thin films are shown below.

contact resistance provides the vast majority of the total circuit resistance. This is distinct from the situation observed by Pesavento *et al* with much thicker pentacene films, in which [32] the contact resistance was smaller than the resistance of the channel. For our monolayer-scale films, the contact resistance is far higher than the resistance due to the film.

Even though the second layer had not percolated, the sheet conductance and mobility increased with increased coverage. The second layer islands can contribute to electrical charge transport by adding a parallel conduction path and locally reducing the resistance of areas covered by a second layer island. The improvement in the two-terminal mobility $\mu_{\mathrm{FET}}$ observed in two-terminal devices could be due either to this large improvement in the channel mobility or, more likely, to improvements in the physically incomplete contact between the metal and the pentacene [33].

The present results suggest a picture of conduction in pentacene thin film devices that is somewhat different from

**Table 1.** Mobilities measured in the saturation regime with a two-contact FET device and using four-terminal van der Pauw geometry structures.

| Coverage (ML) | Mobility ($cm^2\ V^{-1}s^{-1}$) |
|---|---|
| *Two-contact FETs* | |
| 0.9 | $9.8 \times 10^{-4}$ |
| *Four-contact van der Pauw structures* | |
| 0.99 | 0.016 |
| 1.32 | 0.055 |
| 1.4 | 0.085 |
| 1.6 | 0.15 |

the one proposed by Dinelli *et al* for sexithienyl thin films [15], in which the poor charge transport of submonolayer films is attributed to the roughness of the top surface of the film. We find, however, that the extremely low mobilities only apply to two-terminal devices. The rapid increase in hole mobilities with increasing pentacene film thickness observed by Ruiz *et al* occurred at total pentacene coverages of several molecular layers, rather than the single-layer scale we discuss here [34].

## 4. Conclusion

We have found that a number of effects linked to the geometry and connection of single molecular layer islands can contribute to the electrical properties of pentacene FETs. Because the growth of single-layer-high islands is common in organic semiconductor materials, these effects should apply equally to a number of other systems. In addition, understanding these effects, particularly the role of improving contact between islands raises the possibility of studies of the electronic consequences of more subtle structural effects, including potentially new crystalline structures in the first few molecular layers of molecules [35].

By varying the coverage of pentacene continuously across the percolation threshold more gradually, it will be possible in future measurements to probe the critical exponents associated with the development of contact between islands [36]. Because the contacts between islands are widely believed to limit the mobility observed in devices, these results may need to be interpreted in terms of a model that includes resistance at the contacts between islands [37]. The degree to which organic systems at very low coverage are described by the traditional theories of transport in systems with large-scale disorder could lead to the development of new strategies for forming and connecting first-layer islands.

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