Channel-length-dependent transport behaviors of graphene field-effect transistors

Channel-Length-Dependent Transport Behaviors of Graphene Field-Effect Transistors

Shu-Jen Han, *Member, IEEE*, Zhihong Chen, *Member, IEEE*, Ageeth A. Bol, and Yanning Sun

***Abstract*—This letter presents a detailed study of transport in graphene field-effect transistors (GFETs) with various channel lengths, from 5 μm down to 90 nm, using transferred graphene grown by chemical vapor deposition. An electron–hole asymmetry observed in short-channel devices suggests a strong impact from graphene/metal contacts. In addition, for the first time, we observe a shift of the gate voltage at the Dirac point in graphene devices as a consequence of gate length scaling. The unusual shift of the Dirac point voltage has been identified as one of the signatures of short-channel effects in GFETs.**

***Index Terms*—Chemical vapor deposition (CVD) graphene, Dirac point, graphene field-effect transistor (GFET), short-channel effect.**

I. Introduction

DUE to its high carrier mobility and ultrathin body, graphene has attracted tremendous attention as a channel material for future high-speed nanoelectronic devices [1]–[3]. The 2-D geometry of graphene also makes it compatible to the conventional CMOS top-down process scheme. Despite its high quality, the mechanically exfoliated graphene suffers from a low yield and lack of thickness control. In contrast, chemical vapor deposition (CVD)-grown graphene offers good uniformity over a large area. This new material provides an opportunity to perform systematic studies on graphene transport properties and leads to a potential use in VLSI technologies.

While the gate voltage corresponding to the current minimum point (Dirac point, $V_{\rm dirac}$) has been considered to be the indicator for impurity or phonon scattering from the substrate or doping level in graphene, we demonstrated that the drain bias can also shift $V_{\rm dirac}$ through short-channel effects.

II. Materials and Device Fabrication

The method that we used to prepare monolayers of graphene is similar to that in [4]. A piece of Cu foil was placed in a quartz furnace tube at 60 mtorr. The Cu foil was then heated to 875 °C in forming gas and kept at this temperature for 30 min to reduce native CuO and increase the Cu grain size. After reduction, the Cu foil was exposed to ethylene (6 sccm, 500 mtorr) at 875 °C for 30 min. PMMA was spin coated on the top of the graphene layer formed on one side of the Cu foil. The Cu foil was then dissolved in 1-M iron chloride. Subsequently, the PMMA was dissolved in hot acetone. Fig. 1(a) and (b) shows $I_{\rm ds}$–$V_{\rm gate}$ and transconductance–$V_{\rm gate}$ (with $V_{\rm ds} = 0.1$ V) measured from ten random sites on a single piece of CVD graphene (~ 1.5 cm $\times$ 1.5 cm) transferred on a 90-nm SiO_2 substrate. The device size is rather large (200 μm $\times$ 480 μm) to provide some "averaged" film quality across the chip. Excellent uniformity has been observed in our transferred CVD graphene.

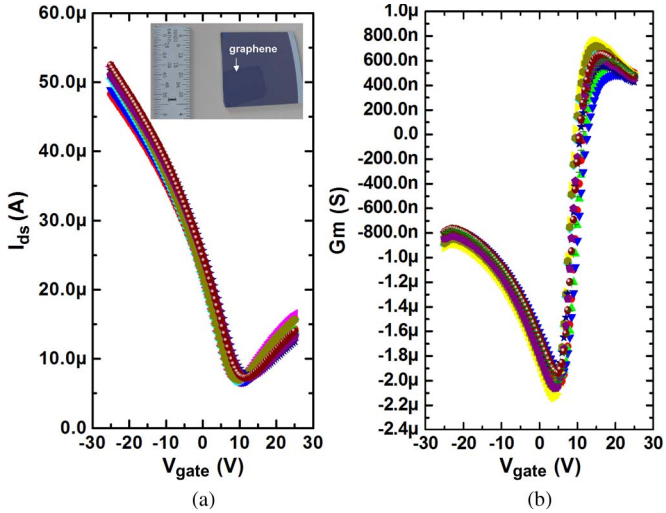

Fig. 1. Uniformity of CVD single-layer graphene film. (a) $I_{\rm ds}$–$V_{\rm gate}$ and (b) transconductance as a function of $V_{\rm gate}$ measured at ten different sites across the chip. (Inset) Greater than 1.5 cm $\times$ 1.5 cm graphene transferred on a 90-nm $SiO_2/P^{++}-Si$ substrate.

Fig. 2 shows arrays of back-gated graphene field-effect transistors (GFETs) with various channel lengths fabricated on single-layer CVD graphene. The gate dielectrics were 90-nm thermally grown SiO_2. The GFET channel region and source/drain region were patterned using electron beam lithography, followed by electron beam evaporation of source/drain contact metals (5-ÅTi/300-Å Pd/200-Å Au).

III. Results and Discussion

A. p-n Asymmetry

Representative $I_{\rm ds}$–$V_{\rm gate}$ curves at low drain bias ($V_{\rm ds} = 0.1$ V) for four different channel lengths are shown in Fig. 3(a). Multiple devices of each channel length were measured to obtain statistical analysis. Long- and short-channel devices exhibit

Manuscript received February 14, 2011; revised March 11, 2011; accepted March 12, 2011. Date of publication April 28, 2011; date of current version May 25, 2011. This work was supported by the Defense Advanced Research Projects Agency under Contract FA8650-08-C-7838 through the CERA program. The review of this letter was arranged by Editor L. Selmi.

S.-J. Han, A. A. Bol, and Y. Sun are with IBM T.J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: sjhan@us.ibm.com; ageeth@us.ibm.com; yansun@us.ibm.com).

Z. Chen is with Purdue University, West Lafayette, IN 47907 USA (e-mail: zhchen@purdue.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2011.2131113

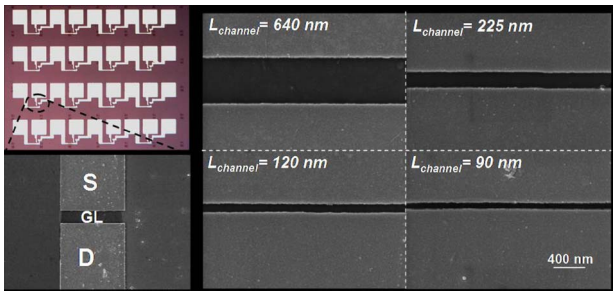

Fig. 2. Optical micrograph and SEM of an array of GFETs. Each array consists of seven different channel lengths (5 μm, 2 μm, 1 μm, 640 nm, 225 nm, 120 nm, and 90 nm). All devices have the same channel width of 5 μm and use 90-nm SiO_2/P + + Si substrate as the back gate.

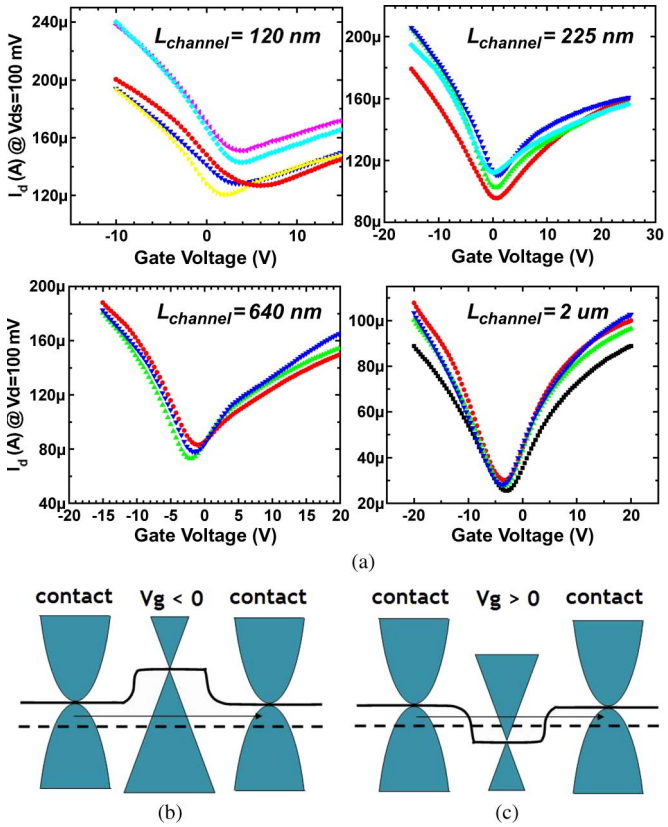

Fig. 3. (a) Comparison of $I_{\rm ds}$–$V_{\rm gate}$ curves for multiple devices with different channel lengths. Asymmetry between n- and p-branches becomes more distinct for shorter channel devices. (b) Band diagram of p-branch when $V_{\rm gate} < 0$ and (c) the band diagram of n-branch when $V_{\rm gate} > 0$.

some very different characteristics: 1) Asymmetry between n- and p-branches becomes more distinct for short-channel devices, where the n-branch gets suppressed, and 2) $I_{\rm on}/I_{\rm off}$ decreases with the decreasing channel length, where $I_{\rm on}$ is defined as $I_{\rm ds}$ at certain overdrive voltage $(V_{\rm gate} - V_{\rm dirac})$ and $I_{\rm off}$ is defined as $I_{\rm ds}$ at $V_{\rm dirac}$.

To explain the observed p-n asymmetry and diverse curves from short-channel devices, we expect that contacts play more important roles in short-channel devices, which is different from long-channel devices which are dominated by the graphene channel. It has been suggested that graphene underneath metal contacts has altered energy dispersion and can be doped to be either p- or n-type depending on the work function

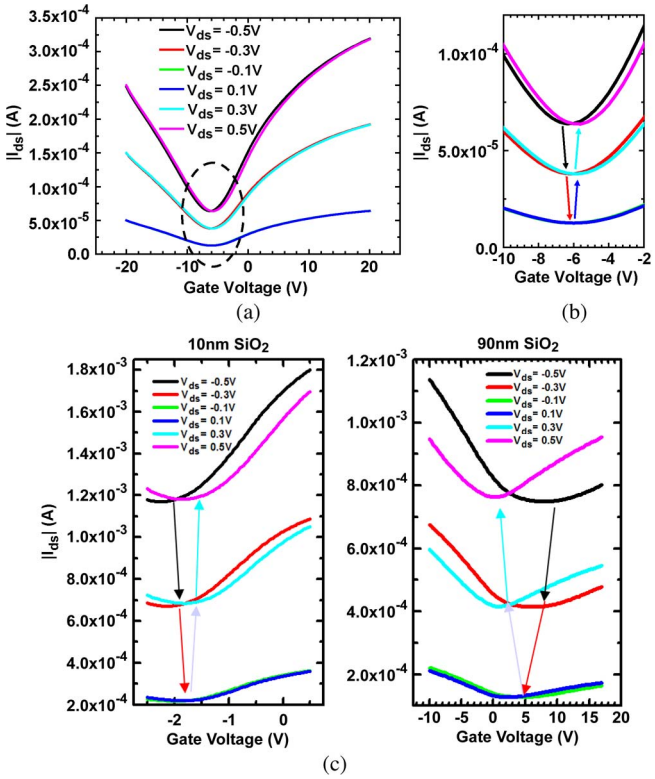

Fig. 4. Effect of $V_{\rm ds}$ on $I_{\rm ds}$–$V_{\rm gate}$ transfer curves. (a) Long-channel device ($L_{\rm channel} = 5$ μm), (b) region near $V_{\rm dirac}$ from (a), and (c) short-channel device ($L_{\rm channel} = 90$ nm) for samples with $T_{\rm ox} = 10$ nm and $T_{\rm ox} = 90$ nm. $V_{\rm ds}$ following arrows are from -0.5 to 0.5 V.

of the metal, and depending on the polarity of carriers in graphene, charges transfer from the metal to graphene, leading to a p-p or p-n junction in graphene [5], [6]. Our contacts (Pd) p-dope the graphene underneath, and when the channel is shifted by the gate into the n-region [Fig. 3(c)], a p-n junction formed between the contact and channel limits the current injection and results in a lower electron current branch. On the other hand, the interfacial barrier of a p-p junction [$V_{\rm gate} < 0$ in Fig. 3(b)] is almost transparent. Using the standard transmission line method, the contact resistances at $V_{\rm gate} = -25$ V and $V_{\rm gate} = 25$ V are 1000 and 1550 $\Omega \cdot \mu$m, respectively. We attribute the difference to the resistance of the p-n junction.

B. $V_{\rm dirac}$ Versus Drain Bias

Another distinguished difference between long- and short-channel graphene devices is shown in Fig. 4. In a long-channel device [Fig. 4(b)], $V_{\rm dirac}$ shifts slightly to be more negative when the drain voltage increases negatively and becomes more positive when the drain bias increases positively. A short-channel device behaves very differently in this context. We see more pronounced shifts in short-channel devices, and the shift directions are opposite to those of the long-channel devices (Fig. 4(c), 90-nm SiO_2). This is not observed for devices with 10-nm SiO_2. We show this comparison in Fig. 5, where the $V_{\rm dirac}$ shift from $V_{\rm ds} = -0.5$ V to $V_{\rm ds} = 0.5$ V is plotted as a function of the channel length. For long-channel devices, an ambipolar device reaches its minimum current when the gate pulls the Fermi level to the point where the carrier injection

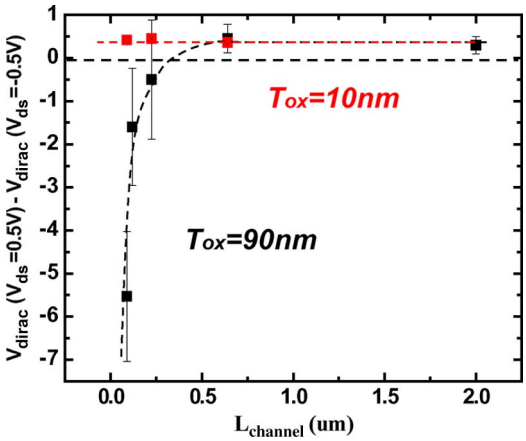

Fig. 5. $\Delta V_{\rm dirac}$ (from $V_{\rm ds} = -0.5$ V to $V_{\rm ds} = 0.5$ V) as a function of device channel length. Devices with 90-nm gate dielectric show a transition from positive shift to negative shift while devices with 10-nm gate dielectric show no transition down to 90-nm channel length.

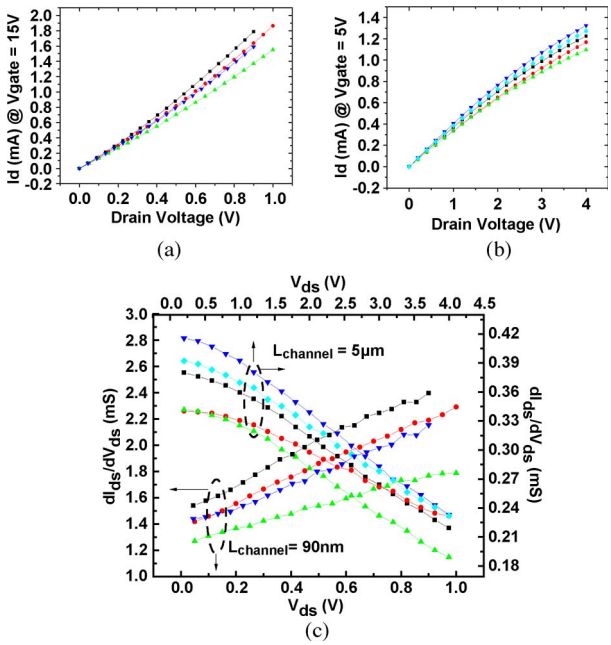

Fig. 6. $I_{\rm ds}$–$V_{\rm ds}$ curves for (a) 90-nm and (b) 5-μm channels at similar overdrive voltages. (c) $dI_{\rm ds}/dV_{\rm ds}$ versus $V_{\rm ds}$ for 90-nm and 5-μm channels at similar gate overdrive voltages. Different colors are different devices on the same chip. The reversed saturation was observed in short-channel devices due to the shift of $V_{\rm dirac}$.

from the source is equal to the injection from the drain (when $\Delta V_{\rm gate} = 1/2\Delta V_{\rm ds}$). On the other hand, the shift in short-channel devices is consistent with short-channel effects, with the results of the drain influencing the channel potential due to weak gate control. When the drain is in strong control, the gate needs to apply more opposite voltages to turn the device to the minimum current point. Since the $V_{\rm dirac}$ shifts with the drain bias for different reasons in long- and short-channel devices, it makes more sense now why we observe quite different $\Delta V_{\rm dirac}$ values for the devices in Fig. 5. As a direct result from the short-channel effect, our short-channel devices suffer from losing the on/off ratios, as shown in Fig. 3. To verify the theory, the same measurement was performed on devices with a 10-nm SiO_2 dielectric and is shown in Figs. 4(c) and 5. It is worth noting that the 10-nm dielectric is the thinnest back-gate dielectric used in GFET ever reported, owing to the large CVD graphene piece where visualization of graphene is unnecessary for the device fabrication. All devices with the 10-nm dielectric show about $+0.5$-V $V_{\rm dirac}$ shift $(= 1/2\Delta V_{\rm ds})$, and no transition from the positive $V_{\rm dirac}$ shift to the negative $V_{\rm dirac}$ shift was observed.

How does this unusual shift of $V_{\rm dirac}$ impact the output characteristics of GFETs? As shown in Fig. 6, in our 90-nm short-channel devices, the extra current gain from the lowering of $V_{\rm dirac}$ at higher $V_{\rm ds}$ results in a reverse saturation characteristic ($dI_{\rm ds}/dV_{\rm ds}$ increases with $V_{\rm ds}$) while 5-μm devices show a normal saturation behavior. This effect needs to be carefully considered and requires a further analysis to assess the applicability of GFETs in analog and digital circuits and systems.

IV. Conclusion

A highly uniform large-scale monolayer of graphene has been fabricated with CVD on Cu and successfully transferred to a SiO_2 substrate. The key factors to identify short-channel effects in zero-bandgap semiconductors have been reported for the first time. Our experimental findings modify the existing pictures about $V_{\rm dirac}$ in graphene and points out the impact of channel length scaling on device characteristics.

References

[1] K. C. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[2] B. Huard, J. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon, "Transport measurements across a tunable potential barrier in graphene," *Phys. Rev. Lett.*, vol. 98, no. 23, p. 236 803, Jun. 2007.

[3] M. C. Lemme, T. Echtermeyer, M. Baus, and H. Kurz, "A graphene field effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[4] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.

[5] B. Huard, N. Stander, J. A. Sulpizio, and D. Goldhaber-Gordon, "Evidence of the role of contacts on the observed electron–hole asymmetry in graphene," *Phys. Rev. B, Condens. Matter*, vol. 78, no. 12, p. 121 402, Sep. 2008.

[6] Z. Chen and J. Appenzeller, "Gate modulation of graphene contacts—On the scaling of graphene FETs," in *VLSI Symp. Tech. Dig.*, 2009, pp. 128–129.