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Channel Length Scaling in Graphene Field-Effect Transistors Studied with Pulsed Current−Voltage Measurements

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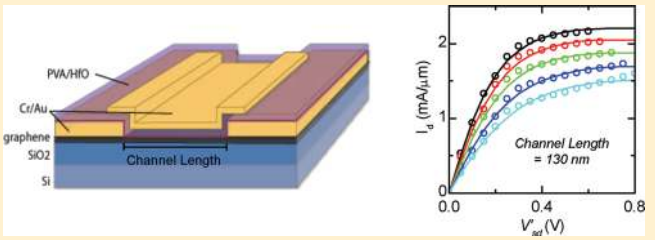
ABSTRACT: We investigate current saturation at short channel lengths in graphene field-effect transistors (GFETs). Saturation is necessary to achieve low-output conductance required for device power gain. Dual-channel pulsed current−voltage measurements are performed to eliminate the significant effects of trapped charge in the gate dielectric, a problem common to all oxide-based dielectric films on graphene. With pulsed measurements, graphene transistors with channel lengths as small as 130 nm achieve output conductance as low as 0.3 mS/μm in saturation. The transconductance of the devices is independent of channel length, consistent with a velocity saturation model of high-field transport. Saturation velocities have a density dependence consistent with diffusive transport limited by optical phonon emission.



KEYWORDS: Graphene, current saturation, high-bias, short channel, pulsed-IV

Much of the technological interest in graphene[1,2] comes from its potential as a field-effect-transistor channel material for high-frequency applications.[3,4] Long-channel graphene field-effect transistor (GFET) operation has been thoroughly investigated both experimentally[5−11] and theoretically.[12−15] Saturating current−voltage ($I-V$) characteristics have been observed down to channel lengths of 1 μm determined by the interplay of velocity saturation and density-of-states modulation in the channel. Saturation velocities are typically in the range of 10^7 to 10^8 cm/sec, offering the possibility of low transit times in short channel devices. However, it is uncertain whether saturating characteristics will continue to be observed with scaling channel length, given the absence of a band gap and the dependence of this saturating characteristic on inelastic scattering in the channel. This uncertainty has been augmented by very recent RF measurements of GFETs with channel lengths as short as 140 nm, which despite demonstrating impressive unity-current-gain cutoff frequency (f_T) of more than 300 GHz, show nonsaturating device characteristics.[16] Current saturation is necessary for both voltage and power gain in these devices.[4]

In this Letter, we explore GFET devices using pulsed current−voltage ($I-V$) measurements, which mitigate the effects of trapped charge in the gate oxide. When measured in this manner, we show strong saturating $I-V$ characteristics in even the shortest channel lengths measured (130 nm) with output conductance in saturation of less than 0.3 mS/μm. The resulting $I-V$ characteristics are well modeled by a density-dependent saturation velocity. Standard dc measurements of these same devices yield nonsaturating characteristics and systematically degrading device parameters with decreasing channel length, demonstrating the importance of trapped charges in these measurements.

The GFET devices studied here consist of dual-gated structures (see Figure 1a) in which the top gate extends to the contacts, minimizing access resistance to the channel. The highly doped silicon substrate acts as a back gate. An important challenge to GFET device fabrication remains establishing a reliable gate dielectric for the top gate. Atomic-layer deposition (ALD) of high-κ dielectric gate oxides has been demonstrated, utilizing a seed layer[17−20] to facilitate ALD growth on the chemically inert graphene surface. Typically, however, these seed layers either have to be thick for a reliable gate dielectric or result in significant degradation of the mobility and substantial doping of the graphene channel. Our approach employs poly(vinyl alcohol) (PVA), which relies on adsorption of the PVA-carbon-chain to the graphene surface with the hydroxyl groups providing a surface to seed ALD growth (see Figure1b). In addition, PVA has a relatively high dielectric constant ($\kappa \sim 6$),[21] leading to minimal gate capacitance reduction when it is present as a component of the gate stack. In this work, single-layer graphene samples are prepared by mechanical exfoliation on silicon wafers ($\rho \sim 0.002$ Ω-cm) with a ~300 nm SiO_2 layer. One nanometer Cr/80 nm Au source and drain contacts are deposited using standard e-beam lithography techniques. After contact deposition, devices are annealed at 330 °C for 3 h in forming gas and subsequently dipped into a 1% aqueous solution of 85 000−125 000 molecular weight PVA (Sigma-Aldrich) for 12 h. The samples are then rinsed with a second dip into deionized water and blown dry with nitrogen resulting in an approximately 2.5 nm thick layer of PVA on the graphene surface.

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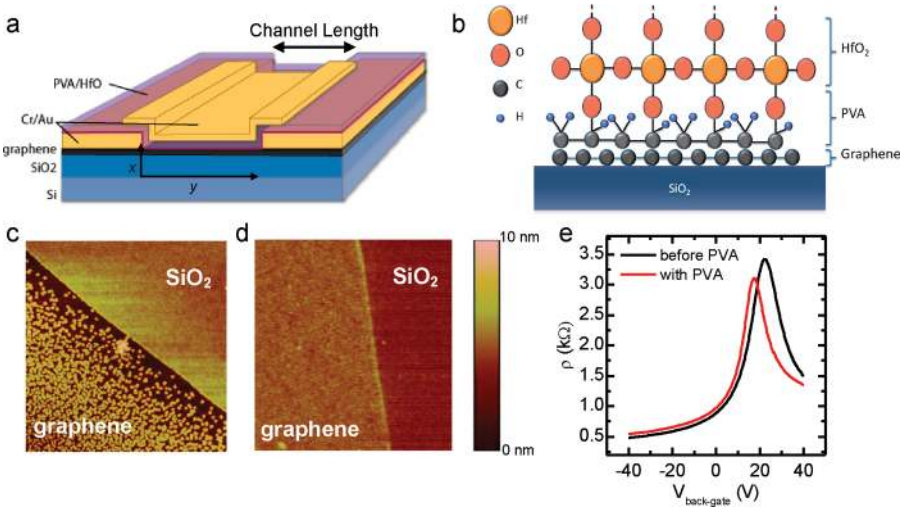

Figure 1. Top-gated GFET device structure. (a) Schematic of the devices with the top gate spanning the entire channel length. (b) PVA functionalization layer used to nucleate the ALD growth of HfO_2 films. (c) AFM image of graphene on a SiO_2 substrate after the deposition of 5 nm of HfO_2 without PVA, showing only patchy growth. (d) AFM image of graphene on an SiO_2 substrate after the deposition of 5 nm of HfO_2 with a PVA functionalization layer, showing improved area coverage with a roughness of only 2.5 Å. (e) Resistivity of a device after annealing and then after the PVA deposition as a function of back-gate bias. The doping and the mobility of the device stay relatively unchanged.

Figure 1e shows resistivity measurements of a representative sample fabricated in this manner after the annealing step and then after the PVA coating. Samples after forming gas annealing are usually heavily p-doped in ambient, which remains unchanged with the addition of the PVA layer. A brief UV/Ozone treatment is employed to activate the −OH groups before the ALD growth of hafnium oxide at 150 °C with $[(CH_3)_2N]_4Hf$ and H_2O for 50 cycles, yielding a 5 nm thick film. Figure 1c,d shows atomic force microscopy (AFM) images of two samples so prepared, one with a PVA layer and one without. Without PVA, ALD growth proceeds only on the SiO_2 area, leaving only patches of oxide at nucleation sites formed most likely by surface contamination. With PVA, films grow uniformly on both the SiO_2 and graphene surfaces with a surface roughness of ±2.5 Å, compared to the film roughness of ±2.0 Å on SiO_2. The breakdown electric field for the PVA/HfO_2 dielectric stack is approximately 0.7 V/nm. We employ a 12 nm thick oxide in the GFETs measured subsequently to achieve a breakdown voltage of approximately 10 V. This oxide thickness yields a top-gate capacitance of $C_{top\text{-}gate} \approx 600$ nF/cm^2, as determined by the relative coupling of the top and back gates.[22]

Devices were fabricated on multiple graphene samples with channel lengths, L, varying from 2.5 μm down to 130 nm. Because of the work-function mismatch between the graphene and the metal contacts,[23] the contacts are p-type. To avoid any additional resistance due to p-n junctions at the source/drain contacts, subsequent large-signal characterization uses these devices in the p-doped regime. Figure 2a shows high-bias measurements of a 2.5 μm channel-length device, showing output characteristics similar to previous demonstrations at these channel lengths. However, for a device of 350 nm channel length (see Figure 2b), made from the same graphene sample, both the transconductance

$$g_m = \left.\frac{\partial I_d}{\partial V_{sg}}\right|_{V_{sd}}$$

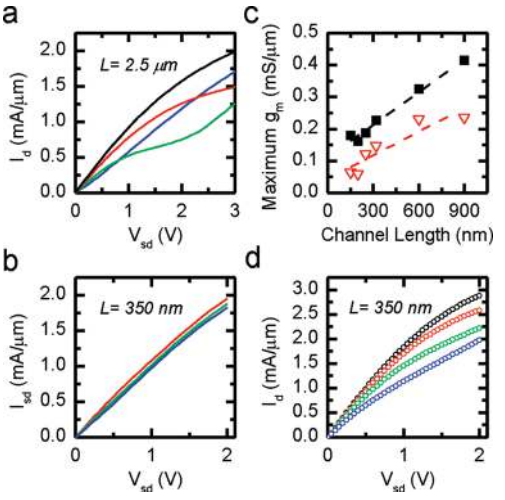

Figure 2. dc current−voltage characteristics. (a) dc $I-V$ measurements of a 2.5 μm channel-length device. Gate voltage varies from 1.5 to −1.5 V to 1 V steps. (b) dc $I-V$ measurements of a 350 nm channel-length device fabricated from the same graphene sample. The strong degradation in device characteristics is clearly visible. (c) Maximum transconductance as a function of channel length. Intrinsic transconductance (black squares), after removing the effect of the contact resistance, is also shown. (d) Pulsed $I-V$ measurements of the same 350 nm device shown in (b).

and output conductance

$$g_0 = \left.\frac{\partial I_d}{\partial V_{sd}}\right|_{V_{sg}}$$

the product of which determines the intrinsic voltage gain of the device, are heavily degraded. This degradation is systematically observed with decreasing channel length. Here, I_d is the drain current of the device, V_{sg} is the source−gate voltage, and V_{sd} the source−drain voltage. The maximum transconductance drops by more than a factor-of-two as the channel length is decreased from 900 to 150 nm as shown in Figure 2c.

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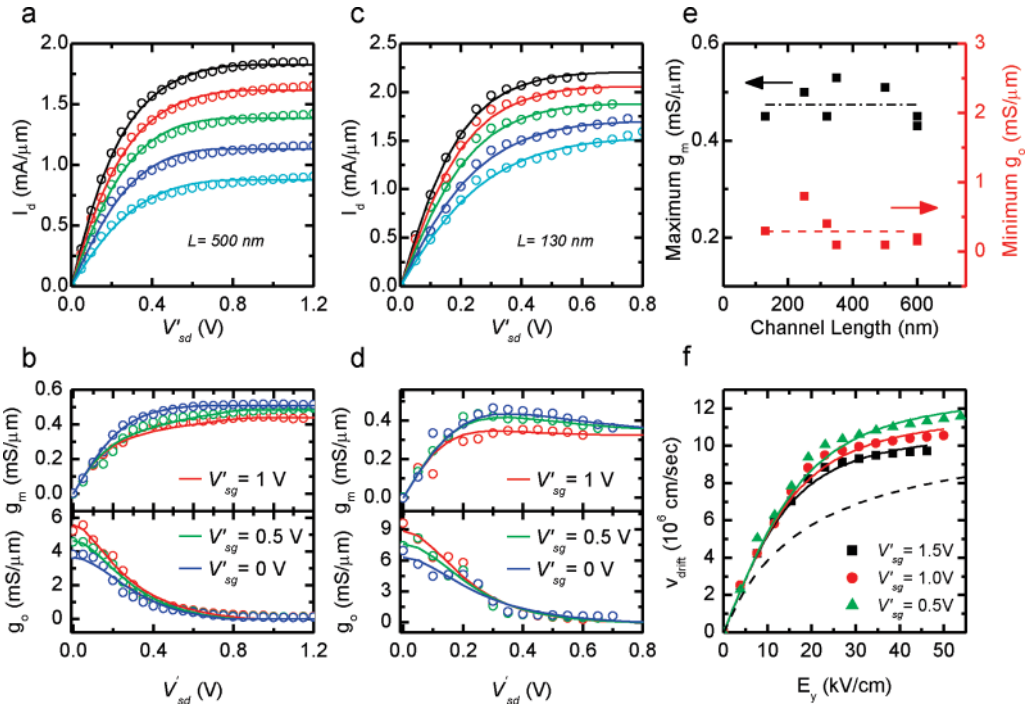

Figure 3. Pulsed $I-V$ measurements. (a) Intrinsic $I-V$ characteristics after the extraction of the contact resistance for a 500 nm device. Model fits are shown as solid lines. The family of curves vary V'_{sg} from 1.5 to −0.5 V in 0.5 V steps. The neutrality point (V_0) for this device is 1.67 V. (b) Intrinsic transconductance and output conductance for the same 500 nm device as a function of V'_{sd}. Model fits are shown as solid lines. (c) Intrinsic $I-V$ characteristics for a 130 nm device for the same gate voltage values as in (a). V_0 = 2.2 V. (d) Intrinsic transconductance and output conductance for the same 130 nm device. (e) Maximum intrinsic transconductance and minimum output conductance as a function of channel length. (f) Drift velocity as a function of transverse electric field in the channel for the 130 nm channel-length device for three different gate voltages. The solid curves show fits calculated from the Thornber's equation for $\beta = 2$. $\beta = 1$ is shown in dashed for comparison.

Contact resistance, $R_{contact}$, as extracted by fitting the channel resistance R_{ds} at V_{ds} = 10 mV to $R_{ds} = 2R_{contact} + L/[W\mu e(n_0^2 + n^2)^{1/2}]$ where W is the width of the top-gated device, n is the carrier density modulated by the top gate, μ is the low-field field-effect mobility, and n_0 is the carrier density at the neutrality point,[19] varies between 190 and 224 Ω-μm for the devices studied here, scaling with width rather than contact area.[24] $R_{contact}$ is expected to be more important at short channel lengths as the relative contribution to the total device resistance becomes larger. To account for the adverse effect of contact resistance, we rescale the source-to-drain and source-to-gate bias according to $V'_{sd} = V_{sd} - 2I_dR_{contact}$ and $V'_{sg} = V_{sg} - I_dR_{contact}$. In Figure 2c, we plot the intrinsic transconductance after this contact resistance subtraction along with the measured one. Despite the increase in the g_m values, the decreasing trend with channel length remains unchanged.

It is well-known that transport in graphene devices is heavily degraded by charge-traps in the oxide or graphene-oxide interface.[25] This charge trapping is made worse by high drain-to-source biasing which strongly affect transistor characteristics and can be expected to have a stronger impact in short-channel devices because of hot carrier injection.[26] Pulsed $I-V$ measurements are a standard technique to avoid these adverse effects.[27,28] Figure 2d shows pulsed $I-V$ characteristics of the same 350 nm channel-length device as in Figure 2b, showing significant improvement in both device transconductance and output conductance in saturation when employing the pulsed measurement method. In these measurements, performed with a Keithley 4200 parametric analyzer, both gate and drain biases are pulsed with a pulse width of 500 ns and period of 100 μs. The back-gate is kept grounded throughout these measurements. Pulsed measurements have little effect on device characteristics for channel lengths longer than approximately 1 μm.

Figure 3a,c shows pulsed $I-V$ measurements at L of 500 and 130 nm (after contact resistance extraction). Strong saturating characteristics are consistently observed in the $I-V$ characteristics. Figure 3b,d shows the measured intrinsic device transconductance and the output conductance as function of V'_{sd}. The intrinsic transconductance of the 130 nm device exceeds 0.45 mS/μm and the minimum output conductance is 0.3 mS/μm. Figure 3e shows the maximum transconductance and minimum output conductance as a function of channel length. Both values are relatively independent of channel length, indicating that velocity saturation is the dominant cause of current saturation.

For sufficiently high vertical electric fields in the channel such that $V_{sg} + V_0 \gg V_{sd}$, where V_0 is V_{gs} ($= -V_{sg}$) at the Dirac point, the density variation in the channel can be ignored. In this case, the drain current is given by $I_d = nev_{drift}$ and the drift velocity (v_{drift}) can then be directly determined from the drain current. As shown in Figure 3f, we find that v_{drift} as a function of transverse electric field, $E_y = V'_{sd}/L$, is accurately modeled by Thornber's equation[29]

$$v_{drift} = \left(\left(\frac{1}{\mu E_y} \right)^{\beta} + \left(\frac{1}{v_{sat}} \right)^{\beta} \right)^{-1/\beta}$$

with $\beta \approx 2$, where v_{sat} is the saturation velocity, and μ the zero-field mobility, consistent with other studies for oxide dielectric

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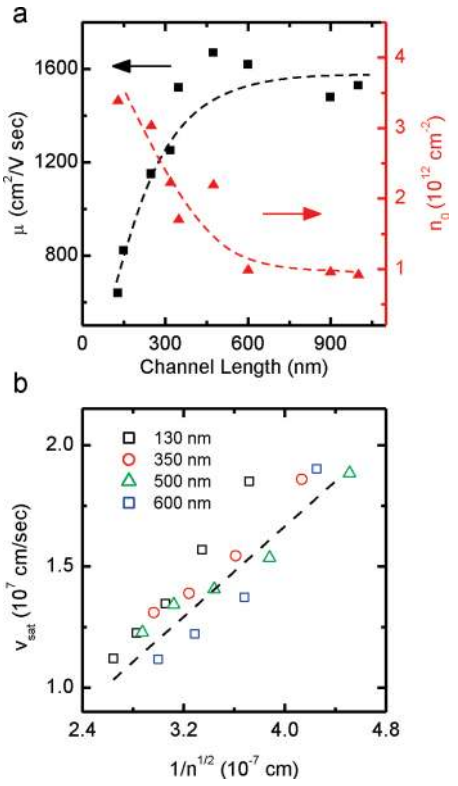

Figure 4. Channel-length scaling. (a) Field-effect mobility and impurity density versus channel length. The dashed lines are guides to the eye. (b) Saturation velocity as a function of $1/(n)^{1/2}$ calculated at the source end for different channel lengths. The dashed line corresponds to an optical phonon energy of 54 meV.

interfaces.[11] Such phenomenological modeling is commonplace in semiconductor device compact modeling and complements microscopic calculations.[10]

Figure 4a shows the field-effect mobility (μ) and minimum charge-density (n_0) as a function of L, extracted from the low-field channel conductance of the pulsed measurements. The coefficient of variation of the root-mean-square error of these fits is better than 3.5% over the full gate bias range. The same results are achieved from dc measurements, indicating that the pulsed measurements have no effect on low-field transport. The field-effect mobility increases from 640 cm^2/V sec at 130 nm channel length to ~1500 cm^2/V sec once a channel length of 500 nm is reached. n_0 follows a similar trend, decreasing from 3.4×10^{12} cm^{-2} at $L = 130$ nm to 0.92×10^{12} cm^{-2} once $L = 500$ nm is reached. We believe that this μ degradation at short channel lengths is due to e-beam damage from the metal-contact fabrication in the vicinity of the contact.[30] This degradation at short channel lengths has also been attributed to a crossover from diffusive to quasi-ballistic transport.[31] For the relatively short low-field mean free paths (28 nm at the highest carrier densities) in these devices, this mechanism is unlikely. We note that despite the degradation in low-field transport with decreasing channel length, high-field transport is unaffected, supporting a model for high-field diffusive transport that is independent of impurity scattering and determined by phonon emission.

Further support for the phonon emission model comes from the density-dependence of the saturated velocity, v_{sat}. Figure 3a−d shows a simple model fit (solid curves) along with the measured data for the $I-V$ characteristics.[5] In this case, v_{sat} is treated as a fitting parameter and the extracted v_{sat} values are shown in Figure 4b as a function of sheet density. The density dependence is consistent with a simple phonon emission model, $v_{sat} = \Omega/((\pi n)^{1/2})$. The extracted phonon energy in this model ($\hbar\Omega$) is approximately 54 meV, close to the phonon energies previously reported for similar device sturucters.[11,32] v_{sat} is independent of channel length down to the shortest gate lengths measured, indicating that transport is diffusive in the high-bias regime.

In summary, we have investigated channel length scaling in GFETs down to 130 nm channel lengths. When characterized with dc $I-V$ measurements, we observe a systematic degradation of device performance with decreasing channel length and attribute this effect to trapped charges in the gate dielectric. High-bias measurements made with a dual-channel pulsed-measurement method show current saturation even at the shortest channel lengths. Measured transconductances and output conductance are significantly improved, demonstrating the importance of trapped charge on the device performance. A method to functionalize graphene with PVA is demonstrated that enables reliable high-κ ALD growth down to 5 nm thickness.

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