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Channel Length Scaling Pattern for Cylindrical Surrounding Double-Gate (CSDG) MOSFET

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ABSTRACT The natural length of MOSFETs helps to describe the potential distribution in the Silicon substrate. This natural length varies in different device structures, from a single gate to multi-gate device geometry. To measure the short channel effects degree, the natural length should be known because various vital parameters such as OFF-current, Roll-off threshold voltage, and drain induced barrier lowering depend on it. In this research work, authors have presented a scaling theory for Cylindrical Surrounding Double-Gate (CSDG) MOSFET, which guide the device design. The scaling method has been derived, based on the application of the Poisson equation, in a cylindrical structure using Parabolic Potential Approximation (PPA) along the radial direction (substrate part only). Furthermore, a comparison with cylindrical surrounding-gate MOSFETs, Silicon-on-insulator, and double-gate device geometries has been obtained. The results obtained using the PPA model show that CSDG MOSFET has the least natural length, making it a better component for SCEs immunity.

INDEX TERMS Channel length, CSDG MOSFET, nanotechnology, natural length, scaling pattern semiconductors, short channel effects (SCEs), VLSI.

I. INTRODUCTION

The MOSFETs scaling is the driving force for the recent developments in the semiconductor industry [1]–[3]. The reason for device scaling is to increase the number of transistors (CMOS devices) in an Integrated Circuit (IC), its functionality, speed, and low operating power from one technological node to another. However, as the MOSFET size decreases, the Short Channel Effects (SCEs) become significant [4], [5]. It has been established that multi-gate MOSFETs families (Double-Gate (DG) MOSFETs, Double FinFET and Cylindrical Surrounding-Gate (CSG) MOSFETs) provides superior immunity to SCEs and higher current drive than traditional planer MOSFETs [6]–[9]. This is because the natural length is a key parameter in suppressing SCEs, and it determines the threshold voltage variation of MOSFET structures. As the multi-gate MOSFETs are scaled down into the nanometre regime ($<30\ nm$), their performance becomes compromised because of the short channel's effects.

In the previous research works, the classical natural length of the multi-gate MOSFETs have been developed for SOI MOSFETs, DG MOSFETs, and CSG MOSFETs [10]–[12].

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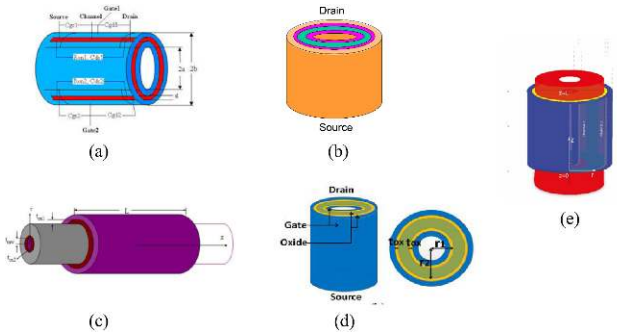

FIGURE 1. Surrounding Structures: a) CSDG MOSFET [19] b) DSG MOSFET [16] c) CSDG MOSFET [14] d) DSG [18], and e) CSDG MOSFET [37].

However, they did not consider the non-symmetrical multi-gate structures in their general analysis. Other researchers have also modeled the Cylindrical Surrounding Double-Gate (CSDG) MOSFETs as a promising device in the nearest future, as shown in Fig. 1 [13]–[19]. The nomenclature, CSDG MOSFET, has been used by several authors with a latent difference as Fig. 1(a) shows CSDG MOSFET with a hollow center for easy analysis based on the 1-D model. Although the accessibility of the source and drain are not

fully described. Fig 1(b) shows DSG (Double Surrounding Gate) MOSFET with a non-hollow (gate material) center based on a 1-D model. Fig 1(c) shows CSDG MOSFET with a non-hollow (metal + gate material) center based on the 2-D model. Fig. 1 (d) shows DSG MOSFET with a hollow center based on 1-D model. Fig 1(e) shows CSDG MOSFET with a hollow center for easy analysis based on the 2-D model.

Verma et al. [14] proposed a new non-hollow CSDG MOSFET, as shown in Fig. 1(c). Their research work focused basically on gate engineering and its behavior at the subthreshold regime. The authors further explored the vacuum gate dielectric in the analysis [20]. It concluded that CSDG MOSFET is better than other multi-gate families based on gate engineering. The 2-D Poisson equation was analyzed with the superimposition model. *Rewari et al.* [17] worked on junctionless CSDG MOSFET. The authors considered its application and replacement of Silicon oxide with Hafnium oxide for better analogue performance.

The derived natural length of close form-expression will enable the device engineers to estimate the maximum allowable Silicon thickness to avoid short channel effects in CSDG MOSFET via the scaling factor. In this present research work, the natural lengths of the CSDG MOSFET have been developed using a 2-D Poisson equation based on the PPA model [21]. These natural lengths are compared with SOI MOSFET, DG MOSFET, and CSG MOSFET concerning the variation in threshold voltage. This research paper has been organized as follows: The review of the scaling theorem of multi-gate MOSFETs is presented in section II. The mathematical derivation of the natural length for CSDG MOSFET is shown in Section III. Various effects of the natural length have been discussed in Section IV. The analytical results have been studied and compared with other multi-gate families in the Section V. Finally, Section VI concludes the work and recommend the future aspects.

II. REVIEW OF THE SCALING THEORY OF MULTI-GATES MOSFETS

The review of procedural derivation of the scaling length for multi-gates MOSFETs (SOI, DG, and CSG MOSFETs) have been performed because the CSDG MOSFETs derivation is based on the same model. These have been discussed as follows:

A. SOI, DG, AND CSG MOSFETs

The prediction of how small the Silicon thickness and gate oxide are designed to minimize the effects of short channel and to maintain the decent subthreshold swing (Fig. 2) have been developed by various researchers [22]–[28]. The researchers used the Young's model [21] to solve the Poisson Equation (cartesian and cylindrical form) with respect to different boundary conditions based on the device geometry.

The Poisson equations, the cartesian, and cylindrical form, with respect to the MOSFETs structures in Fig. 2 is given as [29]–[32]:

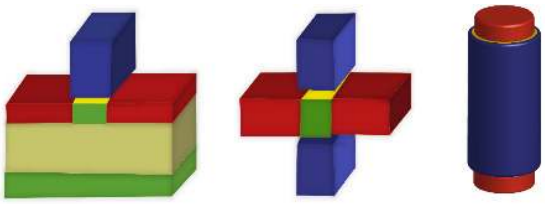

FIGURE 2. The 3D structural view of the (a) SOI MOSFET (b) DG MOSFET, and (c) CSG MOSFET.

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{d^2\psi(x,y)}{dy^2} = \frac{qN_a}{\varepsilon_{si}} \quad (1)$$

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}\psi(r,z)\right) + \frac{d^2\psi(r,z)}{dz^2} = \frac{qN_a}{\varepsilon_{si}} \quad (2)$$

where N_a, ε_{si}, and q are the doping concentration, permittivity of Silicon, and the electric charge, respectively. ψ(x, y) and ψ(r, z) are the potential distributions along with the cartesian and cylindrical form, respectively.

By applying the Parabolic Potential Approximation (PPA) model on Eq. (1) and Eq. (2) using Eq. (3) and (4) w.r.t. their respective boundary conditions along the y-axis and radial axis. The natural length has been obtained as given in Table 1.

$$\psi(x,y) = C_0(x) + C_1(x)y + C_2(x)y^2 (0 \le y \le t_{si}) \quad (3)$$

$$\psi(x,y) = C_0(z) + C_1(z)r + C_2(z)r^2 (0 \le r \le t_{si}) \quad (4)$$

The natural length of SOI MOSFETs is dependent on two parameters: oxide thickness and Silicon film. Based on *Colinge's* [33] research work on SOI MOSFETs, a decrease in Silicon thickness results to reduction in the natural length of any multi-gate MOSFETs. The work of ref. [33] has served as a benchmark for various multi-gate MOSFETs.

TABLE 1. Natural length of the MOSFETs for Figure 2.

Multi-gate MOSFETs	Model	Varying parameters	Natural length and Scaling Factor (α)
SOI MOSFET [34]	PPA	Silicon and oxide thickness	$\lambda_G = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$, $\alpha_1 = \frac{L}{2\lambda_G}$
DG MOSFET [35] (Symmetric)	PPA	Silicon and oxide thickness	$\lambda_{DG} = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right) t_{si} t_{ox}}$, $\alpha_2 = \frac{L}{2\lambda_{DG}}$
CSG MOSFET [36] (Symmetric)	PPA	Silicon and oxide thickness	$\lambda_{CSG} = \sqrt{\frac{2\varepsilon_{si} t_{si}^2 \ln\left(1+\frac{2t_{ox}}{t_{si}}\right) + \varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}}$, $\alpha_3 = \frac{L}{2\lambda_{CSG}}$

The natural length, as reported for DG MOSFETs in ref. [22], [25], have been deduced because the symmetrical device structure results in the identical potential distribution along the channel. Therefore, the minimum potential will be positioned at the center of the Silicon channel leading to a single natural length, as shown in Table 1. With this, the drain field influence on the channel can be determined.

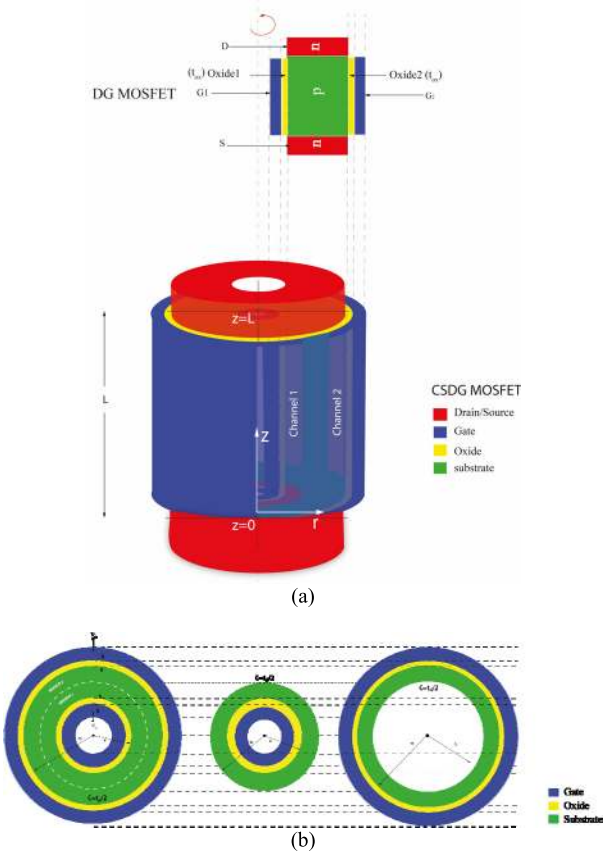

FIGURE 3. (a) CSDG MOSFET in 3D view, and (b) the 2-D circular cross-sectional view of the radial part [37].

B. CSDG MOSFET DEVICE GEOMETRY

The CSDG MOSFET is a new device structure that is like CSG MOSFET but with a double-gate. It is modeled from Double-Gate (DG) MOSFET, as shown in Fig 3(a). In comparison with traditional MOSFET, it has Silicon substrate, Gate oxide, Source, Drain, and Gate. Furthermore, it belongs to the GAA MOSFET family [37].

The DG MOSFET is folded (rotated) with respect to the z-axis to produce the CSDG MOSFET. It has an external and internal radius as $r = a$ and $r = b$, respectively. Similar to DG MOSFET, it has two gates with the extensions forming the drain and source ends [38], [39]. The boundary condition derivations are based on Fig. 3(b).

III. MATHEMATICAL MODELLING OF THE NATURAL LENGTH FOR CSDG MOSFET

The Poisson equations have been solved, based on the boundary conditions from Fig. 3, to obtain its natural length for both internal and external gates. Its relationship with threshold voltage variations has also been shown for design space. Using the Parabolic Potential Approximation (PPA) with respect to CSDG MOSFET geometry, Eq. (4) can be written as given:

$$\psi(r, z) = C_0(z) + C_1(z)r + C_2(z)r^2 (a \le r \le b) \quad (5)$$

where C_0, C_1, and C_2 are unknown variables, and r is the radius, which varies from "a" to "b" (boundary condition) to represent the internal and external gate effect on the Silicon substrate, respectively. The Eq. (5) with the boundary conditions is used to solve Eq. (2) along the radial direction.

1) Considering the center of the CSDG cylindrical structure at radius, r = 0, electric field $E = 0$, potential distribution, $\psi\ (r, z) = 0$ and $C_0(z) = 0$. The reason been that in the center of the device, no electrostatic distribution of charges.
2) The obtained surface potential with respect to the internal radius, "a" and external radius "b" as given:

$$\psi(a, z) = \psi_s(a) = C_0(z) + C_1(z)a + C_2(z)a^2 \quad (6)$$
$$\psi(b, z) = \psi_s(b) = C_0(z) + C_1(z)b + C_2(z)b^2 \quad (7)$$

3) The Electric Field (E) at the surface and at the center of the Silicon w.r.t. a Gaussian surface have been obtained. With this, the internal and external gate are considered, based on Fig. 3(b). w.r.t. the boundary conditions as follows:

- Considering the internal gate from Fig. 3(b) at $r = a$,

$$\left.\frac{d\psi(r, z)}{dr}\right|_{r=a} = C_1(z) + 2C_2(z)a = \frac{C_{oxa}(V_{gs} - V_{fb}) - \psi_s(a)}{\varepsilon_{si}} \quad (8)$$

- Considering the gaussian surface from Fig. 3(b) at point C,

$$\left.\frac{d\psi(r, z)}{dr}\right|_{r=\left(\frac{t_{si}}{2}\right)} = C_1(z) + 2C_2(z)\frac{t_{si}}{2} = -\frac{C_{oxa}(V_{gs} - V_{fb}) - \psi_s(a)}{\varepsilon_{si}} \quad (9)$$

- Considering the external gate from Fig. 3(b) $r = b$,

$$\left.\frac{d\psi(r, z)}{dr}\right|_{r=b} = C_1(z) + 2C_2(z)b = \frac{C_{oxb}(V_{gs} - V_{fb}) - \psi_s(b)}{\varepsilon_{si}} \quad (10)$$

For the internal gate, at the center of the Silicon, the electric field is non-zero because the structure is not symmetrical. Since $(t_{si}/2) > a$, this implies that $(t_{si}\text{-}2a)$ will always be positive, and the electric field with respect to the internal gate will vary within this region around the radial path. Therefore, by solving Eq. (8) and Eq. (9) simultaneously, the variables, C_1 and C_2, are given, and C_0 can be obtained from Eq. (6) w.r.t. the internal gate as follows:

$$C_2(z) = -\frac{2C_{oxa}\left((V_{gs} - V_{fb}) - \psi_s(a)\right)}{(t_{si} - 2a)\varepsilon_{si}} \quad (11)$$

$$C_1(z) = \frac{(2C_{oxa}\varepsilon_{si}t_{si} + (t_{si} - 2a)C_{oxa})\left((V_{gs} - V_{fb}) - \psi_s(a)\right)}{(t_{si} - 2a)\varepsilon_{si}} \quad (12)$$

$$C_o(z) = \psi_s(a) - \frac{(2C_{oxa}\varepsilon_{si}t_{si} + (t_{si}-2a)C_{oxa})\left((V_{gs}-V_{fb}) - \psi_s(a)\right)}{(t_{si}-2a)\varepsilon_{si}} + \frac{2C_{oxa}\left((V_{gs}-V_{fb}) - \psi_s(a)\right)}{(t_{si}-2a)\varepsilon_{si}} \quad (13)$$

By plugging Eq. (11), Eq. (12), and Eq. (13) into Eq. (5) at $r = (t_{si}/2 - a)$, the relationship between the surface potential and center potential w.r.t. the gaussian surface at point C from Fig. 3 is obtained as:

$$\psi_s(a) = \frac{1}{1 + \frac{C_{oxa}t_{si}}{\varepsilon_{si}}}\left(\psi_c(z) + \frac{C_{oxa}t_{si}}{\varepsilon_{si}}\right) \quad (14)$$

where C_{oxa} is the oxide capacitance per unit area with respect to the internal gate, given as:

$$C_{oxa} = \frac{2\varepsilon_{ox}}{(t_{si}-2a)\ln\left(1 + \frac{2t_{ox}}{(t_{si}-2a)}\right)} \quad (15)$$

And for the external gate, the oxide capacitance is given as:

$$C_{oxb} = \frac{2\varepsilon_{ox}}{(2b-t_{si})\ln\left(1 + \frac{2t_{ox}}{(2b-t_{si})}\right)} \quad (16)$$

By substituting Eq. (5) and Eq. (14) into Eq. (2), the obtained radial part of the equation w.r.t. the internal gate is:

$$\frac{8C_{oxa}(V_{gs} - V_{FB} - \psi_c(z))}{(t_{si}-2a)\varepsilon_{si}\left(1 + \frac{C_{oxa}t_{si}}{\varepsilon_{si}}\right)} + \frac{d^2\psi(r,z)}{dz^2} = \frac{qN_a}{\varepsilon_{si}} \quad (17)$$

By substituting Eq. (15) into Eq. (16), the solution obtained is given as:

$$\frac{16\varepsilon_{ox}(V_{gs} - V_{FB} - \psi_c(z))}{\varepsilon_{si}(t_{si}-2a)^2\ln\left(1 + \frac{2t_{ox}}{(t_{si}-2a)}\right) + 2\varepsilon_{ox}t_{si}(t_{si}-2a)} + \frac{d^2\psi(r,z)}{dz^2} = \frac{qN_a}{\varepsilon_{si}} \quad (18)$$

For structures that are asymmetrical, the natural length can be more than one in number. Either by creating a symmetrical structure and asymmetrical structure for the analysis to be convenient. For instance, *Tsormpatzoglou et al.* [40] derived two natural lengths for Tri-Gate MOSFET (asymmetrical structure) by splitting them into symmetrical and asymmetrical DG MOSFETs to deduce a close-form expression of the threshold voltage. In respect of this, the present research work has two natural lengths with respect to the inner and outer gates because the device structure is asymmetrical. However, these natural lengths are approximately the same. Therefore, any of the natural lengths can be used to determine the threshold voltage behavior.

The natural scaling length (λ_{CSDGa}) for CSDG MOSFET, considering the internal radius a in Eq. (18) can be described as:

$$\frac{(V_{gs} - V_{FB} - \psi_c(z))}{\lambda^2_{CSDG_a}} + \frac{d^2\psi(r,z)}{dz^2} = \frac{qN_a}{\varepsilon_{si}} \quad (19)$$

where $\lambda_{CSDGa,}$ is the natural scaling length, dependent on the new parameter, a (the internal radius), Silicon film (t_{si}), and oxide thickness (t_{ox}). Also, $(t_{si}/2) > a$, so $(t_{si} - 2a)$ will always be positive. Furthermore, the value of 'a' contributes in minimizing the short channel effects for CSDG MOSFETs:

$$\lambda_{CSDG_a} = \sqrt{\frac{\varepsilon_{si}(t_{si}-2a)^2\ln\left(1 + \frac{2t_{ox}}{(t_{si}-2a)}\right) + 2\varepsilon_{ox}t_{si}(t_{si}-2a)}{16\varepsilon_{ox}}} \quad (20)$$

Similarly, the natural scaling length (λ_{CSDGb}) w.r.t. the external gate is given as:

$$\lambda_{CSDG_b} = \sqrt{\frac{\varepsilon_{si}(2b-t_{si})^2\ln\left(1 + \frac{2t_{ox}}{(2b-t_{si})}\right) + 2\varepsilon_{ox}t_{si}(2b-t_{si})}{16\varepsilon_{ox}}} \quad (21)$$

where λ_{CSDGb} is dependent on a new parameter, b (the external radius). Also, since b>(t_{si}/2), $(2b - t_{si})$ will always be positive, and its value contributes to minimizing SCEs in CSDG MOSFETs. Therefore, proper care must be taken in choosing the values of 'b' in designing the device structure.

IV. EFFECTS OF THE NATURAL LENGTH ON THE SHORT CHANNEL BEHAVIOUR OF CSDG MOSFET

The natural length derived is used to predict the presence or absence of short channel effects. The major short channel effects considered are:

A. THRESHOLD VOLTAGE VARIATION WITH NATURAL LENGTH USING SCALING THEORY

It has been established that the natural length with respect to the gate length of multi-gate MOSFETs is exponential, dependent on the variation in threshold voltage for minimal conduction in the potential variation [41]–[44]. With this, the relationship between the derived natural length of the CSDG MOSFET and the threshold voltage roll-off is given as:

$$\Delta\varphi_{\min} \propto \Delta V_{th} \propto e^{\frac{-L}{2\lambda_{CSDG_a}}} \propto e^{\frac{-L}{2\lambda_{CSDG_b}}} \quad (22)$$

where ΔV_{th} and L are the threshold voltage roll-off and the effective device length, respectively. From Eq. (22), the scaling factor which predicts the allowable Silicon thickness of CSDG MOSFET is determined and given as:

$$\alpha_4 = \frac{L}{2\lambda_{CSDG_b}} = \frac{L}{2\lambda_{CSDG_a}} \quad (23)$$

The numerical simulation of CSDG MOSFET with variation in Silicon thickness and gate length were carried on Eq. (22) and Eq. (23) and the natural length is calculated from Eq. (21). Therefore, to ensure that the device operates within the threshold variations, the selection of the scaling factor must be done appropriately.

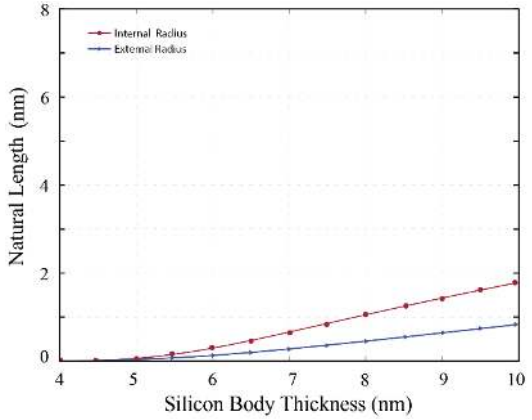

FIGURE 4. Natural length with the Silicon body thickness for the internal and external gate of CSDG MOSFET.

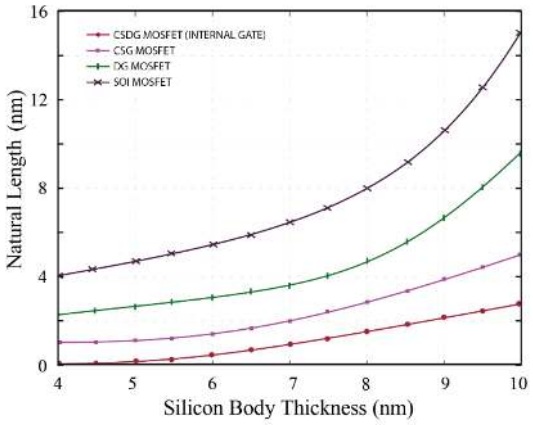

FIGURE 5. The natural length of the internal gate of CSDG MOSFET (this work) with SOI, DG, and CSG MOSFETs w.r.t. Silicon body thickness.

B. THE BEHAVIOR OF THE DRAIN INDUCED BARRIER LOWERING (DIBL) FOR CSDG MOSFET

The DIBL becomes significant when the drain voltage is raised from *0.1 V* to *1.0 V* using constant threshold voltage as given:

$$DIBL = V_{th}(V_{DS} = 0.1V) - V_{th}(V_{DS} = 1V) \qquad (24)$$

According to ref. [36], in order to ensure the acceptable value of DIBL for all multi-gate MOSFET, the scaling factor must be larger than *2.2*. Thus, the DIBL depends on the scaling factor value through the natural length.

V. RESULTS AND ANALYSIS

The natural scaling of CSDG MOSFET, threshold voltage variations, and DIBL behavior are obtained with Eq. (5) to Eq. (24). The results are compared with various multi-gate MOSFETS (SOI MOSFETs, DG MOSFETs, and CSG MOSFETs). The lists of the parameters used are given in Table 2.

TABLE 2. The parameter's values.

Parameters	Values
t_{ox}	2 nm
t_{si}	4 nm to 10nm
A	0.5 nm to 3 nm
B	0.5 nm to 8 nm
L	0 nm to 100 nm

The natural lengths of CSDG MOSFETs with respect to the variations of Silicon thickness is shown in Fig. 4. It is obvious that the natural length decreases with a decrease in Silicon thickness. This implies a decrease in the drain influence over the channel. Hence, the gates control, over the channel, increases. Also, as the Silicon thickness decreases further, the natural length w.r.t. the internal and external gate becomes approximately equal. This implies that with thin Silicon thickness, the gates offer great immunity over the channel with almost equal electrostatic integrity.

Whereas an increase in Silicon thickness lessens the gates control, over the channel, because of the increase in natural length. However, the outer gate exhibits more control over the channel as the Silicon film thickness increases. Hence, minimal values of the radii (a and b) must be chosen for the effective immunity of the SCEs.

The natural length with respect to the internal gate of CSDG MOSFET is compared with the CSG, DG, and SOI MOSFET in Fig. 5. It has been observed that the variation in Silicon thickness with respect to oxide thickness determines the device characterizations. The gates exhibit more control of the channel as the Silicon thickness decreases. Also, the natural scaling length of the internal gate of CSDG MOSFET is minimal compared to that of SOI, DG, and CSG MOSFETs. Since a small natural length is desired to minimize the SCEs on the Subthreshold slope, therefore, CSDG MOSFET is a promising device to replace CSG MOSFET in the nearest future.

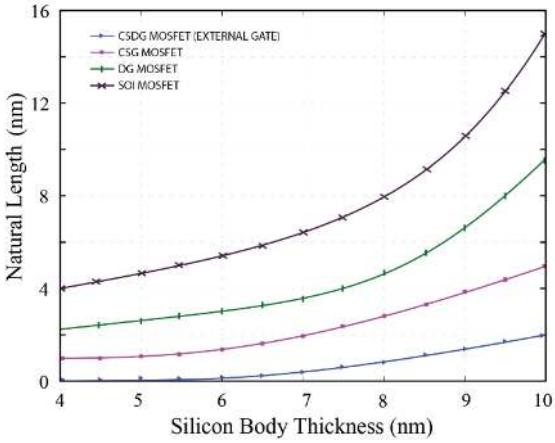

FIGURE 6. The natural length of the external gate of CSDG MOSFET (this work) with SOI, DG, and CSG MOSFETs w.r.t Silicon body thickness.

The natural length with respect to the external gate of CSDG MOSFET is compared with the CSG, DG, and SOI MOSFET in Fig. 6. Similarly, the external gate with respect

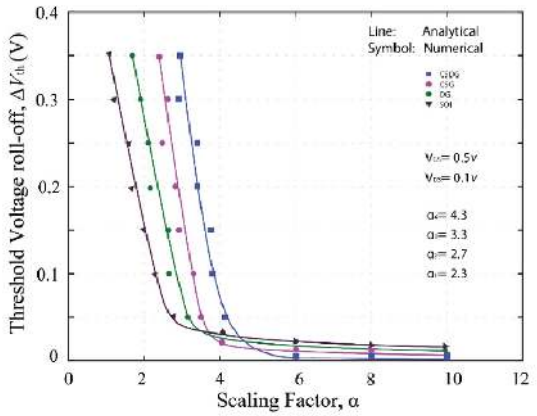

FIGURE 7. Threshold Voltage roll-off versus scaling factor for SOI, DG, CSG, and CSDG MOSFET.

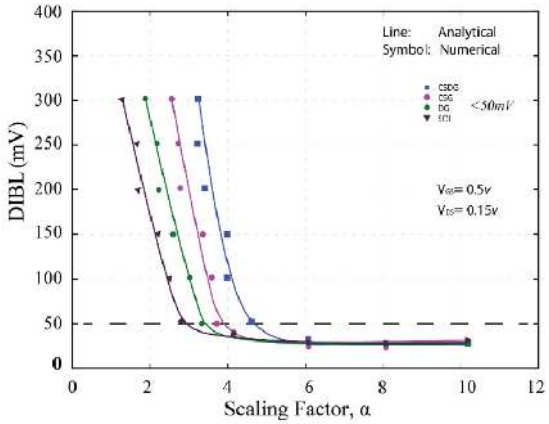

FIGURE 8. Drain Induced Barrier Lowering (DIBL) versus scaling factor for SOI, DG, CSG, and CSDG MOSFET.

to the external radius provides the smallest natural length characterization when compared with SOI, DG, and CSG MOSFET. The small natural length contributes to the device's immunity to SCEs. Also, Fig. 6 shows that the external gate has greater immunity to SCEs as the Silicon thickness increases towards *10 nm* when compared with the internal gate from Fig. 5.

The threshold voltage variation with the scaling factor is shown in Fig. 7. It is obvious that CSDG MOSFET has the least roll-off threshold voltage with the highest scaling factor (α_4) extraction of approximately *4.3* when compared with SOI, DG, and CSG MOSFET. Thus, the small natural length in CSDG MOSFET, which yields increased scaling factors, shows better immunity to SCEs. Also, numerical simulation agrees with the proposed analytical model. Fig. 8 shows a similar approach to Fig. 7. When the DIBL is investigated with respect to the scaling factor (α): As the α is reduced, the DIBL increases due to the decrease of the potential barrier in the channel caused by a short channel. It is obvious that the device structure with the least scaling factor value will be affected the most even though all the devices are within acceptable DIBL of values of < 50mV, as shown in Fig. 8. The DIBL becomes practically negligible as the scaling factor value increases.

VI. CONCLUSIONS AND FUTURE ASPECTS

In this research work, a natural scaling length characterization has been derived for the design of CSDG MOSFETs to access its scaling potential based on the internal and external gates (electrostatics). It has been observed that the external gate has a lesser scaling factor than the internal gate at higher Silicon thickness. Therefore, the electrostatic influence of the external gate over the channel is more compared to the internal gate. However, as the Silicon thickness reduces, the external and internal gate control over the channel are approximately the same. Hence, the thinner the Silicon thickness, superior the immunity of the SCEs. Also, the results show that CSDG MOSFET provides the least scaling factor in comparison with SOI, DG, and CSG MOSFET.

This device approaches the nanometer regime with respect to the variations in threshold voltage. Furthermore, since important device parameters like threshold variation and DIBL (SCEs) depend strongly on the natural length characterization, the newly derived natural length of CSDG MOSFET can be employed in determining the scaling factor.

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