Characterization analysis of UDSM LVTSCR under TLP stress*

Li Li(李立)[1,†], Liu Hongxia(刘红侠)[1], Dong Cui(董翠)[2], and Zhou Wen(周文)[1]

[1]Key Laboratory for Wide Band Gap Semiconductor Materials and Devices of Ministry of Education, School of Microelectronics, Xidian University, Xi'an 710071, China
[2]School of Science, Xidian University, Xi'an 710071, China

Abstract: The characteristics of a low-voltage triggering silicon-controlled rectifier (LVTSCR) under a transmission line pulse (TLP) and the characteristics of high frequency are analyzed. The research results show that the anode series resistance has a significant effect on the key points of the snapback curve. The device characteristics can fit the requirements of a electrostatic discharge (ESD) design window by adjusting the anode series resistance. Furthermore, the set-up time of the ESD has an influence on the turn-on voltage of the LVTSCR. A steep rising edge will cause the turn-on voltage to increase. The parasitic capacitance of the device for different voltage biases and frequencies determines the capacitive impedance, and its accuracy calculation is very important to the ESD design of high frequency circuits. Our research results provide a theoretical basis for the design of an ultra-deep sub-micron (UDSM) LVTSCR structure under ESD stress and the improvement of TLP test technology.

Key words: ultra-deep sub-micron; electrostatic discharge; transmission line pulse; low-voltage triggering silicon-controlled rectifier

DOI: 10.1088/1674-4926/32/5/054002 **EEACC:** 2570

1. Introduction

With continuous scaling down of feature size, decreasing gate oxide thickness in ICs, and increasing work frequency, the performance of ESD protection and compatibility issues becomes more and more prominent. The traditional ESD protection circuit for low-frequency analog/digital ICs cannot be used for the design of RF ICs and MMICs, so it is important to present a UDSM ESD protection circuit of high performance. When ESD happens, the main discharging devices carry much current and occupy a large chip area, which increases the cost of the chip and causes the deterioration of high-frequency parameters. Because of its relatively high discharging capability per unit area and easy adjustment of switch parameters, LVTSCR is playing a very important role in ESD protection circuits.

TLP test systems have been used to evaluate the ESD behavior of silicon devices and integrated circuits since Maloney *et al.*[1] first published the application of transmission line pulses for ESD testing in 1985. Since then, TLP has allowed tremendous insight into the electrical characteristics of ESD protection circuits and devices, which has become one of the industry standards for ESD design. The TLP method measures devices under test (DUT) mainly via a pulse-width adjustable rectangular pulse. The pulse signal has the same energy range with the HBM (human body model) test signal, which can cause similar damage to DUT[2].

Firstly, for an effective ESD protection structure, the turn-on voltage (V_T) must be lower than the breakdown voltage of the gate oxide of CMOS devices. Otherwise, the gate oxide will be broken down before the protection circuit is turned on, which will cause permanent damage when ESD takes place. Secondly, the hold-on voltage (V_H) must be higher than the working voltage of the circuit, which can ensure that the port voltage drop to the normal range and the protection circuit is turned off when the ESD event is over. This is the design window rule.

2. LVTSCR protection structure and TLP model

2.1. Theoretical basis

For a UDSM LVTSCR, ESD stress is more likely to cause local high temperature and rapid changes in high electric field. We must take into account many other effects, such as carrier velocity overshoot, the dependence of carrier diffusion and carrier temperature, the relationship between impact ionization rate and the carrier energy distribution and lattice heating effects. The drift–diffusion model is not suitable in this case, and the energy balance transport model should be taken into consideration. The energy balance transport model includes the dependence of carrier temperature on current density. To consider the influence of temperature on transient ESD events, the model should solve the heat flow equation.

In this paper, the energy balance transport effect under a non-isothermal state is taken into account in the simulation process. The general impact ionization process can be described by the equation

$$G = \alpha_n J_n + \alpha_p J_p, \tag{1}$$

where G is the total generation rate of electron-hole pairs, $\alpha_{n,p}$ is the ionization coefficient for electrons and holes and $J_{n,p}$ is their current densities. The ionization model assumes that

* Project supported by the National Natural Science Foundation of China (Nos. 60976068, 60936005) and the Cultivation Fund of the Key Scientific and Technical Innovation Project, Ministry of Education of China (No. 708083).
† Corresponding author. Email: 332808552@qq.com
Received 14 October 2010, revised manuscript received 30 December 2010

Table 1. Parameters in the impact ionization model.

Parameter	Default value	Used value	Unit
AN	7.03×10^5	default	cm^{-1}
AP	6.71×10^5	default	cm^{-1}
BN	1.131×10^6	default	V/cm
BP	2.036×10^6	default	V/cm
$\tau_0^{n,p}$	—	0.4	ps
ρ	—	0.5	—

the ionization coefficient is the function of the electric field intensity and is based on the following expressions,

$$\alpha_n = AN \exp\left(-\frac{BN}{E}\right), \tag{2}$$

$$\alpha_p = AP \exp\left(-\frac{BP}{E}\right), \tag{3}$$

where E is the electric field in the direction of current flow at a particular position in the structure and the parameters AN, AP, BN, BP are defined as a function of lattice temperature in this model. While the energy balance transport model is introduced in the simulation, for more accurate analysis, the carrier temperature must be taken into account, and the electric field E should be fixed as follows,

$$E_{eff}^{n,p} = \frac{3kT_{n,p}}{qL_{relax}^{n,p}}, \tag{4}$$

where $T_{n,p}$ is the carrier temperature for electrons and holes, $L_{relax}^{n,p}$ is the energy relaxation length, respectively, and can be calculated according to

$$L_{relax}^{n,p} = V_{sat}^{n,p} T_{aus}^{n,p}, \tag{5}$$

where $V_{sat}^{n,p}$ is the saturation velocity for electrons and holes, and can be calculated by default from the temperature dependent model,

$$V_{sat}^{n,p} = \frac{2.4 \times 10^7}{1 + 0.8 \exp\dfrac{T_L}{600}}, \tag{6}$$

where T_L is the lattice temperature, and $T_{aus}^{n,p}$ is the energy relaxation time for electrons and holes. The energy relaxation time is a key parameter that determines the time constant of carrier energy exchange. To make the model more precise, as the lattice heat flow equation is taken into account, the relaxation time is a function of carrier energy and lattice temperature,

$$T_{aus}^{n,p} = \tau_0^{n,p} \left(\frac{\varepsilon_{n,p}}{kT_L}\right)^{-\rho}, \tag{7}$$

where $\varepsilon_{n,p}$ is the average energy for electrons and holes, $\tau_0^{n,p}$ is the constants and value of 0.4 ps, ρ is determined by the scattering mechanism, and is related to the doping distribution and the electric field added, with a value in between –1.5 and 1. ρ is set to 0.5 by calibration in this paper. Table 1 gives the value of parameters in the impact ionization model.

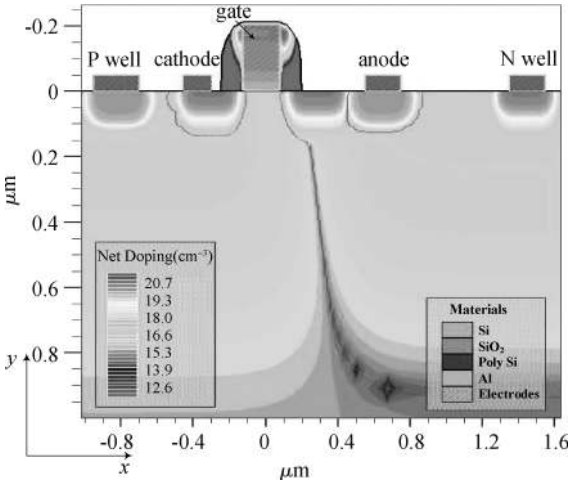

Fig. 1. LVTSCR structure of a 90 nm CMOS process.

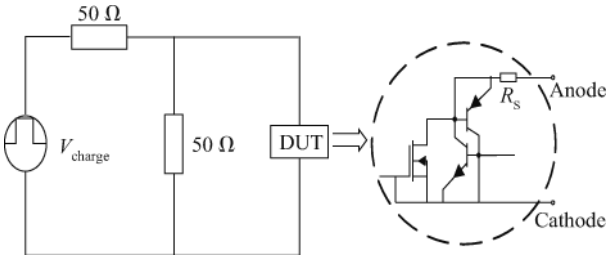

Fig. 2. Equivalent circuit of the TLP testing structure.

2.2. LVTSCR structure and TLP model

LVTSCR is simple in structure. Only an N^+ region is added compared with the traditional SCR, which can be realized with the CMOS process easily. Different from the BJT or GGNMOS, the LVTSCR is a double-injected device that has two high-doped emitters, an anode and a cathode. After turn-on, the N well–P substrate junction can be considered as a recombination centre, the holes and electrons injected from the two said emitters recombined here, furthermore, because of the positive feedback of the NPN and PNP, the collector current of each transistor becomes the base input of the other transistor. Thus, the LVTSCR has a turn-on mechanism superior to that of the single inject of the GGNMOS, and R_{on} is small[4, 5].

Figure 1 shows a LVTSCR structure of a 90 nm CMOS process; the channel length of the parasitical NMOSFET L = 0.20 μm, oxide thickness T_{ox} = 3 nm, junction depth T_j = 1.3 μm, the channel width W = 100 μm. Figure 2 shows the equivalent circuit of the TLP testing structure. Here, DUT represents the LVTSCR. The P substrate, cathode and the gate are grounded, and the voltage is used to simulate the TLP pulse. The impedance of cables and ports is 50 Ω, and R_S is the anode series resistance, which is used to reduce the reflection pulse and increase the turn-on voltage of the device.

3. Simulation results and discussion

3.1. Switching characteristics of the LVTSCR

Using the device structure shown in Fig. 1 and the equivalent circuit of the TLP testing structure shown in Fig. 2, a TLP

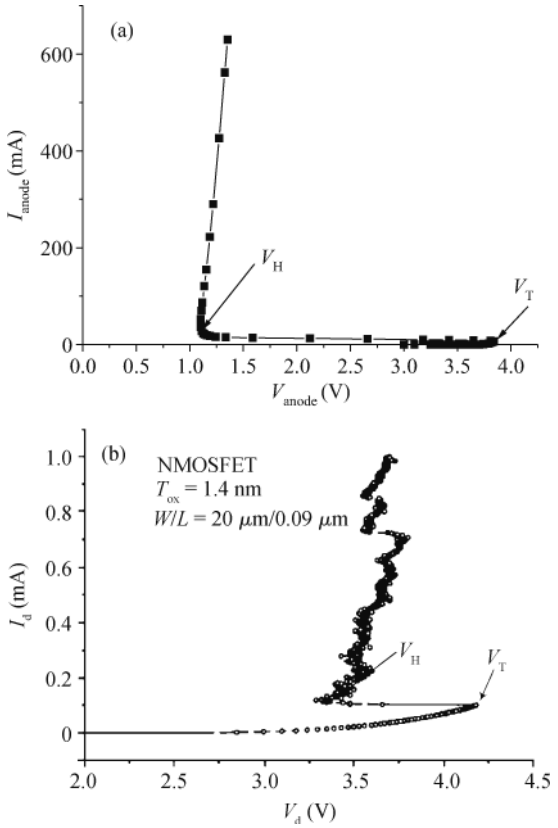

Fig. 3. CD snapback I–V curves of (a) a simulated LVTSCR structure and (b) a GGNMOS structure[4].

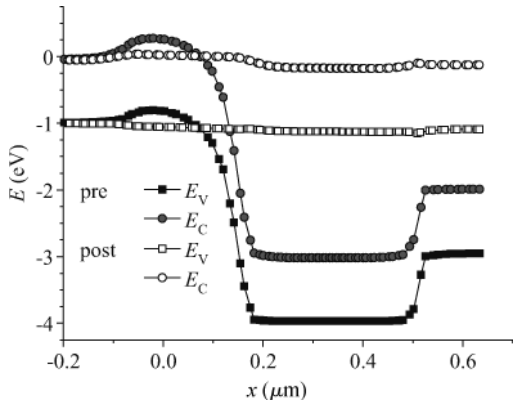

Fig. 4. Energy band of the LVTSCR.

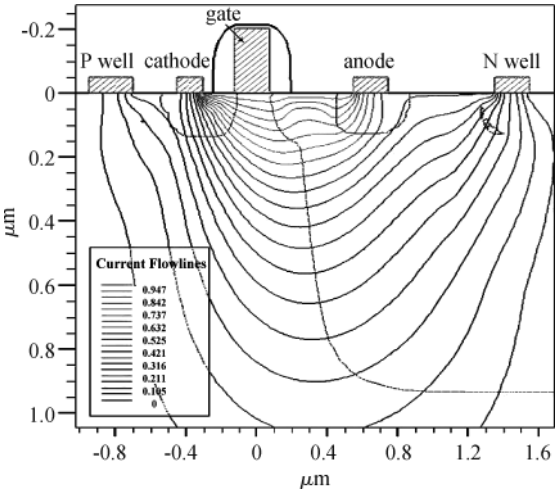

Fig. 5. Current distribution of the LVTSCR after being turned on.

pulse is applied to analyze the transient characteristics of the device. The pulse rising edge is 2 ns and the pulse width is 75 ns. We take into account the intrinsic effect and set $R_S = 0\ \Omega$. Figure 3 shows a comparison of CD snapback I–V curves of the simulated LVTSCR structure and the GGNMOS. The anode voltage is in the hold-on state after the peak, the turn-on voltage $V_T = 3.83$ V, the hold-on voltage $V_H = 1.14$ V.

By comparing the snapback curves of the LVTSCR and GGNMOS structures, we can see that the hold-on voltage of the LVTSCR structure is obviously lower than that of the GGNMOS structure when the turn-on voltages are similar. This is because two back to back P-type and N-type BJTs in the SCR structure form a conductive circuit of positive feedback, which has a smaller series resistance after being turned on. For a standard SCR, the hold-on voltage can be approximated as follows[6],

$$V_H = (V_{ben} + V_{bep} - V_r) + R_{S2}\left[(1-\alpha_{fn})I_H + \frac{\alpha_{fn}V_{ben}}{R_{S1}}\right], \quad (8)$$

where V_{ben} and V_{bep} are the voltages across the P substrate–cathode junction and the anode–N well junction, respectively. V_r is the forward bias voltage across the N well–P substrate junction. They are less than 1 when the SCR has been turned on. α_{fn} is the common-base current gain of the parasitic NPN transistor. It is a constant for the certain doping concentration. I_H is the hold-on current, R_{S1} is the shunt resistor of the parasitic NPN transistor, R_{S2} is the shunt resistor of the parasitic PNP transistor. V_H is affected by the following factors: (1) V_H increases with increasing R_{S2}, (2) V_H increases with decreasing R_{S1}, (3) V_H increases with increasing I_H. Decreasing R_{S1} causes I_H to increase. R_{S2} is related to the channel length of the parasitic NMOSFET. Increasing the channel length of the parasitic NMOSFET causes V_H to increase.

Figure 4 shows the energy band of the LVTSCR structure before and after being turned on. As we all know, the anode and N well are connected to the VDD, and the cathode and P substrate are grounded. The applied voltage minus the build in potential of the JPN, most voltage drops on the reverse biased N well–P substrate junction, which makes the heavily doped N well deviate from the equilibrium. When the reverse bias voltage increases, the distance of the conduction band and the valence band on both sides of the junction becomes so close that the electrons can pass through from the P region to the N region by direct tunneling, which is called zener breakdown. This occurs when both sides of the junction are heavily doped. In this case, the barrier region is very narrow and it does not cause avalanche breakdown.

One side of the N well–P substrate junction is heavily doped in the LVTSCR, and the dominant breakdown mechanism is the avalanche breakdown effect. After the avalanche breakdown, the voltage drops on the PN junction counteracts by the generated electron hole pairs, and the band structure is leveled and forms a pathway.

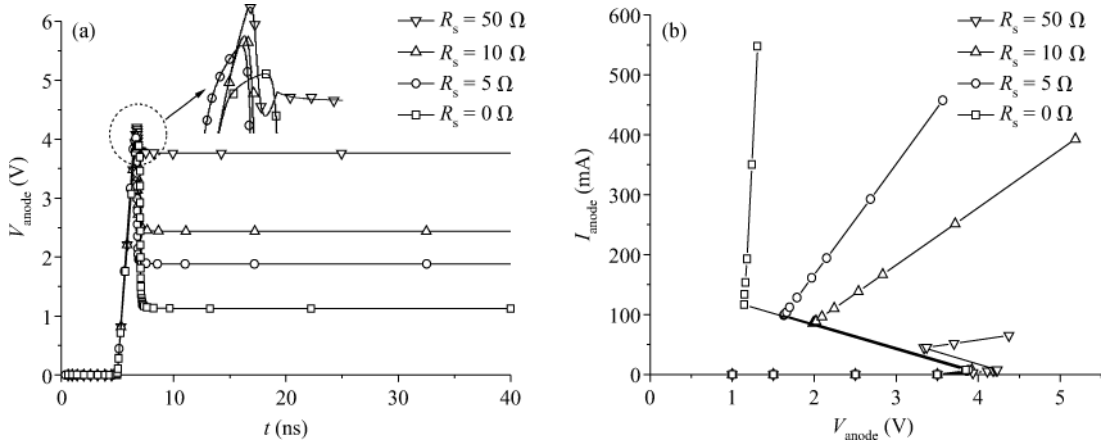

Fig. 6. Simulation results of the TLP test for different R_S. (a) Transient simulation. (b) Snapback $I-V$ curves.

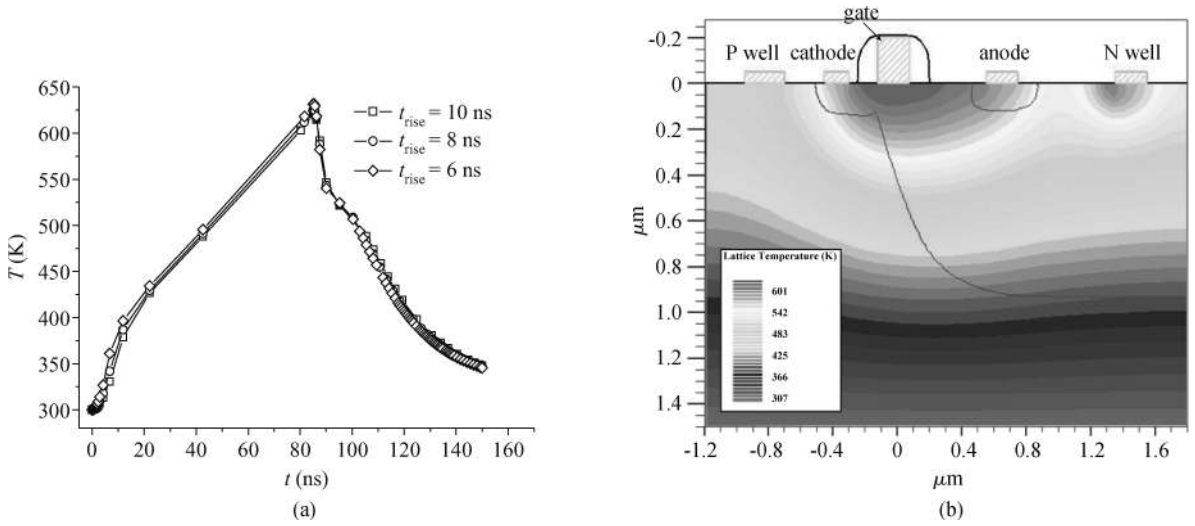

Fig. 7. Thermal effect under TLP stress. (a) Relationship of anode temperature and time. (b) Temperature distribution.

Figure 5 shows the current distribution of the LVTSCR after it is turned on. One can see that the majority of the current concentrate near the surface between the anode and the cathode is due to the heavily doped concentration except the channel region of parasitic NMOSFET. Therefore, temperature increases quickly in the region.

Because of lower turn-on resistance, the LVTSCR has less power dissipation and can carry larger ESD current. Therefore, the ESD protection circuit of the LVTSCR structure is more efficient than that of the GGNMOS structure. In other words, for the same protection level, the parasitic junction capacitance of the LVTSCR structure decreases because of the small area. Therefore, the LVTSCR has many more advantages for high frequency applications.

3.2. Influence of R_S on snapback

After turn-on, the anode series resistor R_S prevents the current discharge. On the one hand, it increases V_T and V_H. On the other hand, it causes much more power dissipation. So, R_S should be designed properly.

In this section, the transient characteristics of the device are analyzed for different anode series resistors. $R_S = 0$, 5, 10 and 50 Ω. Figure 6(a) shows the results of transient simulation with a 2 ns rise time and 100 ns width. Figure 6(b) shows the simulated TLP test for different R_S. V_T and V_H increase with increasing R_S, and V_H increases faster than that of V_T. In order to obey the design rule of the ESD window, R_S needs to be adjusted to an appropriate range. We should also take the thermal effect of R_S into consideration at the same time to avoid the device failure caused by high power dissipation.

Figure 7 shows the thermal effect under TLP stress; the rise times are 2, 5 and 10 ns, respectively. The relationship of anode temperature and time is shown in Fig. 7(a), and the temperature distribution of the LVTSCR is shown in Fig. 7(b). When the ESD happens, the temperature between the anode and the border of the N well increases quickly. When the rising edge of the TLP is over, the anode current is around 120 mA/μm, and the maximum temperature of the device is 621 K at 85 ns, which is close to the failure temperature of the device. In addition, the distribution of the ESD is not uniform because the layout structure is not uniform. In addition, poor heat dissipation is caused by other factors, such as the package, so the actual situation may not be so ideal. Therefore, the redundancy design and layout structure optimization must be taken into consideration. For example, adding the shunt resistors near the interconnections.

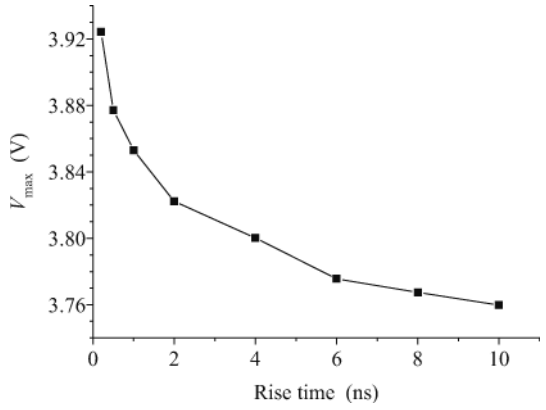

Fig. 8. Relationship of the TLP rise time and the maximum anode voltage.

3.3. Influence of ESD set-up time on device characteristics

Generally speaking, the set-up time of the ESD is about 0.2–20 ns. Considering the impact of the TLP rise time on V_T, we set the rise time of the signal as 0.2–10 ns. Figure 8 shows the relationship between the TLP rise time and the maximum anode voltage. For the same pulse amplitude, V_T increases with decreasing rise time. V_T is 3.760 V when the rise time is 10 ns, and V_T increases to 3.924 V when the rise time is 0.2 ns. This is caused by the delay effect of the N well–P substrate junction capacitance. The shorter the TLP rise time, the more significant the delay effect becomes. The delay effect causes charge accumulation near the junction. The maximum anode voltage increases with decreasing rise time.

3.4. High frequency characteristic

As the main discharging element of the ESD protection structure, the performance of the LVTSCR mainly depends on the capacitance parameters of different ports, especially in high frequency applications. The parasitic capacitance of the device determines the response rate for ESD events. At the same time, it causes additional capacitive load to the working circuit and may cause impedance mismatch, noise or other problems.

To discharge a big ESD current, the LVTSCR is usually much larger than other devices. There will be a big barrier capacitance at the N well–P substrate in the LVTSCR, and the heavily doped N-type bridge area may have some impact on the capacitance. When one side is heavily doped, the PN junction can be approximately considered as an abrupt junction, and the barrier capacitance dominates for the reverse bias.

$$C_T = A\sqrt{\frac{\varepsilon_{Si}\varepsilon_0 q N_B}{2(V_D - V)}}, \tag{9}$$

where A is the junction area, N_B is the impurity concentration of the lightly doped side, $V_D - V$ is the reverse bias voltage, and C_T is proportional to the square root of N_B. The junction capacitance of the LVTSCR can be controlled by adjusting the impurity concentration of the channel region of the parasitic NMOSFET.

Figures 9(a) and 9(b) shows the C–V and C–f characteristics of the LVTSCR for the channel width of 100 μm. Figure

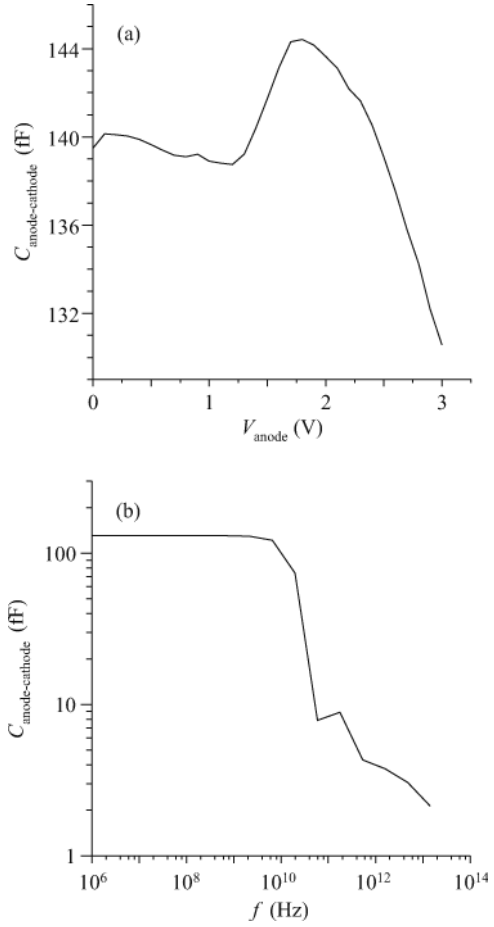

Fig. 9. Capacitive characteristics of the LVTSCR ($W = 100$ μm). (a) C–V. (b) C–f.

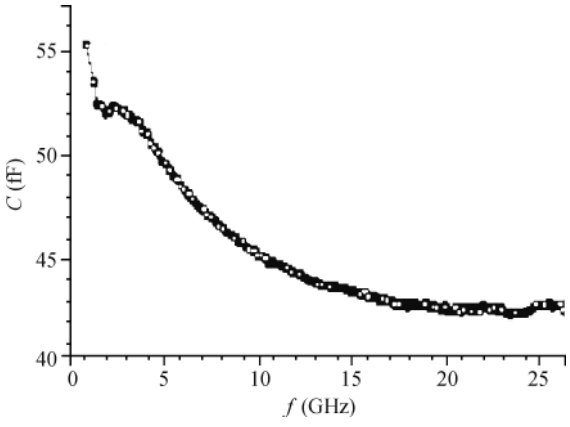

Fig. 10. Measured C–f curve of the LVTSCR with a 50 μm circumference N well.

10 shows the measured C–f curve of the LVTSCR with a 50 μm circumference N well in Ref. [7]. The LVTSCR presented in this paper has a parasitic capacitance of around 100 fF for applications below 10 GHz. However, with the increase in frequency and frequency span, the non-quasistatic effect becomes more significant. The change frequency of the carrier cannot follow that of the signal change, which causes the decrease in the equivalent capacitance.

By comparing Fig. 9(b) and Fig. 10, it can be seen that

the parasitic capacitance of the simulated device is at a reasonable level. Thus, for a LVTSCR structure with a channel length of 0.20 μm, the parasitic capacitance is about 100–140 pF per 100 μm width, while the LVTSCR with a 50–100 μm width can satisfy a 2–4 kV HBM protection sufficiently, and the parasitic capacitance taken into the RF circuit is much less than GGNMOS and is at a similar level with the STI (shadow trench isolation) diode, and the circuit can be easily matched by adjusting other elements.

4. Conclusion

In this paper, a mixed mode simulation is used for the TLP test of a LVTSCR structure[8], and the working mechanism of the device is investigated. The influences of the anode series resistance and the pulse rise time on the device characteristics under TLP stress are analyzed in detail. The results show that the LVTSCR presented here has a relatively lower V_T, and the V_H can be easily adjusted by altering its anode series resistance, which can make the protection structure fit the ESD design window very well. Due to the thermal effect of high current, the ability of the discharging ESD current can achieve 30 mA/μm, which will not cause an obvious increase in the lattice temperature. The ESD set-up time also impacts on the turn-on voltage, and the fluctuation of the turn-on voltage does not exceed 0.2 V in the normal spectrum of the ESD set-up time. In addition, the LVTSCR structure in this paper has a lower parasitic capacitance, which is more suitable for high-frequency applications. The analysis here provides some guidance for the TLP test of LVTSCRs, and it is also a good reference for the application of an LVTSCR structure in an ESD protection circuit.

References

[1] Barth J E, Verhaege K, Henry L G, et al. TLP calibration, correlation, standards, and new techniques. IEEE Trans Electron Packag Manuf, 2001, 24(2): 99

[2] Lee J C, Hoque M A, Croft G D, et al. A method for determining a transmission line pulse shape that produces equivalent results to human body model testing methods. EOS/ ESD Symposium Proceedings, 2000: 97

[3] Mergens M P J, Russ C C, Verhaege K G, et al. Speed optimized diode-triggered SCR (DTSCR) for RF ESD protection of ultra-sensitive IC nodes in advanced technologies. IEEE Trans Device Mater Reliab, 2005, 5(3): 532

[4] Concannon A, Vashchenko V A, Beek M T, et al. A device level negative feedback in the emitter line of SCR structures as a method to realize latch-up free ESD protection. IEEE 41st Annual International Reliability Physics Symposium, 2003: 105

[5] Vashchenko V A, Concannon A, Beek M T, et al. High holding voltage cascoded LVTSCR structures for 5.5-V tolerant ESD protection clamps. IEEE Trans Device Mater Reliab, 2004, 4(2): 273

[6] Troutman R R. Latch up in CMOS technology: the problem and its cure. Kluwer Academic Publishers, 1986: 82

[7] Lee J H, Wu Y H, Peng K R, et al. The embedded SCR NMOS and low capacitance ESD protection device for self-protection scheme and RF application. IEEE Custom Integrated Circuits Conference, 2002: 93

[8] Chatterjee A, Polgreen T. A low-voltage triggering SCR for on-chip ESD protection at output and input pads. IEEE Electron Device Lett, 1991, 12(1): 21