

# Characterization and Application of 600 V Normally-off GaN Transistors in Hard Switching DC/DC Converters

Thomas Heckel and Lothar Frey

Chair of Electron Devices  
Friedrich-Alexander-University Erlangen-Nuremberg  
Cauerstr. 6, 91058 Erlangen, Germany  
thomas.heckel@leb.eei.uni-erlangen.de

Stefan Zeltner

Power Electronic Systems  
Fraunhofer IISB  
Schottkystr. 10, 91058 Erlangen, Germany

**Abstract**—As GaN power devices emerge from research to industry, the characterization of these novel devices itself and its application in power electronic converters is essential. The purpose of this paper is to prove the capabilities of GaN technology using a novel 600 V normally-off GaN-on-Si transistor which shows no dynamic behavior of its on-resistance. A hard switching DC/DC converter prototype reveals efficiencies up to 99.3 % and switching frequencies up to 1 MHz incorporating a high power density up to 28 kW/l.

## I. INTRODUCTION

Since years, the suitability and the application of GaN devices in power electronics is being discussed. In recent years, progress has been made towards commercialization, but devices in the breakdown voltage class of 600V are not available yet. The aim of this paper is to prove the capabilities of the GaN technology using the example of a typical power electronic application.

Table I shows the key characteristics of the GaN device manufactured by Panasonic which is used both for the characterization and the DC/DC converter presented in this paper.

TABLE I. GAN TRANSISTOR KEY CHARACTERISTICS

Manufacturer	Panasonic
Device technology	GaN-on-Si
Gate characteristic	Normally off
Blocking voltage [V]	600
$R_{ds,on,tp}$ [mOhm]	75
Dynamic $R_{ds,on}$	No

## II. DYNAMIC DEVICE CHARACTERIZATION

While static device characterization may be done with curve tracers, the dynamic characterization of the switching behavior in the nanosecond time base remains challenging due to the lack of commercially available measurement setups. Therefore, a detailed study on the measurement itself is necessary. As a result, a special measurement setup has been designed, built, and verified.

## Measurement Setup

A very common application of power semiconductor transistors is clamped inductive switching. Therefore, the well-known double pulse technique [1] was chosen which emulates this use case. Fig. 1 shows the special double pulse measurement setup.



Figure 1. Double pulse measurement test bench with extended features compared to conventional setups.

When measuring high speed power switching devices, the parasitic capacitance and inductance of the setup have to be extremely low compared to commercial power electronic circuit designs. As a result, this was the main focus during the development of the setup.

The energy supply was established by lead accumulators and inverters. The oscilloscope, the high voltage source, pulse generator and auxiliary unit are, therefore, fully galvanic isolated from the AC mains. This is also the case for the gate drive supply which is powered from batteries. Furthermore, plastics were used as construction material to avoid any

parasitic capacitive coupling path. The control of the whole setup is done by a lab computer which is not shown in Fig. 1. The galvanically isolated data connection is realized by optical fiber cables. With every performed measurement, more than 100 setup settings are documented in order to ensure the repeatability of each measurement. Another feature is the automated protocol generation which includes all monitored waveforms and automated calculations e.g. switching energy, switching times, gate charge according to standards, e.g. JEDEC and IEC. The raw data of the waveforms are automatically saved in a separate file to enable further analysis. Table II summarizes the main features of the measurement setup with an excerpt of the extended features compared to conventional double pulse measurement setups [1].

TABLE II. MAIN FEATURES OF THE PRESENTED DOUBLE PULSE MEASUREMENT SETUP

Max. switching voltage [V]	2000
Max. switching current [A]	100
Device temperature [°C]	- 40 - + 200
Gate supply voltage range [V]	- 35 ... + 35
Examples of measured parameters:	
<ul style="list-style-type: none"> <li>• Gate charge</li> <li>• On-resistance and internal gate resistance</li> <li>• Switching energy and transition times according MOSFET- and IGBT standards</li> <li>• Diode characteristics</li> </ul>	

The temperature of the device under test is set with air which flows around the device in order to avoid any additional parasitic electrical capacitance. Moreover, the device temperature is measured contactless with an infrared thermometer.

Another important aspect is the measurement of the drain current and drain source voltage. Due to fully galvanic isolation of the measurement setup, a high bandwidth shunt and a passive high voltage probe can be used. The parasitic inductance of the connection from the probes to the printed circuit board is minimized by fully coaxial adapters. This combination is suitable for high speed switching devices and is shown in the next section.

#### Setup Verification

The verification of the measurement setup is shown within three examples: Measurement of the gate charge  $Q_g$ , on-resistance  $R_{ds,on}$  and switching times in the nanosecond range.

According to standards, the gate charge is measured with a separate measurement setup which supplies a constant gate current source [2]. In this paper, the gate charge is measured within the double pulse technique at clamped inductive load without an additional setup. The gate current is measured indirectly by the gate driver output voltage  $u_{DRV}$  and gate source voltage  $u_{gs}$ . As the resistance of the external gate resistor  $R_{g,ext}$  is known, the gate charge  $Q_g$  can be calculated according to (1).

$$Q_g = \int i_g dt = \int \frac{u_{DRV} - u_{gs}}{R_{g,ext}} dt \quad (1)$$

This technique is verified with a silicon MOSFET showing a typical gate charge of 23 nC. Fig. 2 shows the measurement while taking into account the internal gate resistance and parasitic source inductance. The comparison of the measured values to the datasheet shows good agreement (Tab. III).

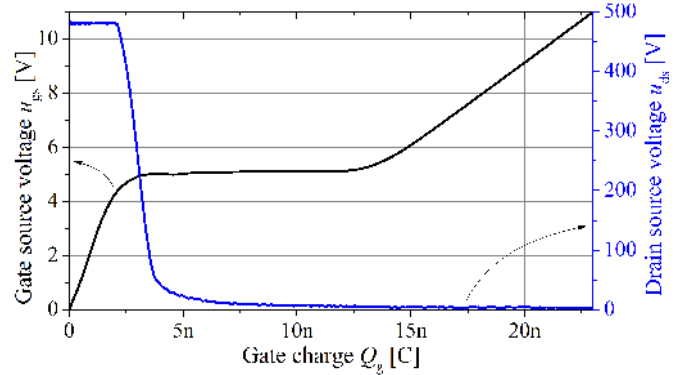


Figure 2. Gate charge measurement results of the silicon reference device obtained within the double pulse setup.

Another serious phenomenon with GaN power transistors is the dynamic  $R_{ds,on}$  [3]. Its measurement within a double pulse test is challenging: For example, when switching 400 V, 10 A with a 50 mOhm device, the drain source voltage in the on state  $u_{ds,on}$  is only 0.5 V. Using a high resolution 12 bit oscilloscope at 42 V/div, the vertical discretization step  $U_{step}$  yields according to (2) to 0.1 V.

$$U_{step} = \frac{420 \text{ V}}{2^{12}} \approx 0.1 \text{ V} \quad (2)$$

Comparing the discretization step of 0.1 V to the on state voltage of 0.5 V, the maximum relative error is at a level of 20 % when the  $R_{ds,on}$  is calculated with a measured drain current of 10 A. A special clamping adapter is used and optimized to perform the verification with a 19 mOhm silicon reference device (Tab. III). The contact resistance of the clamping connection was measured to be 4 m $\Omega$  and taken into account when calculating the  $R_{ds,on}$  from the measurement.

TABLE III. COMPARISON OF TYPICAL DATASHEET VALUES AND MEASUREMENT RESULTS OF SILICON REFERENCE DEVICES

Parameter	Datasheet (typical values)	Measurement
<i>Reference Dev. #1</i>		
$Q_{gs}$ [nC]	2.75	2.5
$Q_{gd}$ [nC]	12	11
$Q_{g,0-10V}$ [nC]	23	21.5
<i>Reference Dev. #2</i>		
$R_{ds,on}$ [m $\Omega$ ]	19	19

The verification of the drain source voltage and drain current measurement is realized with a separate calibration board equipped with a RF MOSFET. This results in extremely fast switching transients compared to common power MOSFETs. The measured transition times of 2.5 ns at a

switching voltage of 600 V were confirmed by simulation using the small signal model provided from the manufacturer of the RF MOSFET. Moreover, this setup also allowed for taking into account the time skew between drain current and drain source voltage measurement.

### III. GAN DEVICE MEASUREMENTS

The measurements performed in this section are based on the techniques described in section II. The results provide necessary information on the GaN devices to determine suitable operating points of the application in a DC/DC converter. Further measurements of parameters like switching energy and body diode characteristics were performed but are not shown in this paper because of its scope.

#### Gate Charge

Fig. 3 shows the measured gate charge characteristics of the GaN transistor which reveals a very low gate charge of 10 nC for a 600 V and 75 mOhm device.

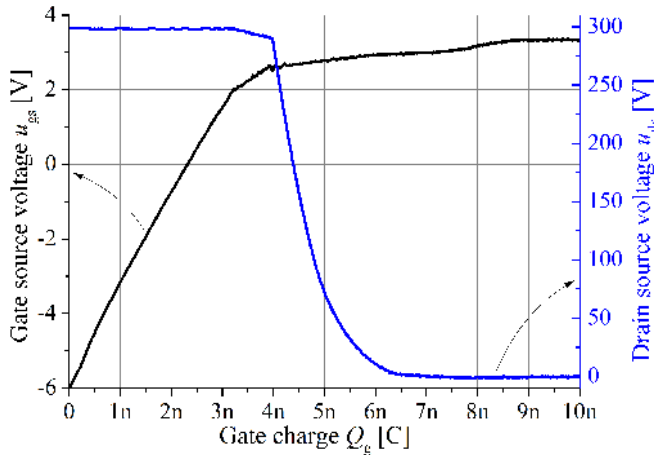


Figure 3. Gate charge of GaN Transistor when switching 300 V, 10 A at clamped inductive load.

The low gate charge results in reduced gate drive power compared to conventional silicon based counterparts. When using  $-6$  V and  $+4$  V amplitude of gate drive voltage and a switching frequency  $f_{sw}$  of 1 MHz, the dynamic gate drive power  $P_{g,dyn}$  is at a very low level of 0.1 W (3).

$$\begin{aligned} P_{g,dyn} &= Q_g \cdot (U_{DRV+} - U_{DRV-}) \cdot f_{sw} = \\ &= 10 \text{ nC} \cdot 10 \text{ V} \cdot 1 \text{ MHz} = 0.1 \text{ W} \end{aligned} \quad (3)$$

The initial rise and plateau of the gate charge  $Q_g$  can clearly be seen in Fig. 3. Compared to the characteristics in Fig. 2, the second rise after the plateau is slightly visible and the gate voltage  $u_{gs}$  does not rise to the drive output voltage level  $U_{DRV+}$  of  $+4$  V. This is caused by the GaN GIT (gate injection transistor [4]) device concept: A constant gate current of approximately 2 mA is necessary to keep the device in the on-state. Due to this current and the resistive voltage divider formed by the internal and external gate resistance, the measured gate source voltage  $u_{gs}$  does not rise to the positive gate drive level  $U_{drv+}$  of 4 V.

#### On-resistance

Another important aspect for the dynamic operation is the verification of the on-resistance  $R_{ds,on}$ . Fig. 4 shows the measurement result of the  $R_{ds,on}$  immediately after turn on of the GaN transistor when switching an inductive load at a switching current of 10 A. As increasing quiescent drain source voltage in the off-state results in a higher dynamic  $R_{ds,on}$  in the on-state [5], the switching voltage is set to a high value of 300 V. For the measurement in Fig. 4, a large time scale of 5  $\mu$ s is chosen to clarify that the  $R_{ds,on}$  does not change even several microseconds after being turned on. In order to emulate the use case in a DC/DC converter, this measurement is performed at different temperatures up to 150  $^{\circ}$ C.

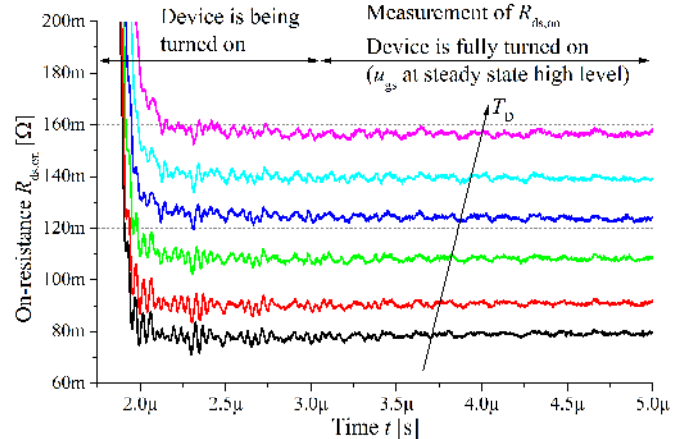


Figure 4. On-resistance of the GaN Transistor as a function of device temperature  $T_D$  at 30  $^{\circ}$ C, 50  $^{\circ}$ C, 75  $^{\circ}$ C, 100  $^{\circ}$ C, 125  $^{\circ}$ C and 150  $^{\circ}$ C. The clamped inductive switching test was performed at 10 A while the drain source voltage of 300 V in the off state was applied for 15 s.

In contrast to previously developed GaN transistors, no dynamic behavior of the  $R_{ds,on}$  can be observed (Fig. 4). Furthermore, the obtained average value of 79 mOhm matches very well with the typical static  $R_{ds,on}$  of 75 mOhm given in the preliminary datasheet at room temperature. As a result, it can be concluded that there is no dynamic behavior of the  $R_{ds,on}$ . Even at a switching voltage up to 400 V, no dynamic behaviour of the on-resistance can be observed in the measured temperature range.

### IV. GAN DC/DC CONVERTER

The results obtained from the single device characterization are used for a proper design of a GaN DC/DC converter. A hard switching boost DC/DC converter topology with a low number of passive components was chosen to demonstrate the performance of the GaN devices (Fig. 5). Beside the GaN transistor, a discrete GaN diode manufactured by Panasonic is used within this topology.

The compact setup of the GaN DC/DC converter shown in Fig. 6 is realized with a single water cooled heatsink for the GaN devices and the inductor. Moreover, the gate drive circuitry is also integrated within the low inductive printed circuit board.

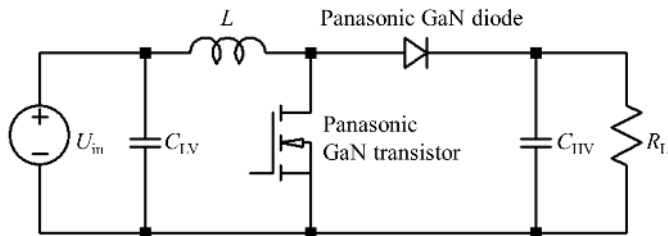


Figure 5. Hard switching boost DC/DC converter topology incorporating GaN transistor and diode.

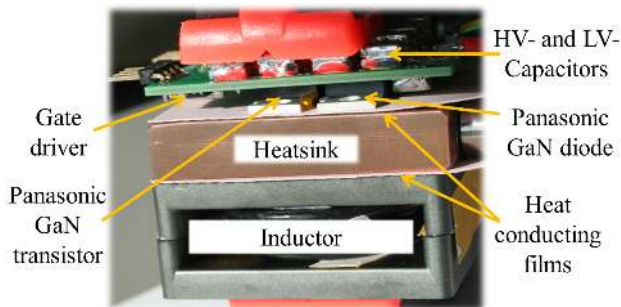


Figure 6. Prototype setup of boost DC/DC converter including GaN devices, gate drive circuit, capacitors, heatsink and inductor.

Table IV shows the parameters for the evaluation of the DC/DC converter including variations in input voltage  $U_{in}$ , output voltage  $U_{out}$  and output power  $P_{out}$ .

TABLE IV. CONFIGURATION OF THE GAN DC/DC CONVERTER FOR EVALUATION PURPOSES

Configuration #	1	2	3
Input voltage $U_{in}$ [V]		200	300
Output voltage $U_{out}$ [V]		240	360
Output power $P_{out}$ [kW]	0.6	1.5	2.5

The converter was operated in continuous conduction mode at configuration 2 and 3 in order to load the GaN devices with turn on and turn off current. Fig. 7 shows the measured efficiencies of the DC/DC converter with GaN devices at output voltages  $U_{out}$  up to 360 V. A maximum switching frequency  $f_{sw}$  of 1 MHz, efficiencies  $\eta$  up to 99.3 % and output powers  $P_{out}$  up to 2.5 kW could be obtained.

As the GaN DC/DC converter has a volume  $V$  of only  $0.09 \text{ dm}^3$ , the maximum power density  $P_{V,max}$  can be calculated (4).

$$P_{V,max} = \frac{P_{out,max}}{V} = \frac{2.5 \text{ kW}}{0.091} = 28 \text{ kW/l} \quad (4)$$

As the calculated loss of 4.2 W at 99.3 % efficiency is very small compared to the output power of 600 W, the electrical measurement becomes very challenging. Therefore, a calibrated calorimetric setup was used to confirm peak efficiencies of 99.3 % calculated from electrical measurements.

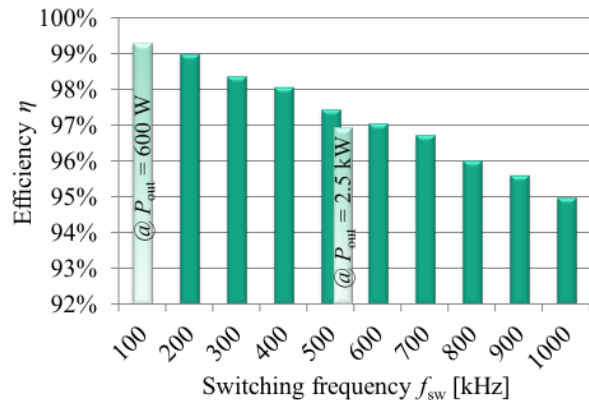


Figure 7. Efficiency results of the GaN DC/DC converter at the operating points given in Table IV. If not otherwise stated, the output power is 1.5 kW.

## V. CONCLUSION

In this paper, an extract of the comprehensive approach from device to system characterization is shown. The special double pulse measurement setup allows for the extensive characterization of the novel GaN transistor which serves as a basis for the proper design of both the gate drive circuit and the operating points of the DC/DC converter. As a result, peak output powers up to 2.5 kW could be realized in combination with a power density up to 28 kW/l. Moreover, peak efficiencies up to 99.3 % could be confirmed with a calorimetric setup and demonstrate the potential of future GaN based power electronic systems. Another aspect of these GaN transistors not discussed in this paper is the very low charge of its body diode compared to silicon counterparts. Therefore this device is beneficial for future power electronic applications requiring soft body diode turn off like hard switching bidirectional power stages.

## ACKNOWLEDGMENT

The work on dynamic device characterization was supported by the German Federal Ministry of Education and Research. The authors would like to thank Mr. Hideki Nakata (Panasonic Corporation) for fruitful discussions and providing GaN device samples.

## REFERENCES

- [1] Zheng Chen; Boroyevich, D.; Burgos, R.; Wang, F., "Characterization and modeling of 1.2 kV, 20 A SiC MOSFETs," *Energy Conversion Congress and Exposition*, 20-24 Sept. 2009
- [2] International Electrotechnical Commission, "Metal-oxide-semiconductor field-effect transistors (MOSFETs) for power switching applications," IEC 60747-8-4:2004
- [3] Hilt, O.; Bahat-Treidel, E.; Eunjung Cho; Singwald, S.; Würfl, Joachim, "Impact of buffer composition on the dynamic on-state resistance of high-voltage AlGaIn/GaN HFETs," *24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2012, 3-7 June 2012
- [4] Ishida, M.; Uemoto, Y.; Ueda, T.; Tanaka, T.; Ueda, D., "GaN power switching devices," *International Power Electronics Conference*, 2010, 21-24 June 2010
- [5] Donghyun Jin; del Alamo, J.A., "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," *24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 3-7 June 2012