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To the Graduate Council:

I am submitting herewith a dissertation written by Seyeoul Kwon entitled "Characterization and Fabrication of Active Matrix Thin Film Transistors for an Addressable Microfluidic Electrowetting Channel Device." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Materials Science and Engineering.

Philip D. Rack, Major Professor

We have read this dissertation and recommend its acceptance:

Michael L. Simpson, Thomas T. Meek, Syed K. Islam

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Characterization and Fabrication of Active Matrix Thin Film Transistors for an Addressable Microfluidic Electrowetting Channel Device

A Dissertation
Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

Seyeoul Kwon

December 2010

Dedicated to Jung Yun, June Esther, and my parents

ABSTRACT

The characterization and fabrication of active matrix thin film transistors (TFTs) has been studied for an addressable microfluidic electrowetting channel device as application. A new transparent semiconductor material, Amorphous Indium Gallium Zinc Oxide (a-IGZO), is used for TFT, which shows high electrical performance rather than amorphous silicon based TFT; higher mobility and even higher transparency. The purpose of this dissertation is to optimize each TFT process including the optimization of a-IGZO properties to achieve robust device for application. To minimize hysteresis of TFT curves, the gate dielectric is discussed extensively in this dissertation. By optimizing gas ratio of NH_3/SiH_4, it is found that the TFT with NH_3 rich SiN_x gate dielectric deposited with NH_3/SiH_4 =5.1 and stoichiometric SiO_2 demonstrates best condition to reduce hysteresis. a-IGZO films is investigated as a function of power and substrate bias effect which affects to electrical performance; the higher power and substrate bias increase the carrier density in the film and mainly cause threshold voltage(V_T) to shift in the negative gate voltage direction and mobility to increase, respectively. In addition, the powerful method to estimate the electrical properties of a-IGZO is proposed by calculating O_2 and IGZO flux during sputtering in which the incorporation ratio with O_2/IGZO ≈1 demonstrates the optimized a-IGZO film for TFT. It is confirmed that both physical and chemical adsorption affects the electrical property of a-IGZO channel by studying TFT-IV characteristics with different pressure and analyzing X-ray photoelectron spectroscopy (XPS), which mainly affects the V_T instability. The sputtered SiO_2 passivation shows better electrical performance. To

achieve electrically compatible (lower back channel current) a-IGZO film to SiO_2 sputter passivated device, a-IGZO TFTs require oxygen rich a-IGZO back channel by employing two step a-IGZO deposition process (2nd 10nm a-IGZO with PO_2 = 1.5mTorr on 1st 40nm a-IGZO with PO_2=1mTor). Electrowetting microfluidic channel device as application using a-IGZO TFTs is studied by doing preliminary test. The electrowetting channel test using polymer post device platform is candidate for addressable electrowetting microfluidic channel device driven by active matrix type a-IGZO TFT.

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Chapter 1

Introduction

1.1 Motivation of this work

Thin film transistors (TFTs) have been used as key elements in order to control, switch, and drive electronic devices. Conventionally, one of the main applications for TFTs has been flat panel display such as liquid crystal displays (LCDs) and organic light emission displays (OLEDs) in which amorphous silicon (a-Si) and polycrystalline silicon (poly-Si) usually have been used as the semiconductor active layer. In spite of the many benefits of silicon based semiconductors, there has been growing limits due to their intrinsic material properties in some applications such as transparent, high speed switching, and large area device due to electrical device requirements [1],[2]. For example, a-Si-TFT with low mobility (< 1 cm^2/Vs) cannot be applied to high speed switching device in spite of its excellent electrical uniformity and poly-Si TFT with high mobility (10 ~ 400 cm^2/Vs) still shows unstable electrical characteristics, namely: first, an non-uniformly formed grain size and protrusions of poly-Si after crystallization induced by laser annealing and second, the high off-current level of TFT through metal residue in the active layer formed by metal catalysis crystallization method such as metal induced crystallization(MIC) and metal induced lateral crystallization (MILC) [3],[4],[5]. These crystallization methods are not adequate to use high performance device such as OLEDs display which requires high electrical uniformity and performance for field effect mobility and electrical stability with time lapse on the whole TFT array panel [6],[7]. In order to improve these issues, Hosono's group proposed amorphous indium gallium zinc oxide (a-IGZO) as an oxide semiconductor material for

active layer by which a-IGZO TFT may offer an attractive alternative for replacing silicon based TFTs. Table 1 compares silicon based TFT properties with oxide based TFT properties. Oxide TFTs provides better electrical uniformity such as threshold voltage (V_{TH}), field effect mobility (μ_{FE}), subthreshold gate swing (S), and leakage current level in the off-state because of its amorphous property and in addition, in spite of its amorphous phase, a-IGZO TFT shows a high mobility of > 10 cm^2/Vs which can be used for driving TFT with high speed switching and high current level. Moreover, this attractive a-IGZO material is transparent and can be deposited at room temperature so that it is an attractive semiconductor material for flexible displays [2], [8]. In spite of these merits, oxide TFTs still have inherent problem to be improved for their commercial application: 1) electrical instability due to environmental changes; 2) correlation of gate dielectric with transfer characteristic; 3) understanding the effects of passivation layers on device characteristics; 4) sensitive properties with different sputtering conditions [9],[10]. In this study, we study of a-IGZO TFTs, which will include device designs, material characterization, process developments, and device characterization. Our motivation is to realize a robust TFT using a-IGZO semiconductor for flat panel display as well as to drive other applicable devices. For example, in this study, an active matrix type TFT will be applied to an addressable microfluidic electrowetting channel device.

Table 1-1 Comparison of silicon based semiconductor TFT and oxide based semiconductor TFT, Nikkei Electronics Asia, Oct 24, 2007 (LG electronics courtesy).

	a-Si TFT	Poly-Si TFT	Oxide TFT
Phase	amorphous	polycrystalline	amorphous
Channel Mobility	1 cm^2/Vs	~ 200 cm^2/Vs	10~40 cm^2/Vs
Switching characteristics (S)	0.4 ~ 0.5 V/decade	0.2~0.3 V/decade	0.09 ~ 0.6 V/decade
S/D Leakage current	~10^{-13} A	~ 10^{-12} A	~10^{-13} A
Characteristic uniformity	Good	Not good	Good
Long-term TFT reliability	Low	High	Unknown
Maximum process Temperature	~ 250°C	~ 400-500°C	RT to 350°C
Manufacturing cost (Number of mask)	Low (4~6)	High(7~11)	Very low (4~6)
Application display	LCD	LCD, OLED	LCD, OLED

1.2 Thin film transistor

1.2.1 Historical background

The first thin film transistor was demonstrated by P.K Weimer (1962) who used a top-gate staggered structure with a microcrystalline cadmium sulfide (CdS) active layer [11]. Since Weimer's work, TFTs based on a wide variety of semiconductor materials including organic and inorganic, and amorphous and polycrystalline have been developed. Currently, the most dominant TFT technology is based on a-Si:H and poly-Si as active layer, which is commonly used as switching and driving devices in active-matrix type displays such as active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light emission displays (OLEDs)[12],[13],[14],[15], [16]. In addition to silicon TFTs, another type of TFTs consists of those which employ organic materials as the channel layer in spite of low mobility of 10^{-3} ~ 1 cm^2/V.s because the low mobility of these organic TFTs can be offset by low cost and easy processing such as spin coating or printing methods [17]. In addition, this technology allows plastic substrates to be used for flexible devices because the process temperature for fabrication of device, most of all, can be decreased below 250°C. Currently promising oxide based TFTs are emerging since they are transparent and demonstrate high performance for advanced TFT applications, [2], [18].

1.2.2 Basic TFT operation

Fig. 1 shows the basic structure of a TFT and several energy band diagrams as viewed through the gate of an n-semiconductor, accumulation-mode TFT. The energy band diagram of Fig.1- 1(b) shows the device at equilibrium, with 0V applied to the

source, drain, and gate. Fig.1-1(c) shows an energy band diagram with the gate negatively biased. The applied negative bias repels mobile electrons from the semiconductor, leaving a depletion region near the insulator-semiconductor interface. When compared to Fig. 1-1 (b), this biasing condition has a reduced conductance due to the reduced number of mobile electrons in the semiconductor. Fig.1-1(d) shows an energy band diagram with the gate positively biased. The applied positive bias attracts mobile electrons, forming an accumulation region near the insulator-semiconductor interface. These excess mobile electrons lead to an increase in the channel conductance. Beginning with the case where the gate is biased positively and accumulation is established, i.e., Fig.1-1(d), consider the effect of an applied drain-source voltage, V_{DS}. Initially the semiconductor is modeled as a resistor, i.e. linearly increasing current with V_{DS}. As V_{DS} increases, accumulation near the drain decreases. As V_{DS} is increased further, the region near the drain eventually begins to deplete. The voltage at which the semiconductor region near the drain is fully depleted of carriers is denoted the pinch off voltage. Therefore, application of V_{DS} greater than the pinch-off voltage results in a saturated drain current characteristic.

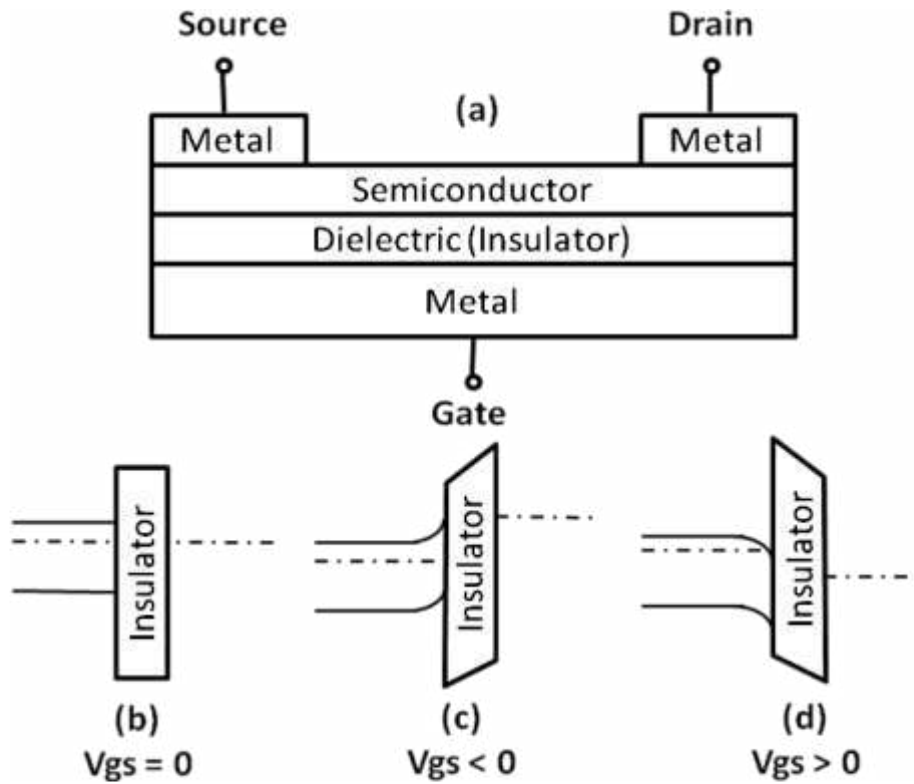
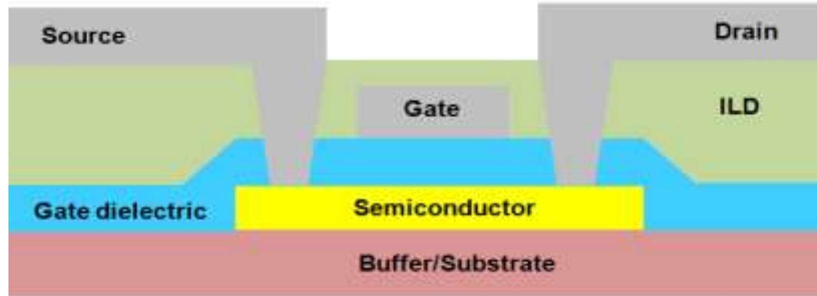


Fig.1-1. (a) basic structure of a TFT and corresponding energy band diagram as viewed through the gate with bias conditions: (b) equilibrium, (c) $V_{gs} < 0$ V, and (d) $V_{gs} > 0$V.

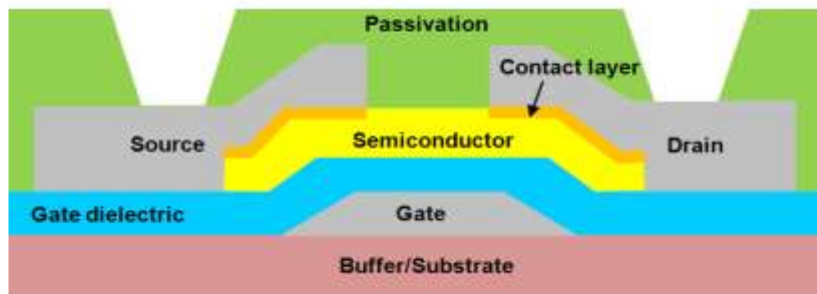
1.2.3 TFT structure

There are two types of TFT structures for silicon based TFTs. Fig. 1-2 shows representative TFT structures. First, the coplanar type is that source/drain and gate are on the same plane as shown Fig.1-2 (a). This type structure is usually used for polycrystalline TFT because of the higher quality of crystalline film and the convenience of crystallization. Second, the staggered type TFT as shown Fig.1-2 (b) is divided into two type of structures depending on the location of gate; 1) the structure with gate under active layer is inverted staggered (bottom gate) type and 2) the structure with gate on active layer is normal staggered (top gate) type. Normal staggered type TFT was proposed earlier than inverted staggered type as shown Fig.1-2 (c). However, the complicated process step to pattern Ohmic contact layer and the exposure of silicon surface before the deposition of gate dielectric degrades the TFT properties. While inverted staggered type TFT is commonly used for a-Si TFT because the interface between gate dielectric and semiconductor (a-Si) including Ohmic contact layer (n^+ a-Si) can be formed without exposing in air therefore the electrical properties can be improved. In addition, the TFT process is simple because n^+ a-Si and a-Si can be etched by using a single source/drain mask. The inverted staggered type is divided into back channel etch (BCE) type (Fig.1-3 (a)) and etch stopper (E/S) type (Fig.1-3 (b)). In spite of simple structure of BCE type of TFT, the over etching or chemical damage on semiconductors deteriorates the characteristic uniformity of a TFT array panel. On the other hand, the E/S type of TFT has higher stability for TFT properties because the E/S layer

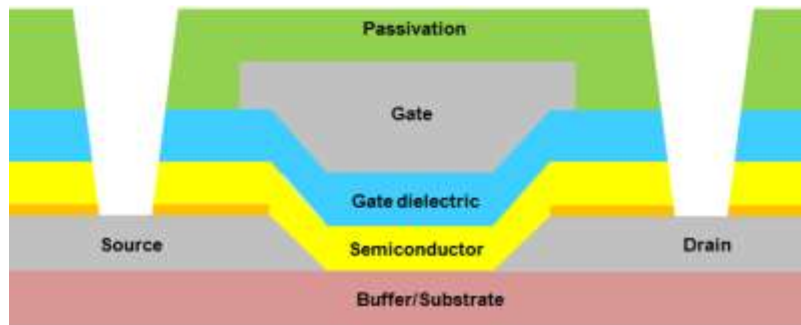
protects semiconductor layer against chemical damage or non-uniform over etching problem in spite of relatively complicated process; n+ a-Si is separately deposited on E/S layer with a-Si layer after E/S layer pattern.



(a) Coplanar type TFT structure

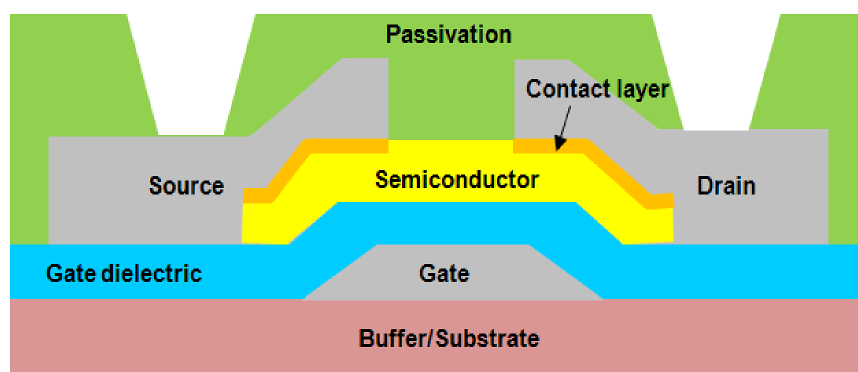


(b) Inverted staggered type TFT structure



(c) Normal staggered type TFT structure

Fig.1-2. Cross section of the various TFT structures: (a) coplanar type TFT structure, (b) Inverted staggered type TFT structure, (c) Normal staggered type TFT structure.



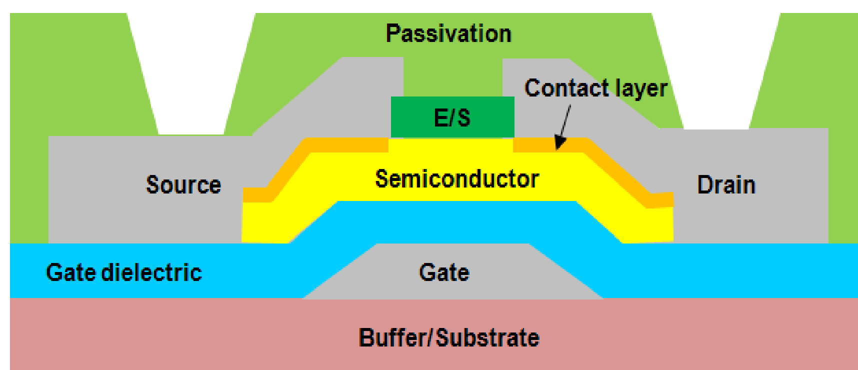


Fig. 1-3.Two type of TFT structures in inverted staggered type TFT structure, (a) BCE type TFT structure and (b) E/S type TFT structure.

1.2.4 Electrical characterization of TFT

There are two operational regimes in a typical MOSFET (metal oxide-semiconductor field- effect transistor): the linear region and the saturation region. In the linear region, the drain current increases linearly with drain voltage ($V_D << V_G$), as in Ohmic conduction. On the other hand, the drain current is constant with increasing drain voltage in the saturated region.

Linear region

Fig. 1-4 shows cross-sectional view of the channel region of a TFT used to derive the gradual channel approximation. The carrier density per unit area in the channel depends on the potential V(y) caused by the drain potential V_D. When the gate potential is higher than the threshold, V_T, the mobile charge Q_I in the channel is related to the gate potential V_G via

$$Q_I = -C_{SiNx}(V_G - V_T) \tag{1.1}$$

where C_{SiNx} is the capacitance per unit area of the SiN_x gate dielectric. The channel potential V in Eq. (1) is assumed to be zero; however, the induced charge Q_I is a function of y, so Eq. (1) is replaced by the following equation:

$$Q_I = -C_{SiNx}(V_G - V_T - V) \tag{1.2}$$

On the other hand, the current induced by majority carriers can be written as

$$I_D = W\mu_n Q_I E_y \tag{1.3}$$

Where W is channel width, μ_n is the electron mobility, and E_y is the electric field at y.

The equation is a simplified form of the current density formula where the diffusion term has been assumed to be negligible:

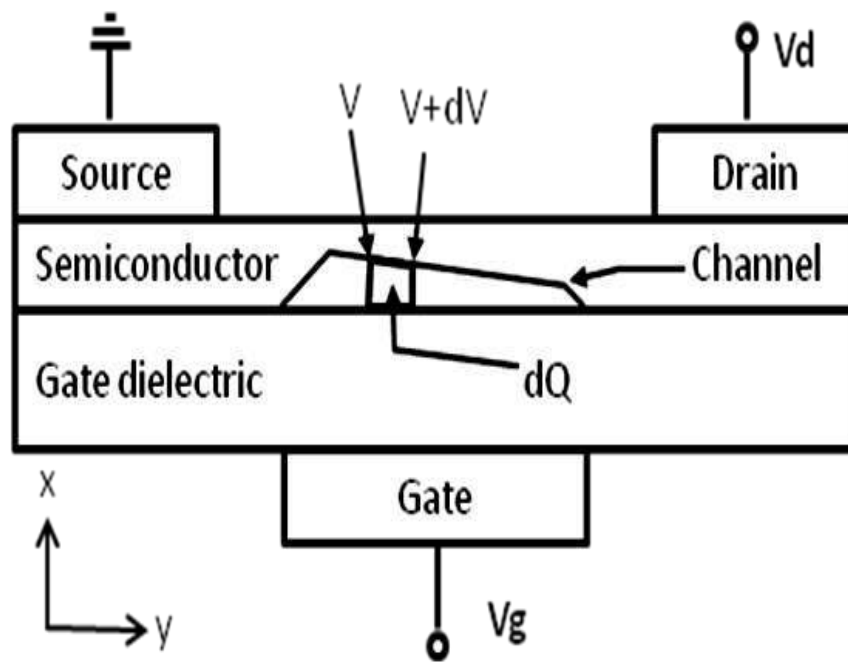


Fig. 1-4. Cross-sectional view of the channel region of a TFT used to derive the gradual channel approximation.

$$J_n = \frac{I_n}{A} = q\left(\mu_n nE + D_n \frac{dn}{dx}\right) \tag{1.4}$$

By substituting E_y = dV/dy and Eq. (2) into Eq. (3) we obtain

$$I_D dy = W\mu_n C_{SiNx}(V_G - V_T - V)dV \tag{1.5}$$

By integration from y = 0 to L, that is, from V = 0 to V_D the gradual channel expression for the drain current is:

$$I_D = \mu_n C_{SiNx} \frac{W}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2 dV\right] \tag{1.6}$$

In the linear region ($V_D << V_T$) the drain current can be written as

$$I_d = \mu_n C_{SiNx} \frac{W}{L}(V_D - V_T)V_D \tag{1.7}$$

Therefore, field-effect mobility in the linear region is obtained from Eq. (7).

<u>Saturation region</u>

The gate field-induced carrier density at the drain disappears as the drain potential increase. When $V_D = V_G - V_T$, the electron channel becomes completely pinched off, the drain current saturated. For $V_D > V_G - V_T$, Eq. (6) is no longer effective. Therefore, the saturation drain current can be obtained by substitution of $V_D = V_G - V_T$ into Eq. (6),

$$I_D = \frac{C_{SiNx}\mu_n W}{2L}(V_G - V_T)^2 \tag{1.8}$$

The field-effect mobility in the saturation region can be obtained by taking the square root of Eq. (8) and differentiating with respect to V_G, and given by,

$$\mu_n = \left(\left(\frac{d\sqrt{I_D}}{d\sqrt{V_G}} \right) \frac{1}{\sqrt{C_{OX} \frac{W}{2L}}} \right)^2 \qquad (1.9)$$

In this study, we will extract the field effect mobility from the saturation region because this region is relatively insensitive to the magnitude of the source-drain resistance (contact resistance); independent of V_D, unlike the linear region.

Fig.1-5 shows the general transfer characteristic of a-IGZO TFT and graphical definition of the on/off current ration in the curve. The on/off current ratio is important for performing active switching in each pixel in the device where the on – current determines the rate of pixel or capacitor charging and off- current is associated with the leakage of the pixel or capacitor voltage. In this study, we will take the lowest drain current value for off-current in the transfer characteristics and on-current will be measured at 20 V (V_{GS}) shifted negatively from V_T.

V_T will be extracted by extrapolating in the saturation region on the $I_{DS}^{1/2} - V_{GS}$ characteristic plot as shown in Fig.1-6. The subthreshold gate swing, S, defined as the voltage required to increase the drain current by a factor of 10 and determined from the equation: $S = \frac{dV_{GS}}{d(\log I_{DS})}$, note that S is given by the maximum slop in the transfer curve as shown Fig. 1-6.

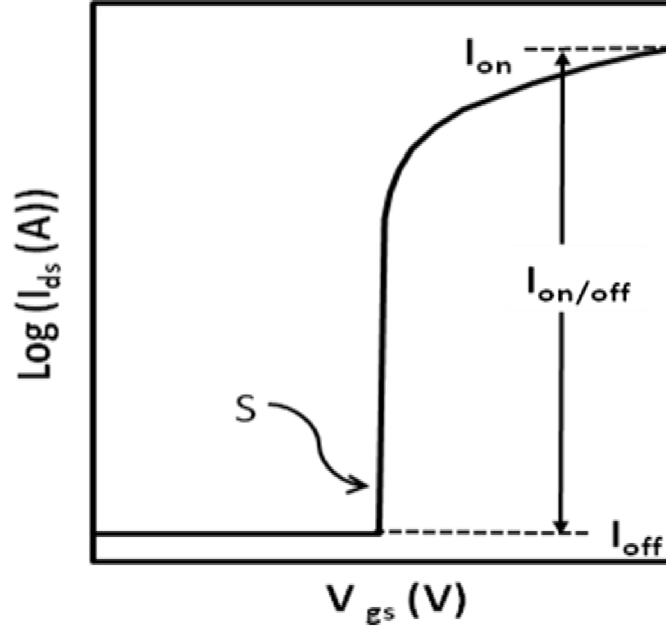


Fig.1-5. General transfer characteristic of a-IGZO for graphical definition of $I_{on/off}$ and (b) subthreshold gate swing (*S*).

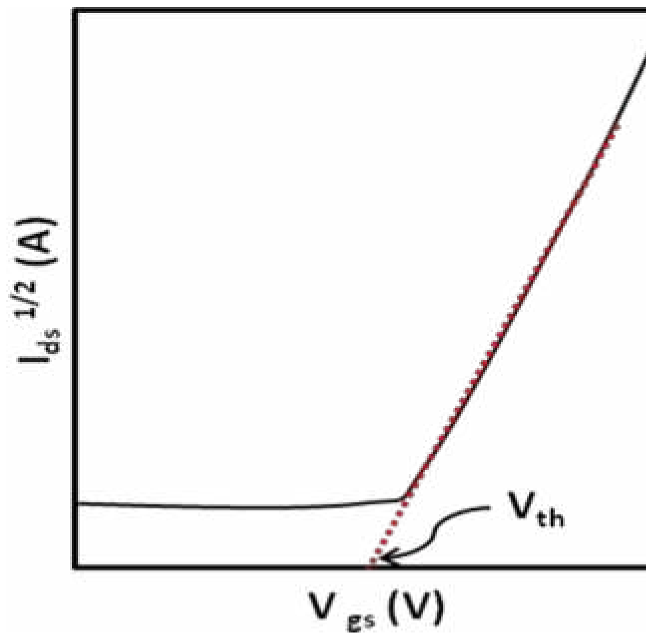


Fig. 1-6. Graphical extrapolation of V_T in the saturation region.

1.2.5 Oxide semiconductor based TFT

1.2.5.1 Overview of transparent oxide semiconductors

Transparent conductive oxides (TCOs) are being studied for flat panel display application as active layer because of transparency and electrical properties[2],[19],[20],[21], where transparency and high conductivity are somewhat contradictory because optical transparency requires band gaps larger than 3.3 eV and such a large band gap makes carrier conduction very difficult [22]. In this sense, TCOs materials are exceptional materials. Historically TCO materials such as In_2O_3:Sn (ITO), SnO_2, and ZnO have been only commercially applied to TFTs as transparent electrodes and interconnections because of the absence of p-type TCOs [23]. In 1997, the discovery of a p-type TCO, $CuAlO_2$ by Hosono's group significantly gave a rise to new functional device which was difficult to realize by Si-based device; specifically a fully transparent flat panel displays. Recently, Samsung SDI demonstrated the 12 inch-transparent OLED display using the TCO amorphous indium gallium zinc oxide. This realization using these materials is due to significant different electronic structure and transport in oxide semiconductor which shows higher Hall mobility (> 10cm^2/Vs) as compared to amorphous silicon material in spite of room temperature process for semiconductor deposition. In this chapter, the electrical structure and carrier conduction of TCOs will be reviewed, including the properties of a-IGZO material [24].

1.2.5.2 Electronic structure and carrier transport

There are significantly different conduction mechanisms between silicon based semiconductor and oxide based semiconductors. Usually, amorphous silicon has poor

carrier transport properties (~1 $cm^2/V.s$) relative to crystalline silicon materials (~ 500 cm^2/Vs). This is fundamentally because the chemical bond in the covalent silicon semiconductors which are made of sp^3 or p-type orbitals with strong spatial directivity as shown in Fig.1-7 (a) and (c). Therefore, for amorphous silicon, the strained and disordered chemical bonds form rather deep and high-density of localized states below conduction band minimum (CBM) and above valence band maximum (VBM), causing carrier trapping. On the other hand, for n-type TCOs, amorphous oxide semiconductors (AOSs) containing post-transition-metal cations make high mobility possible in spite of their amorphous structure because CBMs are made of spherical extended *s* orbitals of metal ions containing high ionicity and overlapping with neighboring metal *s* orbitals which are not influenced largely by disordered local structure. Therefore, the electronic levels near the CBM are insensitive to locally strained bonds, and the electron transport is not affected significantly as shown in Fig.1-7(d) [8]. In a sense of formation of energy gap, Kamiya *et al.* more clearly described the electronic structures of oxides [25]. Fig.1-8 shows the formation of energy gap with a different type of bond. As already described, for Si, CBMs and VBMs are made of anti-bonding (sp^3 $\sigma*$ and bonding states (sp^3 σ) of Si sp^3 hybridized orbitals forming its bandgap by energy splitting of the $\sigma* - \sigma$ levels (Fig. 1-8 (a)). On the other hand, for oxides materials, CBMs and VBMs are formed by different ionic species. In order to study electronic structure, most of all, it is important to understand the Madelung potential in ionic crystals. When metal atoms and oxygen come close, charge transfer occurs due to largely different electron affinity and ionization potential, ionizing these atoms (Fig. 1-8 (b)). As a result, Madelung potential from the difference between anions and cations by virtue of their opposing charges

consequently stabilizes the ionized states in the crystal structure (Fig. 1.8 (c)); the Madelung potential induce energy splitting. Therefore CBMs and VBMs are mainly made of metal cations and oxygen *2p* orbitals, respectively. CBMs are mainly made of *s* orbitals with a large principle quantum number *n* in which *s* orbitals have large spatial size and form large hybridization with second neighbor metal cations. Because of this, TCOs have small electron effective masses. In fact the above electronic structure, there are mainly two representatively electrical merits for oxide based TFTs. First, the small effective mass make high density carrier doping possible in order to improve electron mobility [26], [27]]. Fig. 1-9 shows the relationship between Hall mobility and electron concentration for single-crystalline $InGaO_3 (ZnO)_5$ (sc-IGZO) and a-IGZO film. Hall mobility increases with increasing carrier concentration. In fact, carrier transport is controlled by thermal activation at low temperature, however, according to Takagi *et al.*, when carrier concentration exceeds a threshold value N_{th}= 4 x10^{18} cm^{-3}, the degenerated conduction occurs for both a-IGZO and sc-IGZO. These behaviors are significantly different from conventional semiconductor such as silicon because the carrier mobility typically decreases with increasing carrier concentration due to ionized impurity scattering in highly doped semiconductors, where this peculiar behavior will be explained in the following chapter with percolation conduction model in a-IGZO film. Second, subthreshold voltage swing (S) value is improved due to relatively lower subgap traps. Fundamentally, as already mentioned, the origin of the bandgap of oxide is from the Madelung potential, and therefore, the nonbonding levels of metal cations are located in the vicinity of the conduction band [28]. Even if defective levels are formed in the bandgap, they are generally occupied by two electrons in n-type oxides

and electrically inactive for an electron-only device; the defects in oxides such as oxygen vacancies do not cause strongly active traps because of its strong ionicity and the electronic structure. Indeed, it has been reported that a-IGZO has far fewer subgap traps than a-Si: H even when it is deposited at room temperature. Fig.1-10 shows the comparison of trap density in a-IGZO and a-Si:H. The density of states of a-IGZO near conduction band are much lower than a-Si:H. The low defect densities in the a-IGZO film make possible the low voltage operation for the TFTs because the operating voltage is largely determined by the subthreshold voltage swing (*S*), which is related to the subgap density of states D_{sg} ($cm^{-2}eV^{-1}$) by

$$S = \frac{dV_g}{d\log I_g} = \ln 10 \frac{k_B T}{e}\left(1 + \frac{eD_{sg}}{C_g}\right) = S_0\left(1 + \frac{eD_{sg}}{C_g}\right) \tag{1.10}$$

where k_B is the Boltzmann constant, T is the temperature, C_g is the gate capacitance per unit area, S_0 is temperature dependent constant.

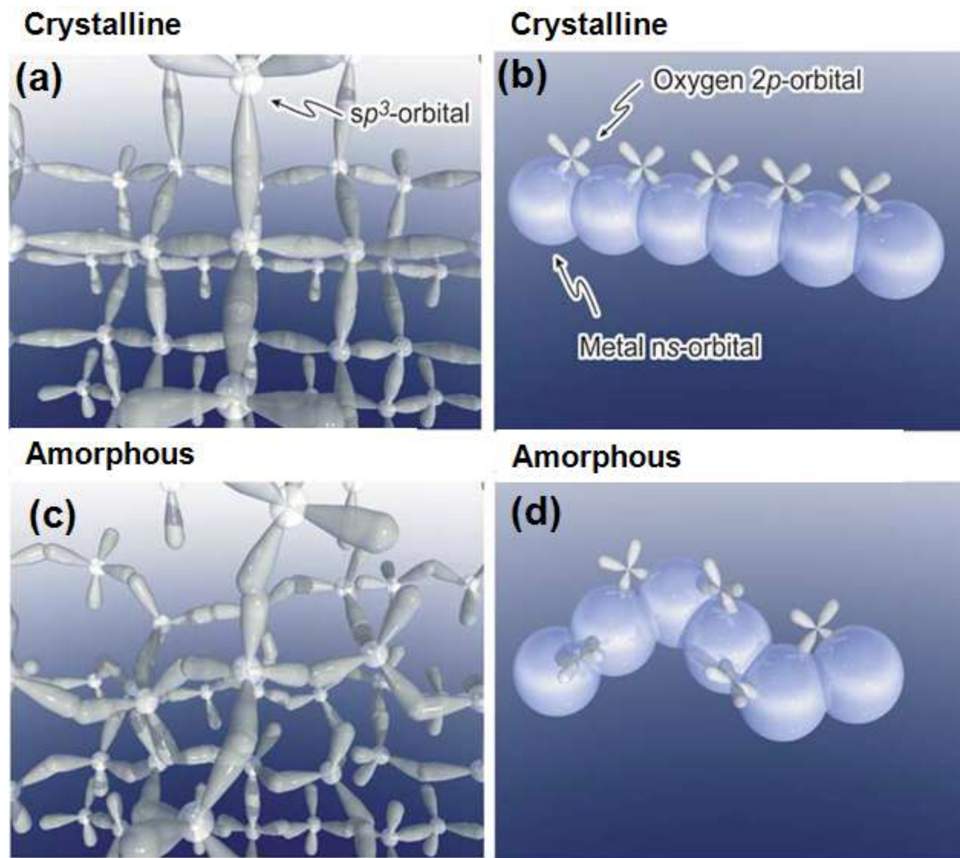


Fig. 1-7. Schematic orbital drawings for the carrier transport paths at the conduction band bottoms in amorphous and crystalline semiconductors; (a) crystalline and (c) amorphous silicon with covalent bonds with strongly directive sp^3 orbitals and (b) crystalline and (d) amorphous oxide semiconductors with post-transition-metal cations.

K. Nomura, T. Kamiya, H. Ohta et al., Applied Physics Letters, vol. 85, no. 11, pp. 1993-1995, Sep 13, (2004)

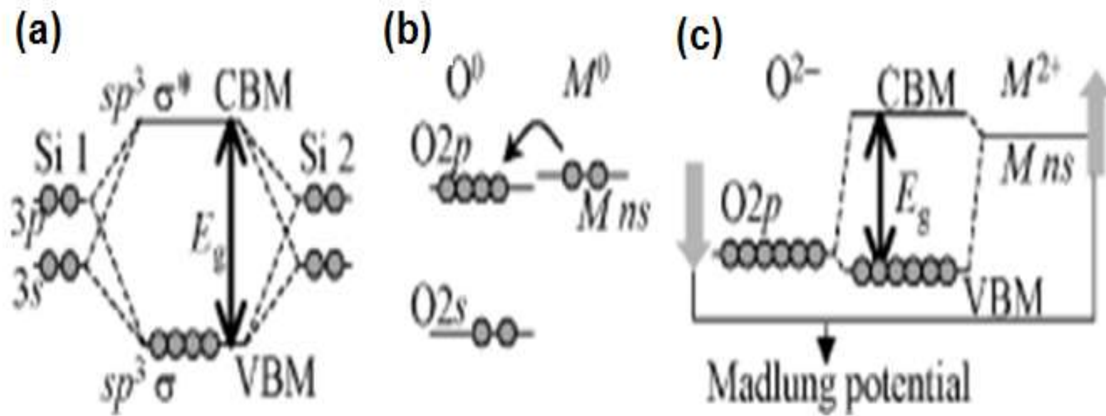


Fig. 1-8. Formation of energy gap, (a) covalent semiconductor (silicon), and (b, c) ionic semiconductor ($M^{2+}O^{2-}$). (b) Energy levels of neutral atoms in vacuum. (c) The atoms are ionized I a crystal structure and form large Madelung potential and large bandgap.

T. Kamiya, H. Hosono, T. Kamiya et al., International Journal of Applied Ceramic Technology, vol. 2, no. 4, pp. 285-294, (2005)

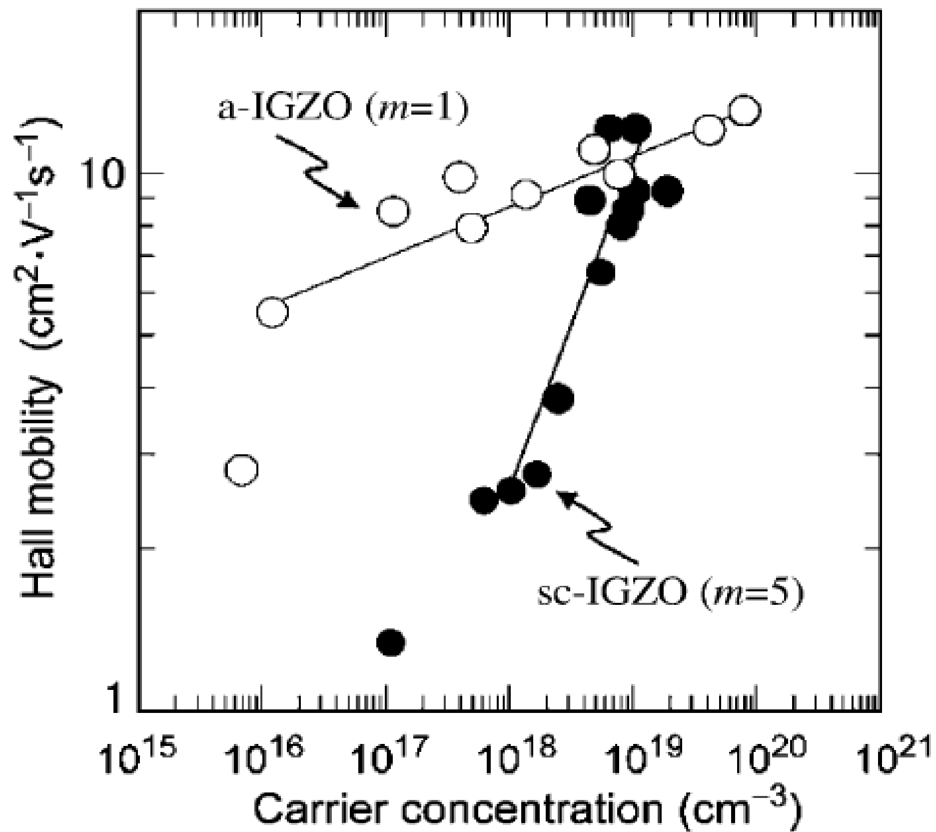


Fig. 1-9. Relationship between Hall mobility and electron concentration for single-crystalline $InGaO_3(ZnO)_5$ (sc-IGZO) and a-IGZO film.

T. Kamiya, H. Hosono, T. Kamiya et al., International Journal of Applied Ceramic Technology, vol. 2, no. 4, pp. 285-294, (2005)

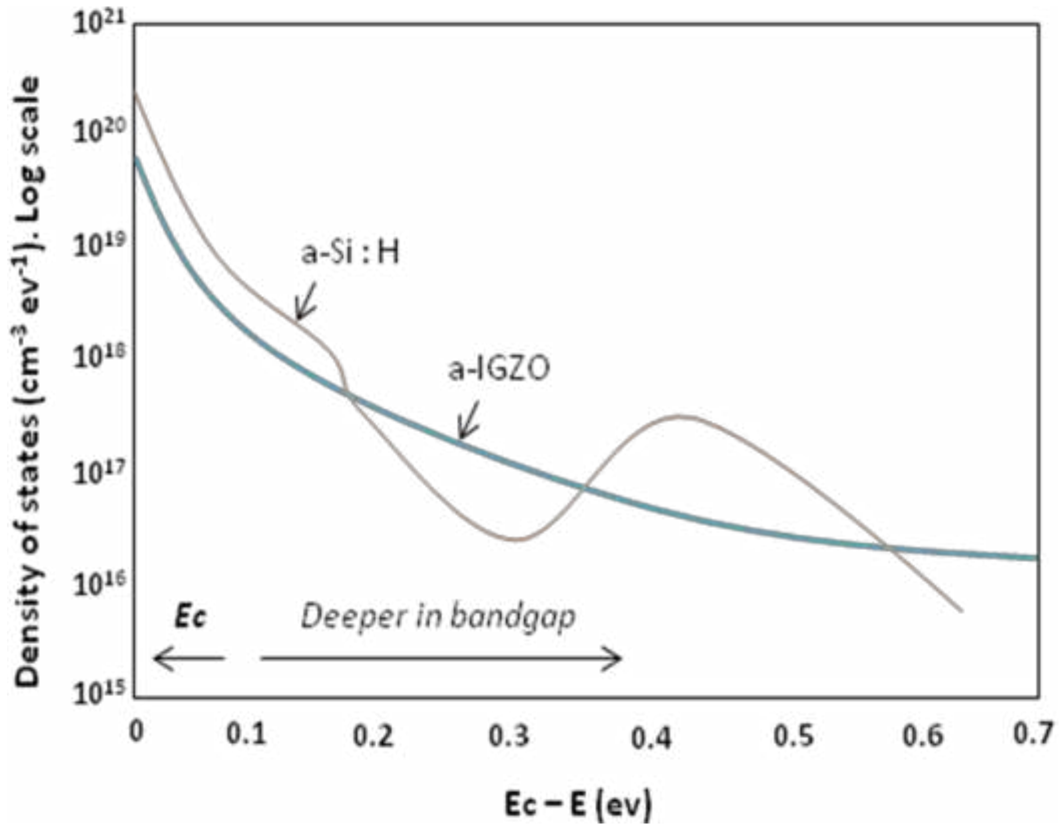


Fig.1-10. Subgap trap density of states in a-IGZO in comparison with a-Si:H.

1.2.5.3 Amorphous indium gallium zinc oxide TFT (a-IGZO TFT)

The first TFT using a-IGZO can be credited to Hosono's group [29]. They proposed transparent flexible TFTs using a-IGZO semiconductors at room temperature, and characterized the material properties and electrical characteristics of the TFTs. The key element to perform high electrical performance was incorporating Ga ions into the semiconductor. The Ga ions can suppress carrier generation via oxygen vacancy formation because the Ga ions forms stronger chemical bonds with oxygen than Zn and In ions; the carrier concentration can be controlled by Ga contents in film and achieve a low off current and large on/off current ratio.

1.2.5.3.1 Structural and optical properties

Takagi *et al.* demonstrated the structure and optical properties of a-IGZ [30]. Fig. 1-11 shows the X-ray diffraction pattern of a-IGZO film deposited on a substrate. Because no sharp peaks are observed in the plot, the film is amorphous. Fig. 1-12 shows optical transmission spectra of a-IGZO films with different carrier concentrations of ~ 10^{13} cm^{-3} and ~ 10^{20} cm^{-3}. Transmissions of both the films are greater than 80% in the visible region. Large optical absorption appears in the wavelength region > 1600nm in the high carrier concentration film, which can be attributed to free carrier absorption. Tauc's plots give optical band gaps of ~ 3.1 *e*V and ~3.3 *e*V for the films with carrier concentrations of ~ 10^{13} cm^{-3} and ~ 10^{20} cm^{-3}, respectively. They explained these results due to a Burstein-Moss (BM) effect, in which the raise of the Fermi level in the

conduction band in a degenerate state increases the optical absorption edge energy using the relationship, $\Delta E_g^{BM} = \frac{h^2}{2m_e}(3\pi r^2 n_e)^{2/3}$.

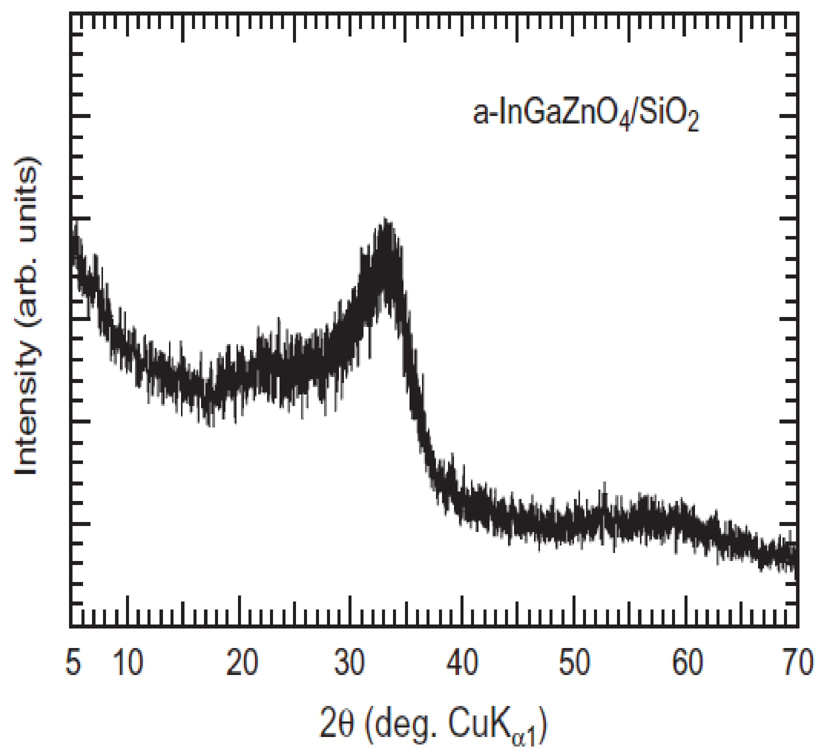


Fig. 1-11. X-ray diffraction pattern of the a-IGZO film deposited on SiO2 a glass substrate at room temperature.

A. Takagi et al., vol. 486, no. 1-2, pp. 38-41, Aug 22, (2005).

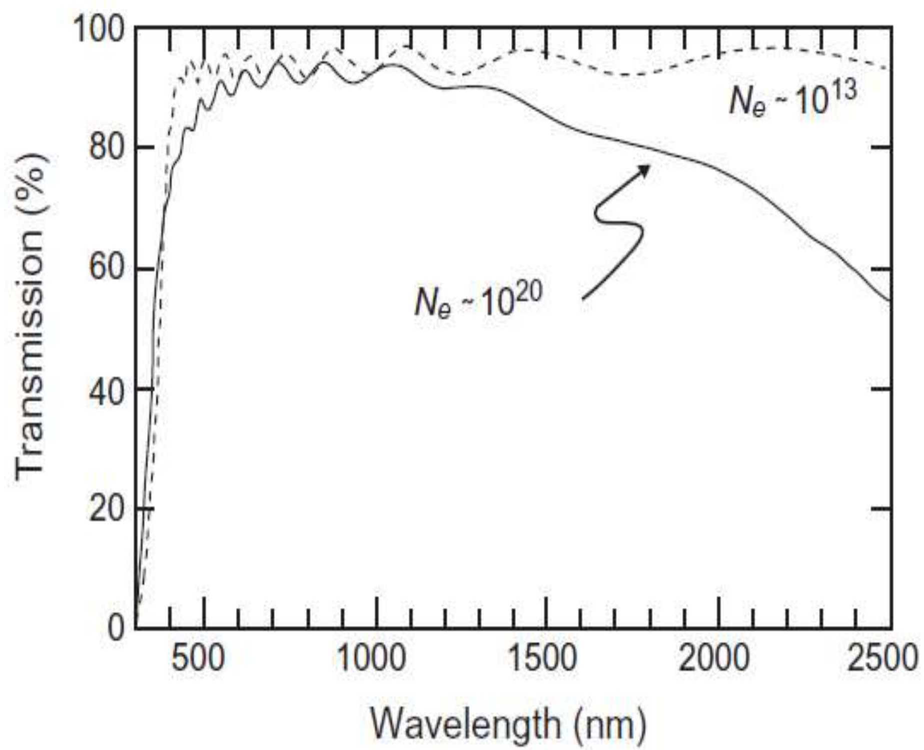


Fig. 1-12. Optical transmission spectra of a-IGZO film with different carrier concentration ~ 10^{13}cm $^{-3}$ and ~ 10^{20} cm $^{-3}$.

A.Takagi et al., vol. 486, no. 1-2, pp. 38-41, Aug 22, (2005)

1.2.5.3.2 Carrier conduction in a-IGZO: Percolation conduction model

The quantum mechanical hopping (Fig. 1-13 (a)), which usually describes conduction mechanism of silicon semiconductor in CBM, is excluded from a conduction mechanism for a-IGZO semiconductor because of the relatively long average distance between mono-energetic states as compared in Fig. 1-13 (b). To explain conduction in a-IGZO, Nomura *et al.* proposed that electron carriers in the edge of conduction band move around 3- dimensional energy barriers without tunneling, thus calling it a percolation conduction mechanism in a-IGZO films. When the Fermi level is very low relative to the edge of conduction band, there are not enough electrons induced above the conduction edge as shown Fig. 1-14 (a). When the Fermi level is below that of the highest energy barriers, which are associated with the random distribution of Ga^{3+} and Zn^{2+} ions in a single crystal structure $InGaO_3(ZnO)_5$, electron conduction is exclusively dominated by the percolation mechanism where electrons travel between the valley of potential energy barriers as shown in Fig. 1-14 (b), and the conductivity temperature dependence goes as $T^{-1/4}$. However, once the Fermi level is located above the energy peaks of potential conduction band, the carrier density is high enough to fill all of the valleys in the tail regions and electron transport is dominated by a temperature-independent, degenerate mechanism as shown Fig. 1-14 (c).

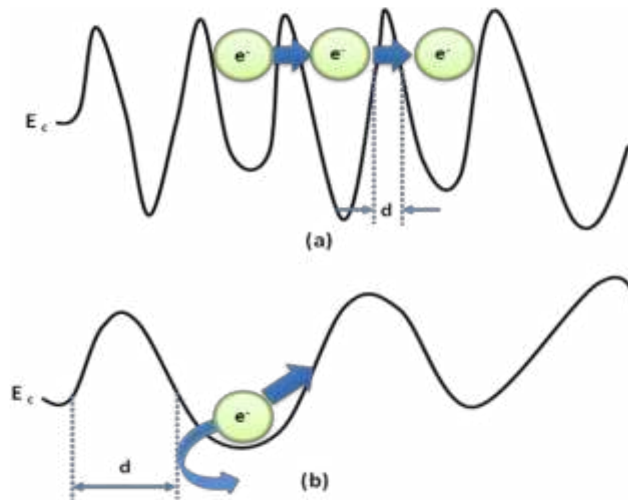


Fig. 1-13. Energyband diagram: (a) hopping conduction by quantum mechanical tunneling and (b) conduction by percolation mechanism.

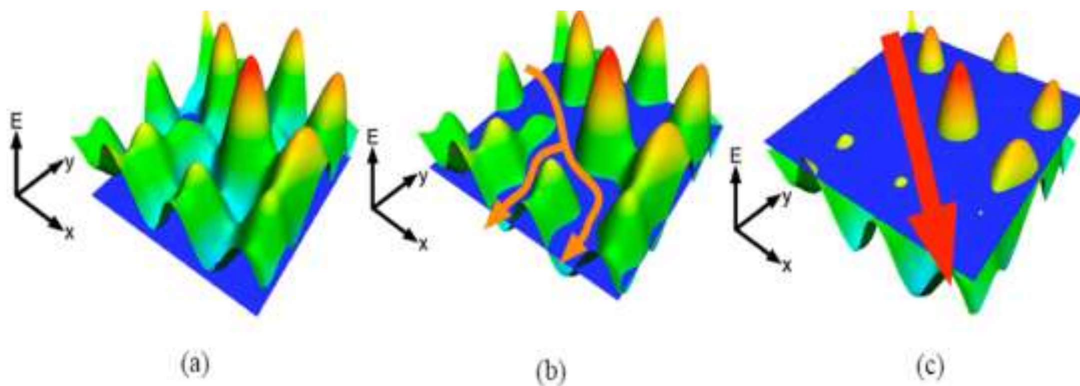


Fig. 1-14. The conduction model suggested by Nomura, et al. (a) The Fermi level (blue plane) is very low than conduction band edge, (b) located above the edge of conduction (percolation conduction), and high enough on the edge of conduction(degenerate conduction).

The figures are from Hoshino, MS dissertation, Oregon State University, 2008.

Chapter 2

Device fabrication and characterization

2.1 Fabrication of a-IGZO TFT

In this study, an inverted staggered bottom gate structure is preferred for a-IGZO TFT structure since the interface between the semiconductor and gate dielectric can be formed without exposure to air, which typically has better electrical properties. Fig.2-1 shows a schematic process flow of the fabricated device structure of a-IGZO TFTs for the BCE type TFT structure.

2.1.1 Gate electrode

The selection of a metal electrode material for gate electrode as well as source and drain electrodes has been considered to be one of the important parameters to design a device for interconnection such as a microchip and a flat panel display for large area application because the resistance in the metal line results in a voltage drop through the metal line inducing signal delay and possible switching problems to drive the device Therefore, the resistance of metal line must be sufficiently low from followed equation:

$$R = \rho \frac{L}{A} = \rho \frac{L}{Wd} = \frac{\rho}{d}\frac{L}{W} = R_S \frac{L}{W} \tag{2.1}$$

Where ρ is resistivity of metal electrode, L and W are the length and the width of metal line, the d is the thickness of metal line, and R_s is the sheet resistance. In this study, chromium (Cr) was used for gate electrode because it has a reasonably low resistivity (ρ_{Cr} = ~ 1 x 10^{-5} ohm-cm) comparable to Al and Cu (ρ_{Al} = 4~5 x 10^{-6} and ρ_{Cu} = 3~4 x 10^{-6}

ohm-cm) and in addition, has a high etching selectivity during fluorine based plasma etching. The chromium bottom gate layer was rf magnetron sputter deposited (typically ~150 nm) with DC substrate bias of 5W (120V) and lithographically patterned and wet etched by Cr etchant (CR-14) (9%$(NH_4)_2Ce(NO_3)_6$ + 6%$(HClO_4)$ + H_2O) onto a 300nm SiO_2 coated silicon wafer (100mm diameter) at a room temperature without agitation. Because of wet etching process is isotropic the sidewall angles are typically shallow (~ 45°) which facilitates good step coverage for next deposition process as shown in Fig. 2-1 (a) and in the SEM image (e).

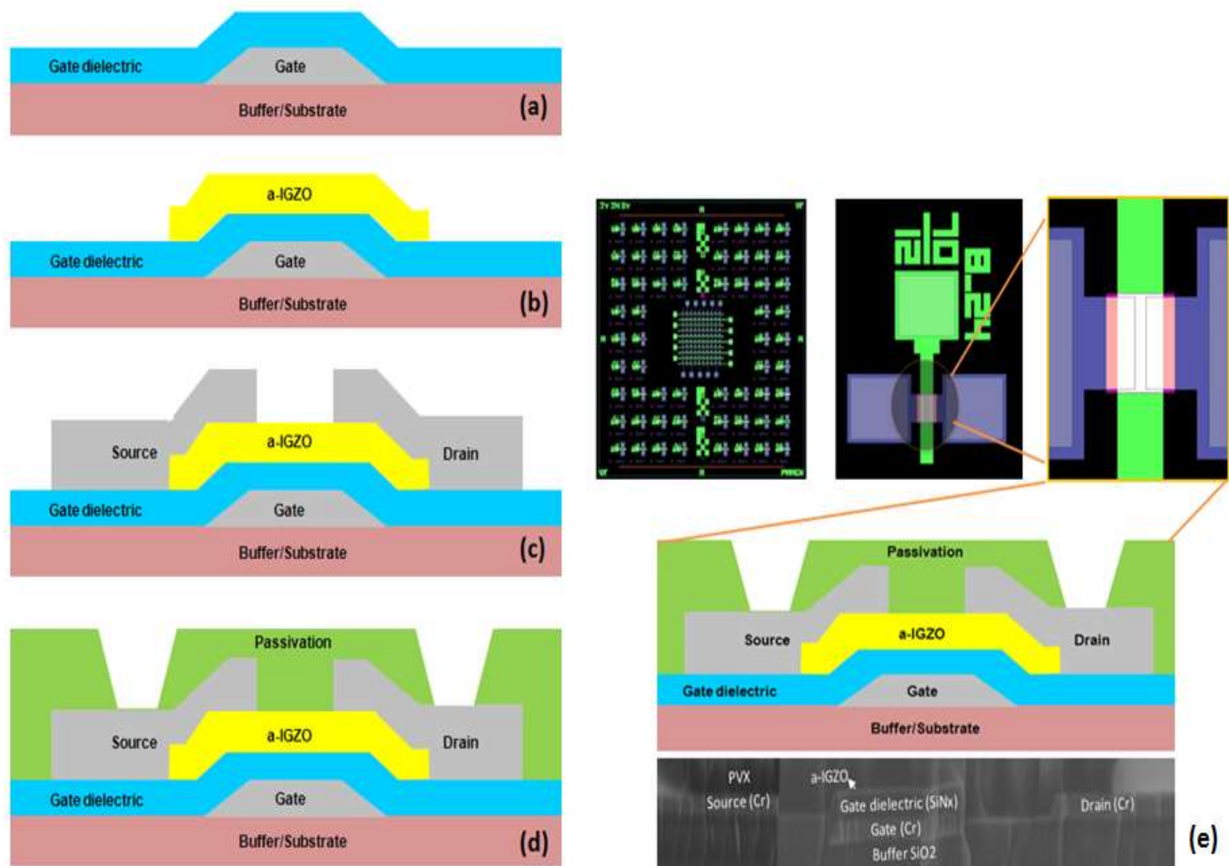


Fig. 2-1. a-IGZO TFT fabrication with BCE type of a-IGZO TFT structure; (a) gate dielectric/ patterned gate electrode (Cr) on buffer SiO_2 /Si substrate, (b) sputtered a-IGZO island formation, (c) source-drain electrode formation by wet etching, (d) passivation deposition and via hole patterning by dry etching, and (e) cross-section SEM image of TFT.

2.1.2 Gate dielectric material

The gate dielectric material in metal oxide semiconductor (MOS) structures requires a high electrical resistance to minimize gate leakage current at the overlapped region of source/drain as well as high compatibility to semiconductor layer such as interface properties and inter-reaction [31]. For a silicon oxide-silicon nitride gate dielectric, the properties depend on the relative atomic concentrations of silicon, nitrogen, and hydrogen [32], [33]. In this study, SiN_x (200 nm) gate dielectric material was deposited by plasma enhanced chemical vapor deposition (PECVD). The standard deposition condition of PECVD SiNx film were 40W RF power, 1200 mTorr pressure, 5%SiH_4-Ar/NH_3/N_2 (150/2/790 sccm) gas flow, and 350°C temperature. The deposition rate was 14.28nm/min. This SiN_x film was optimized for a Si-rich SiN_x with lower film stress as described previously by Park [34]. In chapter 3, the electrical performance and instability with different gate dielectrics which include SiO_2 and SiN_x and with plasma gas chemistry in SiN_x will be presented in order to understand the relationship between gate dielectric property and electrical TFT properties in detail. Fig. 2-1 (a) shows the schematic structure after completion of gate dielectric on gate electrode.

2.1.3 Semiconductor; a-IGZO

As mentioned in chapter 1, compared to Si based TFTs, a-IGZO TFTs have a very unique electrical transport mechanism and sensitive to deposition conditions. To characterize the properties of a-IGZO TFTs, a-IGZO active layers (50 nm) were rf magnetron sputter deposited using an 50mm diameter a-IGZO target (In_2O_3 : Ga_2O_3 : ZnO = 1:1:1 mol %) with different sputtering parameters .The standard sputtering

parameters for the a-IGZO films were: system base pressure was $5\sim9 \times 10^{-7}$ Torr; rf sputtering power was 60 W with 170 V target bias; sputtering pressure was 5 mTorr Ar-O_2 gas mixture (75% Ar-25% O_2). The a-IGZO was wet etched by BOE (0.1%) solution. a-IGZO layers were defined by wet etching and is schematically shown Fig. 2.1 (b). Fig. 2-2 shows an etch depth of a-IGZO as function of etch time in the Buffered Oxide Etchant (BOE, 0.1%). The a-IGZO 50nm was completely etched out after ~50 sec in the solution, showing 1.17nm/sec in etching rate. The diluted BOE (0.1%) minimally etches the gate dielectric; meaning the IGZO has high etching selectivity for the SiNx gate dielectric. For BCE type TFT structure as shown Fig. 1, after active layer deposition, Cr (~200 nm) source and drain (S/D) electrodes were also sputter deposited. For E/S type TFT structure as shown Fig. 1-3 (b), E/S layer with SiO_2 100nm (in this study, it will be called channel passivation (CPVX) layer) was deposited on the a-IGZO without breaking vacuum and CPVX SiO_2 is patterned and etched via a dry etching process (Fig. 2-1 (b)).

2.1.4 Source and drain electrode

Cr was also used for source and drain electrode. To select source and drain metal electrode of a-IGZO semiconductor, the work function difference between metal and a-IGZO was considered in order to form an Ohmic contact as well as the materials of low resistivity. There are two types of metal-semiconductor contact. First, Ohmic contacts, metal work function (Φ_M) is lower than semiconductor work function (Φ_S) which yield linear or quasi-linear current-voltage characteristics. The contact must be able to supply the necessary device

current, and the voltage drop across the contact should be small compared to the voltage drop across the active device regions and the metal electrodes. An Ohmic contact should not degrade the device to any significant extent.

Secondly, the Schottky contact of the metal-semiconductor barrier occurs as $\Phi_S < \Phi_M$ which results in unnecessary voltage drop cross contact region. According to earlier reports, inverted staggered a-IGZO TFTs were shown to be contact-limited electrical behavior because of Schottky contact between a-IGZO and metal electrode which have relatively higher Φ_M [35], [36], [37]. In this study, to realize an Ohmic contact and a better etching selectivity with a low resistivity, chromium (Cr) metal is used as gate and source-drain electrode since Cr has a high etch selectivity during fluorine based plasma etching as well as the work function of Cr with 4.5eV is lower than that of a-IGZO semiconductors with 5.01eV~ 4.3eV [38]. The Cr source/drain layers were deposited with 200nm in thickness with the same sputtering conditions as the gate electrode. Similarly the source/drain layers were patterned by photolithographically, and wet etched by CR 14S solution. Prior to wet etching the Cr, Cr/a-IGZO selectivity by Cr etchant (CR-14s) was tested in order to confirm the BCE TFT structure was possible without an E/S layer on a-IGZO by wet etching process. It was confirmed that the wet Cr etching process was possible based on the determined etch selectivity of Cr/a-IGZO = 13. Fig. 2-1 (c) shows the schematic structure after the formation of source and drain electrode pattern by the above described process.

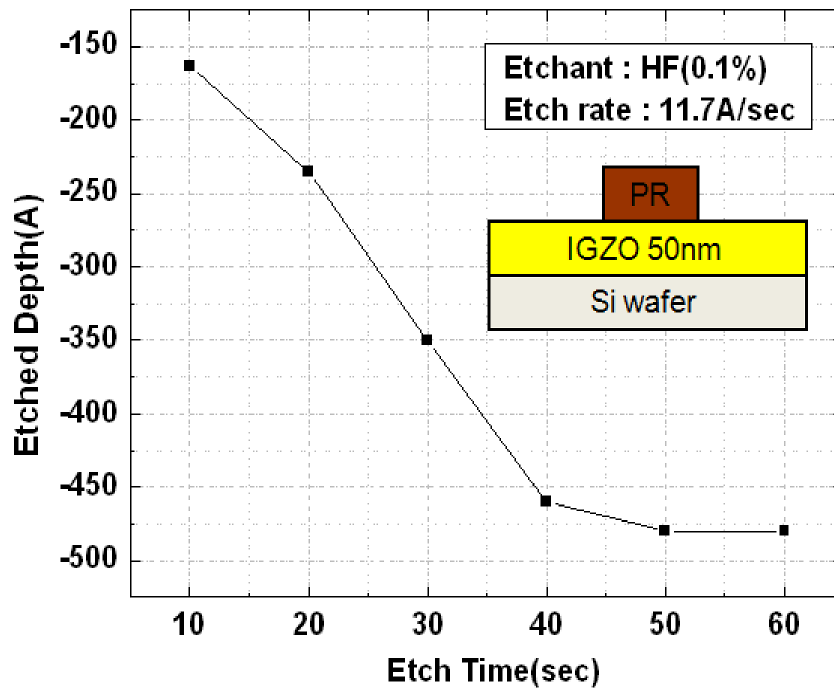


Fig. 2-2. The etch depth of a-IGZO as function of time in the BOE (0.1%).

2.1.5 Passivation

A passivation (PVX) layer in the TFT commonly has been used to protect the device from subsequent processing and environmental effects. However, a-IGZO TFT with passivation shows peculiar characteristics because of sensitive nature of the a-IGZO backchannel to external conditions such as plasma and environmental ambient [39], [40], [41]. This topic will be studied in detail in chapter V. In this study, PVX layers were divided into two kind of PVX notation for convenience; 1) channel passivation (CPVX) is the layer that only passivate the channel area, minimizing plasma or chemical damage on following processes such as sputtered source and drain layer and chemically wet etching process of source and drain metal on the a-IGZO channel. The standard process consisted of a 100nm SiO_2 film as passivation layer which was deposited by rf sputtering method with the following deposition parameters. The system base pressure was 5~9 × 10^{-7} Torr. rf sputtering power was 200 W and sputtering pressure was 5 mTorr Ar-O_2 gas mixture. After photolithographic patterning, in order to contact the gate electrodes, for BCE TFT structure (without CPVX), via hole etching was performed by a combined wet etch using diluted HF etchant and dry etching process using a SF_6 + Ar gas chemistry and for E/S TFT structure (with CPVX), via hole etching was done by only dry etching process using a SF_6 + Ar gas chemistry. Fig. 2.1 (d) shows the final TFT structure after the via hole etching process.

2.1.6 Post annealing

a-IGZO TFTs were typically thermally activated by furnace annealing in an N_2 ambient with 70 sccm in flow rate at 350°C for 1hr. The temperature ramping rate was ~ 15°C/min and naturally cooled down to room temperature. Before ramping up temperature, a sufficient circulation time with 20min with N_2 was performed to minimize unnecessary gas contamination during annealing. In chapter 4, the post annealing effect with annealing conditions will be studied in detail.

2.2 Conclusion

The BCE type with an inverted staggered bottom gate structure was used for a-IGZO TFTs for better electrical performance. Cr metal was used for gate because of low electrical resistivity and easy wet etching process and gate dielectric (SiN_x) was deposited by PECVD. a-IGZO as semiconductor was deposited by rf sputtering and patterned. S/D pad using Cr was deposited by rf sputtering and patterned by wet etching method. To contact gate, the via hole was formed by dry etching method. Finally, the device was post annealed at 350°C in N_2 ambient for 1hr. The fabrication process was summarized in Fig. 2-1.

Chapter 3

Gate dielectric

3.1 Introduction

The gate dielectric film in the MOSFET device is one of the important functional materials, which enables a device to work such that it controls carrier generation and accumulation to the semiconductor by the induced electric field as well as it affects the optical transparency of a device [31]. The gate dielectric in a metal oxide semiconductor field effect transistor (MOSFET) can be simply modeled as a parallel plate capacitor, $C = (k\varepsilon_0 A)/t$, where A is the capacitor area, k is the relative dielectric constant of the material (i.e. ~ 3.9 for SiO_2 and ~ 7.1 for SiN_x), ε_0 is the permittivity of free space (8.85×10^{-14} F/cm), and t is the thickness of the capacitor (dielectric).

There are several important parameters to control transfer characteristics of TFT through a gate dielectric such as dielectric breakdown strength, capacitance, and the interface states between a gate dielectric and a semiconductor, in which parameters are usually governed by the growing film deposition conditions such as gas ratio, power, temperature, and process pressure, affecting the density, structure, stoichiometry, and trap density in the film and thereby they cause the electrical properties to change. In particular they can vary the electrical instability, especially with regard to a threshold voltage shift by carrier injection or capture into traps in the gate dielectric (SiN_x) [31]. The hydrogenated SiN_x deposited by PECVD usually exhibits different physical, optical, and electrical properties due to different stoichiometry by controlling the content of Si-H, N-H, Si-Si, and S-N in the film.

A hysteresis study, investigating ΔV_T at constant drain voltage, from a transfer curve of TFT device is one of the useful methods to evaluate electrical performance and instability. For the hysteresis study, the parameters that affect V_T in the accumulation mode given by: $V_T = qn_0d/C_i + V_{FB}$. Where V_{FB} is the flat-band voltage, which accounts for work function difference between semiconductor and the gate metal, q is the elementary charge, n_0 is the density of free carriers, and d is the thickness of semiconductor. Based on this equation, ΔV_T through the forward and reverse scan occurs and a hysteresis can be expected if: 1) n_0 changes (i.e., due to trapping of free carriers), 2) C_i changes (i.e., charge injection from the gate into dielectric), and 3) V_{FB} changes (i.e., structural changes in the semiconductor). V_{FB} is usually assumed to be constant in this study because a-IGZO semiconductors were deposited with the same sputtering conditions [42].

It is known that a hysteresis in TFT transfer curve as well as other electrical performance such as S, μ_{FE}, and V_T is strongly dependent on microscopic structural and charge effects with the following types. In Si-SiO_2 system, four general types of charge defects are known [31]: 1) interface-trapped charge are defects or impurities at the interface, 2) fixed charge in oxide is a positive charge due to structural defects, 3) trapped charge in oxide are electrons or holes trapped in the bulk of the oxide which can be introduced during device fabrication or operation, and 4) mobile charge in the oxide are mainly alkali metal cations and H^+ such that mobile Na^+ ions in gate dielectric (SiO_2) cause V_T shifts in the device. In addition, Garros *et al.* reported that high-k dielectrics increase the number of traps and thereby the size of hysteresis [43].

The hysteresis behaviors from transfer curve swing strongly depend on sweep rate; if the rate of release of charge from such a trap is sufficiently low, the sweep rate may be faster than the time necessary to reach thermal equilibrium, which results in hysteresis effects in the electrical characteristics of TFT. Fig. 3-1shows the two types of schematically depicted transfer characteristics of n-type semiconductor where, Fig. 3-1 (a), the back sweep current (BSC) is lower than the forward sweep current, called lower BSC hysteresis and Fig. 3-1 (b), the BSC is higher than the forward sweep current, called higher BSC hysteresis. It is known that the lower BSC hysteresis is due to following reasons: 1) trapped majority or minority charges at the semiconductor/dielectric interface (here, the minority trap effect is minor because a-IGZO features a degenerated electronic structure showing electron carrier conduction), 2) charge injection from a semiconductor into a dielectric, and 3) mobile ions in the semiconductor (in case of n-type semiconductor, positive mobile charges) which causes a decrease of the carrier density of semiconductor; decreasing I_{DS}, causing lower BSC hysteresis. While the higher BSC hysteresis depicted in Fig. 3-1 (b) is usually due to mobile ions in gate dielectric. As on-gate voltage (a positive V_{GS}) is applied to gate metal, the cations move towards the interface between gate dielectric and semiconductor and when V_{GS} is swept back to 0 V (backward sweep), the ions stay close to the semiconductor, thereby retaining the diminishing field and causing higher BSC hysteresis [44].

Although the gate dielectric (usually oxide) resistivity is on the order of 10^{15} ohm.cm, it is not infinite. Hence currents flow through a gate oxide for any gate voltage. However, for higher gate oxide electric fields, gate currents increase rapidly with voltage.

Especially, the main degradation mechanism for MOS TFT is known to be trapped electrons near the gate – drain (bottom electrode) interface because of the relatively high electric field at this point. There are several gate current flow mechanisms. Fig. 3-2 shows the MOS diagram which describes two tunneling mechanisms in the gate dielectric, assuming p-type substrate and positively applied gate voltage on top electrode. For $V_{ox} < q\Phi_B$ (barrier height Φ_B has a few eV), as shown Fig. 3-2 (a), the electrons need to penetrate the full oxide thickness and the gate current is due to direct tunneling. For $V_{ox} > q\Phi_B$, as shown Fig. 3-2 (b), the electrons see a triangular barrier and the gate current is due to Fowler-Nordheim (FN) tunneling. However, according to Shannon *et al.* [45], in case of hydrogenated SiN_x(particularly at low biases and electric field), the current transport can be well described by Poole-Frenkel effect in a defect band by which holes transport via dangling-bond states in SiN_x. Fig.3-3 shows the electric field effect in the electron energy diagram in equilibrium. An electron energy diagram at zero electric field is shown by (1) in Fig.3-3. Energy $E_C – E_T$ is required for electron emission from the trap to conduction the conduction band. An applied electric field causes the bands bend, as shown by (2) in Fig. 3-3, and the emission energy is reduced by the energy δE. Poole-Frenkel emission over the lowered barrier is shown as (a) in Fig. 3-3. Even less energy is required for phonon assisted tunneling, shown as (b) in Fig. 3-3, in which the electron is excited by phonons for only part of the energy barrier and the tunnels through the remaining barrier.

In this chapter, to understand and characterize gate dielectric properties with different stoichiometric SiN_x and SiO_2 (reference dielectric), several measurements were performed on standard structures, namely: 1) current versus gate voltage hysteresis (V_T

instability (ΔV_T) with forward and backward swing during transfer curve measurement) and 2) leakage current mechanism via gate dielectric was measured and the electrical performance of a-IGZO TFTs were compared.

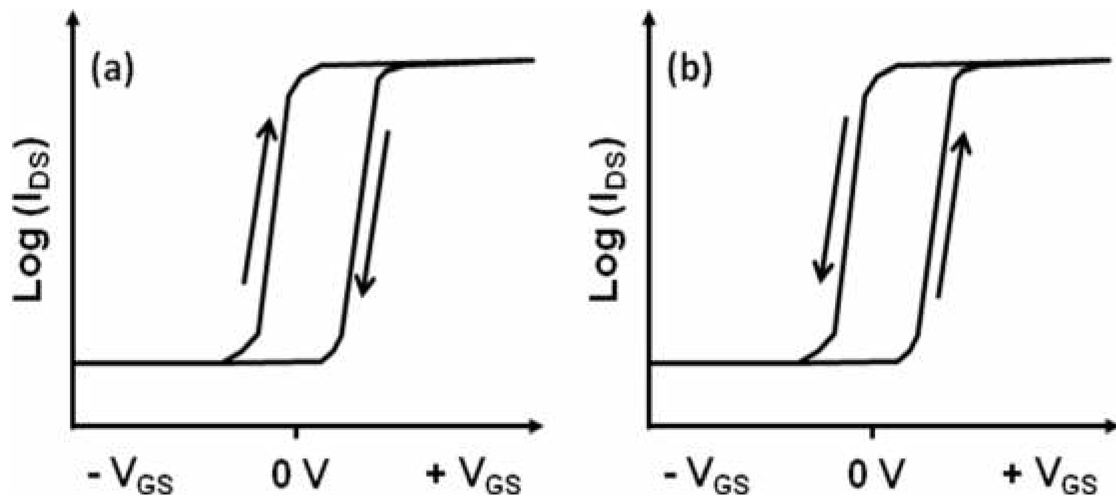


Fig. 3-1. Schematic transfer characteristics (I_{DS} vs. V_{GS}) of n-type semiconductor TFT, (a) lower BSC hysteresis and (b) higher BSC hysteresis.

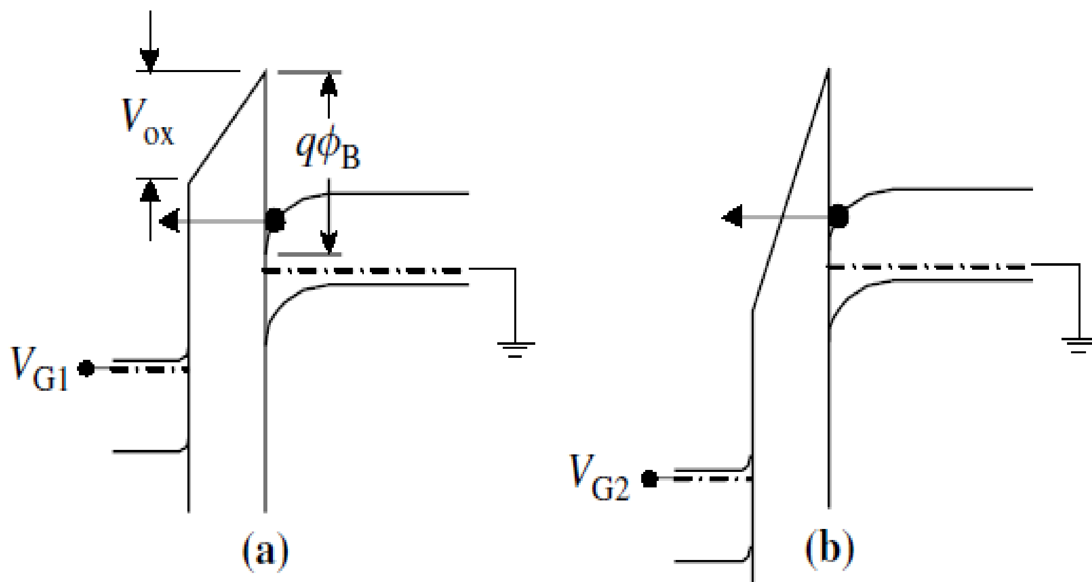


Fig. 3-2. MOS band diagrams for (a) Vox < qΦ_B (direct tunneling) and (b) Vox > q Φ_B (Fowler-Nordheim tunneling).

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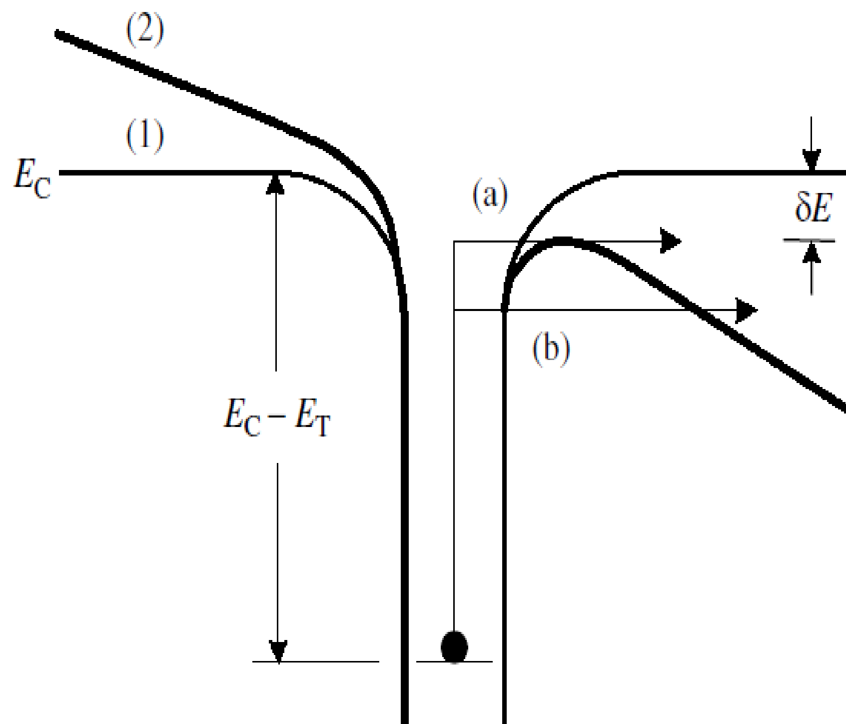

Fig. 3-3. Electron energy diagram in equilibrium (1) and in the presence of an electric field (2) Showing field-enhanced electron emission: (a) Poole-Frenkel emission, (b) phonon-assisted tunneling.

3.2 Experimental

SiN_x and SiO_2 gate dielectrics were deposited with different deposition conditions using PECVD (Oxford system). The SiN_x was deposited with following conditions: 40W RF power, 600 mTorr pressure, 350°C temperature and different (5%SiH_4-Ar/NH_3/N_2) gas ratios; where 5%SiH_4-Ar and N_2 flow rates were 150sccm and 790sccm, respectively. NH_3 flow rates were with 38sccm, 17sccm, and 3sccm in order to form different stoichiometric SiN_x (gas ratio: NH_3/SiH_4=5.1, NH_3/ SiH_4=2.3, and NH_3/ SiH_4=0.3). To compare to SiN_x film, the reference SiO_2 was deposited with following conditions: 20W RF power, 1000 mTorr pressure, 350°C temperature, and 5%SiH_4-Ar/N_2O (85/157 sccm) gas flow rate. The SiN_x and SiO_2 films deposition conditions and their corresponding device properties are listed in Table 3-1. To estimate the film stoichiometry, the refractive index (n) was measured by ellipsometry system (Horiba Jobinyvon MM-16). To extract the optical properties of the films, the transmission of films on quartz substrates were measured by UV/VIS/IR spectrometer (Carrie 5000) from which the optical band gaps were estimated and the reflectance was measured by Filmmetrics and absorption was calculated with following relation; absorption (A) = 1-transmittance (T) + reflectance (R). To characterize the electrical performance of the a-IGZO TFT at V_{DS} = 5.1V, the semiconductor analyzer (HP 4145B) was used and to characterize current flow through dielectrics, the device with the structure of metal-insulator-metal (heavy doped p-type silicon) (MIM) was fabricated as shown Fig. 3-4 where the gate dielectric films using PECVD were deposited on the common gate heavy doped p-type silicon substrate. Cr (top electrode) using electron beam evaporator was deposited on the gate dielectrics and top electrode (180 x 180 um size) was

photolithographically patterned and wet-etched out by Cr 14S (Cr etchant). A capacitance-voltage (CV) was employed to measure the capacitance of gate dielectric and to extract gate dielectric constant (k) by $k = Ct/\epsilon_0$, where C is measured capacitance per unit area (F/cm^2), t is thickness of gate dielectric, and ϵ_0 dielectric permittivity in vacuum (8.85×10^{-14} F/cm) and current-voltage (IV) also was measured to evaluate the gate dielectrics.

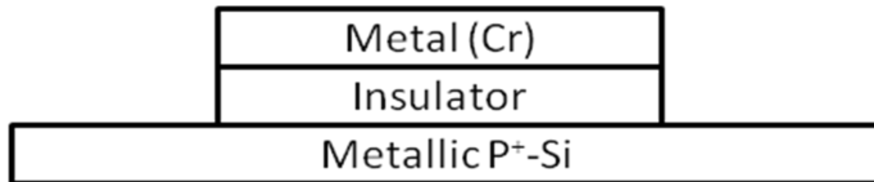

Fig. 3-4. The metal-insulator-semiconductor device structure for capacitance-voltage (CV) and current-voltage (IV) measurement.

Table 3-1 Deposition conditions and resulting optical and electrical properties of different stoichiometric SiN_x and SiO_2 films.

	SiN_x1	SiN_x2	SiN_x3	SiO_2
5%SiH_4-Ar (SCCM)	150	150	150	85
NH_3	38	17	2	-
NH_3/SiH_4	5.1	2.3	0.3	-
Transmittance (%) at 550nm	80	79	70	94
E_g (eV)	4.87	4.75	3.23	~ 8.5
Refractive index, n	1.90	2.03	2.13	1.46
μ_{FE} (cm^2/Vs)	1.2$\pm$0.08	1.3$\pm$1.05	2.0$\pm$0.71	3.95$\pm$0.14
S (V/decade)	1.08$\pm$0.08	1.57$\pm$0.26	1.23$\pm$0.28	0.69$\pm$0.17
I_{OFF} x 10^{-13}(A)	0.25$\pm$0.05	0.38$\pm$0.27	206$\pm$110	0.26$\pm$0.22
V_T (V)	9.1$\pm$0.9	5.2$\pm$0.7	7.2$\pm$1.4	4.8$\pm$0.7
ΔV_T at I_{DS} 1nA (V)	1.1$\pm$0.09	1.5$\pm$0.01	2.9$\pm$0.70	0.82$\pm$0.04
Gate dielectric RMS(nm)	1.52	1.11	1.26	1.28

3.3 Results and discussion

The optical properties of gate dielectrics were initially analyzed. The optical transmittance and reflectance for each gate dielectrics were measured in wavelength range between 200nm and 880nm in which optical transmittance includes the 1mm quartz substrate. The average optical transmission in the visible part of the spectrum is 80%, 79%, 70%, and 94% at 550nm (maximum sensitivity for the human eye) for SiN_x1, SiN_x2, SiN_x3, and SiO_2, respectively, as shown in Fig. 3-5. The noticeable decrease in the transmittance at ~ 320nm and ~500nm were due to relatively increased reflectance rather than absorption at the same wavelength. From measured transmittance and reflectance, the optical bands gap(E_g) were estimated by using the following method; the absorption $(\alpha h\nu)^2$ versus of photon energy ($h\nu$) was plotted in Fig. 3-6 in which α, absorption coefficient, was calculated from $\alpha = (1/t)\mathit{ln}(T/(1-R)^2)$, where t is the thickness. Interestingly, the estimated E_g was changed with gate dielectrics; SiN_x1=4.85eV, SiN_x2=4.75eV, SiN_x3=2.83eV, SiO_2=~ 8.5 eV (from literature), which shows that transmittance and optical band gap of SiN_x films were decreased with increasing SiH_4 gas (approaching Si-rich SiN_x film) [32]. According to Budaguan *et. al* [46], the increased optical band gap in SiN_x film can be changed by the replacement of Si-Si bond by strong Si-N bonds due to the formation of Si-N network. The increase of N/Si atomic ratio in the SiN_x results in both an increase in the deformation of bond angles and a broadening of valence band tail [47], [48]. Refractive index values were also measured with these films because atomic ratio (N/Si) of the films can be estimated; higher n values indicate more Si atoms in the film [49] [50].

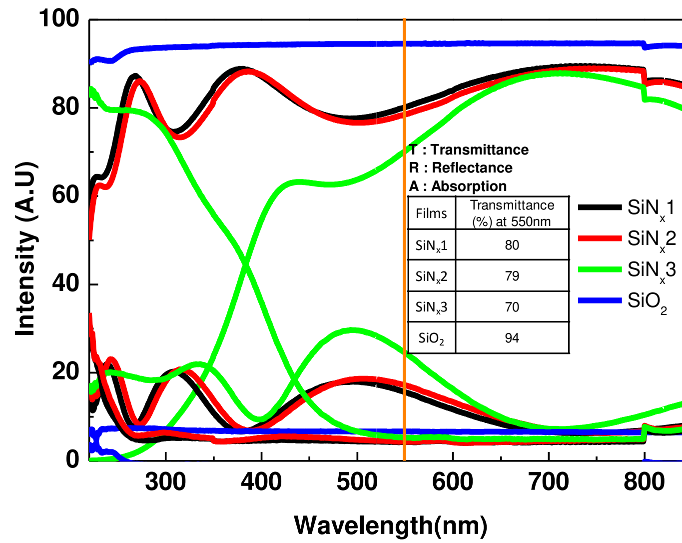

Fig. 3-5. The transmittance with different gate dielectric of SiN_x1(200nm), SiN_x2(200nm), SiN_x3(200nm), and SiO_2(100nm), the inset compares the transmittance at 500nm.

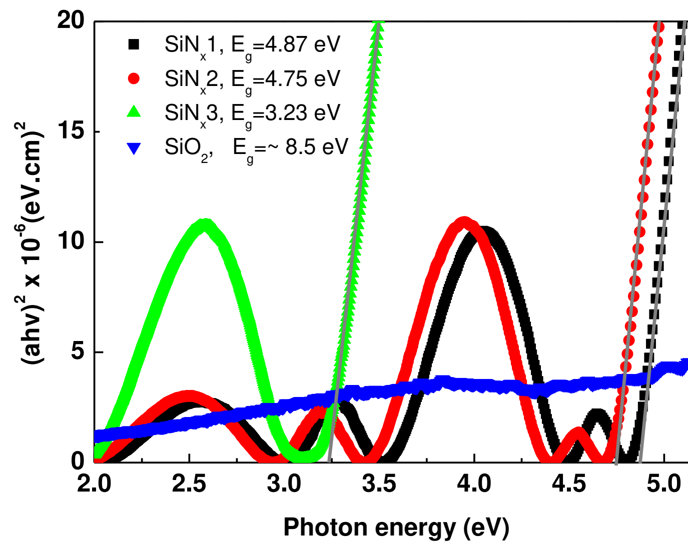

Fig. 3-6. Optical band extraction from $(\alpha h\nu)^2$ plotted as a function of photon energy for SiN_x1, SiN_x2, SiN_x3, and SiO_2 with 200nm in thickness.

For SiN_x films, interestingly, the resulting refractive index was increased with decreasing the ratio of NH_3/SiH_4, indicating the SiN_x film approaches Si-rich films which shows relatively lower optical band gap.

Fig. 3-7 shows the representative transfer curves with different stoichiometric SiN_x and SiO_2 as gate dielectric, Fig. 3-8 shows the comparison of electrical performance which is extracted from each different curve, and the deposition conditions and resulting optical and electrical properties of different stoichiometric SiN_x and SiO_2 films are summarized in Table 3-1. Here, the SiN_x3 deposition condition (Si-rich SiN_x) has been used for the conventional condition of gate dielectric film in our study. Overall, a-IGZO TFT with SiO_2 gate dielectric shows the best electrical performance because the film probably has high stoichiometry close to n=1.46. At a glance, all TFT transfer curves regardless of a type of gate dielectric shows BSC hysteresis; when the scan is started from the off state, the traps are empty. During the off-to-on sweep, the traps are filled, decreasing carrier density in a-IGZO. During the on-to-off sweep, the trapped electrons are slowly released (much slower than the sweep rate), and so fewer mobile electrons are at the interface at any given V_{GS} and the resulting I_{DS} is lower. The release rate of the traps must be slower than the scan rate, meaning that fast sweeps show larger hysteresis than slow sweeps.

For electrical performance of a-IGZO TFT, noticeably SiN_x3 shows relatively higher off-current level and larger ΔV_T at I_{DS}=1nA as compared with SiN_x1, SiN_x2, and SiO_2. As discussed above, the hysteresis difference in the a-IGZO TFTs is mainly due

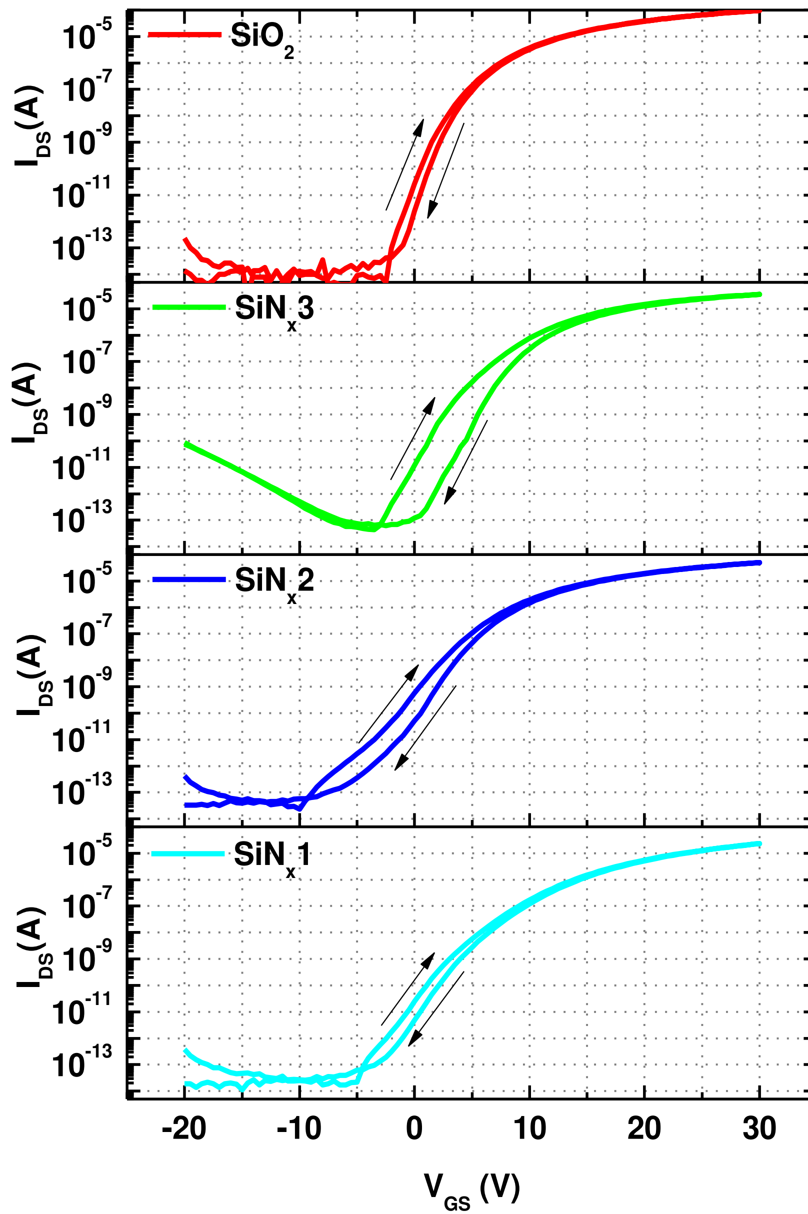

Fig. 3-7. The representative transfer curves with different stoichiometric SiN_x and SiO_2 as gate dielectric at V_{DS} = 5.1V.

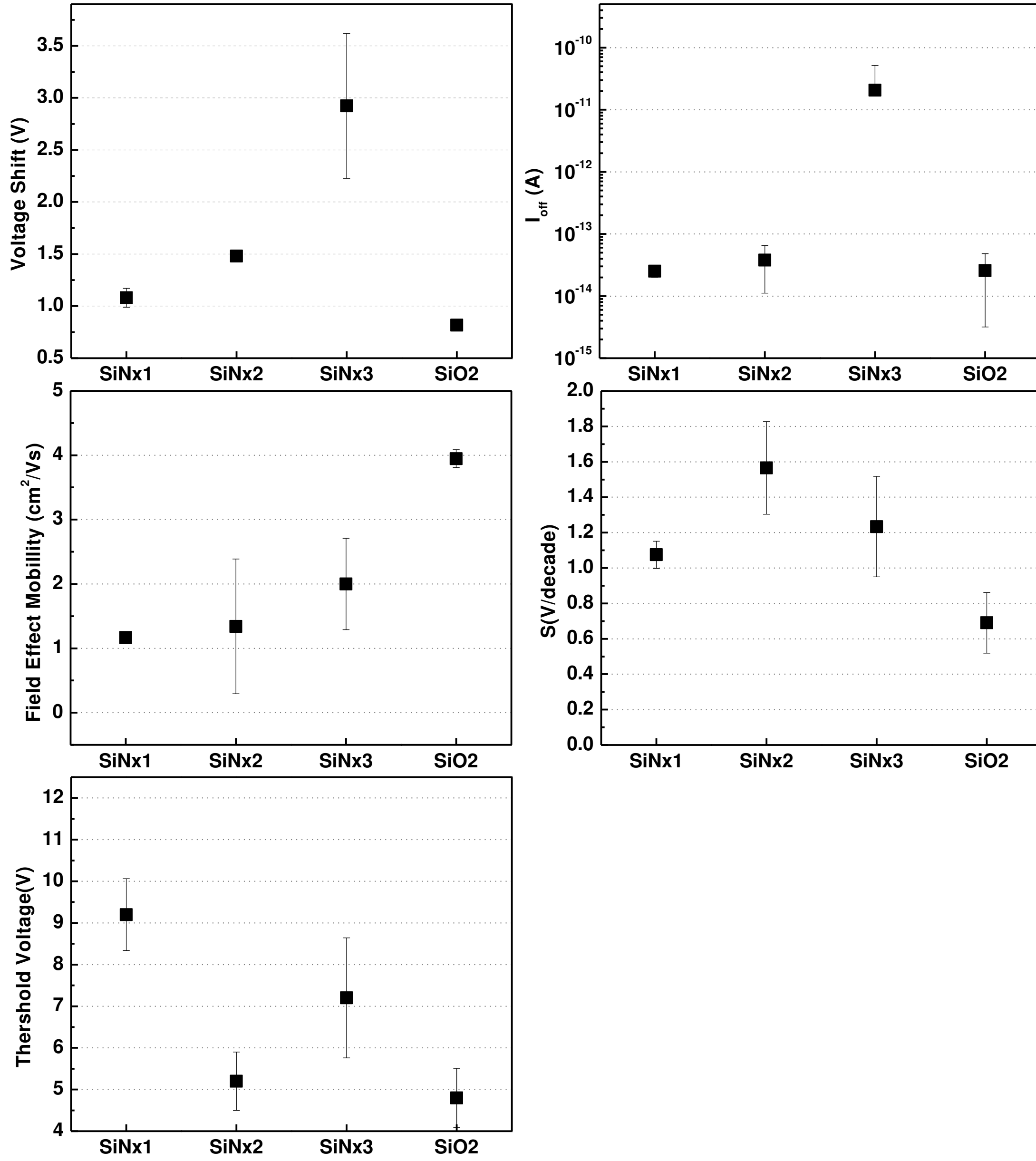

Fig. 3-8. Comparison of electrical performance of a-IGZO TFT.

to majority traps (i.e., electron traps in a-IGZO and in gate dielectric) that fill fast and empty slowly and can result in lower BSC hysteresis. Here, the evolutionary hysteresis difference (ΔV_T) from SiN_x1 to SiN_x3 can be considered to be mainly from the contribution of trapped charges in/near the gate dielectric rather than in/near a-IGZO because the study used the same sputtering conditions for a-IGZO. Therefore, the contribution of mobile ions in a-IGZO also can be ignored. This assumption, hysteresis dependent on gate dielectric, is consistent with by J. Robertson's study [51] who proposed the energy band diagram of amorphous SiN_x is changed with N/Si atomic ratio. Fig. 3-9 shows the band diagram for amorphous SiN_x with different N/Si atomic ratio proposed by J. Robertson. The size of band gap is decreased with decreasing N/Si atomic ratio, approaching Si-rich SiN_x and the dominant trap centers (dangling bonds states) in SiN_x are changed from both Si and N to Si only by increasing Si atoms (this report is consistent with our results; optical band gap is decreased with increasing SiH_4 content in SiN_x (Si-rich film)). Here, N centers, which are known to be a faster trap center than Si center [51], appears with increasing N/Si atomic ratio. Therefore, both Si and N dangling bonds in the band gap may contribute to carrier trapping. However, faster N trap centers may contribute more to trap carriers because Si trap centers are located in deeper level in the band gap. However, in case of SiN_x3, even though N centers do not exist in the band gap in case of SiN_x1 and SiN_x2, the hysteresis was worse as shown in Fig. 3.7. In a view of this narrowing band gap, the increased hysteresis of SiN_x3 (E_g =2.83eV) can be understood. The slow Si trap center (Si dangling bonds) is relatively close to band edge will significantly contribute to trapping the electron during carrier conduction (SiN_x3 at N/Si ratio in Fig. 3-9). Therefore, for

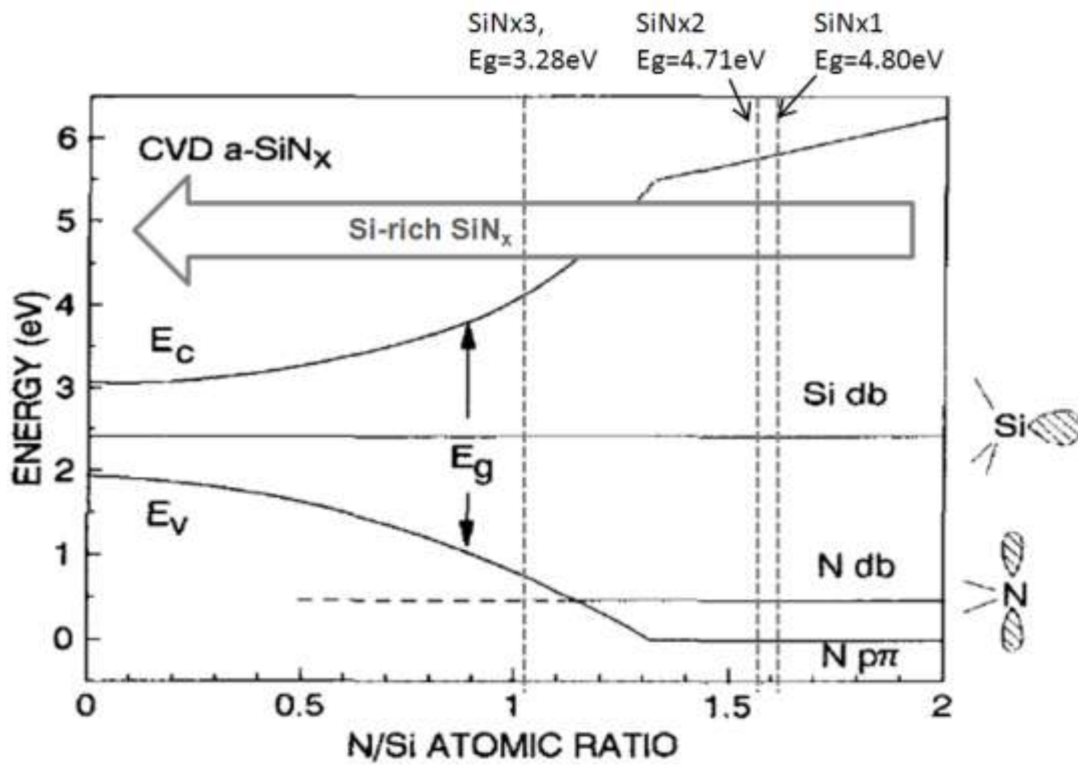

Fig. 3-9. Band diagram for amorphous SiN_x with different N/Si atomic ratio.

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N/Si ratio; thus causing increased hysteresis. Likewise, in a view of trap sites in gate dielectric, a SiO_2 also could be highly candidate for gate dielectric because relatively SiN_x3, the flowing carrier in the channel has more probability to be trapped and slowly released than the carriers trapped in N trap centers of SiN_x1 and SiN_x2 around 1.6 of lower trap sites provide improved hysteresis of TFT curve. In addition, as discussed above, it was reported that high-k dielectrics increase the number of traps and thereby the size of hysteresis [43]. The extracted k values from CV capacitance were 6.9, 6.9, and 8.1 for SiN_x1, SiN_x2, and SiN_x3, respectively. The resulting higher k value of SiN_x3 also may contribute to an increase of hysteresis.

Fig. 3-10 shows the averaged gate current density as a function of gate voltage, which were measured with MIM structure as described in the experimental. The relative high gate current in Fig. 3-10 is due to the smaller SiO_2 thickness (100nm) than other SiN_x (200nm). At the range of gate voltage (0V to -40V), in this gate voltage range, the direct tunneling current seems to overwhelm the total current because of very low gate voltage, $V_{ox} < q\Phi_B$. In addition, the plotted curve in Fig. 3-10 does not show any significant current density change as function of gate voltage; direct tunneling current, $J_{dir} \approx \exp(-1/E_{ox})$ and FN current density, $J_{FN} \approx E_{ox}^2 \exp(-1/E_{ox})$, where E_{ox} is oxide electric field. Fig. 3-11 shows the plot of gate current density verse dielectric oxide electric field (normalized to thickness). The study suggests two different current regimes with electric field intensity; 1) low electric field regime as shown Fig.3-11 (b) (-100mV/cm to 0V, L) and 2) high electric field regime as shown Fig. 3-11 (c) (- 2.0 MV/cm to -1.2 MV/cm, H) (b) because the leakage current could be considered for the

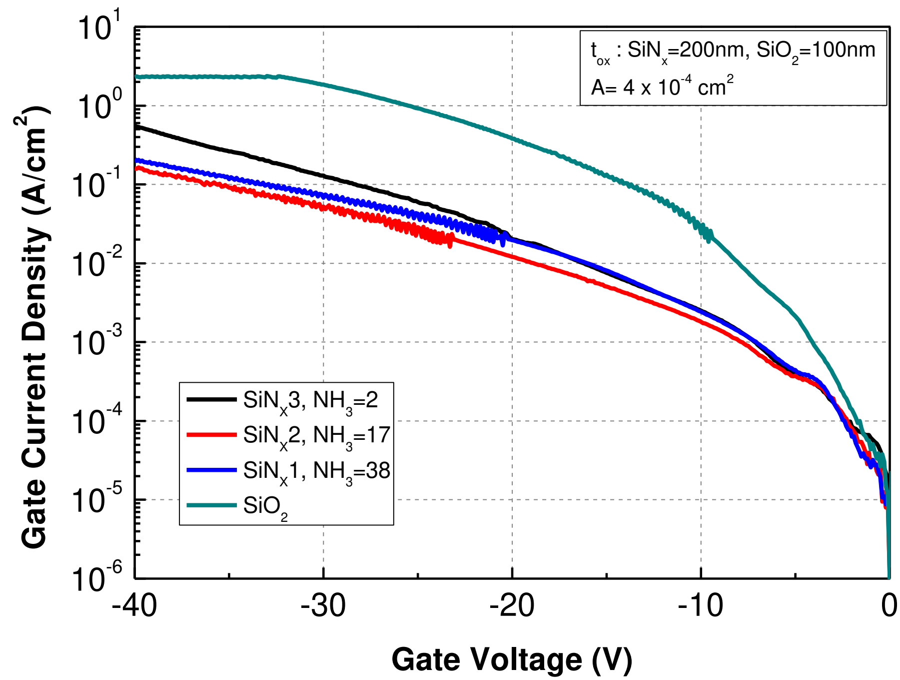


Fig. 3-10. The averaged gate current density as a function of gate voltage with different gate dielectrics.

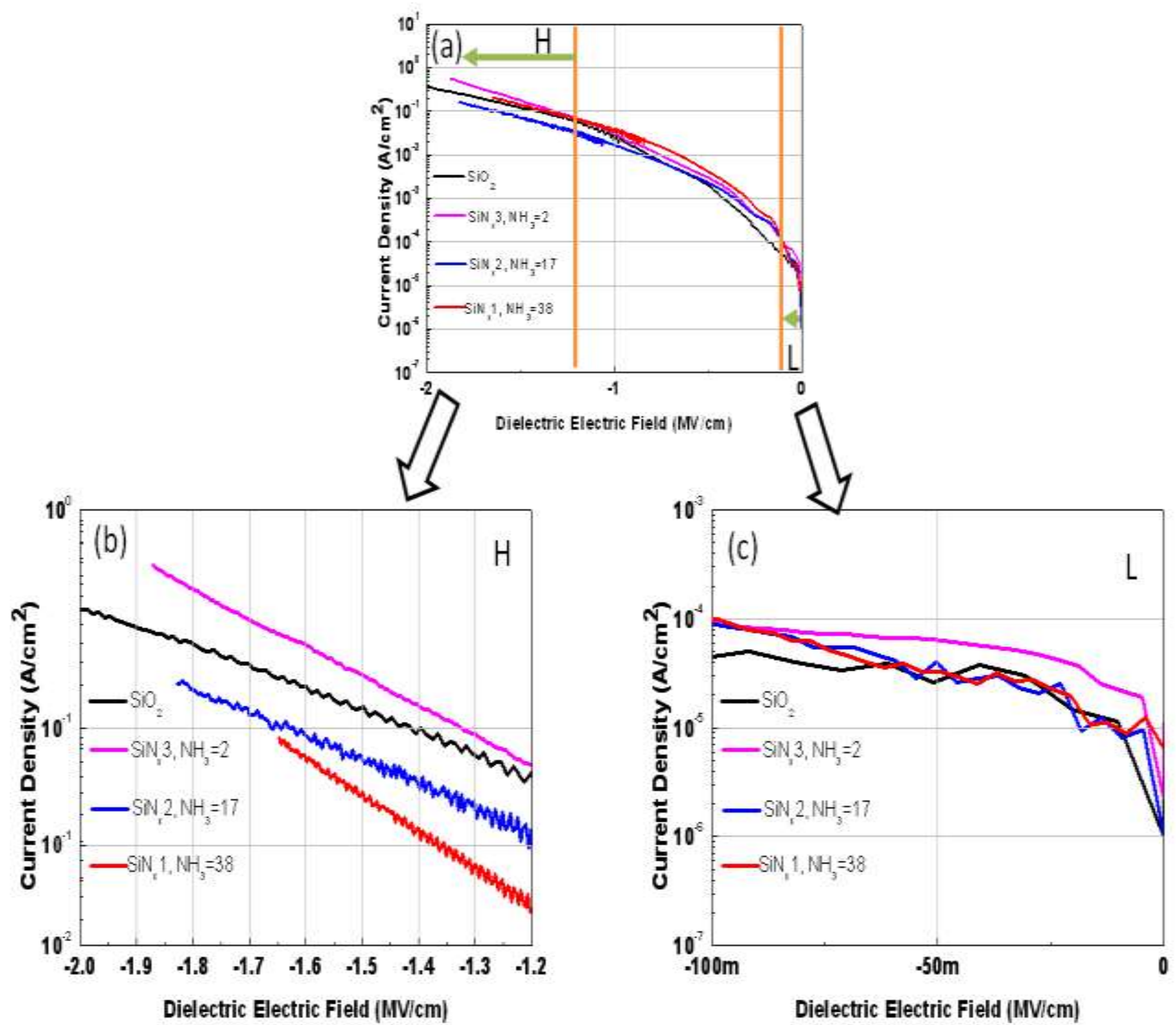


Fig. 3-11. The plot of gate current density verse dielectric oxide electric field (normalized to thickness).

device operating at low voltage (low dielectric field) even to reduce power consumption. In case of the low electric field regime (L), the current of SiN_x3 shows ~ 40 μA higher than others. This current behavior of Si-rich SiN_x3 at low electric field can be understood by Poole-Frenkel hopping, $J_{PF} \approx E_{ox} \exp(E_{ox}^{1/2})$, between defect states (Si dangling bonds) in the bulk of the SiN_x [45], [52]. The initial nonequilibrium process such as electrical stress change a barrier by introducing Si-dangling bond defects, called "current induced conductivity" and they reported that this effect can easily be found in Si-rich alloys and can be very pronounced leading to many orders of magnitude change in current at a given applied voltage. Furthermore, the leakage current at high electric field regime (~ 1.5~2.0 MV/cm, V_G= ~ 40V) was also investigated. The higher current density of SiN_x3 is obvious in the relatively high electric field regime (H), which was believed to be also the contribution of smaller band gap for SiN_x3 (3.23eV) compared to SiN_x1(4.88eV), SiN_x2 (4.75eV) as well as Poole- Frenkel effect more preferred to Si-rich SiN_x 3. The fact the Si-dangling bond defects play a role of inducing current was proved by investigating the SiO_2 curve at < 0.5MV/cm, showing lower current density than the other SiN_x curves. The SiO_2 has relatively lower Si-dangling bonds because of lower remaining Si-H bonds from the precursors (SiH_4) during deposition process and even the bond dissociation energy of Si-O (452 kJ/mol) is much higher than that of Si-H(347 kJ/mol) and N-H (391 kJ/mol) in SiN_x.

To characterize capacitance properties of gate dialectics, each capacitance from CV swing was measured and normalized by ideal C_{ox} (3.14×10^{-8} F/cm^2 for SiN_x, 3.45×10^{-8} F/cm^2 for SiO_2), $C/C_{ox.}$ The resulting C/C_{ox} s of SiN_x1, SiN_x2, SiN_x3, and SiO_2 were 0.98, 0.97, 1.13, and 0.98, respectively. Table 3-2 summarized the date of CV

measurement with different SiN_x and SiO_2. Interestingly, C/C_{ox} of SiN_x3 shows higher than that of stoichiometry SiN_x, meaning that the dielectric constant increased. The dielectric constant SiN_x3 (Si-rich SiN_x film) extracted from C $(F/cm^2)/\epsilon_0$ was 8.1, which is a reasonable result (i.e. dielectric constant of silicon is 11.8) and the SiN_x3 band gap energy decreased due to silicon alloying (the Si band gap = 1.12 eV).

The surface roughness of gate dielectric was studied to understand its affects on electrical performance of TFT such as μ_{FE} and S. Fig. 3-12 shows the surface roughness of different gate dielectrics. As compared to the electrical performance in Table 3-1, they do not correlated to the surface roughness of gate dielectrics. Therefore, this effect in this study is ignored.

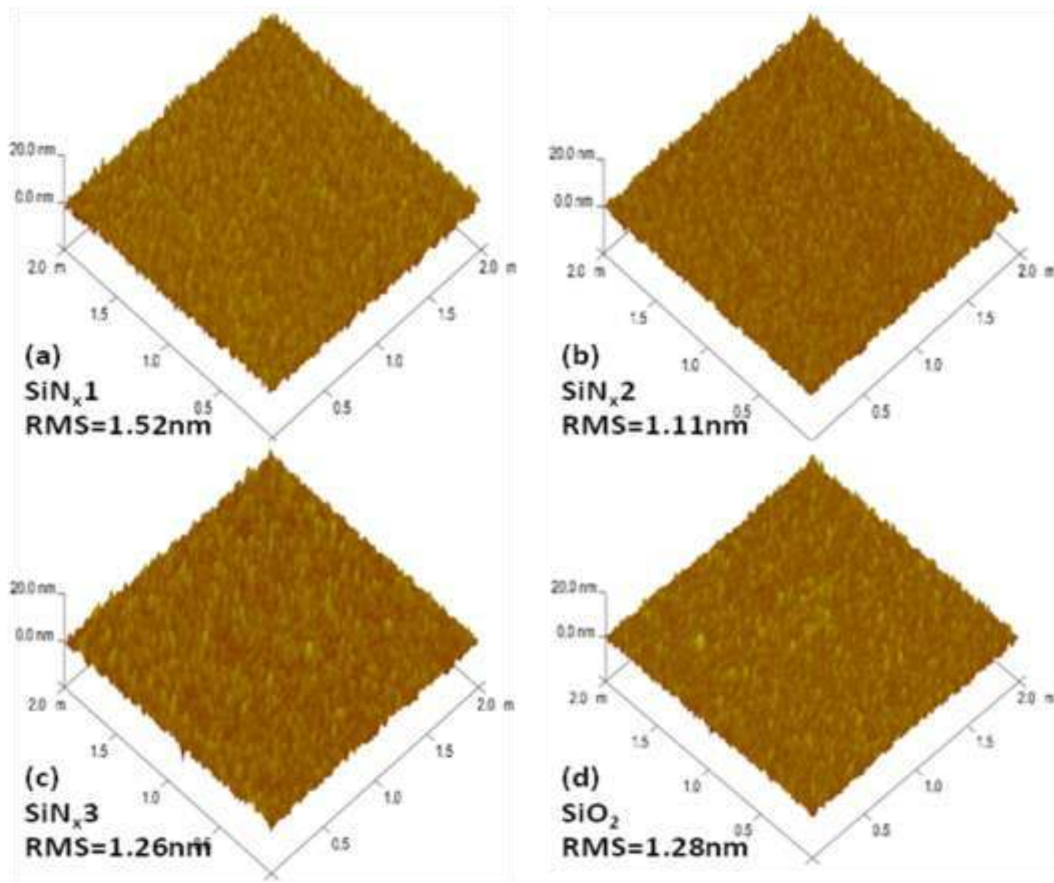


Fig. 3-12. The surface roughness of gate dielectrics using atomic force microscopy (AFM), (a) SiN_x1, (b) SiN_x2,(c) SiN_x3, and (d) SiO_2.

Table 3-2 Capacitance and dielectric properties with different gate dielectrics.

	C (nF/cm^2)	C/Cox	Dielectric constant (k)
SiN_x1	30.7	0.98	6.9
SiN_x2	30.6	0.97	6.9
SiN_x3	35.6	1.13	8.1
SiO_2	33.8	0.98	3.8

3.4 Conclusion

To achieve high performance gate dielectric, the gate dielectric with different stoichiometric SiN_x and SiO_2 were optically and electrically analyzed. The optical properties were significantly dependent on the gas ratio (NH_3/SiH_4); the SiN_x1 deposited with highest NH_3 gas shows highest transmittance and optical band gap because of increased N/Si ratio. The SiN_x1 and SiN_x2 showed the improved electrical characteristics. It was studied that the hysteresis difference in the a-IGZO TFTs is mainly from the contribution of trapped charges in/near the gate dielectric. By studying hysteresis of transfer curve and current –voltage, the film deposited with NH_3/SiH_4 =5.1as well as SiO_2 film showed best electrical performance; less hysteresis and lower gate leakage current. As a result, the SiN_x1 film and stoichiometric SiO_2 film were expected to be best PECVD deposition for gate dielectric.

*Acknowledgment

Of the work presented in this chapter Carlos Gonzalez helped to perform the UV-VIS measurement in SMRC (Scintillation Material Research Center) to achieve transmittance, Joo Hyon Noh helped to measure AFM and capacitance-voltage of gate dielectrics and advised to extract optical bandgap from transmittance, and Jiyong Noh helped to measure the capacitance-voltage in the gate dielectrics. Philip Rack provided direction, funding of the research, discussion and motivation.

Chapter 4

Semiconductor; a-IGZO

4.1 Basic a-IGZO TFT properties with sputtering parameters

4.1.1 Introduction

Amorphous indium gallium zinc oxide layers is usually deposited by sputter deposition because the sputtering deposition process is particularly attractive for low temperature processing which makes it possible to integrate devices on flexible substrate. In spite of these merits, some issues of a-IGZO as an active layer must be solved to achieve robust semiconductor devices. Intrinsic oxide semiconductor materials are very sensitive to the processing conditions because of its high ionic characteristics due to the large difference in electronegativity between the transition metal cations and oxygen atoms [8, 53, 54]. The electrical properties of a-IGZO films can be demonstrated with various sputtering parameters because of the different stoichiometry in the film [25, 55]. In this study, the basic electrical characteristics of a-IGZO TFTs were qualitatively demonstrated with sputtering parameters such as rf power and oxygen partial pressure (PO_2).

4.1.2 Experimental

a-IGZO (50 nm) was rf magnetron sputter deposited using an 50mm diameter a-IGZO target ($In_2O_3 : Ga_2O_3 : ZnO$ = 1:1:1 mol %) with different rf powers and PO_2. The relevant sputtering parameters for the a-IGZO films were: system base pressure was 5×10^{-7} Torr; rf sputtering powers were 60 W and 80W; sputtering pressure was 5 mTorr;

Ar gas was fixed to 25 sccm. The O_2 was changed from 5 sccm to 15 sccm with 5 sccm increments; PO_2 = 0.83 mTorr, 1.66 mTorr, and 2.5 mTorr where PO_2 was derived from Ar/(O_2+Ar) × sputtering process pressure (5 mTorr). The fabricated TFTs have BCE type of structure described in the procedure of chapter II and the characteristic transfer curves of TFT were measured using an HP 4156A device parameter analyzer with a channel width of 70 μm and a channel length of 6 μm and compared at V_{DS}=5.1V.

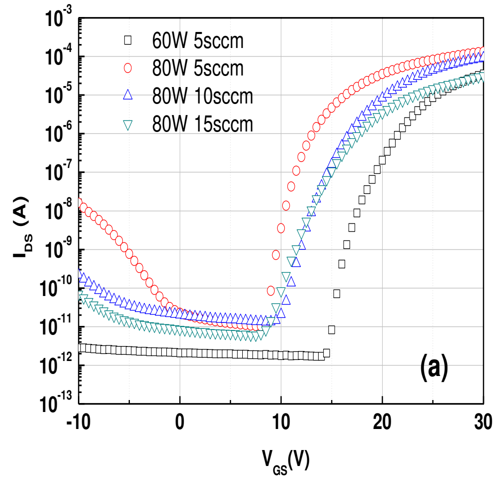
4.1.3 Results and discussion

Fig. 4.1(a) shows the transfer characteristics of a-IGZO TFT with different rf power (60W and 80W) at constant PO_2 = 0.83 mTorr and PO_2 at constant rf power = 80W and the curves of $I_{DS}^{1/2}$ vs. V_{GS} also plotted to compare electrical properties in the saturation region ($V_D > V_G - V_T$). The extracted data from these transfer curves are summarized in table 4.1. First, the rf power effect on a-IGZO TFT was compared at constant PO_2 (0.83 mTorr). The increased rf power gives rise to enhanced field effect mobility from 2.7 cm^2/Vs to 4.2 cm^2/Vs, increased I_{OFF} from 2.96 x 10^{-12} A to 1.74 x 10^{-11} A, respectively. In contrast, V_T was decreased from 19.5V to 12.5V. However, S was not changed with changing rf power. According to Jeong *et al.* and Chiang *et al.*, these electrical behaviors as function of rf power are related to In_2O_3 contents in the a-IGZO film; the ratio of deposited film In/(In+Ga+Zn) can be increased with increasing rf power, in which the content of In_2O_3 with relatively lower bond energy can be preferentially sputtered by higher energetic Ar^+ in plasma from a-IGZO target. It is known that the In^{3+} cations in the a-IGZO primarily form an extended CBM by percolation of the In 5s orbitals [53]. Therefore, the improvement in mobility is consistent with increasing indium

content and the consequent increase in the carrier density (Fig. 4.2 (a)) which caused the threshold voltage to be negatively shifted (Fig. 4-2 (b) with following relation equation: $V_T = V_{FB} + 2\Phi_F + \frac{\sqrt{2qK_S\varepsilon_0 n 2\Phi_F}}{C_{OX}} \approx \frac{\sqrt{2qK_S\varepsilon_0 n 2\Phi_F}}{C_{OX}}$

Where V_{FB} is flat band voltage, Φ_F is surface potential, K_S is semiconductor dielectric constant, ϵ_0 is permittivity of free space, and C_{OX} is the capacitance of oxide, primarily depending on electron carrier density, n. This can be also supported by the fact that I_{OFF} increased at high rf power condition (80W) because of the increased bulk conduction in the a-IGZO channel between source and drain as shown Fig. 4.2 (d). However, in this study, subthreshold gate swing was not deteriorated even at rf power of 80W as shown Fig. 4.2 (c), indicating that, for both 60W and 80W, there were no significant difference of the trap density of interface states between gate dielectric and a-IGZO. Second, the influence of PO_2 to a-IGZO TFT was also investigated. In fact, as described chapter 1, oxygen vacancies are the main source of free electrons in oxide semiconductor. As shown in Fig. 4.2. (b), it is clearly shown that the V_T was increased up to PO_2=1.43 mTorr and saturated due to the decreased number of electron carriers in a-IGZO; essentially, as PO_2 increases carrier concentration decreases, and higher V_G is necessary to accumulate enough free carriers to form a conductive channel path between source and drain electrodes. This electrical behavior also can be explained by percolation model in which Fermi level is in the degenerate state ($E_F > E_C$) and can be moved down with increasing PO_2, causing longer carriers conducting paths around the valley of energy barrier as shown in Fig.1-14 (b). As described above, in the same way,

the lower carrier concentration as PO_2 increases also justifies the significant decrease in field effect mobility as well as the decreased off current level as shown in Fig. 4-2 (a) and (d). In addition, as shown in Fig.4-2 (c), subthreshold gate swing was noticeably increased with increasing PO_2. It is known that the high substrate bombardment by highly energetic negative ions that can damage the surface of gate dielectric and also the growing semiconductor film as also discussed above, increasing the number of defects [56]. The maximum defect densities were increased from $1.68 \times 10^{-12} cm^{-2}$ at PO_2= 0.83 mTorr to $3.6 \times 10^{-12} cm^{-2}$ at PO_2=1.88mTorr as shown in the table 4-1 in which S values were calculated from equation (10).



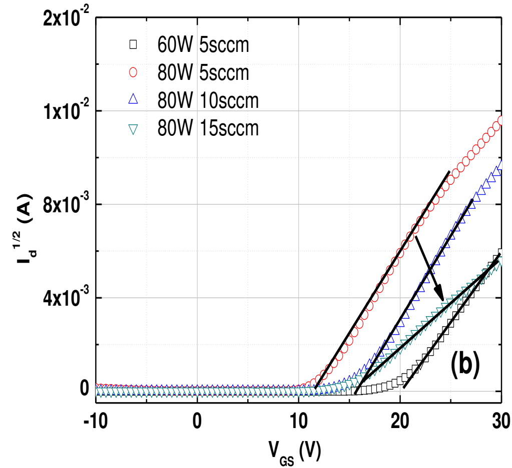


Fig.4-1. (a) Transfer characteristics of a-IGZO TFT with different oxygen partial pressure and rf power at V_{DS}=5.1V in the TFT dimension of W/L=70μm/6μm and (b) $I_{DS}^{1/2}$ vs. V_{GS} characteristics of a-IGZO TFT when biased in the saturation regime with V_{DS}=5.1V. The threshold voltage, V_T and saturation mobility, μ_n were extracted from this plot in which μ_n depends on the slope, $d(I_{DS})^{1/2}/dV_{GS}$.

Table 4-1 Summary of electrical characteristics of a-IGZO TFT different oxygen partial pressure and rf power at V_{DS}=5.1V in the TFT dimension of W/L=70μm/6μm.

	60W PO_2 = 0.83mTorr	80W PO_2 = 0.83mTorr	80W PO_2 = 1.66mTorr	80W PO_2 = 2.5mTorr
V_T (V)	19.5 ± 1.08	12.5 ± 0.14	16.0 ± 1.26	15.5 ± 0.21
μ_{FE} (cm^2/Vs)	2.7 ± 0.06	4.2 ± 0.28	4.4 ± 0.39	1.15 ± 0.07
S(decade/V)	0.59 ± 0.11	0.59 ± 0.06	1.18 ± 0.16	1.2 ± 0.04
N_t	1.68×10^{-12}	1.68×10^{-12}	3.5×10^{-12}	3.6×10^{-12}
I_{OFF} x10^{-12} (A)	2.96 ± 2.63	17.4 ± 0.92	21.0 ± 0.97	0.62 ± 0.28

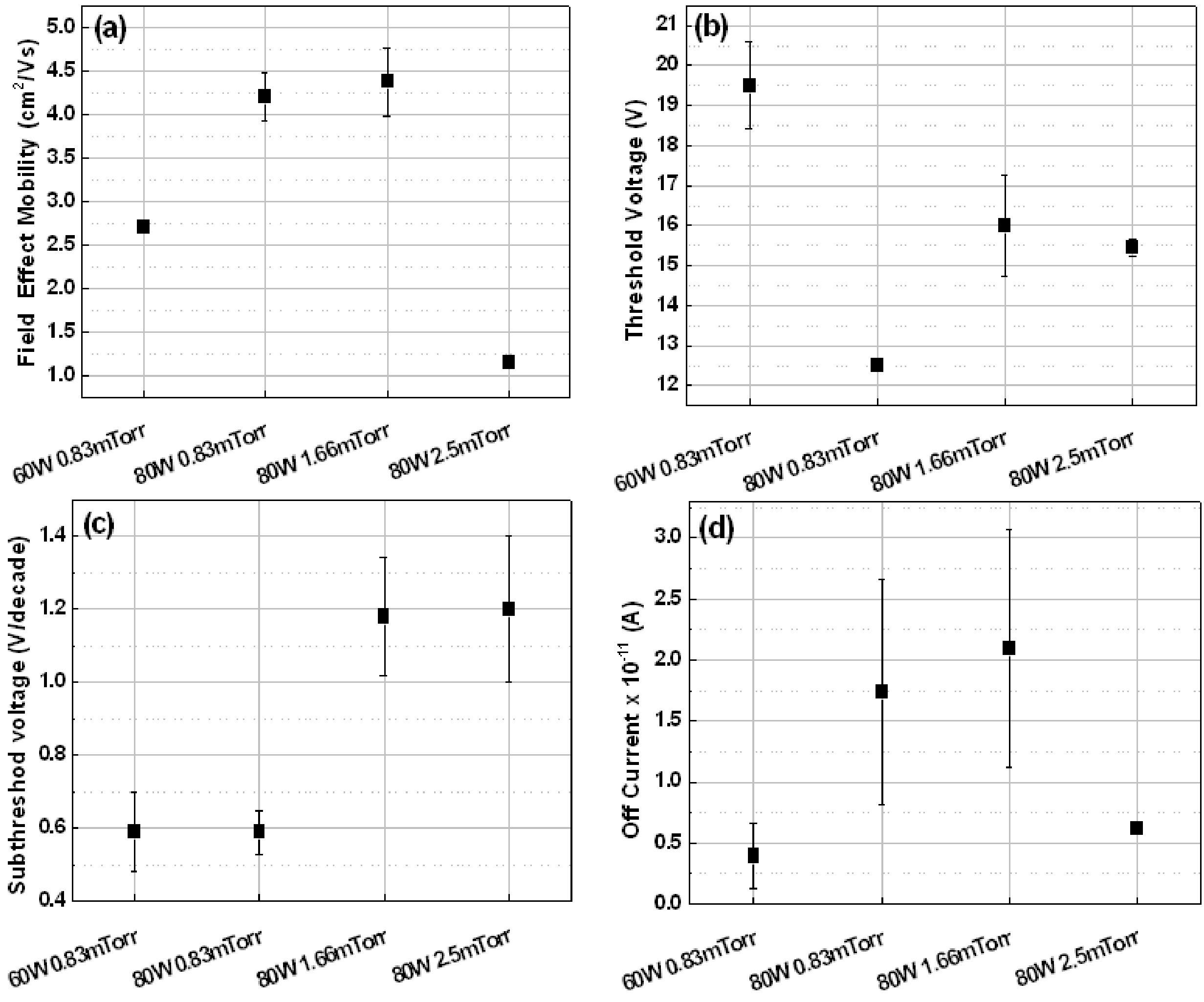
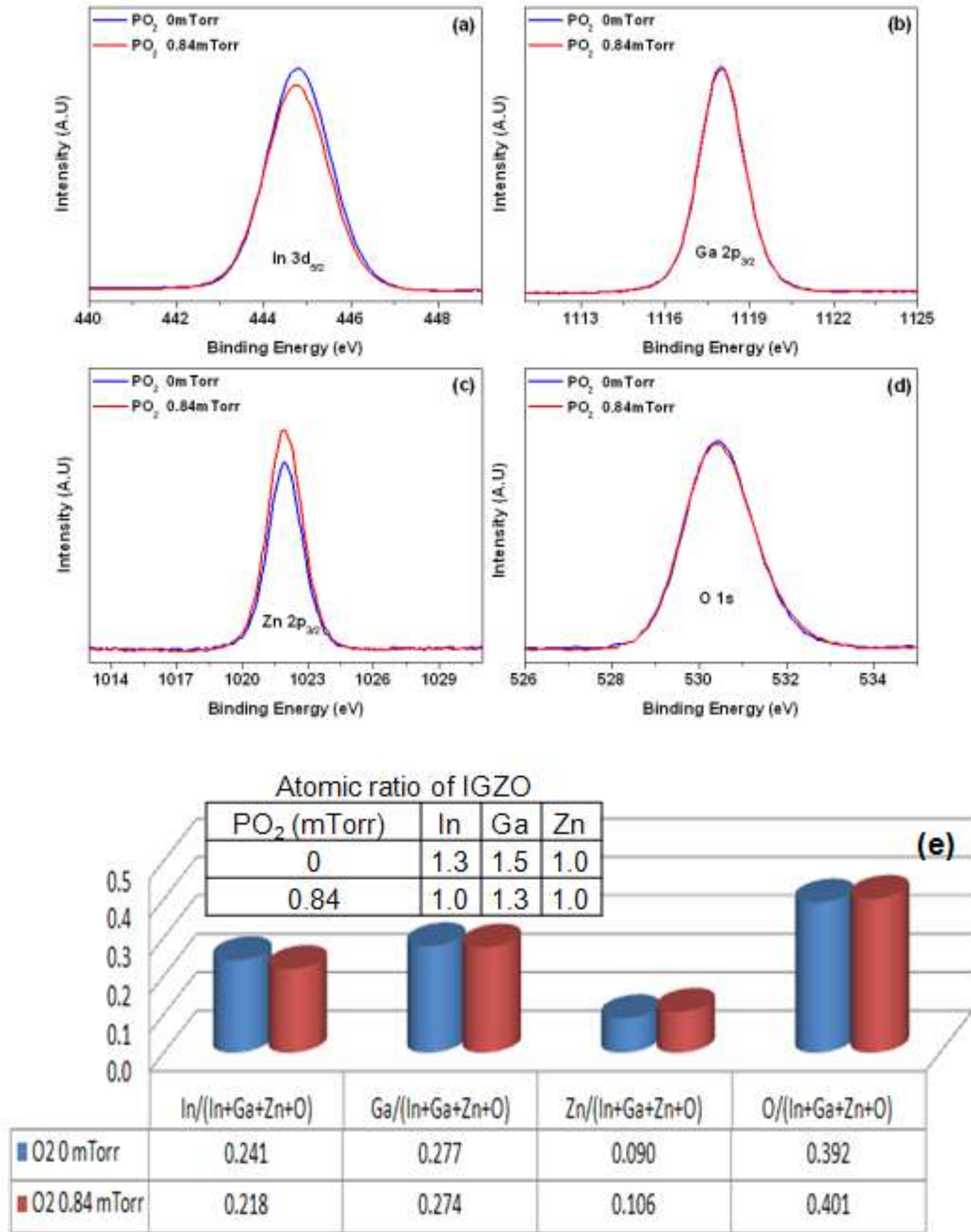


Fig. 4-2. Electrical characteristics of a-IGZO TFT with different oxygen partial pressure and rf power at V_{DS}=5.1V in the TFT dimension of W/L=70μm/6μm (a) for field effect mobility, (b) threshold voltage, (c) subthreshold gate swing, and (d) off current.

The control of oxygen deficiency by changing oxygen partial pressure during sputtering deposition is crucial to achieve the optimum properties of oxide semiconductor as discussed above, which implies that the oxygen supply influences the atomic-scale stabilization of the charge distribution. In this study, the atomic concentration ratios of the a-IGZO deposited as a function of PO_2 were investigated by X-ray photoelectron spectroscopy (XPS). Two representative a-IGZO samples were analyzed; a-IGZO film (50nm) deposited with PO_2 = 0 mTorr and a-IGZO film (50nm) with PO_2 = 0.84 mTorr. The measurement was performed in high vacuum pressure (~ 1 x 10^{-7} Torr) and to remove surface contaminants on the surface of a-IGZO, sputtering was performed for 5 min. Fig. 4-3 shows the core-level XPS spectra of two a-IGZO film (0 mTorr vs.0.84mTorr in PO_2). The different atom atomic concentration ratios were obtained from the area of spectra curves, which is normalized by total atom concentration for comparison with different oxygen pressure. Only core-level spectra were analyzed; In $3d_{5/2}$, Ga $2p_{3/2}$, Zn $2p_{3/2}$, and O 1s as shown Fig. 4-3 (a), (b), (c), and (d). Interestingly, the relative concentration of In/ (In+Ga+Zn+O) was decreased (-9.5%) and Zn/(In+Ga+Zn+O) and O/(In+Ga+Zn+O) were increased for +18.5% and + 2.4%, respectively as shown Fig. 4-3 (e). Likewise, as comparison of atomic ratio of In : Ga : Zn in the inset of Fig. 4-3 (e), the calculated atomic ratio In:Ga:Zn were changed from 1.3 : 1.5 :1 to 1 : 1.3 : 1 for PO_2=0mTorr and PO_2=0.84mTorr, respectively. The resulting atomic ratio at PO_2=0.84mTorr was consistent with the report which was studied by Kim *et al.* proposing In-Ga-Zn-O film with atomic ratio In:Ga:Zn ~ 1:1:1 demonstrated high structural stability [41]. These results are quite reasonable for a-IGZO material. As key components which dictate the electrical conductivity, In is known

to be conduction path in the a-IGZO and oxygen can control carrier concentration in a-IGZO as discussed in chapter 1. Therefore, the resulting electrical conductivity was decreased with increasing oxygen partial pressure. In this study, it was not observed that peak shift due to changing chemical bond.



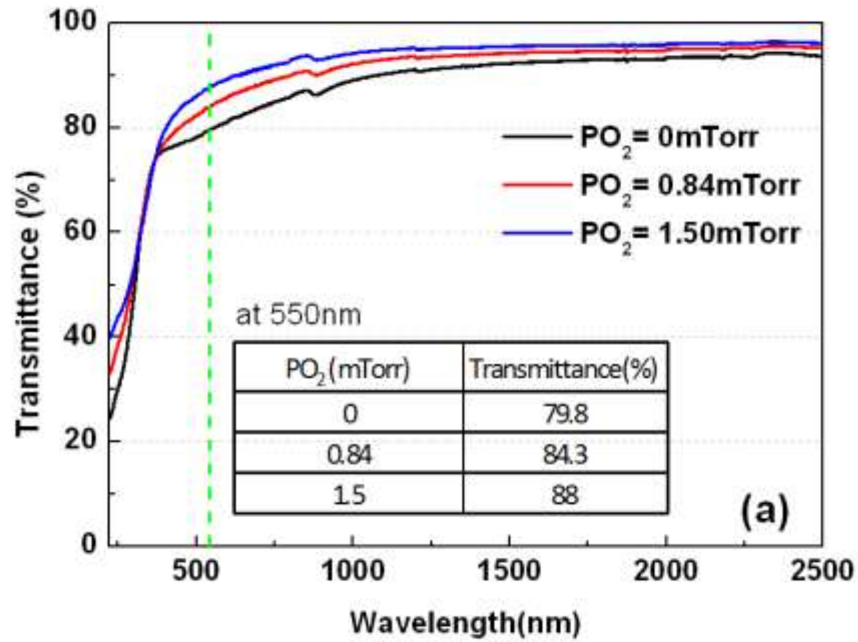
PO2 (mTorr)	In	Ga	Zn
0	1.3	1.5	1.0
0.84	1.0	1.3	1.0

	In/(In+Ga+Zn+O)	Ga/(In+Ga+Zn+O)	Zn/(In+Ga+Zn+O)	O/(In+Ga+Zn+O)
O2 0 mTorr	0.241	0.277	0.090	0.392
O2 0.84 mTorr	0.218	0.274	0.106	0.401

Fig. 4-3. Core-level XPS spectra of the a-IGZO films, (a),(b),(c), and (d) and the atomic concentration ratios obtained from the area of XPS spectra curves, (e) which is normalized by total atom concentration for comparison with oxygen pressure; PO_2 = 0 mTorr verse PO_2 = 0.84 mTorr.

Fig. 4-4 (a) shows the optical transmission spectra of a-IGZO films sputtered in different PO_2. The films are optically transparent in the entire visible and near-infrared region as shown Fig. 4-4 (a) (showing greater than 80%, excluding absorption associated with quartz (~ 5%)). The optical transmittance at 550nm wavelength is increased with increasing PO_2 as shown in the inset of Fig. 4-4(a). The peak wavelengths of the a-IGZO film deposited in a higher oxygen ambient (high PO_2) are shifted to shorter values in the UV range in comparison with those of the film deposited without oxygen (PO_2=0mTorr). However, the transmittances decrease by electron carrier absorption with different PO_2 did not occur in the IR range and even the film deposited with PO_2 = 0 mTorr (probably oxygen deficient film with relatively high electron carriers) was not decreased as well. The fact that the transmittance was unchanged with oxygen content in a-IGZO is likely to too thin a-IGZO film (50nm) to measure electron absorption behavior because adsorbed O_2 molecules on a-IGZO can undergo partial charge-transfer forming depletion a layer below the active surface, decreasing the effective electron carrier concentration in a-IGZO. This was demonstrated by depositing and measuring the transmittance of thicker a-IGZO film (200nm) to improve the sensitivity of electron absorption in IR range as shown Fig. 4-4 (b).Both transmittances (PO_2=0 mTorr and PO_2=0.84 mTorr) of a-IGZO (200 nm) were decreased in the IR range between 1400 nm and 2500nm in wavelength due to free carrier absorption. The transmittance of a-IGZO films deposited with the lower oxygen partial pressure shows transmittance which means a relatively high carrier concentration in the a-IGZO film. To investigate how the reflectance and the absorption affect to the transmittance of a-IGZO film, the reflectance was measured by Filmmetrics

Reflectometer and the absorption was extracted from the relationship: absorption =1 - transmittance - reflectance. Fig. 4-5 shows the plot of transmittance, reflectance, and absorption in the range of wave length from 220 nm to 880 nm (UV-VIS range) with different oxygen partial pressure. Interestingly, contrary to measured above, the transmittance strongly depends on the reflectance regardless of oxygen partial pressure in the visible range and all absorptions showed a very similar value without significant difference with oxygen partial pressure. It was confirmed that the higher reflectance of the film deposited at lower oxygen pressure is due to higher refractive index (n) of the film. The resulting n values for each film were 1.98, 1.87, and 1.85 for PO_2 = 0 mTorr, PO_2 = 0.84 mTorr, and PO_2 = 1.5 mTorr, respectively.



PO2(mTorr)	Transmittance(%)
0	79.8
0.84	84.3
1.5	88

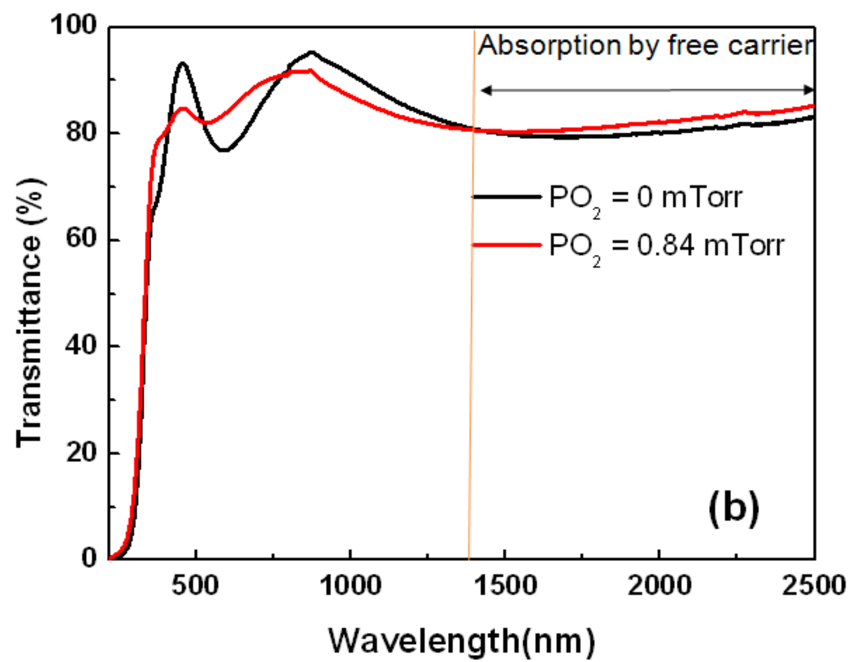


Fig. 4-4 (a) the optical transmission spectra of a-IGZO films sputtered in different PO_2 and (b) the decreased transmittance by free carrier absorption in IR range.

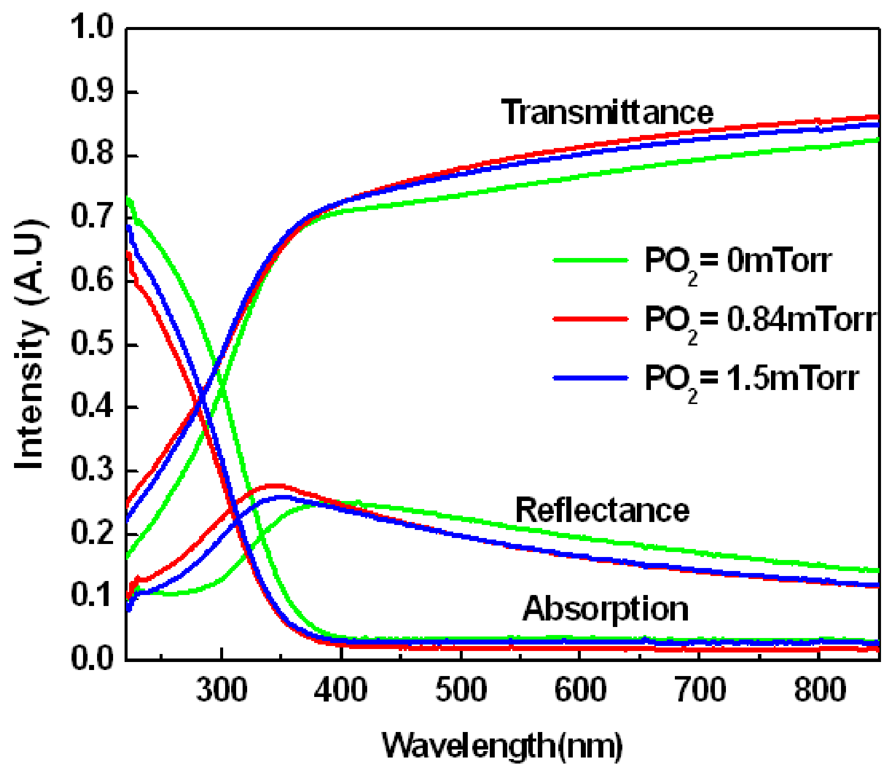


Fig. 4-5.The plot of transmittance, reflectance, and absorption in the range of wave length from 220 nm to 880 nm (UV-VIS range) with different oxygen partial pressure (PO_2=0 mTorr, PO_2=0.84 mTorr, and PO_2=1.5 mTorr).

It is known that the fundamental absorption in the electronic structure is because of electron excitation from valence band to conduction band from which the band gap can be extracted. Fig. 4-6 shows the relationship between $(\alpha h\nu)^2$ and $h\nu$. The estimated E_g (referred to as the Tauc gap) for the a-IGZO film is determined by graphical construction using the Tauc model [57] in the strong absorption region with following relationship, $(\alpha h\nu) \approx (h\nu - E_g)^n$, where h is the Plank constant and ν is the photon frequency and constant n is usually 2 for amorphous semiconductors and direct transition. The Tauc plot has a distinct linear region from which the extrapolation to the abscissa (x- axis) yields E_g of the material. In this study, the absorption coefficient (α) was mathematically calculated from the transmittance data by following relation $\alpha = (1/d) \ln(1/T)$, where d and T are the thickness and transmittance of film, respectively. As shown in Fig. 4-6, as the PO_2 increases from 0 mTorr to 1.5mTorr, E_g increases slightly from 3.21 eV to 3.51 eV. These observations indicate that the optical band gap of the a-IGZO film can be controlled by oxygen content during deposition process. The shifted band gap is presumably from reduced defect states in the band gap which act as photon absorption traps. Therefore effective optical band gap was slightly increased. As will be demonstrated in the chapter 4.3, because of the increased optical band gap (oxygen rich a-IGZO film), the a-IGZO TFT with PO_2=1.5mTorr was not operational as a function of V_{GS}.

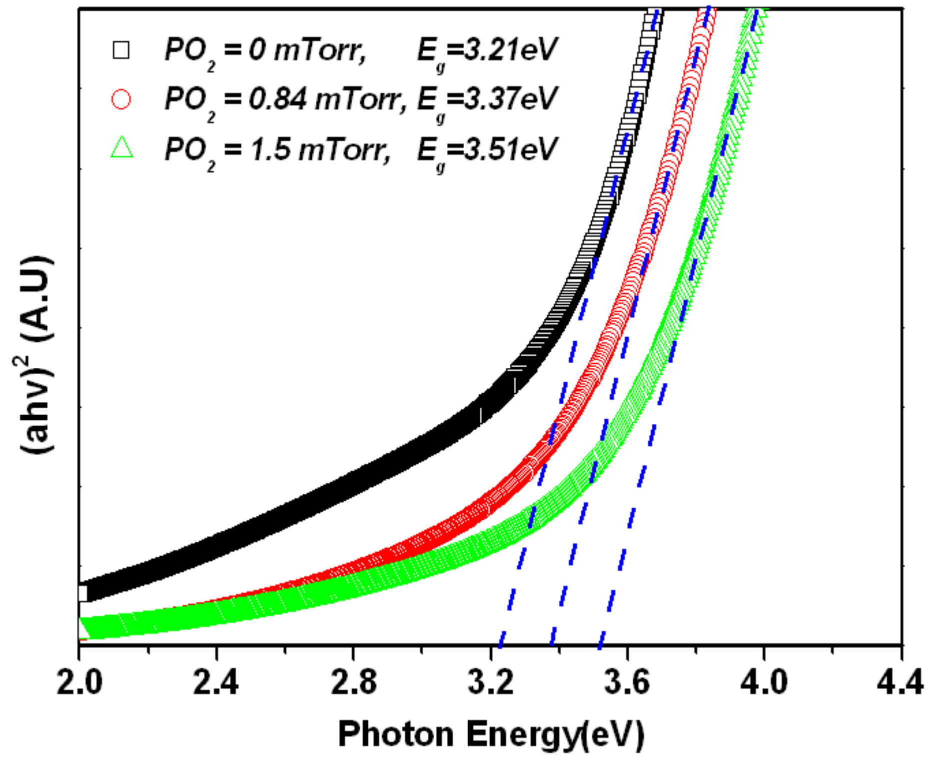


Fig. 4-6. Optical band gap with PO_2; optical band gap was increased from 3.21 eV to 3.51 eV for PO_2=0 mTorr and PO_2=1.5mTorr, respectively.

The evolution of a-IGZO structural properties as a function of the temperature and the different annealing ambient was investigated in order to study how this parameter affects to a-IGZO TFT. As demonstrated above and reported by many researchers, a variety of process factors can affects to TFT performance [55], [58]. The post annealing process is one of the parameters which can dictate the TFT properties because the process can generate or eliminates carriers in the a-IGZO channel and change the properties of TFT [59] . Based on the above TFT study with oxygen partial pressure, the TFT characteristics with different annealing ambient in N_2 and air were investigated because higher oxygen content and unintentional O2 exposure at high temperatures may affect the TFT performance. Fig. 4-7 shows the representative TFT transfer curves after an annealing ambient in N_2 and air at 350°C for 1hr and Fig. 4-8 compares the electrical characteristic for N_2 and air annealing ambient. The V_T (~12.5V) annealed in N_2 has lower (positive) value than the V_T (~18.5V) annealed in air (Fig. 4-8 (a)). However, in this study, the μ_{FE} could not be compared accurately because of the relatively high variation in air annealing results (Fig. 4-8 (b)). S (~0.59V/decade) and I_{OFF} (2.9 x 10^{-12}A) of TFT annealed in N_2 showed better electrical performance (0.98 V/decade and I_{OFF} (1.2 x 10^{-11}A) in air annealed, respectively). Overall the TFT annealed at N_2 ambient shows better electrical performance as well as reliability. These different electrical properties, especially the degraded TFT annealed in air, also seems to correlate with oxygen and unintentional contamination during annealing in air. Significant adsorbed oxygen on/near the surface of back channel results in the decrease of effective electron carrier density in the a-IGZO channel and therefore V_T

decreases. The S also is likely to be degraded because of unintentional contamination during annealing.

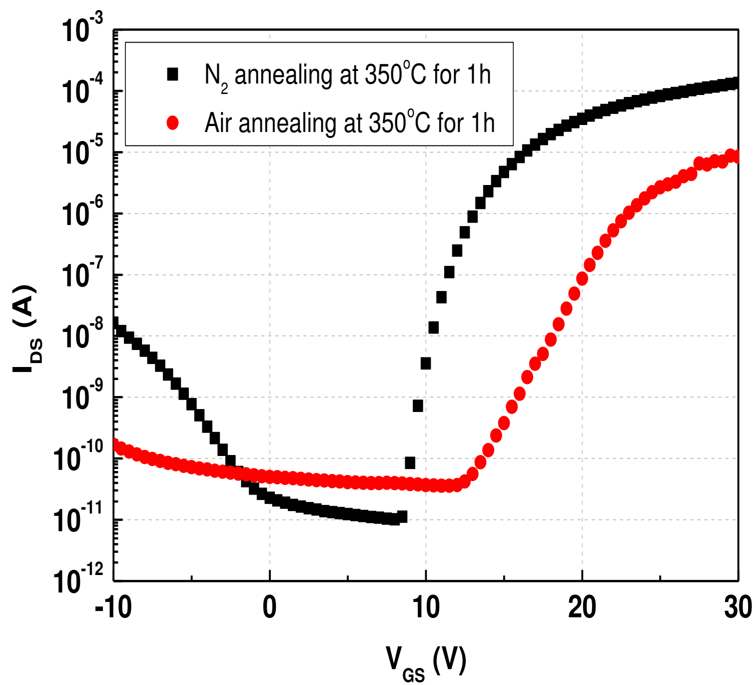


Fig. 4-7. The representative TFT transfer curves after annealing ambient in N_2 and air at 350°C for 1hr.

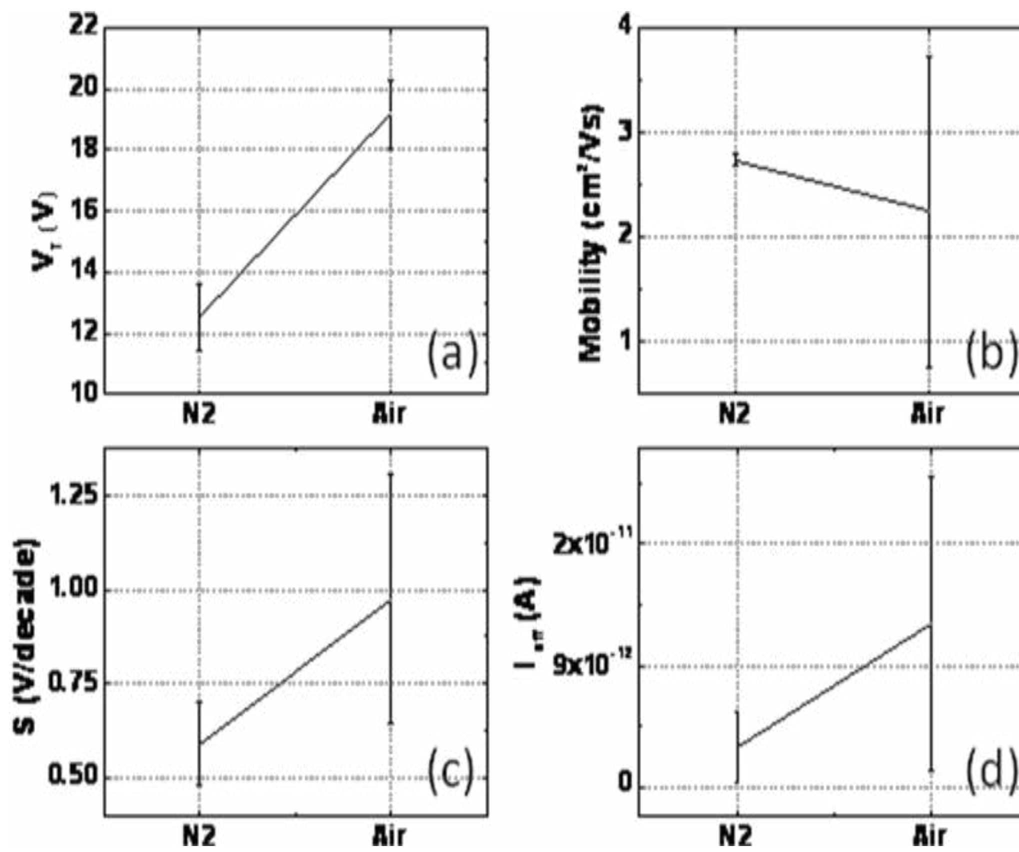


Fig. 4-8.The comparison of electrical characteristics annealed for N_2 verse air for 1hr.

Fig. 4-9 shows the diffraction patterns for a-IGZO films annealed at the different temperatures (room temperature, 250°C, 350°C, 500°C, 650°C, 850°C) for 1hr in N_2 ambient. The a-IGZO films (200 nm) were rf magnetron sputter deposited using a-IGZO target (In_2O_3 : Ga_2O_3 : ZnO = 1:1:1 mol %) with rf powers (60W) and PO_2= 0.84 mTorr. The thin film was measured by grazing angle incidence using Philip X'pert. Up to 650°C temperature, there were no significant structural changes, and the a-IGZO films have amorphous characteristics. For temperature around 850°C, an important structural change occurs, demonstrating crystallization of IGZO. The resulting crystalline temperature was higher than previously reported (~ 520°C) [60]. According to Cho *et al.*, the crystallization temperature is correlated to Zn content in the a-IGZO film and the a-IGZO film does not undergo crystallization if Zn is volatilized during the anneal. They proposed that the presence of Zn in the a-IGZO film destabilizes the octahedral or tetrahedral coordination of the neighboring Ga ions, resulting in the bipyramidal coordination of both Ga and Zn atoms and they confirmed that high temperature annealing process (> 800°C) in an N_2 causes Zn volatilization. Therefore, the resultant crystallization of the a-IGZO film can be obtained [61].

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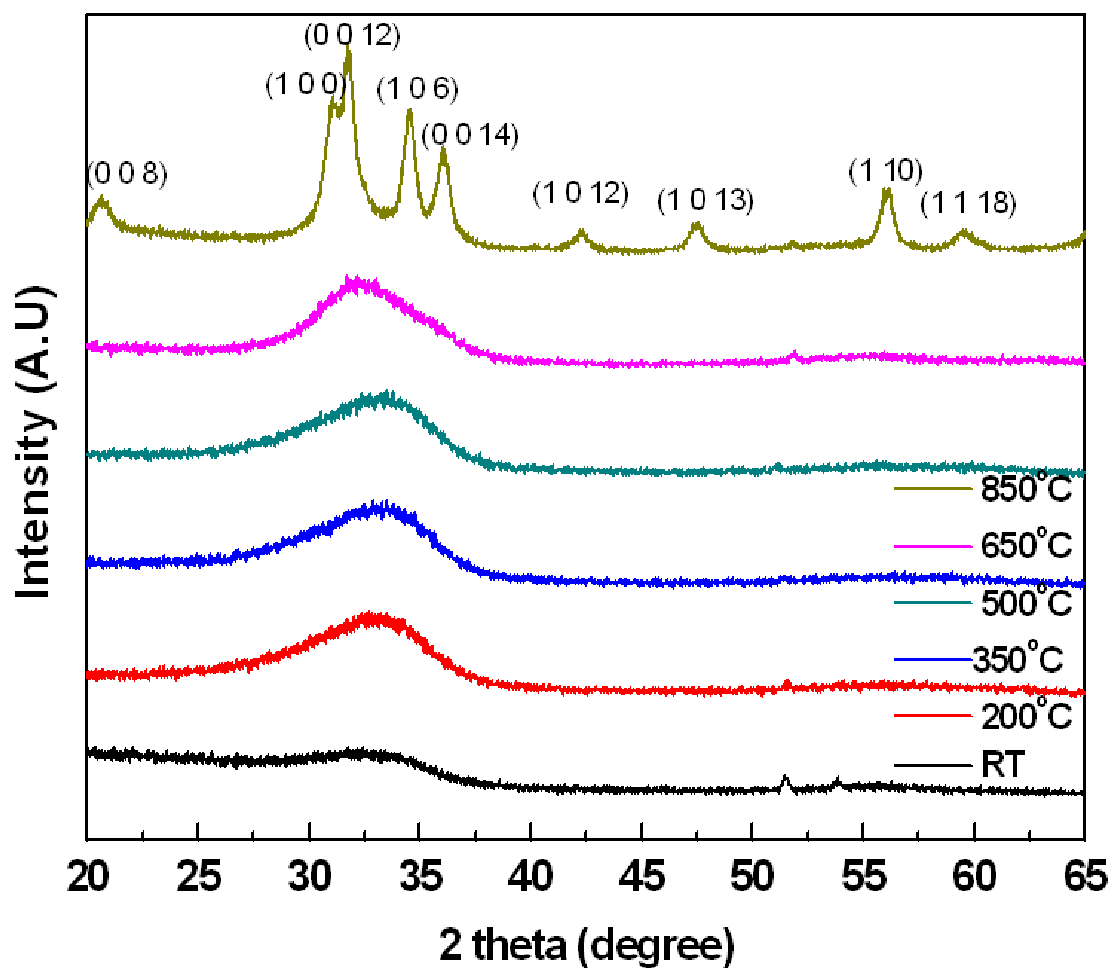


Fig. 4-9. X-ray diffraction analysis as a function of the annealing temperature in N_2 for a-IGZO film.

4.1.4 Conclusion

a-IGZO films deposited at different powers (60W verse 80W) in this study, revealed that there was only difference in the V_T which is attributed to the increased In content. For increasing PO_2, V_T was increased but the negative ions during sputtering with high oxygen pressure caused the traps in a-IGZO to be increased, resulting in an increase of the relative S value. From this study, the power of 60W and 80W with PO_2 = 0.84mTorr were proposed for optimized sputtering condition for a-IGZO TFTs. For increasing PO_2, it was confirmed that the relative In content in a-IGZO was decreased and oxygen content in a-IGZO was increased by analyzing XPS and in addition, the increased optical band gap was also confirmed with increasing PO_2. By comparing the transmittance in the range of IR, the relative free carrier density in a-IGZO was compared (a-IGZO film deposited with higher PO_2 shows lower carrier concentration; higher transmittance). The annealing of a-IGZO in N_2 shows better electrical performance than in air. The crystallization of a-IGZO occurred at 850°C because of Zn volatilization.

4.2 Quantitative calculation of oxygen incorporation in sputtered IGZO films and the impact on the electron transport and TFT properties

4.2.1 Introduction

To study a-IGZO properties, in contrary to qualitatively described in chapter 3.2, this study demonstrates the quantitative calculation of oxygen incorporation in sputtered IGZO films. Many groups have studied a-IGZO active layers by changing the sputtering parameters such as oxygen partial pressure (PO_2) and sputtering power for high performance TFTs [62], [63], [55]. It is particularly important to control the oxygen content in oxide semiconductors because oxygen vacancies contribute to the carrier concentration in the film, showing exponentially changing resistivity over more than ten orders of magnitude as demonstrated for ZnO [64]. In addition, recently, Min *et. al* showed that the Fermi level (E_F) in the band gap of ZnO can be controlled by varying the oxygen vacancy concentration by varying the PO_2 in ZnO [65]. Conventionally, investigating TFTs with optimum a-IGZO semiconducting properties requires studying the sputtering parameters such as PO_2 and sputtering power in order to optimize each parameter for the specific deposition system. In this work, the molecular flux ratio of sputtered IGZO and oxygen molecules is quantitatively calculated and the characteristics of a-IGZO TFTs grown with different O_2/IGZO ratios are compared. We thus elucidate how the electrical a-IGZO properties depend on the incorporation of oxygen from the sputtered IGZO target and the reactive O_2 molecules from the mixed Ar-O_2 processing gas. Finally, we demonstrate that the resistivity varies almost 7 orders of magnitude with different O_2/IGZO which is correlated to the change in the Fermi

energy level (E_F) relative to the conduction band minimum. From this, a robust method to estimate the optimum semiconducting layer for TFT fabrication is proposed.

4.2.2 Experimental

TFT fabrication processes are same to chapter 3.2. The a-IGZO active layer (50nm) was rf magnetron sputter deposited using an a-IGZO target (In_2O_3 : Ga_2O_3 : ZnO = 1:1:1 mol%) with different $O_2/(O_2+Ar)$ gas mixing ratio at fixed total gas flow rate (25 sccm) during sputtering. The electrical characteristics of a-IGZO TFTs were tested using an HP 4156A device parameter analyzer with a channel width of 70 μm and a channel length of 22 μm. Additionally, in order to elucidate the relationship between oxygen and sputtered IGZO fluxes and transfer characteristics of TFT, the a-IGZO resistivity was measured after annealing at 350°C as a function of PO_2 (flux).

4.2.3 Results and discussion

Fig. 4-10 shows representative transfer curves of the a-IGZO TFTs at V_{DS}=5.1V with different PO_2. For PO_2 = 0.85 mTorr, μ_{FE}, V_T, and S were 6.3 cm^2/Vs, 10.8 V, and 0.39 V/decade, respectively. Noticeably, the V_T was increased from 10.8 V to 16.5 V with increasing from PO_2 = 0.85 mTorr to PO_2=1 mTorr but μ_{FE} was slightly decreased and S was increased (see the table 4-2). TFTs with PO_2= 0.24 mTorr have high conductive channels even with highly negatively biased V_{GS}, showing more than 30μA

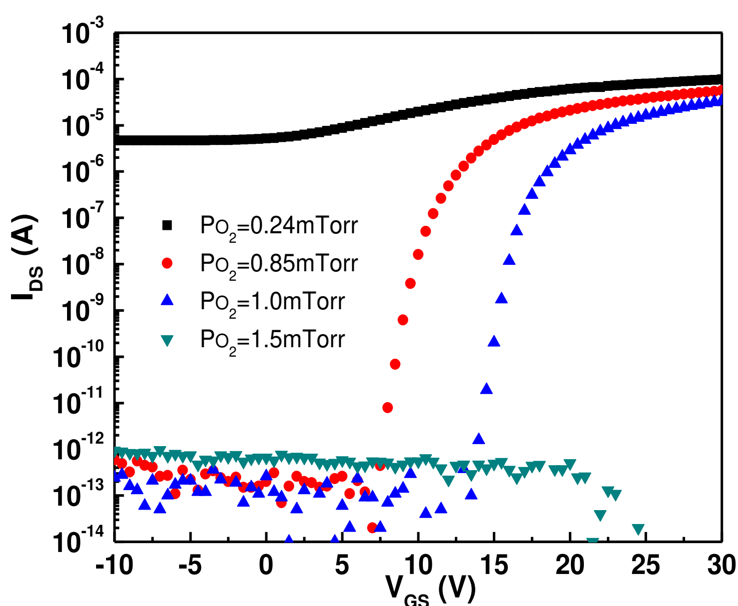


Fig. 4-10. The TFT transfer curve at V_{DS} = 5.1V with different oxygen partial pressure.

Table 4-2 Electrical properties (μ_{FE}, S, V_T, and I_{off}/I_{off}) of a-IGZO TFTs with oxygen partial pressure (PO_2) and deposition rate.

PO_2 (mTorr)	Deposition rate (nm/min)	μ_{FE} (cm^2/Vs)	S (V/decade)	V_T (V)	I_{on}/I_{off}
0.24	0.857	-	-	-	1.9×10^{1}
0.85	0.448	6.4± 0.6	0.39± 0.06	10.9± 1.2	7.4×10^{7}
1.0	0.398	5.4±0.8	0.44± 0.07	16.5± 1.3	1.3×10^{8}
1.5	0.321	-	-	-	-

in the whole range of V_{GS}. On the other hand, TFTs with PO_2= 1.5 mTorr could not be modulated by V_{GS}, suggesting the channels were too resistive.These interesting electrical characteristics with varying PO_2 are known to be dependent on oxygen vacancies as the carriers in the as-deposited a-IGZO material; high oxygen vacancy concentrations in a-IGZO cause the a-IGZO channel to be conductive and very low (near stoichiometry) oxygen vacancies cause the a-IGZO to be too insulating [55], [66]. To investigate whether surface roughness of a-IGZO can affect to TFT characteristics such as μ_{FE}, V_T, and S, the surface roughness of a-IGZO using atomic force microscopy (AFM) was measured as shown Fig. 4-11. It is known that the high surface roughness of the semiconductor causes electrical performance to be degraded due to the following reasons: 1) electron carrier scattering at the channel interface between semiconductor channel and gate dielectric, 2) increased interface trap site between semiconductor channel and gate dielectric, and 3) especially for a-IGZO back channel, larger effective oxygen absorption area, which possibly decreases the electron carrier concentration in a-IGZO due to a depletion effect [41]. The surface roughness was significantly decreased from RMS 2.261nm to RMS 0.558nm with increasing PO_2 = 0 mTorr to PO_2=0.85 mTorr, respectively, however there were no significant difference between PO_2=0.85 mTorr (RMS 0.558nm) and PO_2 = 1.0 mTorr (RMS 0.562nm); it seems that surface roughness of a-IGZO film does not change higher PO_2. The rougher surface of PO_2 = 0 mTorr is likely due to the relatively high deposition rate (1.17 nm/min) than others (0.45 nm/min for PO_2=0.85mTorr and 0.40 nm/min for PO_2=1.0mtorr) during a-IGZO sputtering. Therefore, in this study, the surface roughness effect on the electrical TFT performance was ignored.

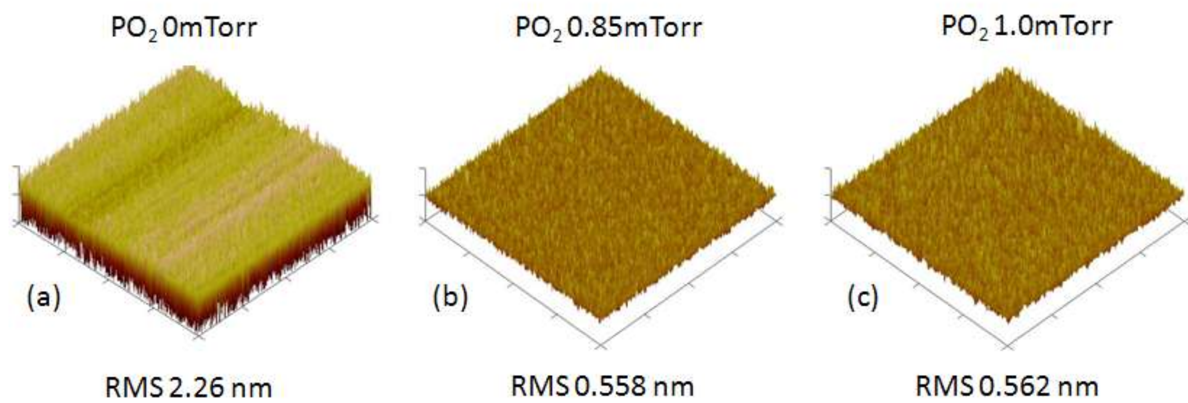


Fig. 4-11. The surface roughness of a-IGZO with different oxygen partial pressure, (a) 0mTorr, (b) 0.85mTorr, and (c) 1mTorr.

The observed electrical results were interpreted in terms of the simultaneous quantitative incorporation rate of sputtered IGZO molecules (more specifically metallic-like IGZO molecules that are oxygen deficient) and the incorporation rate of O_2 molecules on growing IGZO film, and compared with the intrinsic sheet resistance with different PO_2. Fig. 4-12 shows the plot of the incorporation rate of IGZO and oxygen molecules as function of PO_2 in the ambient during sputtering. The estimated IGZO incorporation rate in deposited IGZO can be quantitatively calculated from the sputtering deposition rate (with an assumed sticking coefficient of unity), and the incorporation of O_2 molecules is associated with PO_2 and the sticking coefficient of O_2 on the surface of the growing IGZO film. The IGZO flux (Φ_{IGZO}) on the growing film can be estimated as follows:

$$\Phi_{IGZO} = g_{IGZO} \frac{\rho_{IGZO} N_A}{M_{IGZO}} (molecules \cdot cm^{-2} \cdot \sec^{-1}), \tag{4.3.1}$$

where g_{IGZO} and ρ_{IGZO} are the deposition rate of IGZO (nm/min) and the density of a-IGZO (~5.9 g/cm^3), respectively [53]. N_A is Avogadro constant (6.02×10^{23} mol^{-1}) and M_{IGZO} is the molecular weight of IGZO (546.5 g/mol). As will be demonstrated, the sputtered IGZO is clearly oxygen deficient, however stoichiometric values for density and molecular weight were assumed. Because the IGZO sticking coefficient is assumed to be unity thus the effective incorporation rate of the IGZO is equal to the IGZO flux. The incorporation of O_2 (Φ_{IGZO}) is associated with oxygen gas flux on the growing surface as given by the kinetic theory of gas:

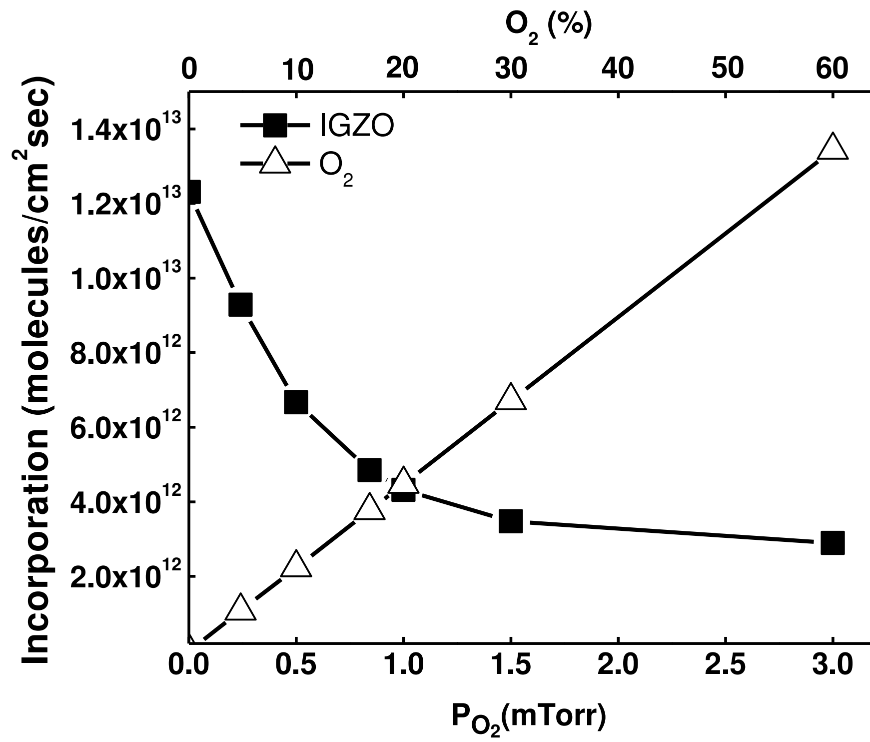
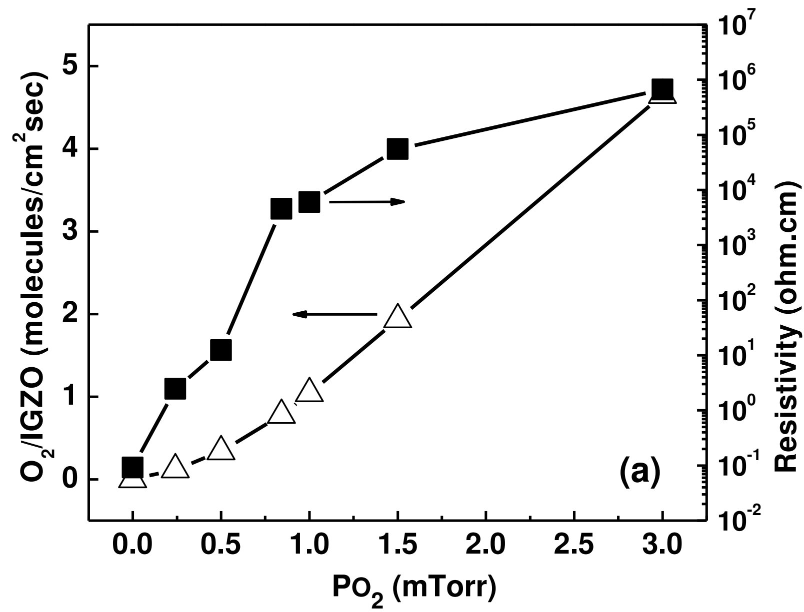


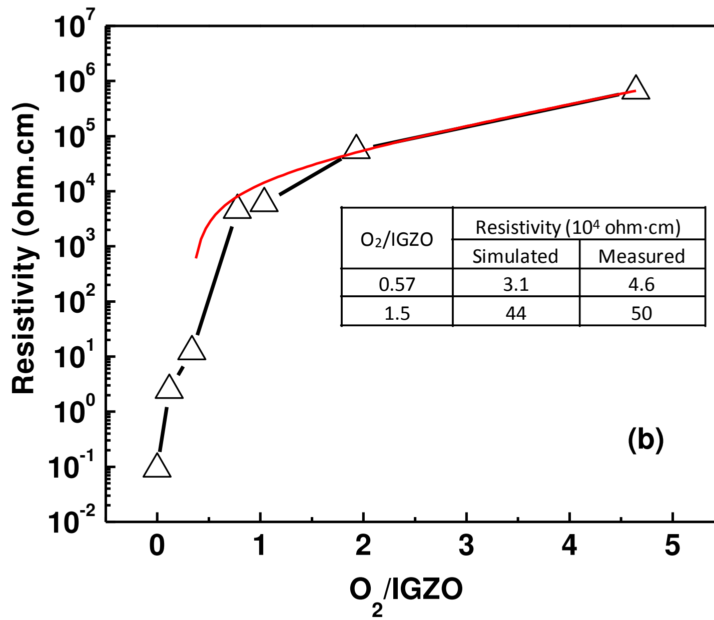
Fig. 4-12. Molecules incorporation of IGZO and O_2 with oxygen partial pressure in growing IGZO film during sputtering.

$$\Phi_{O_2} = \frac{P_{O_2}}{\left(2\pi M_{O_2} kT\right)^{\frac{1}{2}}} (molecules \cdot cm^{-2} \cdot \sec^{-1}) \quad (4.3.2)$$

where M_{O2} is molecular weight of O_2 (32 g/mol), k is Boltzmann constant, and T is absolute temperature during sputtering (assumed to be 298 K). The incorporation rate of O_2 is simply given by the product of the gas flux (Φ_{O2}) and the sticking coefficient (S_{O2}) of oxygen (Φ_{O2} x S_{O2}) on the growing IGZO film. To approximate the incorporation rate of oxygen, we have used S_{O2} (~ 1.25 x 10^{-5}) which is the value for chemisorption of O_2 on ZnO (1000) [67] via a charge transfer reaction with surface point defects in the film in which the oxygen absorption therefore depends on the density of surface point defects; for the ZnO (1000) surface, the surface point defects planar density was estimated to be ~ 2.3 x 10^{13} cm^{-2} [67].

From equation (4.3.1) and (4.3.2), Fig. 4-12 demonstrates that the effective oxygen incorporation rate is linearly increased and IGZO incorporation rate associated with the a-IGZO deposition rate is nonlinearly decreased with increasing PO_2. The decrease in the IGZO sputtering likely comes from enhanced oxidation of the IGZO target surface which effectively lowers the sputter yield [68] and/or decreased sputter yield from oxygen ions versus argon ions. Interestingly, in the region where the effective oxygen incorporation rate is equal to the IGZO incorporation rate (near PO_2= 1 mTorr), our TFTs demonstrate the best performance (see Fig. 4-10).





O_2/IGZO	Resistivity (10^4 ohm·cm)	
	Simulated	Measured
0.57	3.1	4.6
1.5	44	50

Fig. 4-13. (a) IGZO resistivity and O_2/IGZO incorporation ratio as function of oxygen partial pressure and (b) IGZO resistivity with O_2/IGZO incorporation ratio.

In order to better understand how the relative incorporation rates of a-IGZO and O_2 affect the electrical properties, Fig. 4-13 (a) plots the ratio of O_2/IGZO incorporation (left y-axis) and the measured resistivity of the a-IGZO as a function of the PO_2. The resistivity of the films was measured using van der Pauw structures[31]. Overall, the resistivity exponentially increases at different rates depending on O_2/IGZO incorporation ratio as shown Fig. 4-13 (a) and (b). At low PO_2 (O_2/IGZO ≤ 1; PO_2 ≤ 1 mTorr), the resistivity was less than ~ 6.0×10^3 Ω·cm and the increase with increasing PO_2 is almost 7 orders of magnitude. This resistivity behavior as a function of the oxygen incorporation ratio can be understood with the degenerate conduction and percolation conduction model proposed by Nomura [8] *et. al*. Moreover, recently it was reported that the oxygen vacancy concentration and the Fermi energy level position in the band gap of ZnO thin films was correlated to PO_2 [65]. Similarly, the a-IGZO film with O_2/IGZO ≤ 1 likely follows both partially degenerate and thermally activated carriers such that E_F is located above or near the edge of conduction band (E_C) which results in an exponential change with O_2/IGZO as demonstrated previously[65], [8]. To investigate the electrical conduction mechanism of a-IGZO with E_F related to O_2/IGZO incorporation, the electrical conductivity verse O_2/IGZO incorporation ratio was plotted as shown Fig. 4-14. Assuming that the band gap and electron carrier mobility (μ_n) are constant, electrical conductivity (σ) can be approximately written as $\sigma \approx q\mu_n n = q\mu_n\, exp[-(E_C - E_F)/kT]]$ where q is magnitude of electron charge (1.6×10^{-19} C) and here, u_n is assumed to be constant value of ~ 11 cm^2/Vs (actually, μ_n is decreased with increasing O_2/IGZO ratio

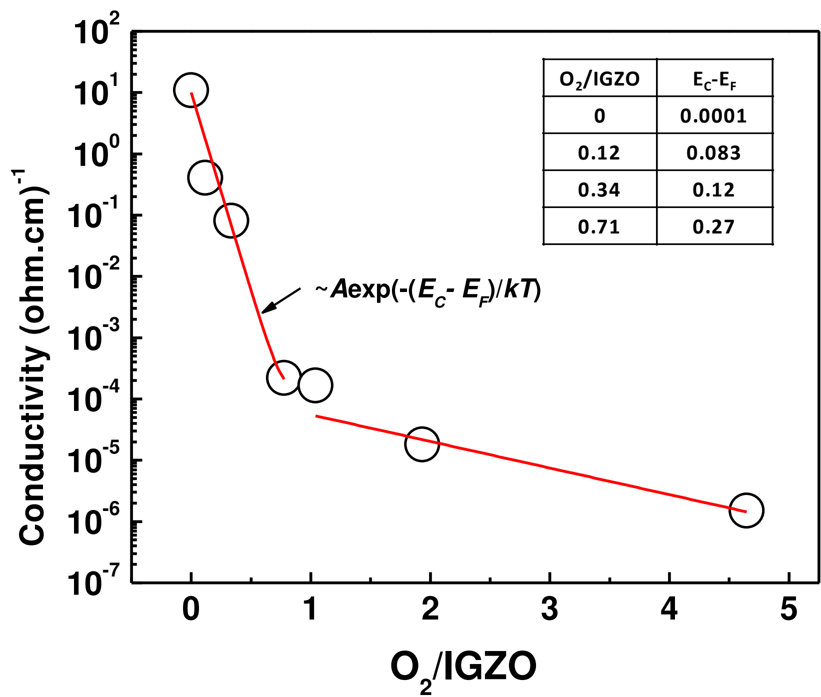


Fig. 4-14. Electrical conductivity with O_2/IGZO incorporation ratio and E_C - E_F with O_2/IGZO incorporation (inset table).

because of decreasing carrier concentration). In this study, the $E_C - E_F$ values based σ versus O_2/IGZO were roughly estimated as shown in the Fig. 4 and the inset table of Fig. 4-14. (Here, $E_C - E_F$ values for O_2/IGZO>1 is not estimated because of μ_n is not likely constant in this range.) Interestingly, the calculated values of $E_C - E_F$ showed negative values and the absolute values decreased with O_2/IGZO incorporation ratio; thus apparently E_F is above E_C and decreases towards E_C with increasing O_2/IGZO incorporation ratio, which demonstrates clearly degenerate conduction with O_2/IGZO ≤1 (higher carrier concentration) as reported in previous studies [8],[30]. However, for O_2/IGZO > 1(PO_2 >1.5mTorr), the slope of conductivity is noticeably changed, as is the TFT transfer curve as shown Fig. 4-10, which did not reveal turn-on characteristics. It is believed that the film becomes close to stoichiometry and percolation conduction mechanism rather than degenerate conduction becomes operative and thus has much lower conductivity[64]. In addition, Nomura *et. al* proposed the existence of a threshold energy (E_{TH}) which separates the conduction mechanism from degenerate ($E_{TH} < E_F$) to percolation conduction ($E_{TH} > E_F$) as function of the density of state($D(E)$) around the conduction band edge. This transition is associated with the transition between metallic/semiconductive behavior and more insulating behavior. In this study, we postulate the transition from degenerate to percolation conduction mechanisms occurs at an incorporation ratio of O_2/IGZO ≈ 1.

Based on these flux calculations and electrical conduction mechanisms in this study, metallic a-IGZO was estimated for O_2/IGZO << 1 and a-IGZO film with O_2/IGZO ~ 1 (PO_2 = 0.85 ~ 1.0 mTorr) was expected to be best deposition condition of a-IGZO for

TFT fabrication. Conversely, the TFT with O_2/IGZO > 1 (PO_2 >1.5 mTorr) does not show the transfer curve because there are too few carriers due to the low oxygen vacancy concentration in the IGZO film. The fact that the transfer curves behave as they do in Fig. 4-10 supports the proposed hypothesis. Therefore, the proposed method for equilibrating the sputtered and oxygen flux can be useful to determine the optimum sputtering conditions and even estimating the resistivity of oxide semiconductors for TFT fabrication. To confirm that the resistivity versus O_2/IGZO ratio can be used as a more universal curve, two samples were run at 80W sputtering power (increased IGZO flux) at two arbitrary oxygen partial pressures of 1.0mTorr and 1.7mTorr. The incorporation ratio (O_2/IGZO) was calculated based on equations (1) and (2) which resulted in: 1mTorr -- O_2/IGZO = 0.57 (O_2 = 7.84×10^{12} molecules/cm^{2}sec/ IGZO = 4.48×10^{12} molecules/cm^{2}sec), and 1.7mTorr -- O_2/IGZO = 1.5 (O_2 = 7.97×10^{12} molecules/cm^{2}sec / IGZO = 5.33×10^{12} molecules/cm^{2}sec), respectively. The measured resistivity for each ratio at O_2/IGZO 0.57 and 1.5 showed reasonably close values to the curve fit values from IGZO film sputtered with 60W power as shown in the inset of Fig. 3 (b). Accordingly, it is proposed that O_2/IGZO incorporation ratio calculated during IGZO sputtering can be effectively used for finding optimized semiconductor layer for TFTs.

4.2.4 Conclusion

In summary, this study showed a powerful method for estimating the electrical properties and optimizing the deposition condition of a-IGZO as a function of the oxygen to IGZO incorporation ratio. The IGZO and O_2 flux during sputtering was calculated on the basis of the deposition rate of IGZO and PO_2, respectively. The transfer curves

showed noticeably different results, depending on PO_2 (O_2/IGZO incorporation ratio); the TFT with PO_2 =0.85~1 mTorr (oxygen deficient regime with ~ 1 of O_2/IGZO) revealed the best transfer curve. However, the TFT with PO_2 > 1.5mTorr (the oxygen-rich regime with 1 < O_2/IGZO) did not show transfer curve. The electrical conductivity of a-IGZO for O_2/IGZO < 1 follows the degenerate conduction model, which depends on the $E_C - E_F$ with oxygen content in a-IGZO. On the other hand, for a-IGZO with 1 > O_2/IGZO, the change in the conductivity versus O_2/IGZO suggests a shift in the conduction mechanism in which we attribute to the percolation conduction model because of the reduced density of states; very few oxygen vacancies exist in the a-IGZO films. The resistivity curve with O_2/IGZO incorporation ratio can be used for the tool to estimate IGZO sputtering conditions for optimum TFT performance.

4.3 The device characteristics of a-IGZO TFTs sputter deposited with different substrate biases

4.3.1 Introduction

A negative DC electric field can be applied to bias the substrate in order to vary the flux and energy of charged species in the plasma during sputtering. With target voltages ranging from – 100V to – 300V, bias voltages of –50 V to – 300V are typically used. This bias sputtering technique has been used to modify a broad range of properties in deposited films, including improved film adhesion during initial stages of film formation; substantial improvement in step coverage; increased film density; significant reduction in resistivity of metal films; change in film hardness and residual stress; enhanced optical reflectivity; change in electrical properties of dielectric film [69]. The bias can control the gas content of film which is proportional to V_b^2, where V_b is the bias voltage [70] and the gases adsorbed on growing film on which physically adsorbed and even strongly chemisorbed species can be resputtered by ion bombardment induced by a DC bias. In addition, the energetic ion bombardment can remove contaminants, change surface chemistry, enhances nucleation, and increase surface mobility of adatoms by increased temperature, which accelerates atomic reaction and interdiffusion rates. Previously, we already demonstrate the effect of DC substrate bias as growing amorphous silicon in which the defects induced by applying bias can enhance the crystallization rate by created defects as nucleation sites as well as we reported the electrical and physical properties with different materials such as amorphous silicon, silicon dioxide, and even molybdenum, comparing the electrical

characteristics of [34], [71-74]. In this study, we study the physical and electrical properties of a-IGZO films and also will investigate the transfer characteristics of a-IGZO TFT with different substrate biases.

4.3.2 Experimental

To study a-IGZO TFTs with different substrate biases, the applied substrate biases were changed from 0V (0W), 50V (~0.5W), 100V (1W), 130V (5W), and 150V (10W) during a-IGZO sputtering. After active layer deposition, Cr (200 nm) source and drain electrodes were also sputter deposited and lithographically patterned via wet etching. In order to contact gate electrodes, via hole etching was performed by a combined wet etch using diluted HF etchant and dry etching process using a SF_6 + Ar gas chemistry. Finally, the samples were annealed at 350°C for 1hr in nitrogen ambient. Fig. 4.15 shows a schematic and SEM micrographs of the fabricated device structure of a-IGZO TFTs, which has an inverted staggered bottom gate structure. The electrical characteristics of a-IGZO TFTs were tested using an HP 4145A device parameter analyzer at room temperature measured on devices with a channel width of 70 μm and a channel length of 6 μm. To characterize the different biased a-IGZO films, Hall measurement (Ecopia HMS-3000) were performed to measure the carrier mobility and concentration, and atomic force microscopy (AFM) was used to measure the film roughness. The index of refraction data was determined via ellipsometry and the thin

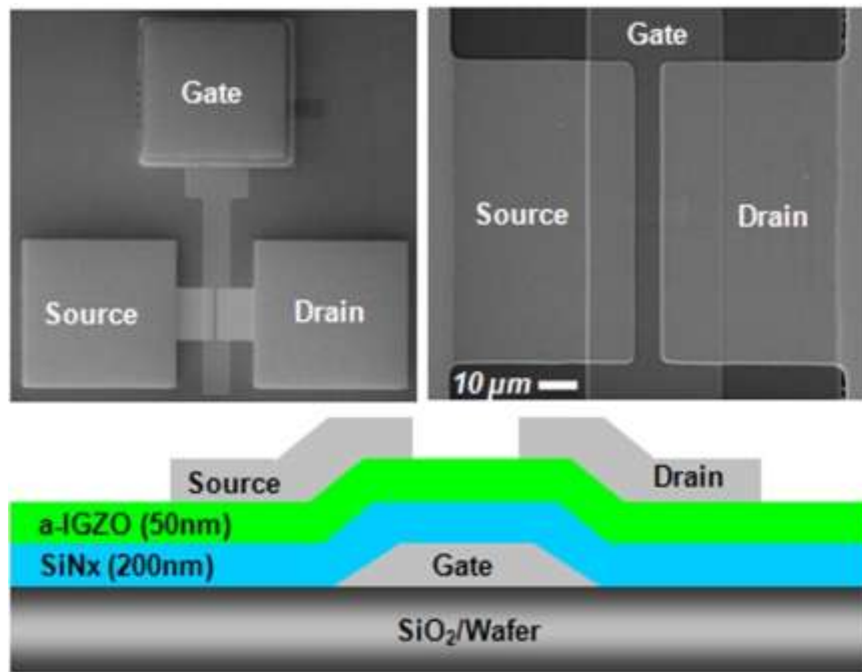


Fig. 4-15. A schematic and SEM micrographs of the fabricated device structure of a-IGZO TFTs with an inverted staggered bottom gate structure.

film stress was determined by measuring the change in the substrate curvature after the a-IGZO deposition.

4.3.3 Results and discussion

Fig.4-16 shows the results of transfer and output characteristics of a-IGZO TFTs with zero and 150V DC biased substrate voltages during a-IGZO sputtering. A summary of the properties from the a-IGZO TFTs are tabulated in the Table 4-3.The V_T value significantly decreased and eventually became negative as the substrate bias increased. The μ_{FE} value was slightly increased with substrate bias from 7 cm^2/Vs for the unbiased a-IGZO device to 10 cm^2/Vs for the 150 V substrate biased device. In addition to mobility, interestingly, the I_{off} value also linearly increased with applied substrate bias during a-IGZO sputtering.

To understand the effects that bias sputtering on the a-IGZO and subsequently the device characteristics, Hall measurements were performed. Fig. 4-17 shows the electrical properties of a-IGZO film [Fig. 4-17 (a)] and a-IGZO TFTs [Fig. 4-17(b)] with different substrate bias. The carrier concentration of a-IGZO increased linearly with substrate bias. Both the Hall and field effect mobility increased proportionally with the increased carrier concentration (the results at 0 V in Fig 4-17(a) are questionable as the results are at the lower limit of the Hall measurement system). The correlation of the carrier density and the field effect mobility is clear. This result is consistent with Park *et al.* who described the effect of Ar plasma treatment on a-IGZO film. The preferential sputtering of oxygen during Ar ion bombardment causes a-IGZO to become oxygen

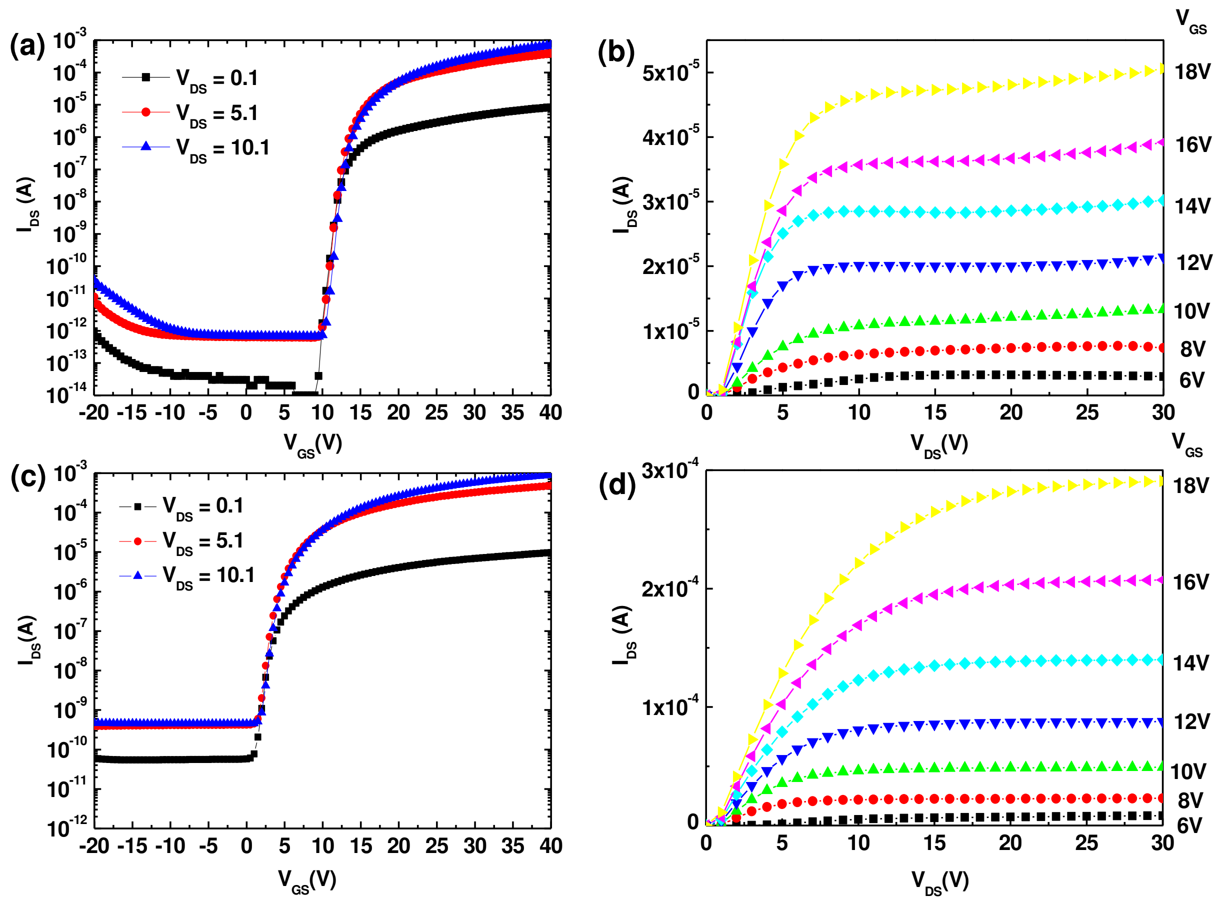


Fig.4-16. Comparison of a-IGZO TFTs with bias: (a) transfer characteristics and (b) output characteristics of unbiased (0V) a-IGZO TFTs, (c) transfer characteristics and (d) output characteristics of biased (150V) a-IGZO TFTs.

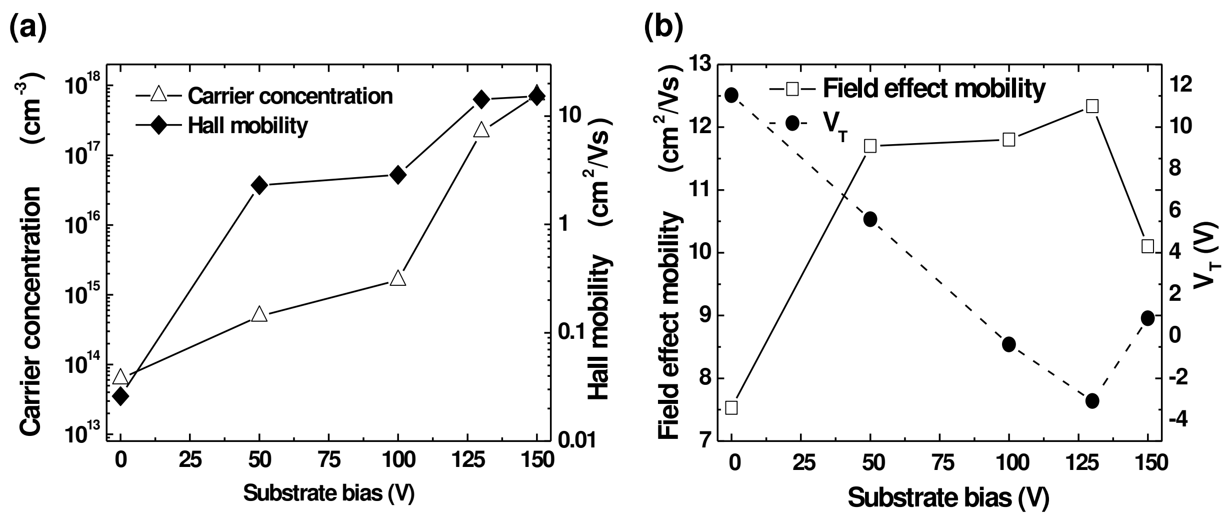


Fig.4-17.The dependence of substrate bias on (a) Hall mobility and carrier concentration in the a-IGZO film (50nm) and (b) the V_T and field effect mobility of the a-IGZO TFTs.

deficient near the a-IGZO surface; oxygen vacancies induce a n-type free carriers near the conduction band because one oxygen vacancy creates two extra electrons in the a-IGZO film. This effects increases donor carrier concentration in a-IGZO [36], [20]. The slight decrease in the carrier concentration at 150 V likely comes from severe sputtering damage which causes degradation in the interface between a-IGZO and the gate dielectric [75]. While the increased carrier concentration increases the a-IGZO field effect mobility, the I_{OFF} value also increases up to 1×10^{-9} A with increasing bias which is likely due to bulk conduction through the a-IGZO film (between the source and drain)[Chung [76]].

Fig. 4-17 (b) also shows the dependence of substrate bias on the V_T and carrier concentration of the a-IGZO TFTs. Interestingly, the V_T values as well as the carrier concentration were strongly dependent on substrate bias. As mentioned above, the threshold voltage decreased with increasing substrate bias; eventually becoming negative at high substrate bias. This is a quite reasonable result because, in the case of the a-IGZO TFTs with lower carrier concentration, the device requires higher positive gate voltage to form electron channel in the a-IGZO. Conversely, the TFTs with high substrate biased a-IGZO shows the V_T value near zero-gate voltage because of the high carrier concentration. Another contributing factor that affects the threshold voltage of un-passivated devices is environmental effects. According to recent report, the threshold voltage of a-IGZO TFTs can be shifted due to adsorbed gases in the channel region of the a-IGZO TFTs [10]. In particular, adsorbed oxygen on a-IGZO results in a positive V_T shift by inducing a depletion layer below the surface. Because the biased films had variable surface roughness as a function of substrate bias as shown in Table

Table 4-3 Electrical properties (μ_{FE}, S, I_{off} and V_T) of a-IGZO TFTs, surface roughness[root mean square(RMS)], deposition rate, refractive index (n), and stress of a-IGZO film as function of substrate bias voltage.

Substrate bias V (Power W)	μ_{FE} (cm^2/Vs)	S (V/dec.)	I_{off} (A)	V_T (V)	RMS (nm)	Deposition rate (nm/min)	n	Stress (Mpa)
0 (0W)	7.5	0.38	5.8×10^{-13}	11.5	0.37	0.65	1.84 ± 0.2	-510 ± 40
50 (~0.5W)	11.7	0.55	3.5×10^{-11}	5.6	0.17	0.61	1.93 ± 0.3	-790 ± 60
100 (1W)	11.8	0.51	6.7×10^{-10}	- 0.4	0.15	0.56	1.96 ± 0.2	-910 ± 70
130 (5W)	12.3	0.74	2.9×10^{-9}	- 3.1	0.16	0.43	1.97 ± 0.2	-850 ± 60
150 (10W)	10.1	0.86	1×10^{-9}	0.9	0.12	0.34	1.98 ± 0.2	-920 ± 70

4-3, it is plausible that higher roughness associated with the zero and low substrate bias increased surface density of adsorbed oxygen and causes a positive V_T shift. To rule out the effects of oxygen adsorption on the V_T, a set of passivated TFTs were fabricated; 100 nm of sputtered SiO_2 was used to passivate the channel region of the a-IGZO TFT where the a-IGZO was deposited with a zero substrate bias. Passivation of the a-IGZO TFTs resulted in a decrease in V_T of ~ 5 V in the negative gate voltage direction (not shown). This does not account for the ~ 10 V V_T shift of the a-IGZO TFT deposited at 150 V substrate bias. Thus, the V_T shift observed for the un-passivated devices with substrate bias is attributed to the change in the carrier concentration as well as a possible contribution from reduced adsorbed oxygen because of the reduced surface roughness.

The S value was also noticeably degraded with substrate bias, ranging from 0.38 V/decade at 0 V bias up to 0.86 V/decade at 150 V bias as shown in Table 4-3. It is well known that the subthreshold voltage can be affected by the bulk trap density in the active layer rather than the interface trap density [20]. The increase in the bulk trap density is likely due to the generation of dangling bonds in the a-IGZO film with increased energetic ion bombardment during bias sputtering. As seen in the data presented in Table 4-3, the index of refraction increased with substrate bias suggesting that the energetic ion bombardment reduces the porosity in the films (and thus increases the density). The measured lower surface roughness is also consistent with enhanced surface mobility of deposited species during biased sputtering. Concomitantly, the compressive stress increased with increasing substrate bias which agrees with an atomic peening model for films deposited with a simultaneous ion bombardment.

Finally the significance of the energetic ion bombardment is evidenced by the reduced deposition rate observed with increased substrate bias. While a slight change in the deposition rate was expected due to the densification, the continued decrease in the deposition rate as a function of increased bias (while the roughness and index of refraction levels off) suggests that likely re-sputtering of the deposited film is occurring.

Interestingly, the bias sputtered results presented here at first glance seem to contradict the recent study by Jeong *et al*. where they reported that the S value is improved (decreased) at lower sputtering pressure. The effect of reduced sputtering pressure has the effect of increasing the sputtered ion/atom energy distribution, in which Jeong *et al.* attributed to increase in a-IGZO density and decrease in the bulk trap density as evidenced by the decrease in the subthreshold gate swing value. The results shown here are likely due to the fact that the ion energy distribution for the IGZO deposited under substrate bias is much larger than the energy distribution of low pressure a-IGZO. We speculate that for the substrate biased TFTs, though the energetic ion distribution increases the density, is high enough to disrupt the a-IGZO bonding arrangement which induces a high density of bulk traps. This increase in the bulk traps results in the increase in the observed subthreshold gate swing value.

To investigate atomic concentration ratios as a function of substrate bias, the core-level spectra of a-IGZO film was analyzed. Fig. 4-18 shows the core-level XPS spectra of two a-IGZO film with substrate bias (0 V vs. 100V). The different atom atomic concentration ratios were obtained from area of XPS spectra curves, which is normalized by total atom concentration for comparison with substrate bias. Only core-level spectra were analyzed; In $3d_{5/2}$, Ga $2p_{3/2}$, Zn $2p_{3/2}$, and O 1s as shown Fig. 4-18

(a), (b), (c), and (d). The relative In content was increased (+18%), oxygen was decreased (-3.1%), and most of all, Zn was significantly decreased (-38%) with increasing substrate bias. As discussed in chapter 4.1 and above, the relatively increased In and decreased oxygen cause mobility to increase and cause V_T to decrease as shown conductivity as shown Table 4-3. These peculiar behaviors are attributed to different chemical bonds strength (1.7eV for In-O, 1.5eV for ZnO, and 2.0V for Ga-O) in a-IGZO [77] during substrate bias sputtering; by high energetic Ar^+ bombardment during bias sputtering, the preferentially weakly bound Zn-O bonds were sputtered. Therefore, the relative In ratio in a-IGZO film was increased as well as the Ga ratio was slightly increased due to relatively high bond strength. As comparison of atomic ratio of In : Ga : Zn in the inset of Fig. 4-3 (e), the calculated atomic ratio In:Ga:Zn were noticeably changed from 1 : 1.3 :1 to 2 : 2.2 : 1 for PO_2=0.84 mTorr and PO_2=0.84mTorr with substrate bias 100V, respectively. The resulting TFT electrical properties with the atomic ratio of In:Ga:Zn ~ 2:2.2:1 were consistent with recent report [78]; a-IGZO with an smaller Zn concentration of atomic ration In:Ga:Zn ~2:2:1 (relatively higher In concentration) shows higher field effect mobility due to higher carrier concentration in a-IGZO film (see Table 4-3 Bias 100V for electrical properties).However, in this study, it was not observed that peak shift due to changing chemical bond.

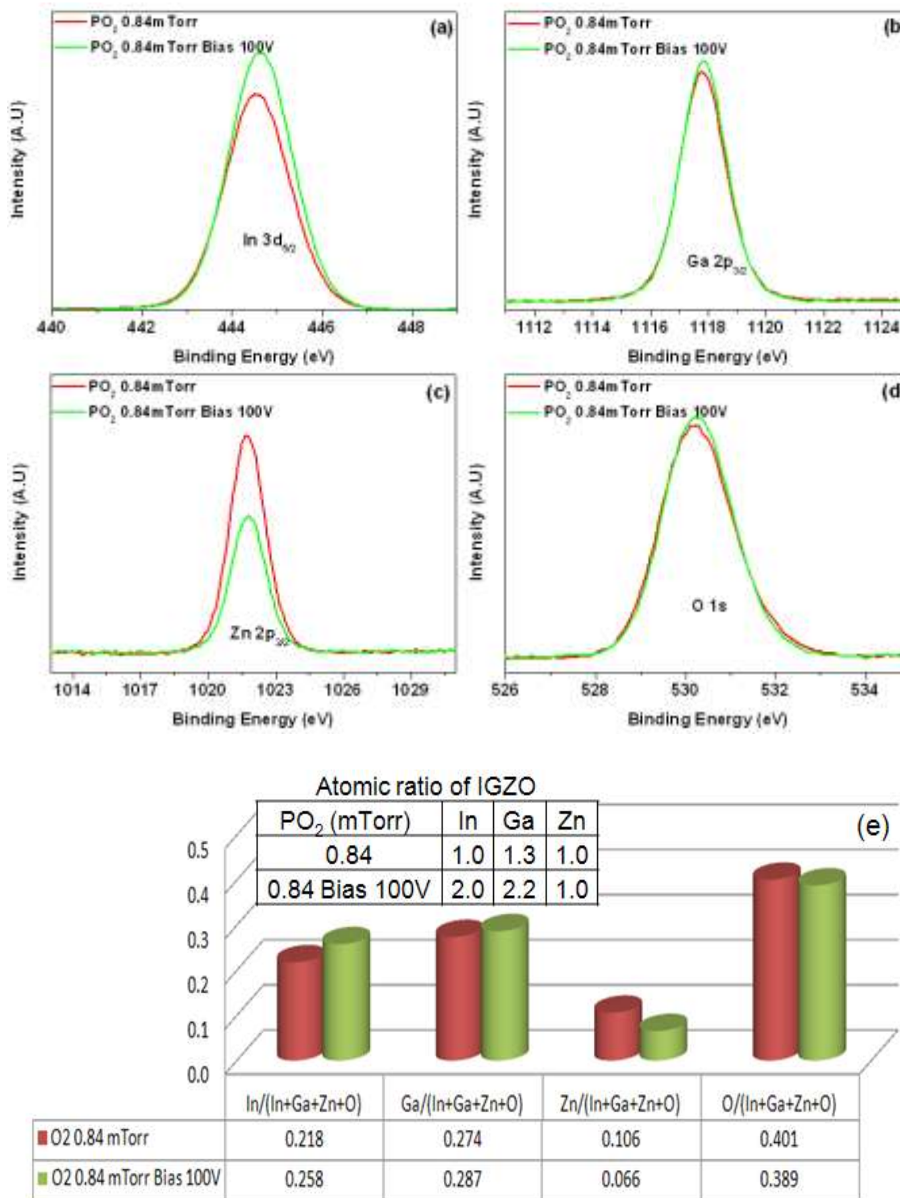


Fig. 4-18. Comparison of core-level XPS spectra of the IGZO film deposited with substrate bias (green color) and without substrate bias (red color),(a), (b), (c), and (d) and the atomic concentration ratios obtained from the area of XPS spectra curves, (e) which is normalized by total atom concentration for comparison with substrate bias (0 V vs. 100V).

4.3.4 Conclusion

In summary, the characteristics of a-IGZO TFTs were changed with applied substrate bias during a-IGZO rf magnetron sputtering. The increased μ_{FE} value and I_{OFF} with substrate increasing substrate bias was attributed to increased carrier concentration associated with preferential oxygen sputtering. The V_T shifts to lower values and eventually becomes negative with increasing substrate bias due to increased carrier concentration in the a-IGZO and a possible contribution from a decrease in the absorbed oxygen on the a-IGZO because of the lower surface roughness. The S value was significantly increased with increasing substrate bias and is attributed to energetic ion induced bulk trap defects in the a-IGZO film.

*Acknowledgment

The device characteristics of a-IGZO TFTs sputter deposited with different substrate biases has been published previously in the Electrochemical and Solid State Letters by myself, Jung won Park, and Philip Rack [79]. Of the work presented in this chapter Carlos Gonzalez helped to perform the UV-VIS measurement in SMRC (Scintillation Material Research Center) to achieve transmittance, Murat Ozer in Hanno Weitering's group helped to measure XPS of a-IGZO films as a function of oxygen partial pressure and substrate biased sputtering, Joo Hyon Noh helped to measure AFM of a-IGZO surface as a function of oxygen partial pressure and substrate biased sputtering as well. Philip Rack provided direction, funding of the research, discussion and motivation.

Chapter 5

Passivation

5.1 Introduction

A passivation (PVX) layer on a TFT is commonly used to protect the device from subsequent process and environmental effects [40], [41], [80]. Fig. 5-1 shows the transfer characteristic of the TFT without (w/o) passivation in comparison with it of TFT with (w/) passivation. The TFT with passivation shows much higher leakage current level at V_{GS} and the V_T seems to be shifted in the negative direction of V_{GS}. The reason of this peculiar characteristic has been described from mainly two points of view. First, the back-channel conduction at the interface or surface of a-IGZO between source and drain where the defect density (current path) depends on 1) the degree of plasma damage during passivation deposition using PECVD or sputtering or 2) the degree of etching damage during wet or dry etching. Second, the intrinsic bulk a-IGZO conduction changes; high carrier concentration in a-IGZO because, according to reports [9], [10], [40], gas absorption or desorption on a-IGZO such as oxygen and hydrogen influence to electrical properties of a-IGZO TFT. Kang *et al.* have described that physically absorbed oxygen at the back channel surface of the a-IGZO exists as O_2^- in a form of $O_2 (gas) + e^- \rightarrow O^{2-} (solid)$, capturing an electron from the conduction band of a-IGZO, and leading to an increase in the V_T of the TFT due to decreased carrier concentration in a-IGZO as shown in Fig. 5-2. Therefore, in the high vacuum chamber, the amount of

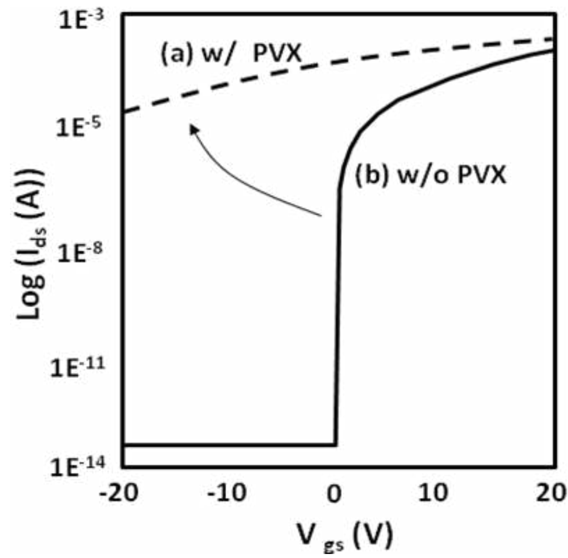


Fig. 5-1. Transfer characteristic of TFTs: (a) TFT with (w/) PVX and (b) TFT without (w/o) PVX.

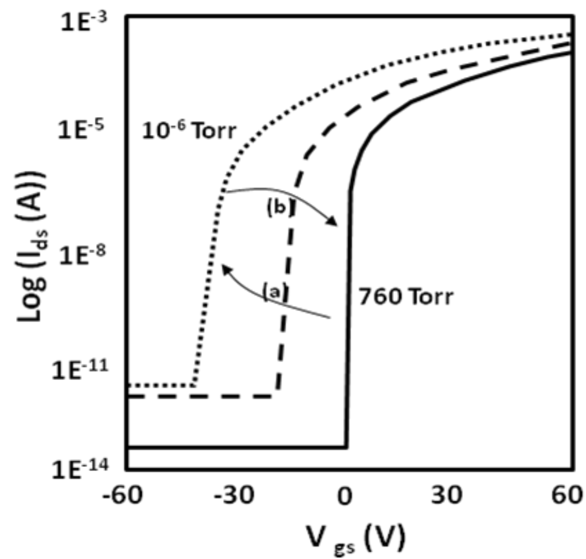


Fig 5-2. The shift of transfer curves at different pressure; (a) decreasing pressure and (b) increasing pressure.

physically absorbed oxygen at the a-IGZO surface of TFT with passivation is minimized because weakly bonded oxygen can be desorbed at low pressure when the chamber is evacuated before the passivation process ensues. Therefore, a highly negative shift in V_T of the TFT can be considered as intrinsic a-IGZO in which environmental effects are minimized from gas reactions. In order to examine these instabilities, this chapter will show a-IGZO TFT passivated with various layers such as SiO_x and polymer films (SU-8) coated by spin-coating method as well as different film deposition method such as sputtering and PECVD. The work also considers different deposition conditions such as different O_2 pressures during a-IGZO to study the correlation between the a-IGZO film properties and the subsequent passivation layer.

5. 2 Experimental

The patterned gate chromium metal (Cr) and gate dielectric (SiN_x) using plasma enhanced chemical deposition (PECVD) were formed onto a buffer 500nm SiO_2 coated silicon wafer. The a-IGZO active layer (50nm) was rf magnetron sputter deposited using an a-IGZO target (In_2O_3 : Ga_2O_3 : ZnO = 1:1:1 mol%) with different Ar/O_2 gas ratio; oxygen partial pressure during sputtering. The active layer was lithographically defined by using diluted 0.1% buffered oxide etchant (BOE). Sputtered Cr (200nm) source and drain electrodes (SDs) were also lithographically patterned via wet etching. After sputter passivation with various passivation materials, via hole etching was performed by a dry etching process to contact electrodes. Finally, the samples were annealed at 350℃ for 1hr in nitrogen ambient. The electrical characteristics of a-IGZO TFTs were tested using

an HP 4145A device parameter analyzer with a channel width of 70 μm and a channel length of 22 μm.

5.3 Results and discussion

Fig. 5-3 shows the representative transfer curves of the a-IGZO *with* and *without* sputter deposited SiO_2 passivation layers at V_{DS} = 5.1V in which a-IGZO was deposited with PO_2=0.84mTorr . For un-passivated TFT devices, the μ_{FE}, V_T, and S were 7.2 cm^2/Vs, 11.8 V, and 0.66/decade, respectively. These characteristics are reasonable for driving an active matrix type device. In contrast, for a-IGZO devices passivated with sputter deposited SiO_2 device characteristics shows a high leakage current level at V_{GS} = 0 V; I_{DS} at V_{DS} = 5.1V was increased from 2.9×10^{-12} A to 1.9×10^{-5} A without passivation and with passivation, respectively. Furthermore, the passivated device seems to be a resistor and cannot be controlled by applying a gate voltage and has a significantly higher I_{DS} than un-passivated devices as shown in Fig. 5-3. The high current in the passivated devices are ascribed to several effects. First of all, gas absorption or desorption on a-IGZO can result in V_T shift as well as an off-current increase [9], [40]. The a-IGZO active layer likely desorbs the physisorbed oxygen due to the low pressure and does not re-adsorb thus the passivated devices do not exhibit depletion effects in the back-channel region relative to un-passivated devices which have physisorbed oxygen. Thus passivated devices have charged (uncompensated)

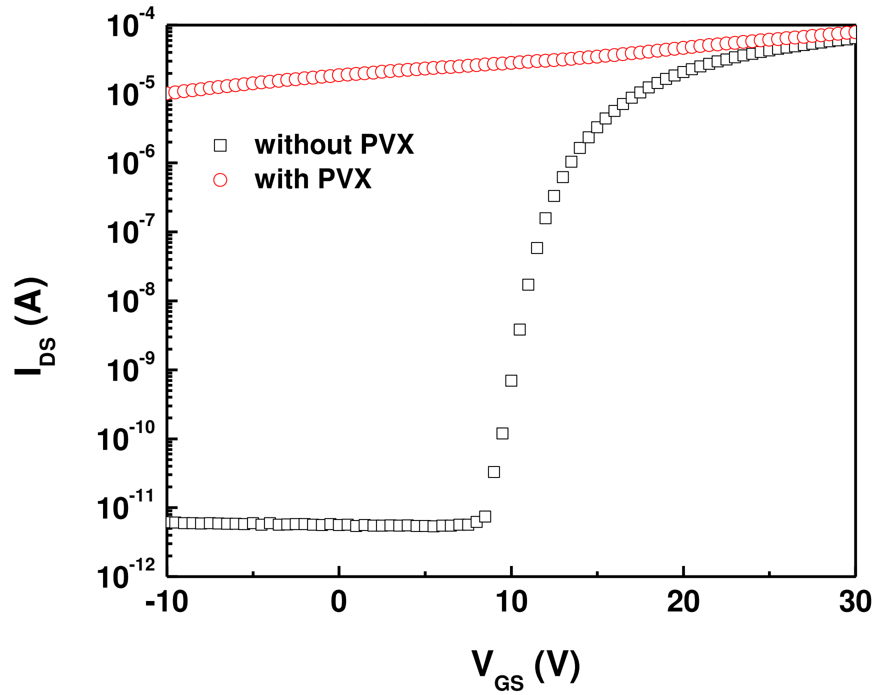
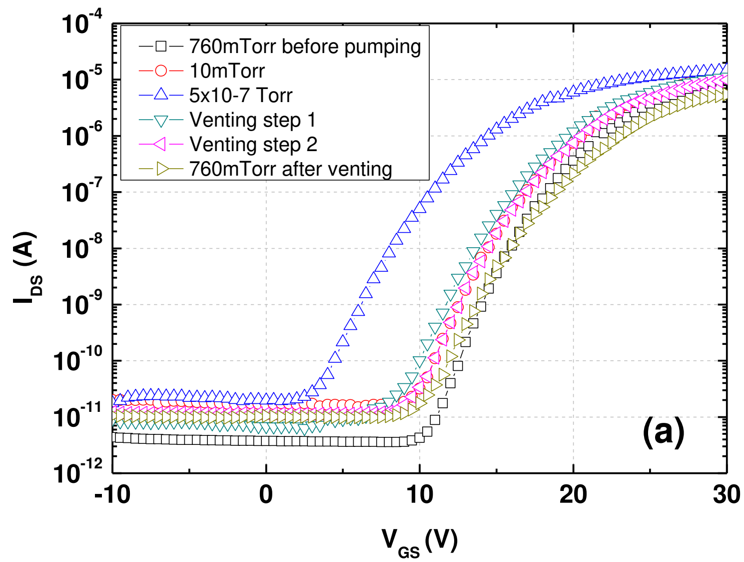


Fig. 5-3. The transfer curve of a-IGZO TFT *without* passivation and *with* sputter SiO_2 passivation at V_{DS} =5.1V.

oxygen vacancies as electron carriers, which decreases V_T and increases the off-current. Second, the back channel current is likely increased due to plasma damage in the near surface region of the in a-IGZO due to the energetic sputtered ion distribution thus creating a slightly oxygen deficient layer and consequently a current path. To verify gas adsorption/desorption on a-IGZO channel of TFT, the a-IGZO TFT without passivation was fabricated and tested in a different pressure ranging 760mTorr to 5 x 10^{-7} mTorr in the vacuum chamber. Fig. 5-4 shows the transfer curve with changing pressure in chamber at V_{DS} = 5.1V in which a-IGZO was deposited with PO_2=0.84mtorr. As the pressure is decreased from 760 mTorr to 5 x 10^{-4} mTorr, the V_T was changed from ~17.9V to ~11V and when vented was increased to ~ 18.7V as shown in Fig. 5-4 (b) but field effect mobility(~ 4.8 cm^2/V.s) and S (1.2 V/decade) were not significantly changed, which can obviously be attributed only physically absorbed/desorbed gases (mainly oxygen) which have very weak bond energy on the channel of a-IGZO TFT; V_T was decreased due to physically desorbed oxygen and increased due to physically adsorbed oxygen as discussed in 5.1 introduction. In addition, by analyzing O 1S peak through XPS analysis, it was investigated whether the chemically adsorbed oxygen exists on the a-IGZO channel surface and assumed that most of adsorbed oxygen on a-IGZO at the high vacuum with ~ 2 x 10^{-10} mTorr is chemically bonded on a-IGZO. Fig. 5-5 shows the oxygen core-level XPS spectra (O1s at 534.4eV) of the a-IGZO film before and after sputtering surface treatment. Interestingly, the sample before sputtering surface treatment shows asymmetric peak shape compared to after surface sputtering treatment. After normalizing the curves, the relative oxygen composition ratio was



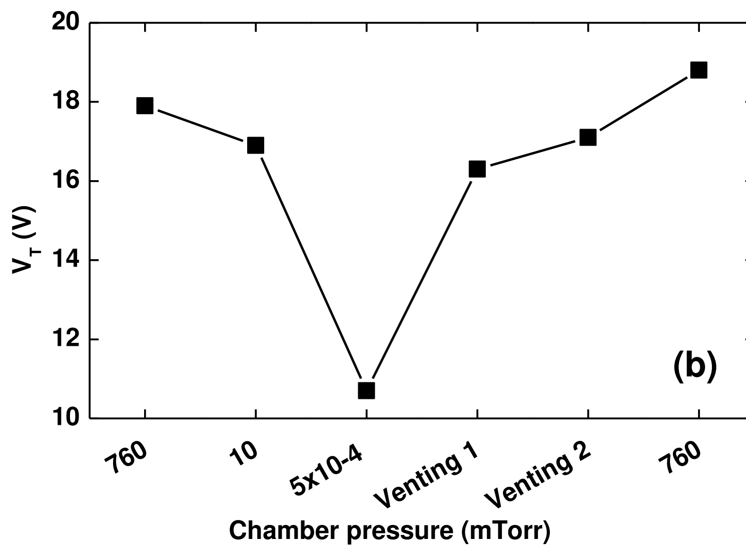


Fig. 5-4. (a) the transfer curve shift with different pressure and (b) V_T shift with changing pressure.

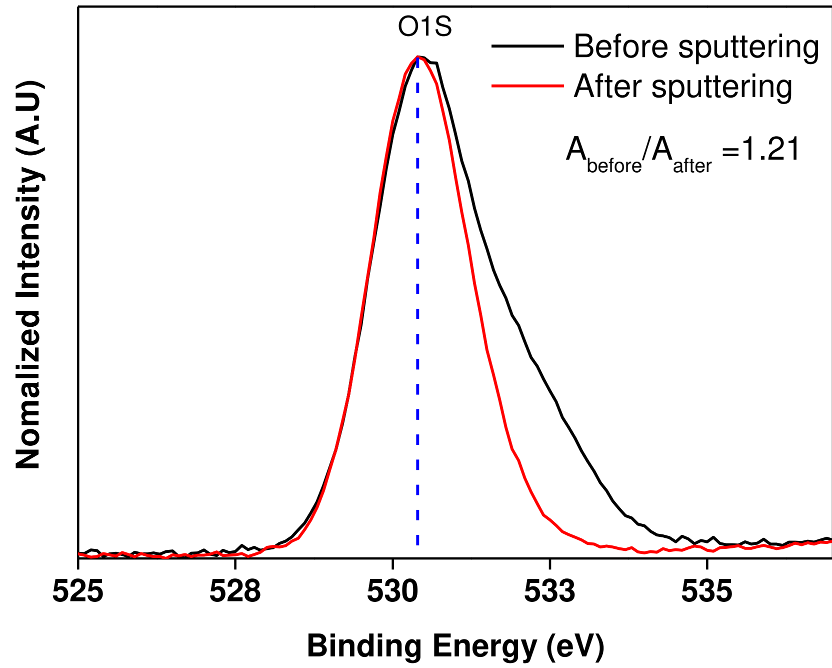
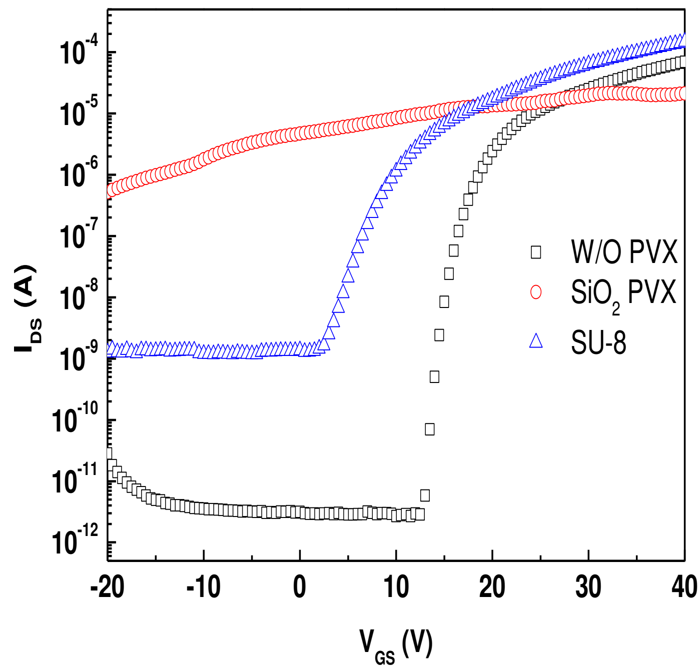


Fig. 5-5. Oxygen core-level XPS spectra of the a-IGZO film before and after sputtering surface treatment.

compared by integrating the area for each curve where the composition ratio (A_{before}/A_{after}) was 1.2. It is indicated that chemically bonded oxygen with carbon (for carbonyl C=O and O-C=O, binding energy is 532.2 eV and for alcohol and ether C-O-H and C-O-C, binding energy is 532.8eV) presumably exists on a-IGZO. Now, to verify the V_T instability with the gas adsorption on a-IGZO and plasma damage from the subsequent passivation process, the polymer SU-8 was employed for passivation because it can be spin-coated in air without exposing the surface to low pressure and plasma damage. Additionally, it is a common passivation layer as well as it is a biocompatible material for a biological devices. Fig. 5-6 shows the TFT transfer curve w/o PVX, with sputtered SiO_2 PVX, and with spin-coated SU-8 PVX. After passivation of a-IGZO TFT, the electrical performance of both sputtered SiO_2 and spin-coated SU-8 passivated TFTs was degraded and the SiO_2 passivated device could not be modulated in the range of gate voltage due to high negative shift in V_T (the actual V_T was – 29V) as discussed above. However, SU-8 passivated a-IGZO TFT shows a reasonable transfer characteristic with increased off-current (from I_{DS} = ~ 2 x 10^{-12} to I_{DS} = ~ 1 x 10^{-9} A) and ΔV_T (- 9.3 V). Based on this study, it is confirmed that the interaction between the active backchannel and ambient plays a critical role in determining the V_T instability. In the case of SU-8 passivated device, the physically adsorbed oxygen on the a-IGZO channel is presumably not desorbed by the spin coating and baking compared to low pressure and plasma damage processes. Thus there is presumably enough oxygen at the a-IGZO channel surface to deplete the a-IGZO channel; minimizing leakage current



	V_T (V)	Mobility (cm^2/Vs)	S (V/decade)
w/o PVX	16.1	3.6	0.52
SU-8 PVX	6.8	2.2	2

Fig. 5-6. TFT transfer curve with different passivation layer; 1) w/o passivation, 2) sputtered SiO_2, and 3) spin-coated SU-8.

through back channel. The relatively increased off-current and shifted properties can be attributed to the intrinsic property of polymer material (SU-8) as passivation. According to Jeong *et al.* and Park *et al.*, the V_T instability due to polymer materials as passivation layers contains H_2O molecules and the H_2O molecules on or near the a-IGZO surface can act as electron trap centers as well as donors, providing electrons to the a-IGZO channel and it can diffuse into a-IGZO channel [9], [10]. Therefore, the increased carrier concentration in a-IGZO causes the V_T to be shifted in the negative direction as well as the off-current to be increased. The density of the net created electron charge in the channel due to H_2O adsorption on the a-IGZO surface was estimated from the extent of the V_T shift ($Q_{induced} = C\ \Delta V_T/q$, where C is gate capacitance per unit area). The $Q_{induced}$ due to SU-8 passivation was 1.8×10^{12} cm^{-2} (C is from 35.6 nF for SiN_x in Table 3-2 in chapter 2 and ΔV_T between w/o PVX and SU-8 PVX is from Fig. 5-6). The S also was significantly increased from 0.52 V/decade to 2.0 V/decade. The H_2O-related traps on a-IGZO surface can be in either the tailing state (shallow) or deep level state in the forbidden band gap of the a-IGZO. However, in this study, the increase in the shallow density is not the dominant mechanism causing the degradation of the S value because the field effect mobility was not significantly changed as shown in Fig. 5-6. Therefore, it is believed that the degradation of S of SU-8 passivated a-IGZO TFT due to H_2O adsorption (increased trap density) can be considered due to created deep level trap states in a-IGZO.

Based on the above discussion, a reliable passivation condition which is formed by deposition method must be developed. In spite of plasma damage on a-IGZO channel by sputtering process, the sputtered passivation layers is preferred to be used

to protect an active layer because of the advantages such as room temperature and hydrogen free processing as compared with PECVD process which, at high temperature and rich hydrogen content, can induce conductive a-IGZO due to oxygen vacancies and hydrogen donor levels [38], [81] in spite of its merits such as high quality film, fast process, and excellent step coverage. To optimize the passivation process for robust a-IGZO TFT, the work was done with following approaches: 1) correlate the device performance with different W/L ratio and passivation, 2) investigate different deposition methods using PECVD and sputtering methods, 3) explore different oxygen concentration profiles in a-IGZO channel including 2 step a-IGZO deposition with different PO_2, and 4) study post annealing effects with different temperatures. The experimental plan in detail is summarized in Table 5-1. To do 1), the SiO_2 passivation layer using PECVD was deposited at 250°C as low as possible to minimize hydrogen diffusion into a-IGZO and a-IGZO (PO_2=1.5mTorr) with relatively high oxygen content was used with the deposition condition developed in chapter 4. Basically, the used a-IGZO deposition with PO_2 =1.0mTorr which was optimized in chapter 4 was used.

Table 5-1 Experimental plan to study passivation with different process condition.

Sample	a-IGZO (nm)	PVX(100nm)	Post annealing (in N_2 for 1hr)	W/L
PE	50 (O2 30%)	SiO_2(PECVD)	250°C/350°C	70/6,40/22,20/18
S1	50 (O2 20%)	SiO_2(sputter)	250°C/350°C	
S2	10 (O2 30%)/40(O_2 20%)	SiO_2(sputter)	250°C/350°C	

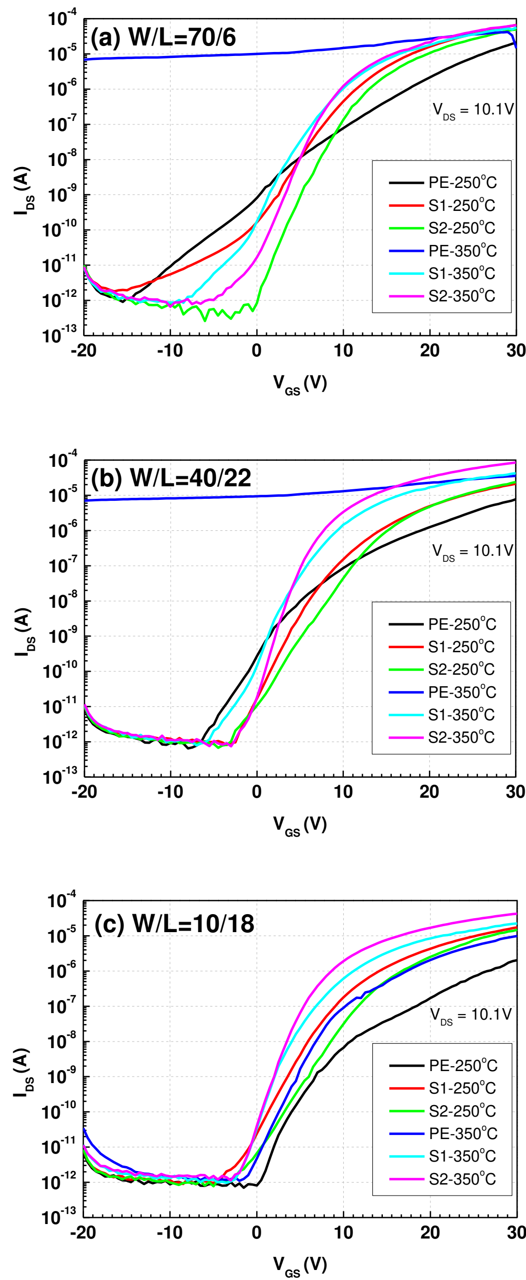


Fig. 5-7. Comparison of transfer curves with deposition method (sputter vs. PECVD), annealing temperature (250°C vs. 350°C), and W/L ratio (70μm/6μm, 40μm /22μm, and 10μm /18 μm).

Fig. 5-7 shows the transfer curves with different passivation deposition and all electrical properties are summarized in Table 5-2 in detail. At a glance, interestingly, the transfer curves with decreasing W/L ratio regardless of passivation conditions show more reliable results; the electrical properties are more consistent than higher W/L ratio. While, in case of W/L =70μm/6μm and 40μm/22μm, the TFT passivated by PECVD and annealed at 350C shows high drain current level as function of gate voltage swing. In particular, most TFTs with W/L= 70μm/6μm show increased leakage current between V_{GS}= -10 V and 0 V as shown in Fig. 5-7 (a). Interestingly, these peculiar characteristics agree with reverse current-voltage characteristic of a-Si:H TFTs reported by P. Servati *et al.* who proposed the models for leakage current in the channel of TFTs [82]. For a-IGZO TFT, it would be quite reasonable results to see this electrical behavior as considering the pliable back channel affected by following sputtering passivation process, which may induce leakage current between source and drain. However, this behavior does not occur for low W/L ratio (especially, small W) and significantly appears at high V_{DS} (not shown in figure). It is proposed that the leakage current via back channel are significantly dependent on the intensity of electric field between source and drain, showing resistor-like properties controlled by L size.

Fig. 5-8 shows the comparison of electrical properties with different passivation deposition methods for each temperature (250°C and 350°C). As compared in the a-IGZO TFT with PECVD SiO_2 passivation (sample PE) verse sputtered SiO_2 passivation (sample S1), noticeably PECVD passivated TFTs were significantly degraded; large

Post annealing	Electrical characteristics	W/L = 70um/6um			W/L = 40um/22um		W/L = 10um/18um		
		PE(70/6)	S1(70/6)	S2(70/6)	PE(40/22)	S2(40/22)	PE(10/18)	S1(10/18)	S2(10/18)
250°C	μ (cm^2/Vs)	0.69	1.11	0.97	1.28	2.67	1.37	5.25	5.24
	V_T	15.7	9.7	10.9	14.8	11.7	16.6	9.6	12.1
	S	3.33	2.09	1.44	2.29	2.30	1.43	2.11	2.19
	I_{off}	8.2E-10	1.7E-10	8.4E-13	2.7E-10	1.1E-11	8.1E-13	2.4E-11	6.7E-12
350°C	m (cm^2/Vs)	0.16	0.82	1.00	0.59	6.01	3.66	6.18	9.89
	V_T	-15.6	7.1	7.1	-18.5	5.4	11.5	6.7	5.0

Fig. 5-8. Summary of electrical properties with different deposition conditions.

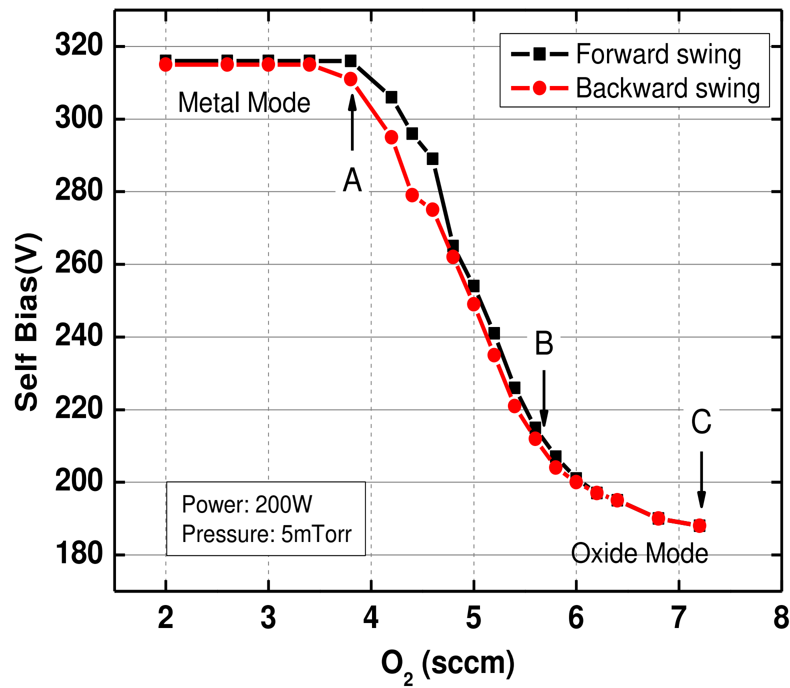
negative V_T shift, higher I_{OFF}, and even S value as shown. Additionally, as the post annealing is performed at 350°C, the V_T was highly negatively shifted as shown Fig. 5-8 (d) but the sample annealed at 250°C does not show significant V_T change at all. This electrical property can be attributed to hydrogen diffused from SiO_2 in which the hydrogen incorporated by precursors such SiH_4 is presumably diffused into a-IGZO channel at relatively high temperature [33] [83]. Therefore, sputter passivation methods are more favorable to a-IGZO TFT. Based on the discussion above, it is clear that the back channel of a-IGZO must be robust against the subsequent passivation process to realize high performance a-IGZO TFTs.

Next a two step sputtered a-IGZO process with different oxygen pressure was employed; 1st a-IGZO (40nm) on gate dielectric was deposited with conventional a-IGZO sputtering condition (PO_2=1.0 mTorr), called front channel and 2nd a-IGZO (10nm) with PO_2 = 1.5mTorr was continuously deposited on 1st a-IGZO, called back channel (sample S2) and compared to sample S1 in which the a-IGZO was deposited with PO_2=1mTorr only. The compared results also were demonstrated in Fig. 5-7 and 5-8. For field effect mobility, there was no significant change as shown Fig. 5-8 (a) and (b). For threshold voltage, they showed different electrical properties for each temperature. $V_{T,S2}$ at 250°C regardless of W/L ratio shows higher value than $V_{T,S1}$, which can be understood by considering effective carrier density in a-IGZO channel; it is due to back channel a-IGZO with higher oxygen content therefore relatively lower carrier concentration causes the V_T to increase. However, interestingly, in case of the a-IGZO TFT annealed at 350°C, both S1 and S2 show quite similar V_T value. It is clearly correlated to oxygen vacancies as electron carrier in a-IGZO exponentially depending

on temperature. According to Takagi *et al.*, the rate of increasing carrier concentration with temperature is more dependent on the a-IGZO film with lower carrier concentration and saturated at critical temperature (at sufficiently high temperature) [30]. In addition, it is considered the intermixing of vacancies generated from each 1st and 2nd a-IGZO layer. Therefore, the similar V_T values at 350^oC are quite reasonable. Most of all, 2 step a-IGZO deposition process significantly affects the off-current level at V_{GS} = 0V as compared in Fig. 5-8 (g) and (h). The significant drain current was decreased by employing this advance process. Likewise, the improvement is more effective the a-IGZO TFT annealed at 250^oC because of discussed reasons above.

Based on the results above, it is believed that the second (back channel) layer minimizes oxygen depletion for high performance a-IGZO TFT with passivation. Here, based on this idea, the flux calculation of oxygen during passivation process was also employed to achieve optimized passivation condition. Fig. 5-9 shows the hysteresis curve with oxygen during reactive SiO_2 sputtering. Based on the IGZO incorporation rate, I_{IGZO}, 4 .31 x 10^{21} (molecules/cm^2.sec) during a-IGZO sputtering, three oxygen pressures (incorporation rates) were selected from the hysteresis curve; sample A, sample B and sample C. The calculated oxygen incorporation rate from equation 4-3-2 were 3.6 x 10^{12} (molecules/cm^2.sec), 4.1 x 10^{12} (molecules/cm^2.sec), and 5.0 x 10^{12} (molecules/cm^2.sec) for sample A, sample B, and sample C, respectively. The incorporation ratio (I_{O2}/I_{IGZO}) were 0.83, 0.95, and 1.16 for sample A, sample B, sample C, respectively. The resulting transfer curves are demonstrated in Fig. 5-10. Noticeably, sample C shows best electrical performance as compared to sample A and sample B. It

is obviously that the oxygen incorporation rate during SiO_2 passivation is higher than IGZO incorporation rate during a-IGZO sputtering.



	I_{O2} during PVX	I_{O2}/I_{IGZO}
Sample A	3.6×10^{12} (molecules/cm^2.sec)	0.83
Sample B	4.1×10^{12} (molecules/cm^2.sec)	0.95
Sample C	5.0×10^{12}(molecules/cm^2.sec)	1.16

Fig. 5-9. Hysteresis curves both for both self bias in the cathode vs reactive oxygen gas flow rate during reactive SiO_2 sputtering for passivation.

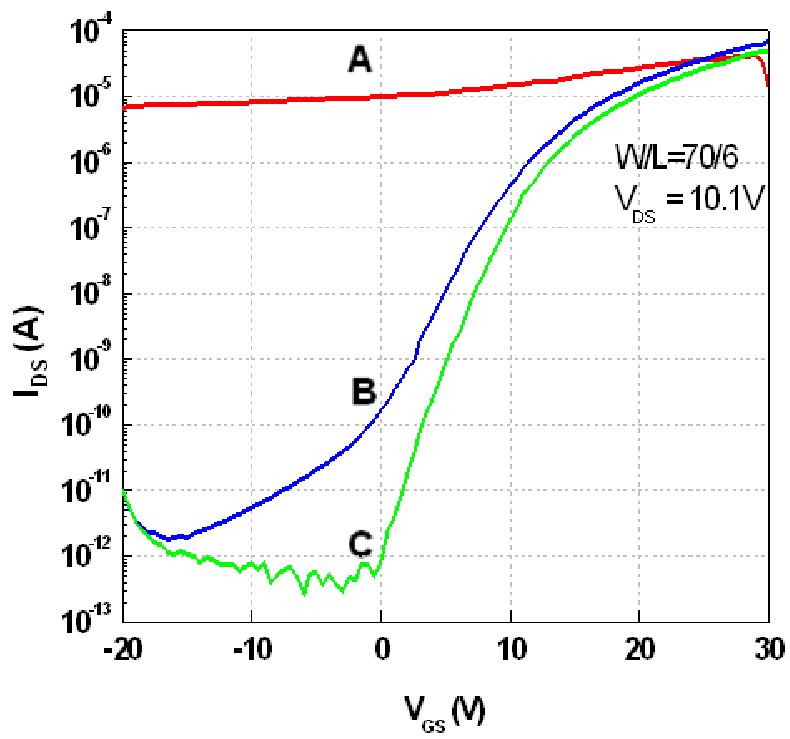


Fig. 5-10. Transfer curves of a-IGZO TFT passivated with different oxygen incorporation ratio.

5.4 Conclusion

It was confirmed that both physical and chemical adsorption affects the a-IGZO channel by studying TFT-IV characteristics with different pressure and analyzing O1S peak from XPS spectra, which mainly affects the V_T instability. The SU-8 spin-coated passivated a-IGZO TFT was compared to a-IGZO TFT with sputtered passivation in which water in SU-8 degrades the TFT performance by diffusing into a-IGZO and acts as electron trap states and ultimately a donor level. The PECVD SiO_2 passivated a-IGZO devices have increased carrier density and shifted V_T which is attributed to hydrogen in the SiO2 films which effectively dope the a-IGZO during the annealing process. The sputtered SiO_2 passivation shows better electrical performance. a-IGZO TFTs with the two step a-IGZO deposition (2nd 10nm a-IGZO with PO_2 = 1.5mTorr on 1st 40nm a-IGZO with PO_2=1mTor) shows best electrical performance among all experiment results. Finally, the flux calculations were used to estimate the O_2 flux on the active layer. In the case of higher oxygen incorporation rate during sputtered SiO_2 passivation greater than the IGZO incorporation rate during a-IGZO sputtering, the transfer curve shows the best electrical properties.

*Acknowledgment

Of the work presented in this chapter Kai Xiao in Oakridge National Laboratory helped to measure the transfer curves of TFT in vacuum chamber as a function of pressure. Philip Rack provided direction, funding of the research, discussion and motivation.

Chapter 6

Application: Microfluidic electrowetting channel device

6.1 Introduction

Electrowetting has been studied due to its potential for manipulating, controlling, and separating ionic/polar liquid droplets on platforms for Lab-On-Chip (LOC) microfluidics and even applied to electronic displays [84],[85],[86]. Fig. 6-1 shows the schematic of the electrowetting mechanism with applied voltages. The electrowetting effect is defined as the change of electrolyte contact angle due to induced potential difference between the solid and the electrolyte as shown Fig. 6-1 (a) in which contact angle can be changed with parameters by Young's equation :

$$Cos\theta_V = \cos\theta_Y + \frac{\beta \cdot \varepsilon}{2 \cdot z \cdot \gamma_{so}}(V)^2 \quad (6.1)$$

where θ_V is contact angle with applied voltage, θ_Y is Young's contact angle, γ_{so} is saline-oil interfacial surface tension, β is fractional surface contact area, ε is permittivity, z is dielectric thickness, and V is applied voltage. For conventional electrowetting (Fig. 6-1 (a)), a polar liquid droplet rests on a planar electrode coated with a hydrophobic dielectric and an electric field is applied between droplet and planar electrode where the electrowetting behavior can be programmable with a 2-dimensional (2D) array.

In this study, we demonstrated the electro wetting with 3-dimensional (3D) surface structure (post structures such as silicon post and carbon nanofibers). Fig. 6-1 (b) and (c) show the schematic concept of an electrowetting behavior with applied voltage on 3D post structure. Once dropping saline liquid on the posts with oil, it shows a high

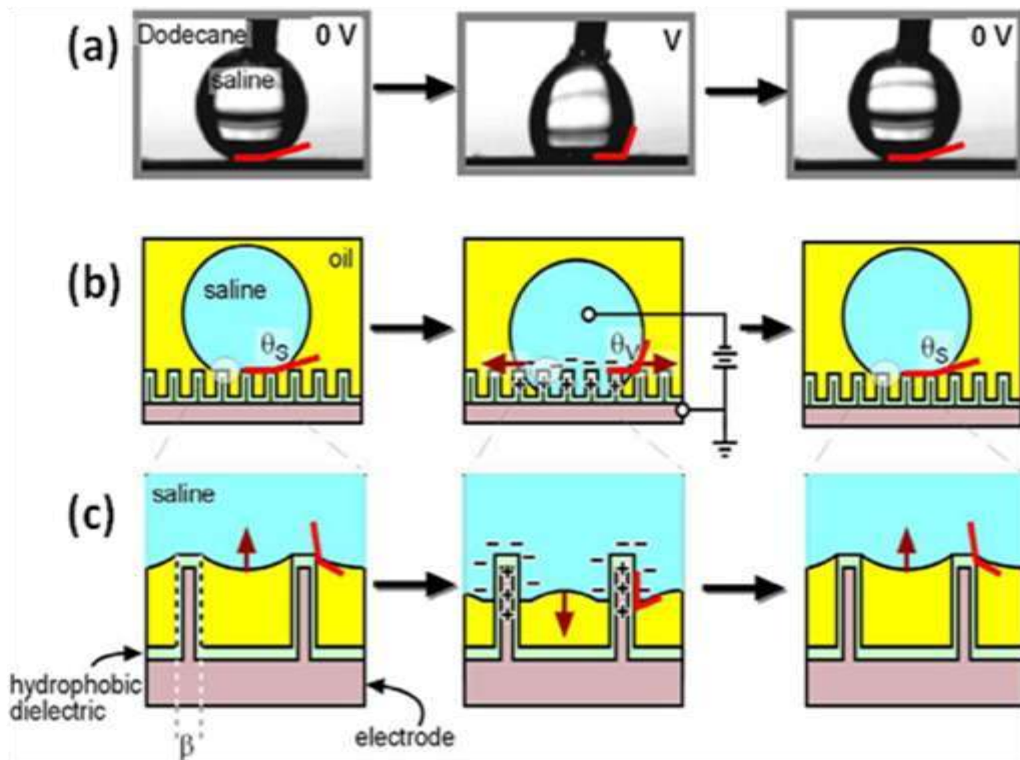


Fig. 6-1. Schematic of electrowetting effect mechanism with applying voltage, (a) contact angle change on 2 dimensional surface, (b), and (c) 3 dimensional surface (post structure).

contact angle between saline and surface of posts because the surface of posts is hydrophobised (high surface energy) and as the voltage was applied to post, the generated surface charge on posts will change the surface energy of posts to lower energy, showing more hydrophilic behavior, therefore, droplet recedes down into posts, separating oil out. Once the applied voltage is off, the wetted liquid move back to its original position, showing high contact angle again. These reversible electrowetting effects allow posts to form liquid channels due to reducing contact angle between liquid and dielectric. Our original motivation embodies an agile transport system for LOC by mimicking a cell membrane in nature as shown Fig. 6-2. The proposed device consists of 3D surface structures (post structures). This approach is highly unique since all separation mechanisms, if active matrix type TFTs are integrated to each cell, are simultaneously active and switchable in each cell having the following functions: 1) fine-pitch posts act as a physical filter; 2) hydrophobic surface of posts will experience an increase in effective surface energy via electrowetting; 3) electrically biased posts can gate ionic transport through Debye screening. Figure 6-3 shows schematic multidimensional agile fluidic transport system.

In this study, the preliminary electrowetting studies with surface energy change will be demonstrated to achieve 3D multidimensional platform as shown Fig. 6-3, the devices with changing surface energy by applied voltage were demonstrated with following schemes; 1) generation I device platform (vertically aligned carbon nanofibers (VACNFs) electrowetting posts + a-Si TFT) and 2) generation II device platform (photoactive polymer posts + a-IGZO TFT). This study is a collaboration with team members at the University of Cincinnati (J. Heikenfeld group).

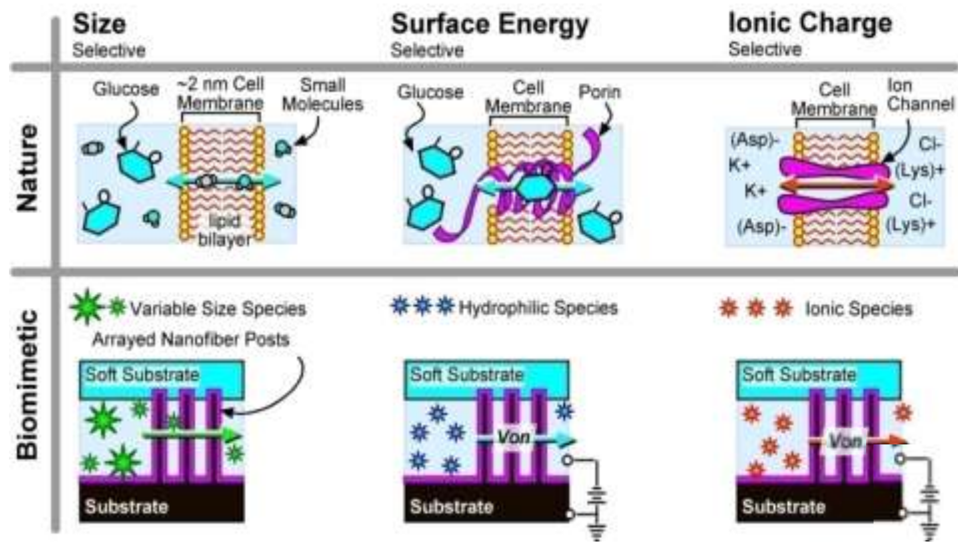


Fig. 6-2. Biomimetic transport mechanism and proposed schematic device structure.

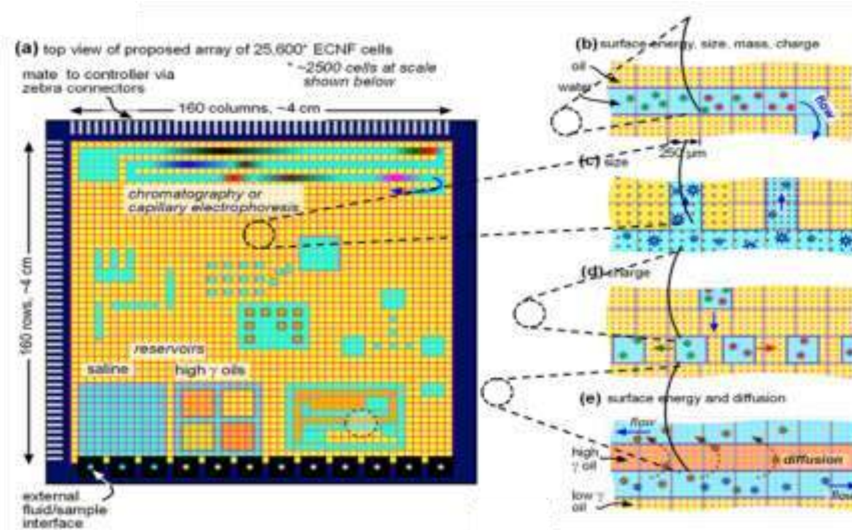


Fig. 6-3. Multidimensional agile fluidic transport system.

6.2 Generation I device platform (VACNFs electrowetting posts + a-Si TFT)

6.2.1 Passive electrowetting scaffolds

Based on the previously demonstrated reversible electrowetting study using VACNFs as posts by our group [87], electrically addressable VACNFs were fabricated as nanoscale functional elements for the platform with schematic top view as shown in Fig.6-4. The device layout was composed of 3 mask pattern process, 1) metal electrode line, 2) VACNFs, and 3) PDMS mold. VACNFs with different spatial separation (3μm, 4μm, 5μm, 10μm and 15μm) were grown on electrode arrays. Fig.6-5 shows the fabrication process of VACNFs on array for passive electrowetting scaffolds. PECVD SiO_2 (500nm) was deposited on silicon substrate and then a ground contact hole, to avoid surface charging effect during VACNFS growth using DC-PECVD, was formed via dry etching process with mixed SF_6 and Ar gases after the photolithography process (Fig. 6-5 (a)). Sputtered Cr (200nm) with substrate bias (~100V) was deposited for gate metal electrodes (Fig. 6-5 (b)). Ni/Ti (60nm/10nm) cylinders were patterned by a lift-off process for fiber growth as catalyst (Fig. 6-5 (c) and (d)) and then VACNFs with 13μm in height were grown by DC-PECVD with following growth condition; C_2H_2=80sccm, NH_3=200sccm, and at 700°C for 13min with current of 1A (Fig. 6-5 (e)). The gate metal electrode with VACNFs were carefully patterned photolithographically with 2 step coating using lower spin speed coating process to improve the step coverage of PR on VACNFs and then wet etched by Cr etchant (CR-14S) (Fig. 6-5 (f)). Parylene C (1μm, εr~3, Ebd~2 MV/cm, γ~ 20 mN/m) was CVD coated as a conformal dielectric and low

surface energy fluoropolymer (250nm) was applied via dip-coating (Fig. 6-5 (g)). After covering PDMS on the array, electrolyte was injected into device channel (Fig. 6-5 (h)). The VACNFs array was dosed with Dodecane (non-polar hydrocarbon oil) and the test droplet was compose of 1 wt% blue pigment and 1 wt% sodium dodecyle sulphate (surfactant) solution in DI water. To characterize the device, the grown VACNFs were analyzed by SEM as shown in Fig. 6-6. The fibers were well-aligned on the Cr gate line and each catalyst area was composed of a merged bundle of fibers. The height of fibers was 12 μm. To investigate electrowetting behavior of VACNFs to form agile liquid channels, a voltage was applied to device as shown in Fig. 6-7. Reversible (water/Dodecane) electrowetting can be performed to form liquid channels within fibers, which is tested in fibers of 5μm in pitch size. The liquid channel (red color) advanced with increasing applied voltage. The length of liquid channel was longest at V_g=60V. However, at V_g =0V, no channel is formed. It is clearly supported by the fact the applied voltage cause the hydrophobised surface of the fibers to change to a more hydrophilic surface with electrowetting mechanism as described above (see 6.1 introductions). Here, the black circle defects are likely breakdown of the Parylene dielectric at high voltage. In summary, the controlled liquid motion through the VACNFs was demonstrated with reversible electrical wetting behaviors to form agile liquid channels within the VACNFs; electrically induced channel by Vg. In addition, it was confirmed that advanced active addressable VACNFs on TFTs could be demonstrated for a programmable lab on a chip platform from this work.

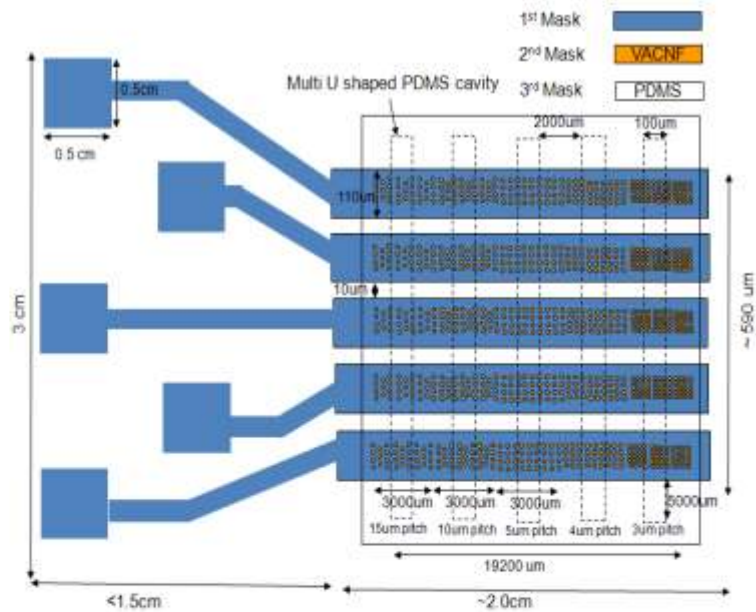


Fig. 6-4. Layout of passive electrowetting scaffold.

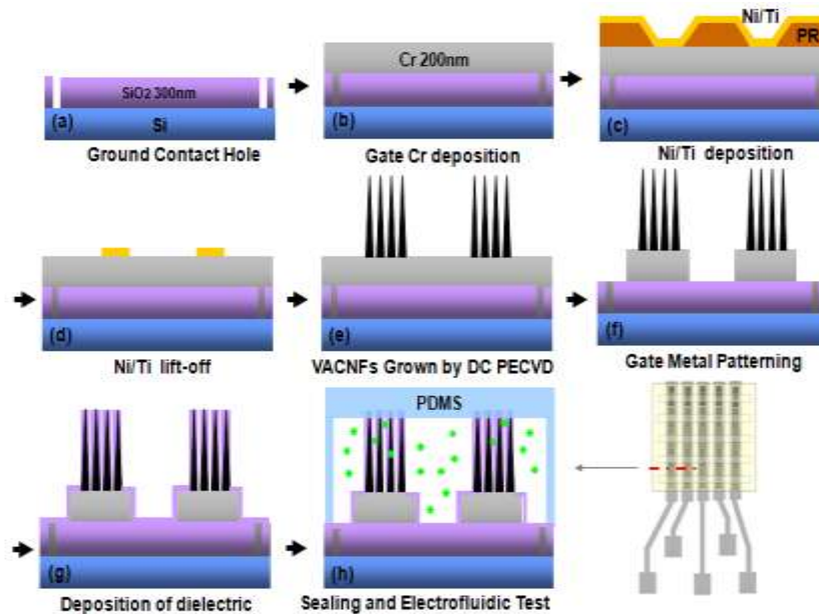


Fig. 6-5. The fabrication process of VACNFs on array for passive electrowetting scaffolds.

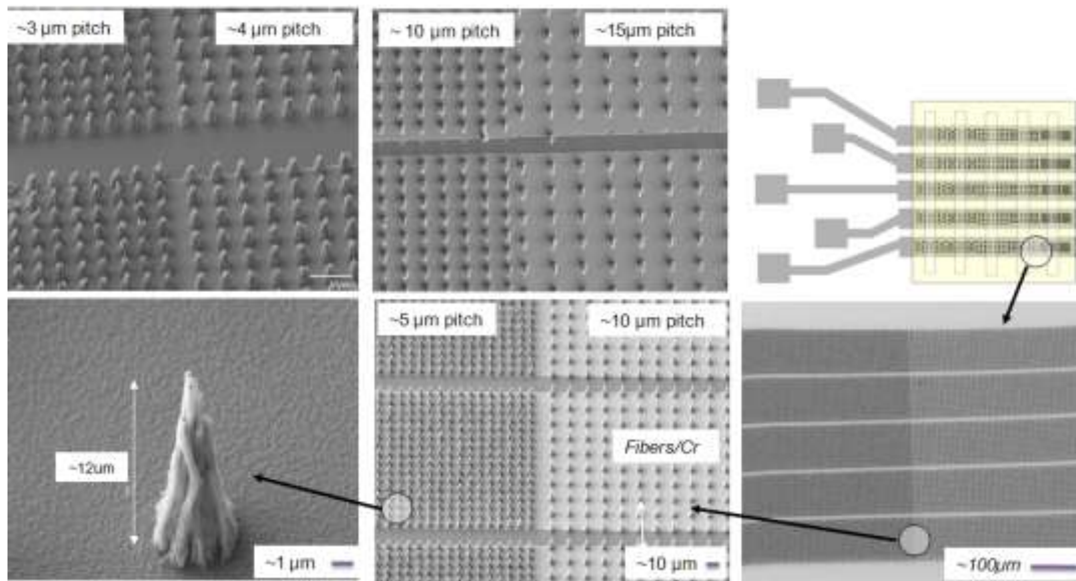


Fig. 6-6. The SEM images of fabricated VACNFs on addressable device with different pitch sizes.

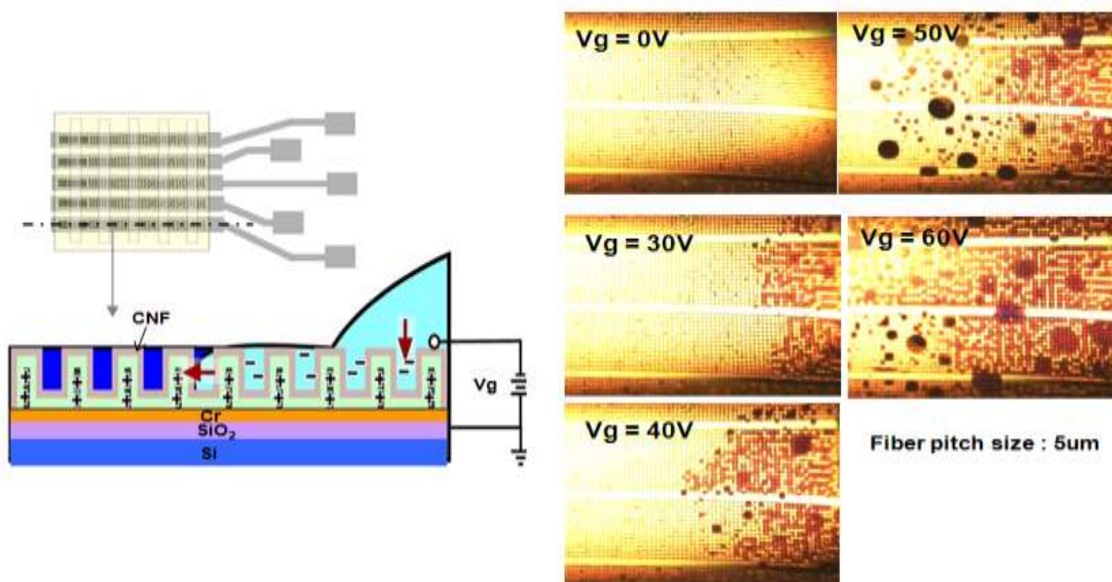


Fig. 6-7. The demonstration of addressable electrowetting device to form agile liquid channels.

6.2.2 Process issues for passive and active addressable electrowetting scaffolds

In this study, there were some critical process issues to overcome for demonstrating the device. These issues were originated from the growth process of VACNFs because the fiber growth process required high temperature process at 700°C. Fig. 6-8 shows the representative process issues to integrate VACNFs on addressable device. First, as shown in Fig. 6-8 (a), the tensile stressed Cr electrode caused the electrode to be peeled off during fiber growth. This delaminating problem was solved by Park *et. al* controlling film stress by applied substrate bias during Cr sputtering (tensile stressed film changed to close zero film stress at ~5W substrate) (Fig. 6-8 (b)) [park dissertation]. Second, the surface charging during fiber growth caused plasma arcing during DC-PECVD growth of fiber growth as shown in Fig. 6-8 (c). This problem is solved by forming ground contact paths (by photolithographically formed holes) between Cr electrode and Si substrate with the structure as shown Fig. 6-5 (a). Fig. 6-8 (d) shows the optical and SEM images in which the arc are solved clearly as well as Cr delaminating issue. Even if some issues are clear on addressable device, the potentially high temperature process for fiber growth caused the device to be degraded. As the VACNFs were integrated on a-Si TFT, necessarily Cr electrode on a-Si (active layer) formed Cr silicides in the active channel degrading electrical performances [88]. Therefore, the plan was changed with new proposed schemes as will be discussed in chapter 6.3 (photoactive polymer posts + a-IGZO TFT).

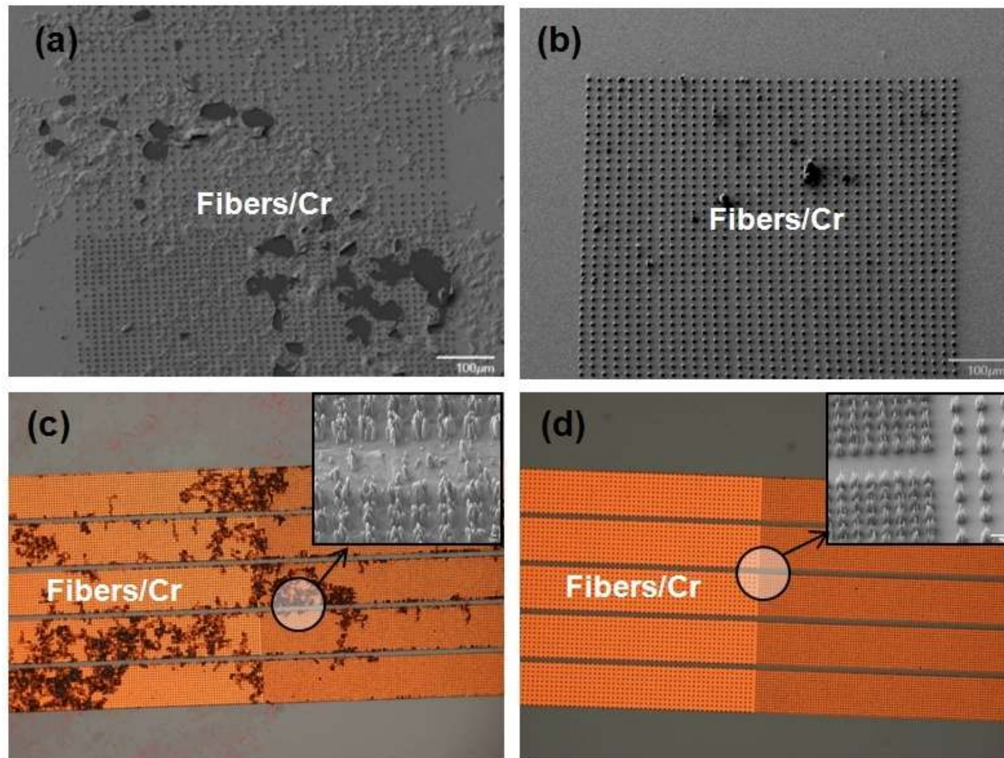


Fig. 6-8. The process issues for addressable electrowetting device, (a) Cr electrode delaminating issue because of tensile Cr film, (b) stress optimized Cr electrode with fibers, (c) surface plasma arcing defect (carbon residues) due to surface plasma charging effect during fiber growth using DC-PECVD , and (d) fiber on Cr after solving plasma arcing by forming ground contact paths.

6.3 Generation II device platform (photoactive polymer posts + a-IGZO TFT)

6.3.1 Electrowetting test using polymer posts

As discussed in chapter 6.2, because of some process issues, the plan to realize the device platform was changed to a device using photoactive polymer posts and a-IGZO TFTs (Generation II). The photoactive polymer instead of VACNFs used for post and transparent a-IGZO TFT will be used for active addressing device instead of a-Si TFT. The polymer post can be easily built on addressable device near room temperature; not degrading the device performance beneath the posts. By using a-IGZO instead of a-Si, the TFT has achieved significantly enhanced electrical performance ($I_{ON/OFF}$ ratio, field effect mobility) relative to the a-Si TFT. While easier integration and enhanced electrical performance expected for polymer post on a-IGZO TFT. In addition, the most attractive benefit is the optical transparency of the a-IGZO which will enable the use of important fluorescence and other optical microscopy techniques in lab-on-chip. Preliminary electrofluidic tests were performed. Fig. 6-9 (a) shows the schematic cross-sectional device structure using polymer posts. DuPont PerMsx negative acting dry film photoresist was laminated with ~21μm in thickness (post height). After exposure and development, the polymer posts are formed. Cu was sputter coated onto the polymer post as conductive material and then 1μm Parylene C dielectric and hydrophobic fluoropolymer were coated on the Cu, respectively. Fig. 6-9 (b) shows the SEM images of the completed post-array; the posts were fabricated on

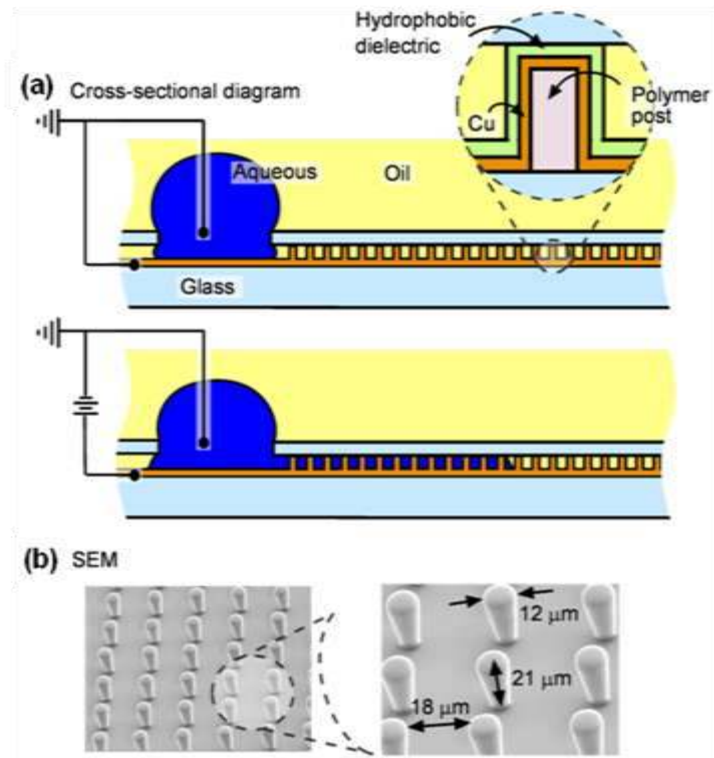


Fig. 6-9. (a) cross-sectional device diagram, (b) SEM image of completed post-arrays.

21μm in height, 12μm in diameter, and 18μm in pitch size. The aqueous liquid (0.1 wt% NaCl) and tetradecane oil were implemented (all space not occupied by aqueous liquid). Fig. 6-10 shows the image of channel formation by post-guided electrowetting, voltage OFF and voltage ON. Applying voltage to top (contacted on the source of aqueous solution (without top electrode) and bottom electrode (Si)) induced the electrowetting channel and move it out along posts because of low contact angle with higher applied voltage. The channel propagation occurs as the contact angle between posts and aqueous liquid has more than 40 V applied in this study. Here, contact angle (θ_V) vs. voltage is predicted by the electrowetting equation $cos\theta_V = (\gamma_{od}-\gamma_{wd})/\gamma_{ao} + CV^2/2\gamma_{ao}$, where C is capacitance per unit area of the hydrophobic dielectric and γ is the interfacial surface tensions between the aqueous liquid (a), oil (o), and the dielectric (d). In order to understand post-guided electrowetting, the effects of the Young-Laplace pressure ($\Delta p = \gamma_{ao} (1/R_1+1/R_2)$) need to combine into a simple predictive equation. However, because of the complex device geometry, only a qualitative description is provided for the post-guided electrowetting. Fig. 6-11 illustrates the qualitative diagrams to explain the mechanism behind post-guided electrowetting. At V=0V, θ_Y imparts a convex meniscus, a positive Δp and therefore the aqueous liquid (blue lines) will clearly not propagate forward. The voltage can then be increased, and the aqueous liquid contact angle reduced by electrowetting on the side-surfaces of the posts and the bottom substrate. However, because the top substrate is not electrowetting, no matter what voltage is applied Δp cannot be inverted (if θ_Y on the top plate is ~170, then θ_V on

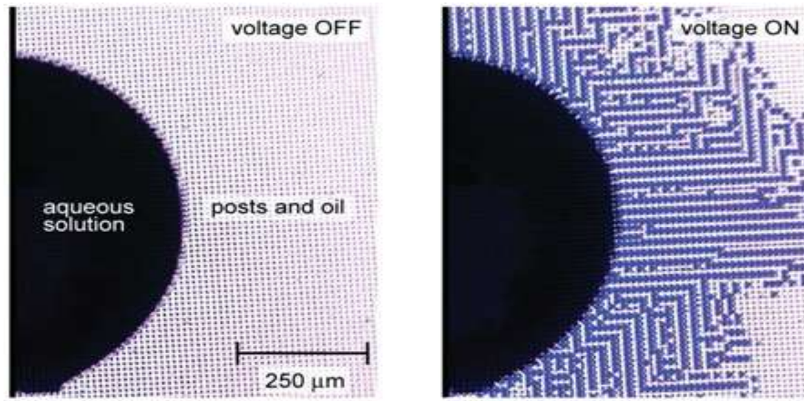


Fig. 6-10. The image of channel formation by post-guided electrowetting, voltage OFF and voltage ON.

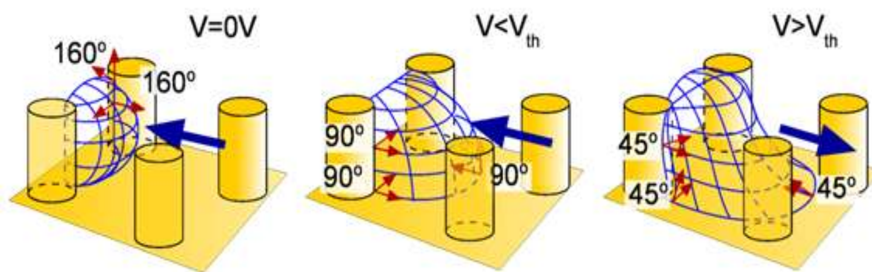


Fig. 6-11. Diagram of the mechanism of post-guided electrowetting.

the bottom would need to be an impossibly small 10°or less). This is where the posts play a critical role. With posts, the system only needs to reach a voltage (V_{TH}) where the electrowetted contact angle θ_V causes the aqeuous contact line to touch the base of the next set of posts. Once the aqueous contact line touches the next set of posts, the contact angle is then transferred from the horizontal substrate to the vertical post surface (a 90°shift). The resulting wetting geometry then inverts Δp and the aqueous liquid moves forward through the posts. In the absence of finite conductivity effects, this ratcheting forward of the aqueous liquid will continue indefinitely, until the voltage is reduced below the threshold voltage. As shown Fig. 6-9(b) and Fig. 6-12, the channels were formed randomly with applied voltage and clearly propagated with increasing voltage. At first glance, one might expect the channel to form continuous wetting in all directions. However, distinct channels are dominant in the experimental results. We believe that the formation of distinct channels is associated to the electromechanical pressure which drives the electrowetting effect. Two adjacent channels are partially screen each other's electric field and slightly reduce the related electromechanical pressure [89]. Therefore, this screen effect strongly affects the random channel propagation. Next, directional channel formation was studied in order to demonstrate preliminary functionality for lab-on-chip. The posts were arranged in particular patterns. As shown in Fig. 6-13, several linear rows of pared post were fabricated, tested at 50V, and time-lapse images were demonstrated. This work demonstrated the preliminary basis for directional flow. The speed of liquid propagation was investigated. The rate of liquid flow was initially ~800-1500 µm/s for all channels, and decreases to ~200 µm s^{-1} after reaching ~1000 µm in length. The average rate of liquid flow was ~ 305 µm s^{-1}.

However, this speed is still very slow compared to conventional droplet- based electrowetting transport (~ 10 cm/s). There are two reasons that appear to be at play. First, the much shorter height (d) and longer length (L) than the channel used in conventional electrowetting lab-on-chip caused the speed of wetting to be slower. Therefore, the increased post height and shorter pitch are expected to increase propagation speed. Second, it is because the channel still connected to large source droplet. The source droplet imparts a very small Δp because of its large radius. By this work, it is confirmed that post-guided electrowetting approach allows for introduction of aqueous liquid into an electrowetting lab-on-chip module without need for syringe-pump pressure. In addition, it is expected that patterned electrodes could be controlled by an underlying array of TFT; active matrix addressing.

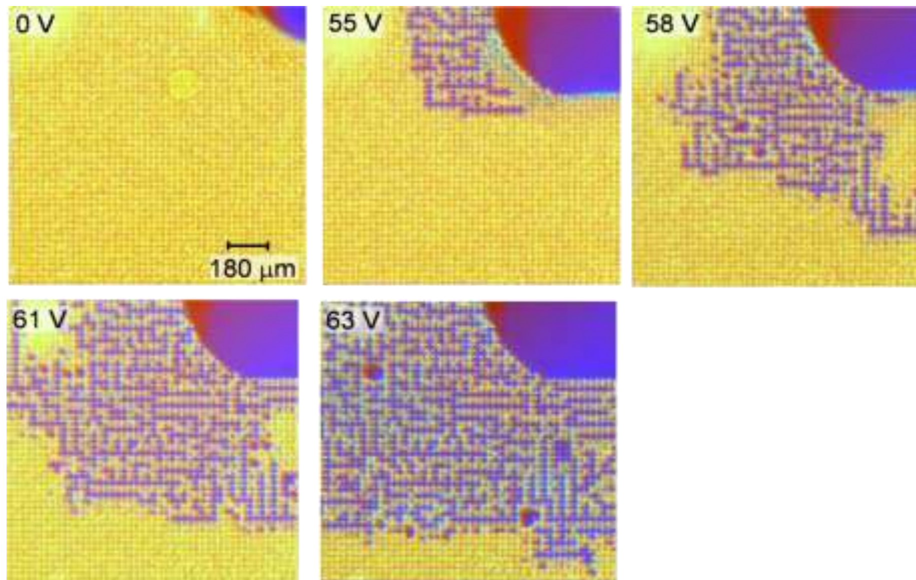


Fig. 6-12. Channel formation and propagation with applied voltage.

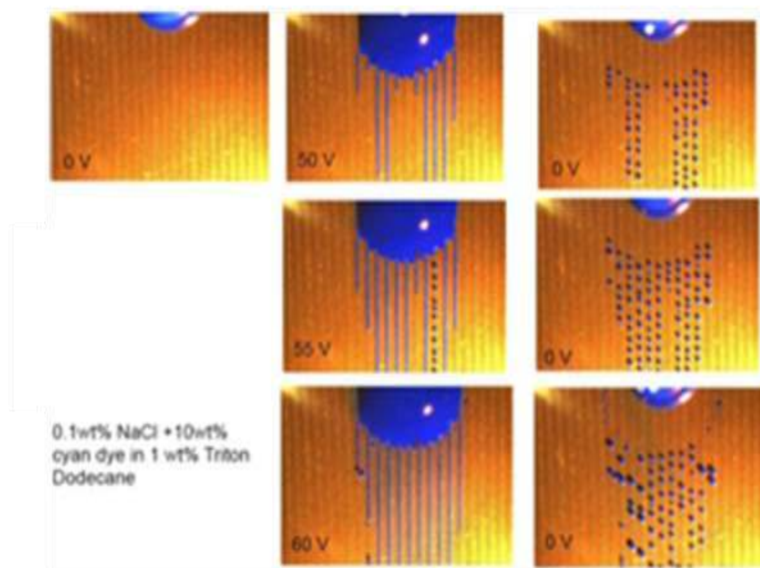


Fig. 6-13. Time lapse photographs of directional channel formation.

6.4 Design and issues of addressable electrowetting microfluidic device

Based on previous plelimiary electrowetting work and robust a-IGZO TFT, the integrate TFT with electrowetting platform(Fig. 6-3) will be demonstrated, which will be agil and re-repragramble device as shown Fig. 6-14.

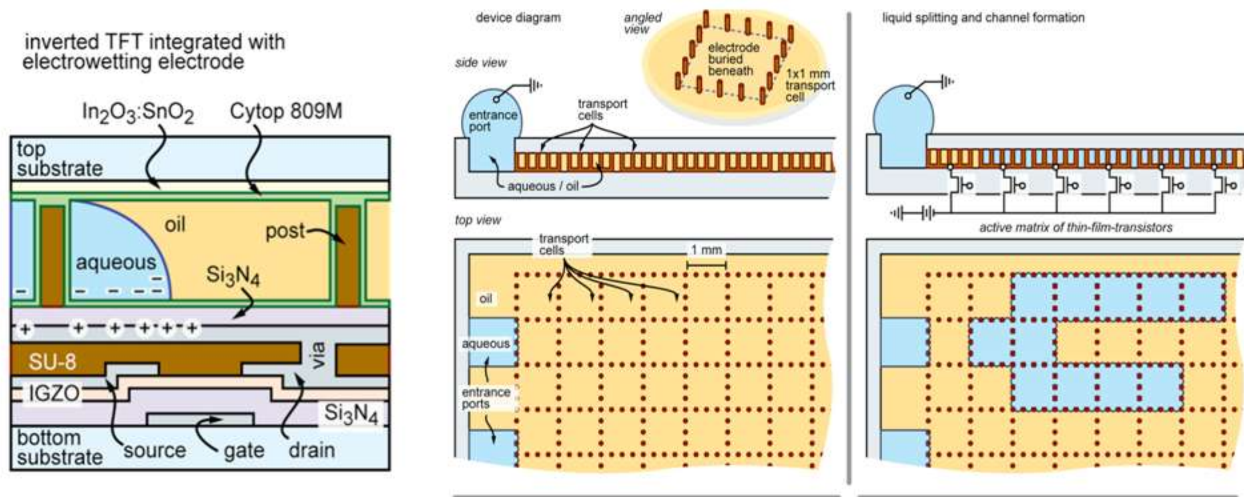


Fig. 6-14. Integrate TFT with electrowetting platform and proposed Agile and Re programable microfluidic device.

6.5 Conclusion

For generation I device platform (VACNFs electrowetting post + a-Si TFTs), the preliminary electrowetting test using carbon nano fiber on addressable elelctrodes were demonstrated. For generation II device platform(photoactive polymer posts + a-IGZO TFTs), to sove process issues and easier process, the elelctrowetting channel device using the photoactive polymer posts were demonstrated.

*Acknowledgment

The work presented in this chapter has been collaborated with Jason Heikenfeld's group and Ian Papautsky in University of Cincinnati. The VACNFs array processes were performed in Center for Nanophase Materials Science of Oakridge National Laboratory by myself in which the carbon nanofibers were grown by Dale Hensley and advised by Anatoli Melechko. Manjeet Dhindsa fabricated the following electrowetting channel on carbon nanofibers and tested the agile liquid channel. The work presented in chapter 6.3, electrowetting test using polymer posts, was performed by Heikenfeld group as preliminary test for following active addressable electrowetting channel device and has been published previously in Lab on a Chip by Manjeet Dhinsa, Jason Heikenfeld, myself, Jung won Park, Philip Rack, and Ian Papautsk [90]. Philip Rack provided direction, funding of the research, discussion and motivation.

Chapter 7

Conclusion

In this dissertation characterization and fabrication of active matrix thin film transistors using a-IGZO as semiconductor was studied. Potential application includes an addressable microfluidic electrowetting channel device. Material characterization was performed to optimize the fabrication of a-IGZO TFT, suggesting the best process conditions in each TFT process to achieve a robust a-IGZO TFT for application. The summary suggested for optimum a-IGZO TFT was listed in Table 7-1.

The BCE type with an inverted staggered bottom gate structure was used for a-IGZO TFTs for better electrical performance. Cr metal was used for gate because of low electrical resistivity and easy wet etching process and gate dielectric (SiN_x) was deposited by PECVD. a-IGZO as semiconductor was deposited by rf sputtering and patterned. S/D pad using Cr was deposited by rf sputtering and patterned by wet etching method. To contact gate, the via hole was formed by dry etching method. Finally, the device was post annealed at 350°C in N_2 ambient for 1hr.

To achieve high performance gate dielectric, the gate dielectric with different stoichiometric SiN_x and SiO_2 were optically and electrically analyzed. The optical properties were significantly dependent on the gas ratio (NH_3/SiH_4); the SiN_x1 deposited with highest NH_3 gas shows highest transmittance and optical band gap because of increased N/Si ratio. The SiN_x1 and SiN_x2 showed the improved electrical characteristics. It was studied that the hysteresis difference in the a-IGZO TFTs is mainly from the contribution of trapped charges in/near the gate dielectric. By studying hysteresis of transfer curve and current –voltage, the film deposited with NH_3/SiH_4 =5.1

as well as SiO_2 film showed best electrical performance; less hysteresis and lower gate leakage current. As a result, the SiN_x1 film and stoichiometric SiO_2 film were expected to be best PECVD deposition for gate dielectric.

a-IGZO films deposited at different powers (60W verse 80W) in this study, revealed that there was only difference in the V_T which is attributed to the increased In content. For increasing PO_2, V_T was increased but the negative ions during sputtering with high oxygen pressure caused the traps in a-IGZO to be increased, resulting in an increase of the relative S value. From this study, the power of 60W and 80W with PO_2 = 0.84mTorr were proposed for optimized sputtering condition for a-IGZO TFTs. For increasing PO_2, it was confirmed that the relative In content in a-IGZO was decreased and oxygen content in a-IGZO was increased by analyzing XPS and in addition, the increased optical band gap was also confirmed with increasing PO_2. By comparing the transmittance in the range of IR, the relative free carrier density in a-IGZO was compared (a-IGZO film deposited with higher PO_2 shows lower carrier concentration; higher transmittance). The annealing of a-IGZO in N_2 shows better electrical performance than in air. The crystallization of a-IGZO occurred at 850°C because of Zn volatilization.

This study showed a powerful method for estimating the electrical properties and optimizing the deposition condition of a-IGZO as a function of the oxygen to IGZO incorporation ratio. The IGZO and O_2 flux during sputtering was calculated on the basis of the deposition rate of IGZO and PO_2, respectively. The transfer curves showed noticeably different results, depending on PO_2 (O_2/IGZO incorporation ratio); the TFT with PO_2 =0.85~1 mTorr (oxygen deficient regime with ~ 1 of O_2/IGZO) revealed the

best transfer curve. However, the TFT with PO_2 > 1.5mTorr (the oxygen-rich regime with 1 < O_2/IGZO) did not show transfer curve. The electrical conductivity of a-IGZO for O_2/IGZO < 1 follows the degenerate conduction model, which depends on the E_C - E_F with oxygen content in a-IGZO. On the other hand, for a-IGZO with 1 > O_2/IGZO, the change in the conductivity versus O_2/IGZO suggests a shift in the conduction mechanism in which we attribute to the percolation conduction model because of the reduced density of states; very few oxygen vacancies exist in the a-IGZO films. The resistivity curve with O_2/IGZO incorporation ratio can be used for the tool to estimate IGZO sputtering conditions for optimum TFT performance.

The characteristics of a-IGZO TFTs were changed with applied substrate bias during a-IGZO rf magnetron sputtering. The increased μ_{FE} value and I_{OFF} with substrate increasing substrate bias was attributed to increased carrier concentration associated with preferential oxygen sputtering. The V_T shifts to lower values and eventually becomes negative with increasing substrate bias due to increased carrier concentration in the a-IGZO and a possible contribution from a decrease in the absorbed oxygen on the a-IGZO because of the lower surface roughness. The S value was significantly increased with increasing substrate bias and is attributed to energetic ion induced bulk trap defects in the a-IGZO film.

It was confirmed that both physical and chemical adsorption affects the a-IGZO channel by studying TFT-IV characteristics with different pressure and analyzing O1S peak from XPS spectra, which mainly affects the V_T instability. The SU-8 spin-coated passivated a-IGZO TFT was compared to a-IGZO TFT with sputtered passivation in which water in SU-8 degrades the TFT performance by diffusing into a-IGZO and acts

as electron trap states and ultimately a donor level. The PECVD SiO_2 passivated a-IGZO devices have increased carrier density and shifted V_T which is attributed to hydrogen in the SiO_2 films which effectively dope the a-IGZO during the annealing process. The sputtered SiO_2 passivation shows better electrical performance. a-IGZO TFTs with the two step a-IGZO deposition (2nd 10nm a-IGZO with PO_2 = 1.5mTorr on 1st 40nm a-IGZO with PO_2=1mTor) shows best electrical performance among all experiment results. Finally, the flux calculations were used to estimate the O2 flux on the active layer. In the case of higher oxygen incorporation rate during sputtered SiO_2 passivation greater than the oxygen incorporation rate in a-IGZO, the transfer curve shows the best electrical properties.

For generation I device platform (VACNFs electrowetting post + a-Si TFTs), the preliminary electrowetting test using carbon nano fiber on addressable elelctrodes were demonstrated. For generation II device platform(photoactive polymer posts + a-IGZO TFTs), to sove process issues and easier process, the elelctrowetting channel device using the photoactive polymer posts were demonstrated.

Table 7-1 The summary of optimum condition for each process of a-IGZO TFT to achieve robust device.

	Optimized condition
TFT structure	BCE type with an inverted staggered bottom gate
Gate dielectric	NH_3 rich SiN_x or stoichiometric SiO_2
Semiconductor	1) Incorporation ratio (I_{O2}/I_{IGZO})=~1 2) 2 step a-IGZO deposition (10nm PO_2=1.5mTorr/ 40nm PO_2=0.84mTorr)
Passivation	Sputtered SiO_2 with $I_{O2,PVX}$ >$I_{IGZO,IGZO}$
Electrowetting microfluidic device	Polymer post on a-IGZO TFT

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Appendix: Run sheet for a-IGZO TFT

Layer	Process	Equipment	Condition	Time	Remark
Wafer	Stress check	Stress measurement			
Buffer	INI Cleaning	Cleaner			
	PECVD (SiO2:500nm)	PECVD (oxford) [Silicon dioxide]	RF:20W SiH_4/N_2O(85/157) Pressure: 1000 mTorr Temp: 350oC	7min15sec	Stress:
	Post Cleaning	Spin cleaner	DI water		
Gate	Deposition (Cr:100nm)	Sputter (#4)	RF: 200W(~380V)/5W(121 V) Gas: Ar(25) Pressure: 5mT Temp: RT	40min	RS=~0.85 Ω
	Precleaning	Hand cleaning	DI water		
	Cr pattern	Spinner Aligner(pressure mode)	SPR 2.1 (w/o primer) 3000 rpm, 45 sec PreBake: 90°C, 90 sec Exposure time=8 sec PEB: 115°C, 90sec Develop:60 sec		PR =1.7 um, Lamp density= 11 W/cm2
	Cr etch	Wet etch	Cr 14S etchant (R.T)	2min 20sec	
	PR stripping	Stripper	10min		
	Descum	Technics RIE	100W	30sec	
	Post Cleaning	Spin cleaner	DI water		

Active	gate dielectric	PECVD (oxford) [SiNx]	RF: 40W Gas: $SiH_4/NH_3/N_2$(150/38//790) Pressure: 600 mTorr Temp: 350°C	21min 18sec	
	Post Cleaning	Spin cleaner	DI water		
	active layer (IGZO:50nm)	Sputter (#3)	RF: 60W Gas: Ar/O2 = 20/5 Pressure: 5mTorr Temp: RT		
	CPVX	Sputter (#1)	RF: 200W(188~189V), PO2=1.12mTorr Gas: Ar/O2 = 25/7.2 Pressure: 5mTorr Temp: RT	78min	
	Active pattern	Spinner Aligner(pressure mode)	SPR2.1 (w/ primer) 3000 rpm, 60 sec PreBake: 90°C, 90 sec Exposure time=10sec PEB: 115°C, 90sec Develop:60		
	Descum	Technics RIE	100W	30sec	
	a-IGZO wet etch	Wet etch	HF (10:1) : 0.1%	40sec	
	PR strippin	Acetone with US	1min		
	Post cleaning	Spin cleaner	DI water		
S/D	Deposition (Cr:200nm)	Sputter (#4)	RF: 200W(250V)/5W(125V) Gas: Ar(25) Pressure: 5mT,Temp: RT	40min	
	Precleaning	Spin cleaner	DI water		
	Cr pattern	Spinner Aligner(pressure mode)	SPR2.1 (w/ primer) 3000 rpm, 60 sec PreBake: 90°C, 90 sec Exposure time=9sec PEB: 115°C, 90sec Develop:60		
	S/D etch	Wet station	Cr 14S etchant (R.T)	End+10sec	
	PR strip	Acetone with US	1min		
	Post Cleaning	Spin cleaner			

PVX	Precleaning	Spin cleaner	DI water		
	Via hole pattern	spinner aligner(pressure mode)	SPR 2.1 (w primer),3000 rpm, 60 sec PreBake: 90oC, 90 sec Exposure time=25 sec PEB: 115oC, 90sec Develop time: 60sec		
	Descum	Technics RIE	RF:100W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	Wet etch	Wet station	HF (10:1)	1min 30sec	
	Dry etch	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	1min 30sed	
	Descum	Technics RIE	RF:100W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	PR strip	Stripper	10min		
	Post Cleaning	Cleaner			
ANL	Annealing	Tube quartz furnace in UT	350oC, N2	1hr	
Measurement	TFT-IV	Probe station			

Vita

Seyeoul Kwon received the B.S degree and M.S degree in ceramic engineering from Hanyang University, Seoul, South Korea, in 2000 and 2002, respectively. From 2002 to 2004, he worked at TFT-LCD R&D center in BOE hydis, Ichon, South Korea, where he worked as thin film process engineer developing AMLCDs using polycrystalline thin film transistors. From 2005 to 2006, he worked at display R&D center in Samsung SDI, Yongin, South Korea, where he worked as process integration engineer for flexible display using AMOLEDs with metal foil substrate and thin film engineer for developing AMOLED display using polycrystalline thin film transistors. He received the Ph.D degree in materials science and engineering in 2010, Knoxville, TN, USA. His research interests include the characterization and fabrication of active matrix thin film transistors and an addressable microfluidic electrowetting channel device for application.