Characterization and reduction of microfabrication-induced decoherence in superconducting quantum circuits

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(Dated: February 3, 2022)

Many superconducting qubits are highly sensitive to dielectric loss, making the fabrication of coherent quantum circuits challenging. To elucidate this issue, we characterize the interfaces and surfaces of superconducting coplanar waveguide resonators and study the associated microwave loss. We show that contamination induced by traditional qubit lift-off processing is particularly detrimental to quality factors without proper substrate cleaning, while roughness plays at most a small role. Aggressive surface treatment is shown to damage the crystalline substrate and degrade resonator quality. We also introduce methods to characterize and remove ultra-thin resist residue, providing a way to quantify and minimize remnant sources of loss on device surfaces.

arXiv:1407.4769v1 [cond-mat.mes-hall] 17 Jul 2014

Improving the coherence times of superconducting qubits is of central importance for pushing quantum integrated circuits to a practical level of fault-tolerance for quantum computation,[1–4] as even moderate improvements to coherence can drastically reduce the overhead required for quantum error correction.[1,4] Substantial evidence has pointed to dielectric loss and fluctuations due to two-level system (TLS) tunneling defects[5,6] as a source of energy relaxation in superconducting qubits and noise in sensitive superconducting photon detectors.[7–18] These studies strongly suggest that TLS defects are located not in the bulk, but at the interfaces between device substrate, metal and vacuum, and that they can vary significantly with device materials, though the precise reason for this variation is usually a matter of speculation. The impact of TLS can be mitigated by increasing circuit dimensions,[9,14,19] but this strategy cannot be continued indefinitely. Nonetheless, the variable nature of the TLS-hosting circuit interfaces has not been carefully analyzed.

Here, we use superconducting resonators as sensitive probes to study TLS dielectric loss as a function of the processing used to construct these circuits, while concurrently analyzing the substrate-metal (S-M), substrate-vacuum (S-V), and metal-vacuum (M-V) interfaces. This allows us to separately extract the contributions of chemical contamination and induced disorder at the S-M interfaces of superconducting aluminum coplanar waveguide (CPW) resonators. In particular, we show how traditional processing methods can limit internal quality factors Q_i to the range of $10^5 - 10^6$ at single-photon operating powers where TLS effects dominate. In addition, by characterizing resist residue we predict that without careful post-processing techniques, residual films of e-beam resist polymer on the vacuum interfaces may soon start to limit state-of-the-art superconducting qubit lifetimes.

We expect that measurements of resonator Q_i will be predictive of dielectric loss in similarly fabricated superconducting qubits for two reasons: superconducting CPW resonator Q_i are limited by energy relaxation and predict excitation lifetimes T_1 at single-photon powers,[10,18,20] and the large single-layer shunt capacitors of many superconducting qubits, such as the transmon, have interface participation ratios and hence dielectric losses comparable to those of a CPW.[16,19,21–23]

Transmon qubit capacitors have traditionally been fabricated using lift-off aluminum deposited together with their double-angle-evaporated Josephson junctions: first a ground plane is etched at the desired location of the qubit, and then electron-beam lithography is used to define the qubit pattern that is subsequently evaporated onto the etched substrate.[24–26] This means that the capacitor's S-M interface sees more processing than it would if the capacitor were formed by a subtractive etch alone. Improved coherence times have recently been found in transmons using lift-off metal for only a small fraction of the qubit,[16,17] where the capacitors are first formed by an etch and the Josephson junctions are later evaporated after ion-milling the initial layer to remove native oxide and establish superconducting contact. In such a process, only a small fraction ($\sim 1\,\%$) of the qubit self-capacitance is formed with lift-off metal,[27] and accordingly any extra dielectric loss induced by lift-off processing should be reduced by a similar factor. A systematic test to compare these two processes while keeping all other parameters constant, including metal type and growth conditions, has not been performed and could reveal information useful for improving qubit coherence.

We perform such a controlled study by comparing the quality factors of CPW resonators fabricated with transmon-style lift-off versus a pure etch, both on the same chip, as follows. First, a polished *c*-plane sapphire wafer is solvent-cleaned,[28] and a base layer of aluminum is deposited in a high vacuum (HV) electron-beam evaporator after a gentle *in situ* argon ion beam clean. Photolithography and a BCl_3/Cl_2 inductively coupled plasma (ICP) etch are then used to define $\lambda/2$ CPW resonators coupled to a feedline [Fig. 1(a)]. During this etch the ground plane slot of total width $W + 2G$ is defined for "lift-off resonators"; the center traces of width W for these resonators are deposited later with a lift-off

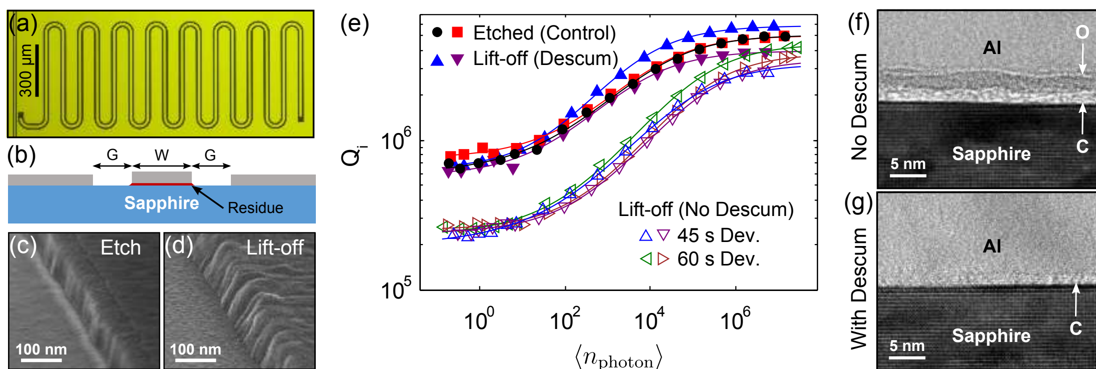

Figure 1. Etch versus lift-off, and descum versus no descum: low-power Q_i is degraded using lift-off without descum. (a) Optical micrograph of a "hanging" $\lambda/2$ CPW resonator capacitively coupled to a feedline (left). (b) Schematic of lift-off resonator cross-section. (c/d) SEM image of center trace edge of an etched/lift-off resonator. Etched metal sidewall is nearly vertical, with slight etching on the metal due to resist delamination, while lift-off metal sidewall has angle $\sim 25°$ from vertical. (e) Plot of internal quality factor Q_i versus mean photon population for resonators made with lift-off with and without a pre-deposition descum, as well as for etched control resonators. Different marker types represent distinct resonators. Solid lines are guides to the eye. (f/g) Edge-on cross-sectional HRTEM image of S-M interface that saw processing similar to that of the lift-off resonators without/with descum. TEM sample (~ 50 nm thick) prepared via gallium focused ion beam lift-out. Elemental peaks in C and O from qualitative EELS scans across the interfaces are indicated.

technique [Fig. 1(b)]. During the ICP etch, as an on-chip control for the experiment the entire CPW structure (including the center trace) is defined for purely etched resonators. The center traces for the lift-off resonators are then defined in a way that mimics conventional transmon capacitor fabrication: the wafer is solvent-cleaned and then dehydration-baked[29] and allowed to cool, after which a bilayer of 950K PMMA atop copolymer MMA(8.5)MAA e-beam resists are spun, each baked at 160 °C for 10 minutes. The center traces are then defined with e-beam lithography,[30] after which the bilayer is developed with various development times in a 1:3 mixture of methyl isobutyl ketone (MIBK) to isopropanol (IPA), followed by a 10 second IPA dip and thorough nitrogen blow-dry. After development, the surface is optionally treated with a downstream oxygen ash descum before center trace deposition. During this descum,[31] the substrate is heated to 150 °C and sees purely chemical cleaning with reactive oxygen, but not ions or plasma. We note that this cleaning is *ex situ* with respect to the subsequent center trace deposition. The wafer is then transferred to and pumped overnight in the same HV e-beam evaporator used for the initial ground plane deposition, and the center traces are then deposited *without* an *in situ* clean. The metal is then lifted off in N-Methyl-2-pyrrolidone (NMP) at 80 °C (3 hrs.) and cleaned in IPA.

The resonator chip is wirebonded into an aluminum sample box, which is mounted on the 50 mK stage of an adiabatic demagnetization refrigerator equipped with sufficient filtering and shielding so that radiation and magnetic vortex losses are negligible.[15,32] All resonators had $W, G = 15, 10\,\mu$m with frequencies near 6 GHz. Using a feedline[15] allows us to reproducibly extract Q_i for multiple lift-off and etched resonators on the same chip. The resulting internal resonator quality factors are shown in Fig. 1(e). The decrease and saturation of Q_i at low powers for all resonators is consistent with TLS-dominated loss. A clear difference (factor of 3) is observed in low-power Q_i between the etched resonators and the lift-off resonators without descum. As seen in Fig. 1(e), the descum increases the low-power Q_i back to or slightly below that of the control resonators. These measurements suggest that the edge profile of the resonators [Fig. 1(c/d)] had a negligible effect on loss at this level of coherence. It is also apparent that roughness of the S-M interface had a minimal effect on loss: the substrate under the center trace of the lift-off resonators was previously etched,[33] and is three times rougher than that under the center trace of the control resonators (0.3 versus 0.1 nm RMS roughness as measured by AFM).

To help understand the increased loss in the lift-off resonators, which we attribute to a contaminated S-M interface, we use cross-sectional high-resolution transmission electron microscopy (HRTEM) to examine the S-M interfaces of samples that saw similar[34] processing to the center traces of the lift-off resonators without/with the descum [Fig. 1(f/g)]. With no descum, we observe two sublayers at the S-M interface. Directly above the substrate is a film of average thickness 1.6 nm, presumably residual resist polymer, which shows a peak in carbon content when probed with electron energy loss spectroscopy (EELS). Above this, a ~ 2 nm layer with similar phase contrast to aluminum oxide is observed, accompanied by a peak in oxygen content when probed with EELS. This layer is likely formed by a reaction of the unpassivated Al with resist and/or solvent residue either as the metal is evaporated onto the substrate, or during a later processing step when the wafer is heated. As such, it may contain contaminants such as hydrogen that may increase dielectric loss through the introduction of GHz-frequency TLS defects.[7,35–37] Oxide contamination from residue may be relevant to previous experiments finding that thermally oxidized submicron Josephson junctions are made significantly more stable by cleaning the sub-

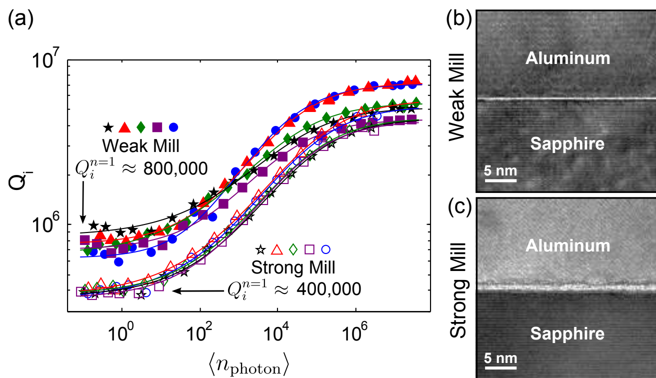

Figure 2. Comparison of weak and strong ion beam treatment, the latter inducing resonator degradation. (a) Q_i of etched CPW resonators whose bare substrates saw weak or strong *in situ* ion milling before base metal deposition (five resonators of each). (b/c) Cross-sectional HRTEM of S-M interface for weak/strong ion mill, showing thicker disordered interfacial layer for strong mill.

strate with oxygen plasma before metal deposition.[38,39]

The S-M interface of the descummed substrate on the other hand shows a decreased average thickness[40] of carbon-containing residue and no observed peak in oxygen content. We note that our data is not sufficient to determine whether or not the decrease in carbon residue is in direct proportion to the decrease in resonator loss.

In situ descum techniques such as ion beam cleaning may perform similarly to the downstream ash explored here. However, as this involves physical bombardment, a cleaning which is too aggressive might degrade the substrate quality at the interface. To test this hypothesis independently from questions of resist residue contamination, we fabricate etched superconducting $\lambda/4$ resonators whose substrates saw different strengths of *in situ* argon ion beam cleaning prior to the base aluminum deposition: a weak clean (beam energy 200 eV, dose $\sim 5\times10^{15}\,\mathrm{cm}^{-2}$) and a stronger mill (beam energy 400 eV and dose $\sim 5\times10^{17}\,\mathrm{cm}^{-2}$). The stronger parameters are identical to those used to etch away native AlO_x in the fabrication of Xmon transmon qubits[16] and similar to those used for substrate preparation in previous planar superconducting resonator experiments.[41] The resulting resonator quality factors are shown in Fig. 2(a), and display a power dependence consistent with TLS-dominated loss at low powers. We observe a clear difference (factor of 2) between the low-power internal quality factors, with the *stronger* ion beam yielding a lower Q_i.

Fig. 2(b/c) shows cross-sectional HRTEM images of the S-M interface for the weak/strong ion beam treatments. The strong mill creates a ~ 1.2 nm interfacial layer, significantly thicker than the weakly-treated interface of unresolvable thickness. EELS reveals no measurable elemental peaks at either interface, including Ar, C, and O. We do not believe the uniform interface is an artifact of surface roughness, as AFM scans reveal no change in roughness between a bare and a strongly milled wafer, consistent with literature on sapphire.[42] We therefore attribute the excess loss to TLS induced by sapphire amorphization. Using finite-element COMSOL simulations,[19] assuming a relative permittivity $\epsilon_r = 10$ for this layer we extract an intrinsic TLS loss tangent $\delta^0_{\mathrm{TLS}} \sim 1\times10^{-2}$.[43]

Returning to Fig. 1(f), one may ask which of the interfacial sublayers of the lift-off resonators dominates the added loss, which could help inform future superconducting qubit fabrication. COMSOL simulations suggest that the added loss in the lift-off resonators without descum could be explained by a 2 nm thick interface with $\epsilon_r = 2$ (e.g., e-beam resist) and $\delta^0_{\mathrm{TLS}} = 3\times10^{-3}$, or with $\epsilon_r = 10$ (e.g., AlO_x) and $\delta^0_{\mathrm{TLS}} = 1.5\times10^{-2}$. In light of this, we more directly extract δ^0_{TLS} for the contamination by trapping it in a parallel plate capacitor, as illustrated in Fig. 3. The bottom plate of the capacitor (formed by part of the aluminum ground plane) is thoroughly cleaned, and then copolymer e-beam resist is spun, exposed and developed, after which the top capacitor plate is deposited along with the CPW center trace, trapping any residue. By forming a large (but physically small and thus lumped element) load capacitance C_L at the end of a $\lambda/4$ CPW transmission line resonator, its net capacitance and loss tangent can be extracted from the shift in resonator frequency and the quality factor. We derive analytical expressions for the load-dominated frequency shift and quality factor in the limit $C_L \gg C_{\mathrm{CPW}}$, where C_{CPW} is the total capacitance to ground of the CPW segment of the resonator. We model the lossy load capacitor as an ideal capacitor with an effective series resistance, $R_{ESR} = \tan\delta/\omega C_L$. For a single-dielectric C_L,

$$\omega_r - \omega_{\lambda/4} \approx \frac{2}{\pi C_L Z_r}, \qquad Q \approx \frac{1}{2\tan\delta} C_{\mathrm{CPW}} C_{\mathrm{L}} \omega^2 Z_r^2. \quad (1)$$

Numerical SPICE simulations indicate that these expression are accurate to 1% and 5%, respectively, for our experimental conditions. For a capacitor with more than one dielectric layer, voltage division allows one to extract the capacitance and $\tan\delta$ of one layer given those of the other. Using this fact and taking into account uncertainty in the thickness (3.3 - 4.0 nm),[44] ϵ_r (9 - 10), and δ^0_{TLS} $(0.7 - 1.6\times10^{-3})$[7,35,45,46] of the bottom native[47] AlO_x layer, we conclude that the net δ^0_{TLS} of the contamination is in the range $1.6 - 3.6\times10^{-3}$.

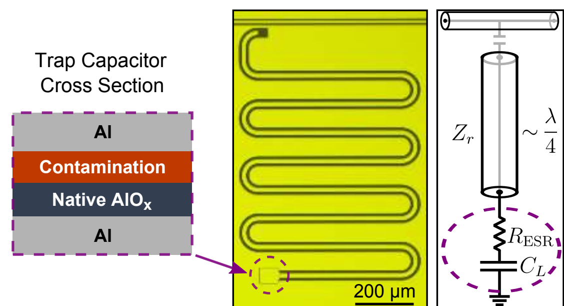

Figure 3. Schematic of "trap capacitor" experiment to characterize resist contamination. Left: capacitor cross-section. Middle: Optical micrograph of device. Right: Equivalent circuit diagram.

We can compare this contamination loss tangent with that of bulk copolymer resist at low temperature and power. To measure $\delta^0_{\rm TLS}$ of the bulk resist, we spin-coat CPW resonators with 500 nm of copolymer, using the same 160 °C bake. From the resulting frequency shifts and low-power Q_i of hanging $\lambda/4$ CPW resonators with multiple geometries, we extract (by simulating the capacitance per unit length of the coated resonator cross-sections in COMSOL) for the copolymer $\epsilon_r = 2.6 \pm 0.1$ and $\delta^0_{\rm TLS} = (5.1 \pm 0.3) \times 10^{-4}$. This loss is too small to quantitatively predict $\delta^0_{\rm TLS}$ of the contamination layer extracted from the lift-off resonators or the trap capacitor. We conclude either that the lift-off loss comes from the oxide sublayer [Fig. 1(f)] or that $\delta^0_{\rm TLS}$ of residue exposed to an e-beam is higher than that of the bulk polymer.

To test the effect of exposure, we expose the resist-coated chip in deep ultraviolet (DUV) light sufficient to expose copolymer for development.[48] We then repeat the measurements, observing a modestly increased bulk $\delta^0_{\rm TLS}$ of $(7.7 \pm 0.5) \times 10^{-4}$ with no measurable shift in ϵ_r, still insufficient to quantitatively explain the contamination loss. Although PMMA has a very similar polymer fragmentation pathway and molecular weight distribution upon DUV exposure as it does for e-beam exposure,[49] ultra-thin polymer films may have significantly different properties from the bulk, due for example to interaction with the substrate.[50–52] We are thus unable to definitively conclude whether the polymer itself or contaminated AlO_x dominated the loss in the lift-off resonators.

The question of oxide contamination deserves further study, but in any case, it would be useful to detect and remove residual polymer, including on the vacuum interfaces. Previous interface participation simulations[19] have focused on interfacial $\epsilon_r = 10$, for which the S-M and S-V interfaces participate equally and the M-V interface (i.e., surface oxide) is negligible. However, as shown in Fig. 4, the relative dielectric participation of the three CPW interface types depends strongly on the effective interfacial ϵ_r. Note that S-M contamination is particularly

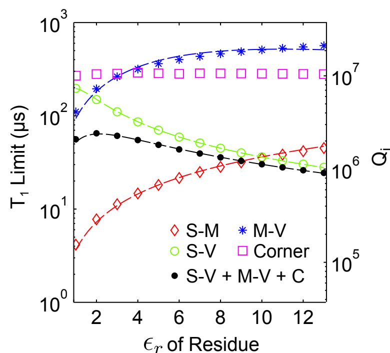

Figure 4. Markers: COMSOL simulations of the $T_1 = Q/\omega$ limit at 6 GHz due to loss at the different types of CPW interfaces (considering separately "corners" where the interface types intersect[19]), as a function of ϵ_r of the interface, assuming a $W, G = 15, 10\,\mu$m untrenched CPW resonator with 3 nm thick interfaces of $\tan\delta = 2 \times 10^{-3}$, with $\epsilon_r^{\rm substrate} = 10$. Lines are fits to a simple model.[19]

Table I. Unexposed resist residue thicknesses of e-beam resist [MicroChem copolymer MMA(8.5)MAA) EL9] and i-line photoresist (Megaposit™ SPR955-CM) on sapphire, aluminum, and silicon, measured by ellipsometry (native oxides are accounted for).

Unexposed Resist Residue (±0.3 nm)	Post-strip (nm)	Post-descum (nm)
E-beam resist on Sapphire	4.2[a]	0.0[b]
E-beam resist on Sapphire	2.5[c]	0.0[b]
E-beam resist on Aluminum	2.8[c]	0.1[b]
E-beam resist on Silicon	3.9[a]	1.6/0.0[d]
E-beam resist on Silicon	0.4[c]	0.0[b]
Photoresist on Sapphire	0.2[a]	0.1[b]
Photoresist on Silicon	0.1[a]	0.1[b]
Photoresist on Aluminum	0.6[a]	0.1[b]

[a] 5 min. ultrasonic agitation in acetone then IPA; spin dry.
[b] 1 min. Gasonics downstream oxygen ash at 150 °C.
[c] 1 hour soak in heated NMP (∼ 70 °C), followed by 5 min. ultrasonic agitation in heated NMP then IPA; spin dry.
[d] UV-Ozone clean for 10/20 min., respectively.

detrimental at low ϵ_r. We also see that post-processing residue on the substrate and even on the metal may start to limit coherence near the 100 μs level for planar transmon qubits of modestly large size. It would therefore be useful to characterize the presence of residual films.

To detect and eliminate post-processing residue, we use variable angle spectroscopic ellipsometry to measure, on various surfaces, the ultra-thin residual films left by unprocessed e-beam resist and photoresist. Here, the resist is spin-coated onto a clean surface, baked, and then stripped. The results are summarized in Table I and are reproducible. We observe that the e-beam resist leaves substantially more residue than the photoresist, perhaps in part due to its higher bake temperature (160 °C versus 95 °C), justifying the assumption of 3 nm for the S-V and M-V interfaces in Fig. 4, although the nature of leftover resist residue may depend strongly on any previous processing steps. Ultra-thin residue at the vacuum interfaces, then, may soon start to affect transmon lifetimes.

From Table I it is evident that some form of oxygen treatment is needed to completely remove the residual films. We note that UV-Ozone cleaning (row 4) is an effective alternative method that doesn't involve heating the substrate, which may be preferable for post-processing devices with Josephson junctions.[39] We do not observe any statistically significant change in Q_i at the ∼ 1 million level after post-downstream-ashing the etched control resonators (which saw e-beam resist). Higher-quality epitaxial aluminum resonators[15,53] would be necessary to detect improvement or degradation due to this vacuum-interface residue or post-downstream-ashing. We do however observe a significant decrease in low-power Q_i (to ∼ 200,000) upon post-treating the etched resonators in a Technics PE-IIA oxygen plasma etch system (300 mT O_2, 100 W power for 30 sec., a common "descum" recipe), for reasons yet to be determined.

In conclusion, we have investigated the effects of interface processing on planar superconducting circuit coherence at the $Q_i = 10^5 - 10^6$ level at single-photon powers.

At the S-M interface, we showed that contamination from resist residue and substrate damage from ion bombardment both significantly degrade resonator quality, while substrate roughness had a minimal effect. At the S-V and M-V interfaces, without oxygen treatment we observe post-processing residue at the vacuum interfaces that may start to limit planar superconducting qubit coherence at the level of $Q_i \sim$ several million, but find that post-treatment with aggressive oxygen plasma significantly degrades resonator quality. It would be worthwhile to test the effect of gentler types of post-ashing techniques on the coherence of superconducting qubits, about which there have only been anecdotal reports but no systematic study.[54] It would also be important to investigate the influence, if any, of residual films and substrate damage on SQUID flux noise and other superconducting qubit dephasing mechanisms.[18,55–58] Such post-processing studies will likely play an important role in further improving superconducting circuit coherence.

We thank B. Thibeault, U. Sharma, and C. Palmstrøm for helpful discussions. Devices were fabricated at the UCSB Nanofabrication Facility, a part of the NSF-funded National Nanotechnology Infrastructure Network, and at the NanoStructures Cleanroom Facility. HRTEM and EELS were performed at the facilities of Evans Analytical Group in Sunnyvale, CA. This research was funded by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), through Army Research Office Grant No. W911NF-09-1-0375. All statements of fact, opinion, or conclusions contained herein are those of the authors and should not be construed as representing the official views or policies of IARPA, the ODNI, or the U.S. Government.

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[27]This neglects the Josephson junction itself, but experiments suggest that ultrasmall junctions exhibit remarkably low loss,[14,59] presumably due to statistical avoidance of TLS.
[28]5 min. sonication in acetone and then isopropanol [IPA]; spin dry.
[29]4 min. on a hotplate at 115 °C.
[30]100 kV, 2 nA beam; dose 2000 μC/cm^2. Copolymer thickness 500 nm, PMMA thickness 300 nm.

[31] 3 min. in a Gasonics Aura 2000-LL downstream asher. We found it necessary to pre-clean the tool's chamber with a stronger recipe to obtain consistent descum results at the relatively low 150 °C.

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