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Characterization of a 4H-SiC High Power Density Controlled Current Limiter

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Keyword: Current limiter, JFET, serial protection device, high voltage, electrical characterization.

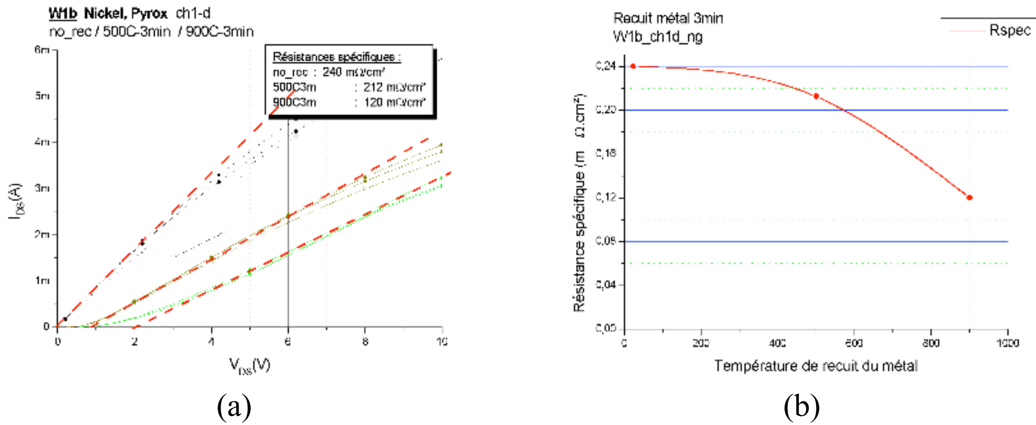
Abstract: Critical steps for the fabrication of SiC devices are thermal annealing and metal ohmic contact formation. Metal annealing effect on the electrical characteristics of the current limiter underlines the necessity to control this device fabrication step. Measurements of contact resistivity as a function of temperature demonstrate the stability of the N type Ni/SiC contact in the range of 175 K – 450 K as its value remains constant around 40 $\mu\Omega.cm^2$. Post implantation annealing effect on the sheet resistance (R_{sh}) shows that a 1700°C/30 min annealing gives better trade off in terms of dopant activation and surface roughness. High power density has been measured up to 600 V. Current thermal stability has been measured for an applied drain to source voltage of 100 V and exhibits high power density capabilities of SiC VJFET as a controlled current limiter.

Introduction.

Considering fault current limiters for serial protection, a lot of structures exist, from regulation to other complex systems such as circuit breakers, mechanical switches or more conventional fuses. Up to now, only few silicon [1,2] or silicon carbide [3,4] semiconductor current limiter structures were described in papers. This device was designed for serial circuit protection in order to limit I^2t value. Although SiC semiconductor based devices are very suitable for high current and high voltage systems [5,6], a promising application of SiC-based devices are the fault current limiters for power system protection, which benefit from its high thermal conductivity (l = 4.9 $W\times cm^{-1}\times K^{-1}$) and wide band gap energy (E_g = 3 eV). This work is devoted to the design, fabrication and characterization of a new etched VJFET [7], which implements both gate and source in buried layers. As in steady state the voltage drop across the component must be as low as possible, in the active state (limiting phase) a current limiter must sustain a high current, under high voltage bias. The resulting high power density must not cause the failure of the component. In this paper, ohmic contact formation and their thermal stability are presented. Then the device thermal stability under constant voltage is shown.

4H-SiC VJFET contact characterization

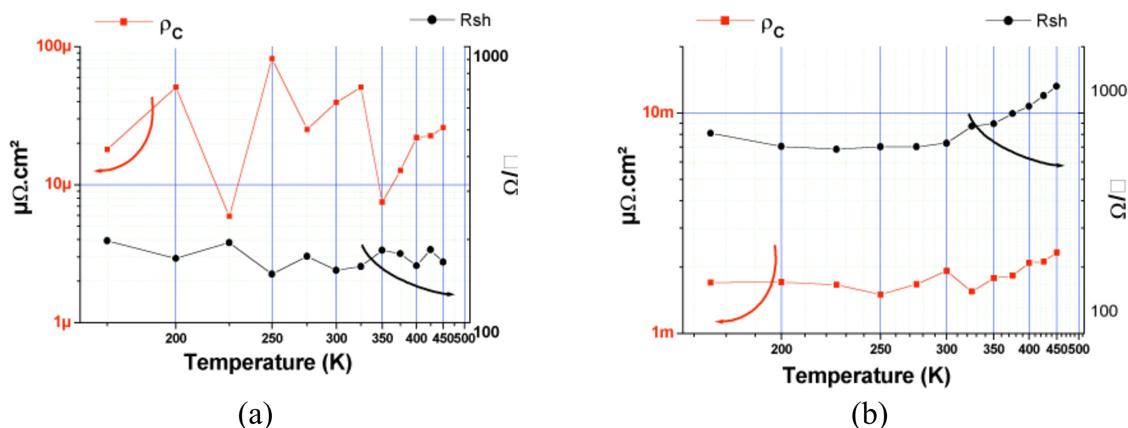
The key parameter for high power devices is ohmic contact formation in order to reach high current densities using silicon carbide. The dependence of VJFET channel specific resistance on metal annealing temperature is presented in Figure 1. A value of 120 mW.cm² is reached for 950°C metal annealing condition, close to the value of 90 mW.cm² expected from simulations.



(a) (b)

Fig 1. Ohmic contact formation (a) and specific resistance variation (b) for different metal annealing temperature

Temperature dependence of the specific contact resistance rc has been measured on TLM structures (Figure 2). Contact resistivity remains in the range of 40 µW.cm² for Ni/SiC stack. The low sheet resistance value (R_{sh} < 200 W/□) underlines the good electrical activation of N+ implanted layer after post implantation thermal annealing. Its temperature dependence is very low.



(a) (b)

Fig. 3. Contact specific resistance and R variation versus temperature for high dose 10^{15}cm^{-2} (a), and low dose 10^{13}cm^{-2} (b) N implanted layers

For lower doping concentrations, variations of ρ_c remain low. The increase of R_{sh} is attributed to the mobility temperature dependence $\left[\mu(T)=\mu_0\left(\frac{T}{T_0}\right)^{-\alpha}\right]$. Coefficient variation extracted from R_{sh} measurement (made on TLM) gives a coefficient α=1,54. This low value compared to the value of 2 generally found [8] may be due to the presence of defects or to the effective mass dependence on temperature. Two post implantation thermal annealing conditions have

been investigated. Considering R_{sh} measurement (Table 1), a 1700°C / 30 min post implantation annealing leads to the best results (in term of electrical activation and global process cost). The roughness is the same for both conditions tested.

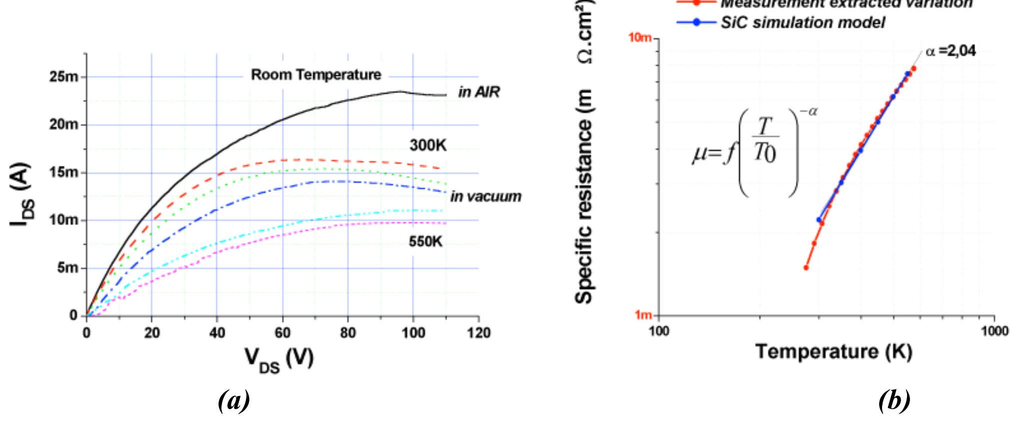
Annealing setup		N^+ layer (Dose $=10.^{15}cm^{-2}$)	N layer (Dose $=10.^{13}cm^{-2}$)
		$R_{\square}$	$R_{\square}$
1650 °C / 60min *4H*		1105	4015
1700 °C / 30min	*4H*	646	3007
	6H	670	2886

Tab. 1. R_{sh} for two post implantation annealing setup

Considering previous results, we can consider that ohmic contacts for N-type layer are good and thermally stable in the range of temperature from 200 K to 450 K. The temperature was limited to 450 K, the highest temperature reached by the VJFET during the limiting state (estimated by simulation).

VJFET power capability analyses.

Using VJFET as a current limiter for high voltage application involves high power density in the device. Self heating effect is important as the carrier mobility of electrons (i.e. the current) strongly depends on temperature).



(a) ***(b)***

Fig. 4. VJFET thermal characterization: I(V) (a) and specific resistance (b)

The variation of the specific channel resistance ρ_{ch} with temperature is extracted from I-V pulsed measurements between VJFET drain-to-source (Figure 4(a)), at V_{DS} = 2 V, for temperature varying from 200 K up to 550 K. As ρ_{ch} is directly proportional to μ_n, the coefficient α was extracted. The obtained value (α = 2.04) presents a good agreement with parameter used is simulation as illustrated in figure 4(b). Current time dependence measurements underline thermal capabilities of the VJFET as presented in Figure 5. The current was normalized to the current I_0 at t = 0 s for several voltages (V_{DS}). Current stabilization shows the ability of VJFET to sustain short circuit current for long time. Considering for example a voltage V_{DS} = 100 V, current reduction due to self heating is around 12% and current remains constant during more than 100 s.

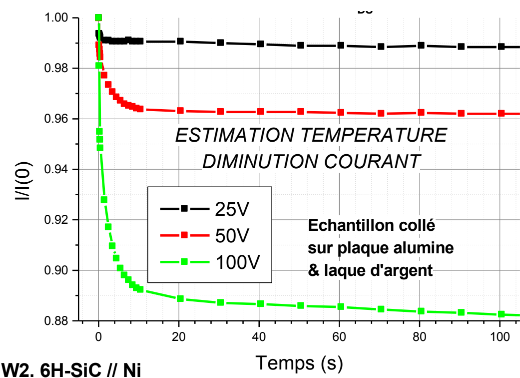


Fig.5. VJFET current time dependence under constant Drain to Source bias

Repetitive measurements were done and no degradation of the electrical characteristics has been noticed. Highest breakdown in "current limiting state" for 0.5 s pulsed mode bias was measured to be around to 811 V, corresponding to a high power density of 140 kW/cm^2.

Conclusion:

This work underlines the fabrication requirement of good ohmic for high power density device. Both lowest value and thermal stability versus temperature is needed. Temperature measurements exhibit ohmic contact stability from 200K up to 450K. A post implantation thermal annealing and metal process have been setup and lead to optimistic results for the fabrication of higher capabilities devices (a rising up in terms of cells current). This device could be used in application such as current limitation in case of a short circuit of an electrical system. It could permit an elevation of the current ratings of classical mechanical switch with the serial addition of this controlled device.

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