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Characterization of Cdv/dt Induced Power Loss in Synchronous Buck DC-DC Converters

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As Presented at APEC 2004

***Abstract* — Good understanding of power loss in a high frequency synchronous buck converter is important for design optimization of both power MOSFET and circuit itself. Most of the MOSFET power losses are relatively easy to quantify. The exception is the power loss associated with Cdv/dt induced turn on of the low-side MOSFET (synchronous rectifier). This paper characterizes the Cdv/dt induced power loss in two ways. First, detailed device characterization, in-circuit testing, and modeling are used for a comparative loss calculation. This method requires specialized test equipment and is rather complicated and time consuming. A simple method is then introduced to very accurately quantify the Cdv/dt loss. With this method, the impacts of the Cdv/dt power loss on synchronous buck converters at different operation conditions can be readily assessed. The impacts of Cdv/dt induced turn on different applications are addressed.**

Index Terms — Synchronous rectifier, switching loss.

I. Introduction

The stringent requirements for low voltage, high current voltage regulators (VRs) impose various challenges to the power management design [1]. High conversion efficiency is one of the most critical issues in order to improve power density [2]. Careful MOSFET and driver optimization as well as layout are the key factors to achieve high conversion efficiency.

Synchronous buck converter is the most popular topology for today's VRs. In this converter, the freewheeling Schottky diode of the regular buck converter is replaced with a power MOSFET. This results in tremendous conduction loss reduction, but also creates new challenges and device requirements. One of the issues frequently discussed but not fully understood or characterized is so-called *Cdv/dt induced switching loss* of MOSFETs used as synchronous rectifiers (referred to in this paper as sync FETs) [3][4][5]. *Cdv/dt* induced turn on of the sync FET can happen after its body diode recovers; the increased voltage across the sync FET induces a voltage on the gate through the drain-to-source capacitor, C_{gd}. The induced voltage can possibly turn on the sync FET for a short time. The overlapping of the V_{ds} voltage and the current generates additional switching loss. The issues of *Cdv/dt* induced turn on are not well understood because of the complexity resulting from the involvement of the V_{ds} slope (which is also determined by many factors) and various MOSFET characteristics (such as interelectrode capacitances, internal gate resistance, threshold voltage, body diode properties, and package characteristics) [5][6], driver capability, layout, etc.

In this paper, a comparison study is conducted first to quantify the *Cdv/dt* induced power loss based on detailed device characterization, loss modeling, and in-circuit testing.

A simple and practical method is then introduced to experimentally quantify the *Cdv/dt* induced turn on loss. The results show that the *Cdv/dt* loss could be significant - depending on switching frequency, input voltage, and load conditions. The results also point out certain benefits of *Cdv/dt* induced turn on - the reduction of sync FET V_{ds} ringing induced by the body diode reverse recovery and loop parasitic inductance. MOSFET packaging inductance and body diode reverse recovery have to be minimized in order to allow optimally designed silicon (with high *Cdv/dt* immunity) to maximize circuit efficiency without generating excessive parasitic ringing.

II. Methodology of the Study

Analytical calculation of the *Cdv/dt* induced power loss is not very practical, since many of the involved parameters cannot be easily extracted or accurately modeled. An alternative approach is to compare two sync FETs with similar parameters – except those that dominate the *Cdv/dt* induced turn on. The sync FET No.1 (*Case 1*) turns off without *Cdv/dt* induced turn on. For the sync FET No.2, (*Case 2*), the *Cdv/dt* induced gate-source voltage is high enough to turn the channel on, and introduce additional switching losses. The *Cdv/dt* induced turn-on loss is then quantified by the comparing the losses between the two cases. This method, described in Section V, can be quite accurate, however, it requires complete sync FET device characterization (obtained with special testers), detailed incircuit waveforms, as well as measurements of the in-circuit efficiency and device operating temperature. It is therefore very time consuming and in general not practical for most design engineers.

A more practical engineering approach that does not need any device characterization is described in Section VI. The idea is to modify the gate drive circuit so that an adjustable negative gate-source offset voltage can be generated.

The purpose of the negative offset voltage is to shift the induced gate voltage below the gate threshold voltage, By applying a sufficient negative offset, the *Cdv/dt* induced turn on loss can be completely eliminated.

III. SYNC FET TURN-OFF LOSSES WITHOUT CDV/DT INDUCED TURN-ON

Fig. 1 shows a synchronous buck converter with control FET denoted as Q_1, and sync FET denoted as Q_2. In this figure, Q_2 is shown with its body diode, three parasitic capacitors (drain-gate capacitor C_{gd}, gate-source capacitor C_{gs}, and drain-source capacitor C_{ds}) and an internal gate resistor R_{g_in}. The inductance of the current transition loop (comprised of input cap ESL, PCB parasitic inductance, and package capacitance of Q_1 and Q_2) is lumped as L_{kloop}.

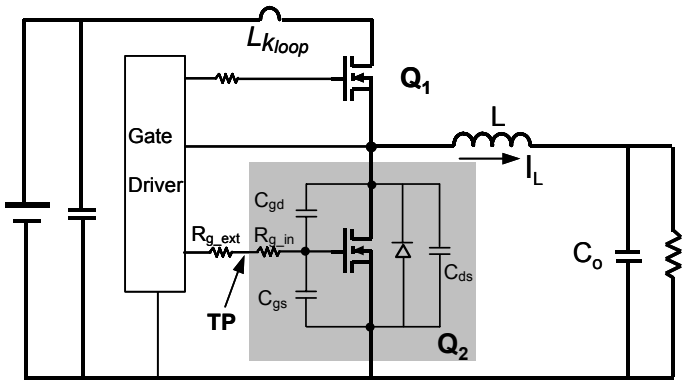

Fig. 1. A synchronous buck converter with a simplified model of the FET Q_2.

Key switching waveforms for the *Case 1* (the sync FET has high *Cdv/dt* immunity and the induced gate voltage is not high enough to turn on the sync FET), are given in Fig. 2.

The turn-off transition of the sync FET can be briefly described as follows:

[T_0 – T_2]: At t_0, the sync FET gate turns off and the V_{gs} decays exponentially determined by C_{iss} and total gate impedance. As the gate voltage of Q_2 falls below its threshold voltage at t_2, all the Q_2 channel current is diverted back into its body diode.

[T_3 – T_5]: After a predetermined driver delay, the top switch Q_1 begins to turn on (at t_3). The gate voltage on Q_1 quickly reaches and exceeds the threshold voltage, $V_{th\text{-}Q1}$, commencing the current transition. Because of high di/dt and the package leakage inductance, the V_{ds} voltage of Q_2 increases slightly from about –0.7V negative to some small positive voltage.

[T_5 – T_6]: The current through Q_1 is equal to the inductor current at t_5, and Q_2 current is zero. Starting from t_5, reverse recovery current flows through Q_2's body diode. At t_6 the reverse recovery current reaches its peak value I_{rrm}, and the body diode recovers.

The energy stored in the loop parasitic inductor, L_{kloop}, at time t_6 is:

$$E_{loop} = \frac{1}{2} \cdot L_{kloop} \cdot I_{rrm}^2 \qquad \text{Eq. 1}$$

[T_6 – T_8]: The recovered body diode starts to block the voltage at t_6. The $V_{ds\text{-}Q2}$ rises with a very high dv/dt slope. This voltage rise is capacitively coupled into the gate thru the gate-drain capacitor, C_{gd}, resulting in an induced voltage at the gate of the sync FET. However, this voltage for *Case 1* is lower than the threshold voltage, and therefore insufficient to turn on the Q_2.

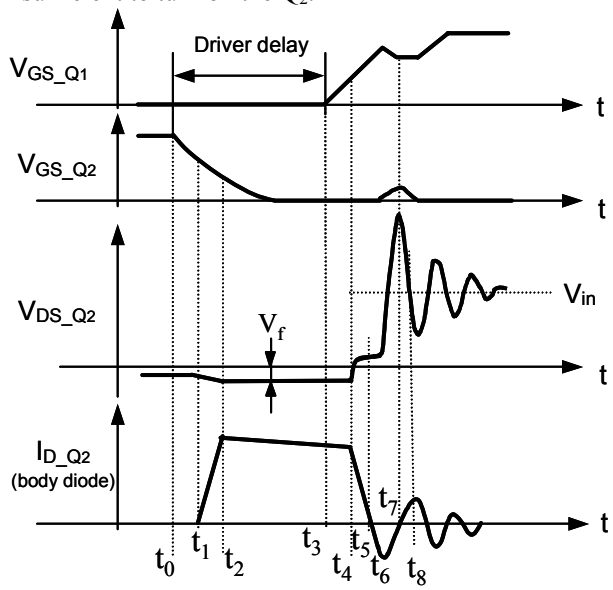

Fig. 2. Key waveforms during the transition of the current from Q_2 to Q_1 without *Cdv/dt* induced turn on.

The loop parasitic inductor now forms a resonant circuit with Q_2's output capacitor C_{oss}, resulting in V_{ds} oscillations. Approximately all of the leakage energy is transferred to the output capacitor of Q_2 in the initial resonant cycle. The resonance is then damped over many cycles by the high frequency AC resistance in the C_{in}-Q_1-Q_2 loop, resulting in the final V_{ds} voltage being equal to V_{in}. The remaining C_{oss} energy at V_{in} is recycled at the next cycle (since the turn-on of the sync FET is with zero V_{ds} voltage). Therefore, the energy dissipated at Q_2 turn off can be expressed as:

$$P_{off\_Coss\_case1} = \frac{1}{2}(Q_{oss(Vpk)} \cdot V_{pk} - Q_{oss(Vin)} \cdot V_{in}) \cdot f_s \qquad \text{Eq. 2}$$

For standard MOSFET packages, such as SO8 and D-Pak, parasitic package inductance is the key component of the loop inductance. When silicon die with good *Cdv/dt* immunity is used in these packages, the V_{ds} ringing caused by the inductance and body diode reverse recovery current can easily exceed 30V with 12V input voltage. High peak voltage as well as ringing can result in excessive EMI and can reduce controller/driver reliability. It was shown in [7] that by replacing a SO8 package with a package with much lower inductance (such as DirectFET®), the switch node voltage ringing can be reduced by as much as 50%**.**

IV. SYNC FET OPERATION AND LOSSES WITH CDV/DT INDUCED TURN ON

For *Case 2*, the *Cdv/dt* induced gate-source voltage is high enough to turn on the sync FET. Once the sync FET is turned on, the dv/dt is reduced. This prevent further gate voltage rise. Consequentially, the value of the induced gate voltage is whatever is required to support the peak reverse recovery current I_{rrm}. (Note that due to internal R_{g_in}, the gate-source voltage measured at the gate terminal of a sync FET is different from the internal voltage across individual cells).

Fig. 3 shows the key waveforms of the converter during this mode of operation. The circuit operation and losses are significantly different for this case. The $V_{ds\text{-}Q2}$ will be either clamped (as shown in Fig. 3) or will have reduced dv/dt increase rate. For this study we consider clamped V_{ds} case.

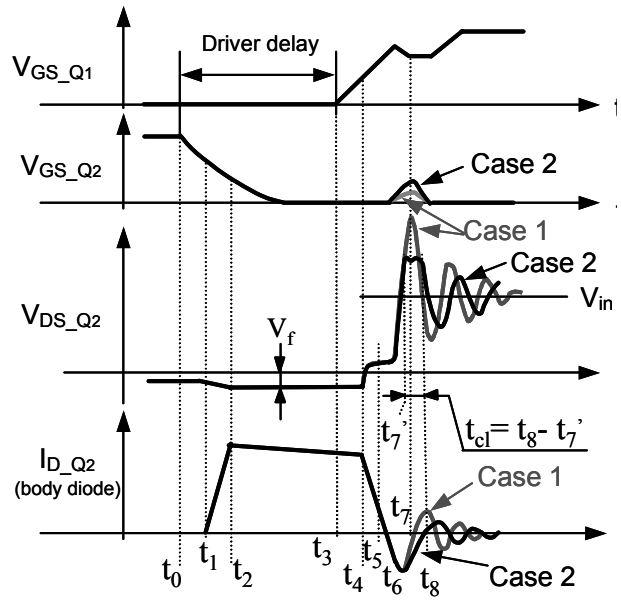

Fig. 3. Key waveforms during the transition of the current from Q_2 to Q_1 with *Cdv/dt* induced turn on.

Up to time instance t_6, the circuit operation is the same regardless of *Cdv/dt* immunity of the sync FET. After T_6, the operation is as follows:

[$T_6 - T_7$']: The Q_2 body diode recovers and starts to block the voltage at t_6. The voltage change *dv/dt* of $V_{ds\text{-}Q2}$ is coupled to the gate via gate-drain capacitor, and an induced gate voltage is now higher than the threshold voltage.

[T_7' – T_8]: At time t_7', the *Cdv/dt* induced turn on happens and the voltage $V_{ds\text{-}Q2}$ is clamped. The FET turns off at time t_8. The duration of this clamped time period is t_{cl} (t_8-t_7').

Multiple factors determine the *Cdv/dt* immunity. These include the slope of the V_{ds}, internal gate resistance, threshold voltage, body diode properties, package characteristics, driver capability [4], and layout, etc. However, one of the key factors for well-designed circuit with typical driver resistance and FET gate resistance is the gate charge ratio (CR) [3]. CR is defined as:

$$CR = Q_{gd} / Q_{gs1}, \qquad \text{Eq. 3}$$

where Q_{gd} is the gate-drain (Miller) charge at a specified V_{ds} voltage, and Q_{gs1} is pre-threshold gate-source charge.

During *Cdv/dt* induced turn on, the V_{ds} of Q_2 is clamped due to the channel conduction. With the assumption that the clamped voltage is constant (also observed in experimental test), the induced switching loss during the Q_2's clamping time for *Case 2* can be expressed as:

$$P_{off\_Clamp\_case2} \approx V_{cl} \cdot \frac{I_{rrm}}{2} \cdot t_{cl} \cdot f_s, \qquad \text{Eq. 4}$$

where V_{cl} is the value of the clamped V_{ds} voltage; f_s is the switching frequency; I_{rrm} is the peak reverse recovery current; and t_{cl} is the time for the reverse recovery current to reduce from I_{rrm} to zero. V_{cl} and t_{cl} are most accurately determined from the circuit waveforms, while I_{rrm} needs to be determined with a special tester (it is not possible to measure I_{rrm} inside the circuit because insertion of a current sense element would significantly alter circuit operation).

Note that Eq. 4 is most accurate when V_{cl} is up to about $2V_{in}$. If a device measures higher V_{cl} (better *Cdv/dt* immunity), the reverse recovery current that needs to be entered in the Eq. 4 will be lower than I_{rrm}. This is due to $L_{kloop} - C_{oss}$ resonance, which reduces reverse recovery current toward zero as the V_{ds} increase toward its peak oscillation value.

Aside form *Cdv/dt* turn on loss, there is still power loss associated with C_{oss} high frequency resonance, given by Eq. 5 below. However, due to the clamping action, the peak V_{ds} voltage will be reduced, and there will be less energy transferred into C_{oss}. Consequently the power dissipated in the C_{in}-Q_1-Q_2 loop will be lower than that using the device with better *Cdv/dt* immunity.

$$P_{off\_Coss\_case2} = \frac{1}{2}(Q_{oss(Vcl)} \cdot V_{cl} - Q_{oss(Vin)} \cdot V_{in}) \cdot f_s \qquad \text{Eq. 5}$$

Total turn off power loss for the sync FET with *Cdv/dt* induced turn on is the sum of Eq. 4 and Eq. 5

$$P_{off\_case2} \approx P_{off\_Clamp\_case2} + P_{off\_Coss\_case2} \qquad \text{Eq. 6}$$

The *Cdv/dt* induced turn-on causes sync FET to dissipate an additional energy from the source, higher than the loop leakage energy given by Eq. 1. If other parameters can be excluded from affecting the loss difference, then the *Cdv/dt* induced loss can be expressed as:

$$P_{Cdv/dt\_case2} \approx P_{off\_case2} - P_{off\_Coss\_case1} \qquad \text{Eq. 7}$$

V. Quantification of Cdv/dt Loss based on the Analysis Method

A typical 5mΩ sync FET power MOSFET in SO8 package was processed in two different ways for the purpose of *Cdv/dt* power loss calculation. With varying trench channel depth, it was possible to find one device with higher $R_{DS\text{-}on}$ and lower CR (better *Cdv/dt* immunity), and the other one with much higher CR and lower $R_{DS\text{-}on}$. Most of the other relevant parameters were the same or very similar. The relevant device parameters are shown in Table 1.

	Device No. 1	Device No.2
R_{DS_on} (mΩ) @ 25°C	5.38	4.83
Q_{gs1} (nC)	8.81	10.85
G_{gd} (nC)	8.59	16.37
CR (Q_{gd} / Q_{gs1})	0.98	1.51
V_{th} (V)	2.02	2.08
R_g (Ω)	1.4	1.4
Q_{rr} (nC) @10A	62.85	74.88

Table 1. The comparison of device parameters.

The measured Q_{oss} vs. the drain-source voltage of the two devices is shown in Fig. 4.

Fig. 5 shows the performance comparison for the two devices in the sync FET socket using the same Q_1 (10mΩ, low-charge device) in 1MHz, 14V_{in} , 1.3V sync buck circuit.

The loss difference at 10A is about 0.72W. This loss difference is due to the different R_{ds_on}, C_{oss} and *CR* of the two devices. To find the exact *Cdv/dt* induced loss, in-circuit switching waveforms, device temperature and reverse recovery peak current are also necessary.

Fig. 6 compares V_{ds} and V_{gs} waveforms for the sync FETs. *Case 1* does not have the *Cdv/dt* induced turn on (the peak V_{ds} voltage is 35V), while a 23V clamped drain-to-source voltage can be observed for the *case 2*. The clamping time can be found as 7ns.

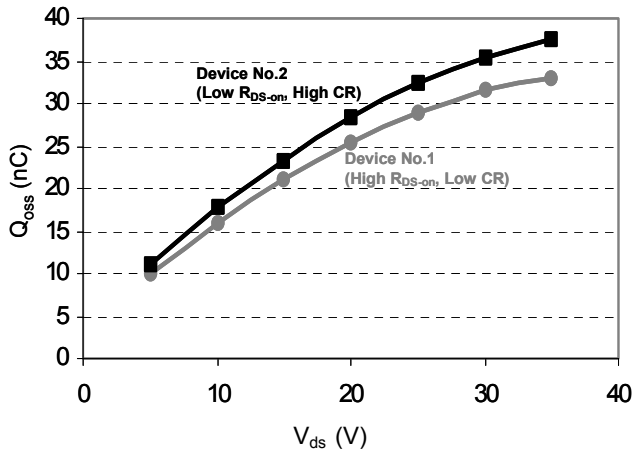

Fig. 4. Measured output charge of the two devices at different drain-source voltage.

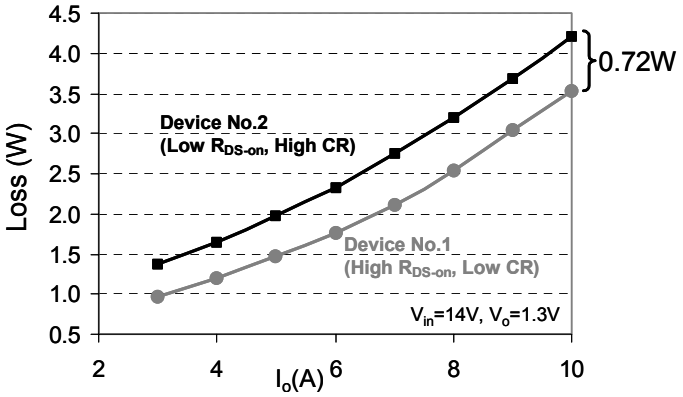

Fig. 5. Loss comparison between two sync fets processed in different ways (one with low CR, and one with high CR).

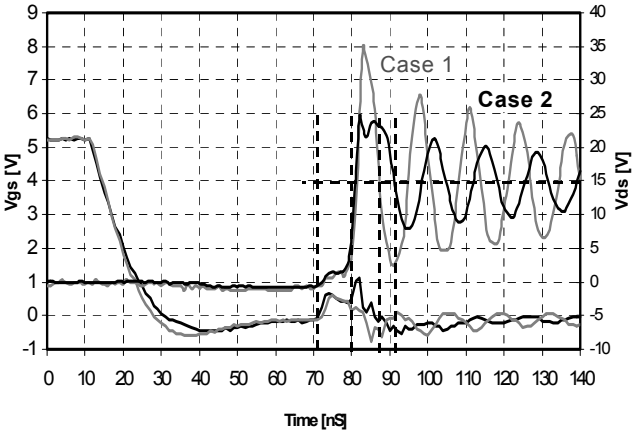

Fig. 6. Waveform comparison for loss quantification between two sync fets (one with low CR, and one with high CR).

Table 2 summarizes the calculated power loss based on the device information and in-circuit waveforms. It can be seen that the calculated loss using a device with high CR (poor *Cdv/dt* immunity) at 10A output current is 0.70W higher than the loss using a low CR device. This value matches the measured 0.72W very well.

The *Cdv/dt* inducted loss for this circuit and under given operating conditions can be calculated as 0.75W. Since all device parameters are very similar, this loss difference can be attributed to high CR and *Cdv/dt* induced switching losses. At 10A, 1MHz operation condition, the *Cdv/dt* induced loss for the device No. 2 is 18% of the total circuit loss, which is very significant.

	Device No. 1	Device No.2
R_{DS_on} (mΩ) @ Temp	6.73	6.28
P_{Cond} (W)	0.76	0.71
V_{pk}/V_{cl} (V)	35	23
Q_{oss} (nC) @ (V_{pk}/V_{cl})	33 (@ 35V)	32 (@23V)
Q_{oss} (nC) @ (Vin)	20	22
P_{off_Coss} (W)	0.46	0.24
I_{rr} (A) @10A	12.0	12.0
T_{cl} (ns) @10A	-	7
P_{off_Clamp} (W)	-	0.97 (Eq. 4)
Δ Loss (W)	**0.70W**	
Cdv/dt Loss (W)	**0.75W** (Eq. 7)	

Table 2. Calculation of *Cdv/dt* induced power loss.

VI. Practical Way to Quantify Cdv/dt Induced Power Loss

It was shown in the previous section that the *Cdv/dt* issues relate to many factors such as the voltage rising slope, charge ratio, tradeoffs between Q_{gd} and $R_{ds(on)}$, threshold voltage, and total gate impedance. Furthermore, extracting some of the device parameters required for *Cdv/dt* power loss characterization requires specialized test equipment, typically not available to most circuit designers. Therefore, this process can be both time-consuming and costly.

A faster, more practical way for a designer to quantify *Cdv/dt* induced power loss is to use simple circuit shown in Fig. 7. The purpose of this circuit is to create a negative gate drive voltage (rather than zero) during the turn-off time of the sync FET. This negative voltage will prevent sync FET from turning on due to *Cdv/dt* effect. The purpose of C_s is to change the standard gate drive signal coming from a driver IC into an AC signal with positive and negative values proportional to the duty cycle. The purpose of the V_+ is to offset the new gate drive signal and allow negative gate bias to be varied in order to identify *Cdv/dt* induced power loss, and/or find optimum negative gate drive.

Fig. 8 shows the loss measurement (excluding control power, the PCB and inductor loss), obtained in a $12V_{in}$, $1.7V_{out}$, 1MHz, 20A VR module using single control FET and a single sync FET. The on-state V_{gs} was kept constant at 5V, in order to keep the $R_{DS\text{-}on}$ (and conduction loses) constant. The off-state gate drive was varied from zero to –2V. In this way, all the measured power loss difference can be associated with *Cdv/dt* loss.

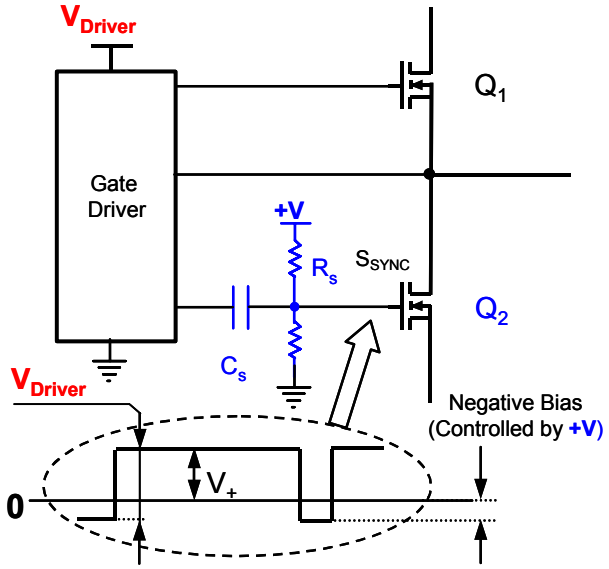

Fig. 7. Modified driver circuit to generate negative voltage.

It can be seen from Fig. 8 that the loss can be reduced by 0.57W with –1V bias and by 0.84W with up –2V negative bias. The loss remains constant as the negative gate bias is further increased, indicating that all *Cdv/dt* induced power loss have been eliminated.

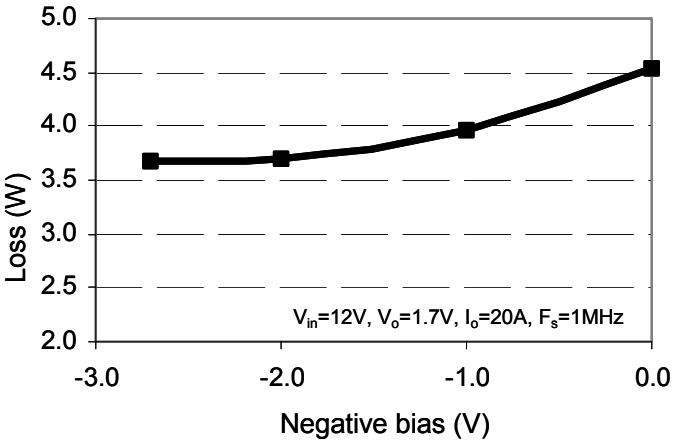

Fig. 8. Loss measurement with a fixed V_+=5V and variable negative bias.

VII. Impacts of Cdv/dt induced Loss on the Device and Circuit Design

As a switching loss, the *Cdv/dt* induced loss is proportional to the switching frequency. It has been demonstrated that the *Cdv/dt* loss could be a significant part of the total circuit loss at 1MHz. The *Cdv/dt* induced loss imposes challenges on both device and circuit design for high frequency VRs, which is a future direction of VR's.

At prevailing 200-500KHz operating frequency, *Cdv/dt* induced loss could also be a serious problem depending on the applications. Three devices with the parameters shown in Table 3 are used as the sync FET for the comparison in notebook applications. The major difference of the three devices is the Miller charge, therefore, the CR.

	Device No. 1	Device No.2	Device No.3
R_{DS_on} (mΩ) @ 25°C	3.6	3.5	3.3
V_{th}(V)	1.7	1.8	1.8
CR	1.0	1.2	1.4
Q_{gd} (nC)	10.9	13.6	15.9
Eff (%) @ 4A	85.94	83.88	81.00

Table 3. The comparison of device parameters and the efficiency at light load.

The converter input voltage is 19V and the output voltage is 1.3V. Fig. 9 shows the measured efficiency.

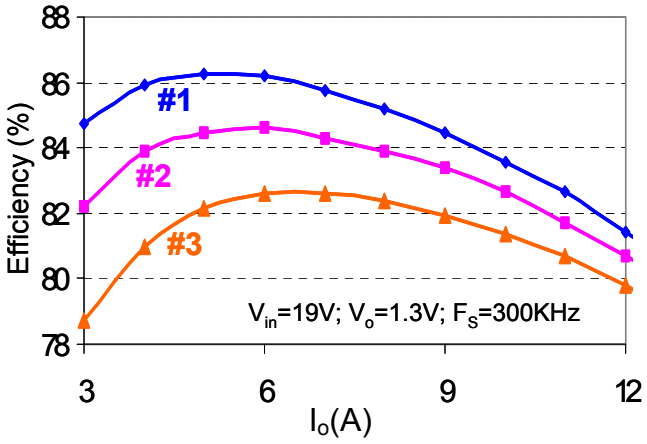

Fig. 9. Impact of *Cdv/dt* induced loss on notebook applications.

Device No.1 with CR=1 outperforms the part with CR=1.4. The efficiency improvement is about 5% at 4A, around where device would be running most of the time in typical notebook application. For the three evaluated devices, Q_{gs1} varies only 5%, while Q_{gd} varies by over 45%. Q_{gd} is a key factor for achieving optimized device design. The conduction loss reduction due to the $R_{ds\text{-}on}$ reduction is very small and does not offset the increased *Cdv/dt* loss.

As discussed and demonstrated in Sessions III to V, the *Cdv/dt* induced turn on can help to reduce the voltage spike of the sync FET. Aside from EMI reduction, the spike reduction makes it easier to use more efficient 20VN devices for 12Vin processor power applications for desktop and servers.

VIII. Conclusion

This paper presents detailed characterization of the power loss associated with *Cdv/dt* induced turn on of a MOSFET used as synchronous rectifier in high frequency synchronous buck converters. A simple and effective method is also introduced that allows engineers to accurately quantify *Cdv/dt* loss. On one hand, the *Cdv/dt* induced turn on can introduce quite significant loss depending on switching frequency, input voltage, and load conditions; on the other hand, the *Cdv/dt* induced turn on can reduce the voltage stress of the sync FET. The *Cdv/dt* induced switching loss imposes challenges on device and circuit design not only for high frequency VRs, but also for the applications running at light load conditions most of the time, such as notebook applications.

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