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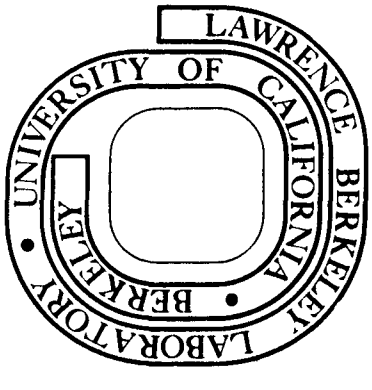

DISCLAIMER

CHARACTERIZATION OF CHARGE-COUPLED ANALOG MEMORIES FOR NUCLEAR DATA ACQUISITION

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Introduction

The Charge-Coupled Device (CCD) is one of the recent products of continuing technological progress in semiconductor component development. Basically, the CCD consists of a number of contiguous cells together with a mechanism for transferring electrical charge from one cell to the next. During the transfer process, the amplitude, or quantity of charge is preserved. Thus, the CCD in effect behaves as an analog shift register. An analog shift register is, potentially, a very useful device for instrumenting certain large scale high-energy physics detectors and other nuclear data acquisition systems; this paper reports on work aimed at characterizing two commerically available CCDs (Fairchild Types 311 and 321)** in terms of such applications.

The construction of a typical CCD is shown in Fig. 1. The transfer of charge along the shift register chain is controlled by an external clock. A packet of charge existing initially in the first cell appears at the output cell after (n-1) clock pulses, where n is the number of cells in the chain.

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**Manufactured by Fairchild Semiconductor, Mountain View, California. Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Energy Research and Development Administration to the exclusion of others that may be suitable.

In addition to the transfer mechanism, CCDs must have a means of introducing charge into the chain. In the case of chains used as linear delay devices, two common configurations exist. In the first, a charge injector is provided for each CCD cell. This configuration is often used for parallel-to-serial conversion of electrical input signals. It is also used in light-sensitive scanning devices, in which the injected charges are replicas of the quantity of light falling along-side each cell. In the second, a single injector is used for each chain of cells. This configuration is used for devices that are designed to provide a controllable delay between input and output. An example is the CCD digital dynamic memory, used to store binary information. Another example is the analog shift register, in which a replica of the input waveform appears at the output, delayed by n clock pulses. The action of such a CCD is similar to that of a delay line, except that: (1) the delay is controlled by the clock frequency; and (2) the output signal is quantized in time, rather than continuous.

An Application of Shift Register CCDs

An application of analog shift register CCDs which is being investigated is in the field of high-energy physics instrumentation.[1] Here, wire grid chambers of various fillings (gases and liquids) and configurations (planes, cylinders, etc.) are common. These are typically used to measure the trajectories, times-of arrival, or ionizing density of charged particles. These measurements are based, in turn, on measurements of electrical pulses emanating from the individual wires of the chambers. Typical chamber arrays have wires (and corresponding signal channels) numbering in the thousands. The electrical pulses are in the millivolt range, and are tens of hundreds of nanoseconds in duration. The dynamic

range of the pulses (in terms of peak amplitude or total charge) may be as high as several hundred.

The task of measuring and recording all the signals can be formidable. For example, to record an amplitude measurement to 8 bit resolution (one part in 256) on each of 1000 wires once every 100 nsec would require recording data at the rate of 8×10^{10} bits per second. Fortunately, this is not necessary. An "event" of interest occurs rather infrequently; all signal information occurring between events is useless. Also, even when an event does occur, only a few wires have useful signals. Thus, the recording problem is made manageable by recording only when events occur and then recording only the significant wire data.

However, deciding when events occur and which data are significant takes time. This is where the CCD comes in. It is continually memorizing the wire signals--and continually forgetting them after a delay of n clock periods. If the event recognition signal (often called the secondary trigger) can be generated in a time shorter than n clock periods, then steps can be taken to save the data that reside, at that instant, inside the CCD. Also, circuitry at the outputs of the CCDs can be brought into play to recognize and store only significant data. In the scheme described here, both these steps depend on having the facility to stop or slow the clock that is controlling the rate at which data flows through the CCD. For example, the clock can be slowed sufficiently that the quantized signals at the CCD outputs can be measured by relatively slow ADCs, and the results can be stored in relatively slow digital memories.

Figure 2 shows an example of a part of a system using CCDs in this way. Here, 16 CCDs are connected to 16 wires of a chamber. While searching for an event, the transfer clock runs at a read-in frequency of 20 MHz.

Thus, the instantaneous amplitude of each wire signal is input to its CCD every 50 nsec. After n x 50 nsec, where n is the number of CCD cells, the signal reaches the output of the CCD and is lost. When an event occurs, a secondary trigger is generated soon thereafter. The speed of the transfer clock is then slowed to the read-out frequency. In Fig. 2, since 16 CCDs are multiplexed into the ADC, the read-out frequency will be 1/16 MHz if the ADC conversion time is 1 μsec.

The ADC makes a total of 16n conversions. However, only the small percentage of these that are non-zero are stored in memory. Decisions as to whether each datum is non-zero and also corrections for non-ideal CCD characteristics are made in the block which is labeled "Digital Data Selector and Corrector" in Fig. 2.

CCD Characteristics

Commercially available CCDs have characteristics which, while not ideal, are suitable for this application. As described below, suitable calibrating and correcting subsystems can greatly reduce the effects of non-ideal characteristics. The important characteristics are summarized here. The details of measurements that support that statement are presented later.

Linearity

Linearity is a measure of how faithfully the output signals systematically reproduce the input amplitudes. Non-linearities can be tolerated if they are reasonably stable with time. If so, the non-linearities can be measured (calibrated) and corrections can be applied to the output data. The correction process is simplified if the deviation from linearity can be described by a simple algebraic expression.

Noise Level

Because a CCD is a clocked device, the output consists of a succession

of voltage levels, each level lasting for one clock period. Noise that causes random variations in output level within a given clock period is generally negligible. The concern here is with noise processes that cause the levels to have a random uncertainty. For example, with a constant input voltage, the output levels during successive clock periods will differ from one another because of noise generated internally to the CCD during the transfer process. Because this noise is unpredictable and cannot be corrected, it represents a fundamental limit to amplitude resolution.

Dark Current

There are processes within the CCD that add charge to the quanta of signal being transported through the CCD. The amount of charge added is proportional to the time the signal is contained within the CCD. In the situation described in this paper, the clock frequency is suddenly lowered during the readout sequence. Thus, successive output levels (during the readout sequence) result from quantas of signal charge that have spent successively longer times within the CCD. The effect of dark current is to cause the output baseline (i.e., the output level that would correspond to a constant zero input signal voltage) to vary linearly with time during the readout. This situation is shown in Fig. 3. This "baseline shift" can be corrected if it is sufficiently stable with time. However, the dark current imposes a practical lower limit on the readout clock frequency, and hence influences the usable level of analog multiplexing at the output. This is because the baseline shift cuts into the available dynamic range at the output of the CCD.

Transfer Inefficiency

The transfer process within the CCD, whereby signal charge is shifted

from one cell to the next, is not perfectly efficient. Consider a step function applied to the input such that the signal level changes abruptly between two transfer clock periods. Because of transfer inefficiency, the output signal is not a pure step; the total transition may require several clock periods at the output. The effect of transfer inefficiency, therefore, is a signal shape distortion. In this application, the result can be errors in determination of peak amplitude and time-of-arrival of input pulses. Corrections can be applied if the nature of the transfer inefficiency is known.

Measurement Techniques

Figure 4 shows a block diagram of the equipment used for CCD measurements. The transfer clock generator normally generates clock signals at the chosen read-in frequency (RIF). Upon receipt of a shift frequency signal, the transfer clock generator shifts to the pre-selected readout frequency (ROF) for n cycles, where n is the number of cells in the CCD.

The event trigger simulates the detection of an event in a real application. The event trigger, synchronized with the clock, triggers the signal generator at a constant, but controllable, phase of the clock signal. The synchronized event trigger is also delayed by a preset number of clock cycles to cause the shift frequency signal to occur; it also enables the ADC, and starts the storage of the digital outputs of the ADC.

At the end of the sequence, the digital memory contains n 10-bit words of data. These data represent the complete set of information contained within the CCD at the instant the shift frequency signal occurred. This includes the signal from the signal generator, which has been delayed by its passage through the CCD. The data are later transmitted to a digital computer for analysis.

Data Analysis

Dark Current Measurements

For dark-current measurements, the signal generator was disconnected, and the CCD input held at a constant voltage level. The baseline shift was determined by making a least-squares straight-line fit to the data acquired during the readout.

Noise

Noise determinations were made by calculating the rms deviation of the data acquired during the readout from the least-squares straight-line fit.

Linearity

The linearity of the CCD was determined by measuring the output signal voltages resulting from pulse inputs of various amplitudes. A calibrated attenuator was used to vary the input signal, and the 10-bit ADC was used to measure the output voltages.

Transfer Inefficiency

Figure 5 shows an output signal resulting from a square pulse voltage signal applied to the input of the CCD. (The variable delay shown in Fig. 4 is set so that the front edge of the input pulse occurs at 0° phase of the read-in transfer clock). The deviations from a square pulse signal at the output are due to transfer inefficiency.

In order to get good statistics, it was necessary to combine the results of from 30 to 100 events. Since the computer took a fraction of a minute to calculate each event, the following procedure was used to remove the effects of various drifts in the system over this number of events. The signal generator was adjusted to generate a pulse that lasted no more than 20 clock periods. A straight-line fit was made, for each event, to the data in regions A and C of Fig. 5. In region B, the

differences between the actual data points and the straight-line were calculated and stored. For each clock period of region B, these differences were accumulated, then divided by the number of events. The result is an output pulse shape averaged over the total number of events, with effects owing to baseline shifts and drifts reduced.

Results of Measurements on the Fairchild CCD 311

The internal organization of CCD 311 is given in Fig. 6. Analog input signal in voltage form is applied to the input V_I (A or B channel). The input sampling clock ϕ_S samples the input voltage signal and injects a proportional amount of charge into the first cell of the 130-cell-long register. This charge is then transferred from cell to cell by the transport clock signal, ϕ_{1A} or ϕ_{1B}. Charge packets which have been transferred through the entire analog shift register are applied to a precharged diode which is connected to the gate of the output MOS amplifier transistor. By means of a reset clock ϕ_R, which drives a reset MOS transistor, the charge on the detector-diode capacitance is recharged during the interval between two charge packets. The sampled input voltage between t = o and t = t_c appears at the output terminal OS at t = 260 t_c. The reset clock ϕ_R is summed internally with output waveform and the composite waveform appears at the output terminal OS. During the measurements, a differential amplifier was used to eliminate the reset clock pulses from the video waveform to recover the analog information.

Measurements have been carried out on two samples, which are referred to as Samples 1 and 2.

Linearity Measurements

The results of the linearity measurements of Samples 1A (i.e., the A channel of Sample 1) are given for positive-going pulses in Fig. 7(a) and

for negative-going pulses in Fig. 7(b). Measurements have been carried out at a transport clock frequency of 10 MHz and for dc bias values of 0, 0.1, 0.25, and 0.5V applied to V_{IA}. The most linear operation and largest dynamic range for positive-going pulses is obtained at a dc bias of 0V (see Fig. 7(a)). For dc bias values above zero, it can be seen that the curve moves downward. If the dc bias is considered as a part of the input signal, other curves corresponding to different values of dc bias can be obtained very easily if only the curve for zero dc bias is known. As the dc bias is increased, the linear portion of the curve for negative-going pulses increases (see Fig. 7(b)). For a dc bias of 0.1V, the curve can be considered linear for input pulses in the range of (-33 mV) to (+167 mV); this gives a 5:1 ratio for positive- and negative-going pulses.

In Fig. 8, linearity measurements of four channels are given. These measurements have been made at 10 MHz and at zero dc bias. The curves are the same to within 5 percent. This similiarity has also been observed for the dc bias values above zero volt.

In Fig. 9, linearity measurements on Sample 1A at transport clock frequencies of 0.5 MHz, 5 MHz, and 10 MHz are given. This figure shows that the insertion loss of the CCD increases with frequency.

In Fig. 10, the frequency responses of the samples are given. Measurements were made at zero dc bias and with an input signal of 0.5V. The change with transport clock frequency is 15 percent for Sample 1A and 10 percent for Sample 2B.

Noise Measurements

Measured rms noise values versus transport clock frequency for the different samples are given in Fig. 11. A 0V dc bias was used. It is found that noise increases slightly with frequency. At 10 MHz, Sample 2A

had the lowest measured noise (0.702 mV). This corresponds to a signal-to-noise ratio of 49 db (maximum signal amplitude 200 mV). A ratio of 48.6 db was measured for Sample 1A. The signal-to-noise ratio is given in the data sheet as 50 db at a clock frequency of 10 MHz.

Transfer Inefficiency Measurement

Transfer inefficiency product ($n\varepsilon$) measurements of Sample 1A as a function of the output signal amplitude are given in Fig. 12. A transfer clock frequency of 0.5 MHz was used. In the upper set of points, the diamonds show the calculated $n\varepsilon$ values considering only the first deficit (ΔV_1, see Fig. 5) in the leading edge of the pulse, and the deltas show the calculated $n\varepsilon$ values taking into consideration the first and second deficits, (ΔV_1 and ΔV_2) in the leading edge of the pulse. No more than two deficits are taken into consideration because it is evident that, by neglecting the high order deficits (ΔV_3, ΔV_4, ...), a negligible error on the calculated $n\varepsilon$ is introduced. Within the experimental errors, $n\varepsilon$ is constant through the dynamic range except for large output values. In the literature, $n\varepsilon$ or ε is often given using an input signal that corresponds to the half of the maximum full well (1/2 maximum dynamic range). If we follow the same rule, for about 100 mV output $n\varepsilon = 5 \mp 0.35$ percent (considering the first two deficits) and $n\varepsilon = 4.70 \mp 0.25$ percent (considering only first deficit). These values correspond to values of $\varepsilon = 1.923 \times 10^{-4} \mp 0.135 \times 10^{-4}$ and 1.807×10^{-4} per transfer, respectively. In the lower part of Fig. 12, the experimental errors in measuring $n\varepsilon$ are given.

Some $n\varepsilon$ versus output measurements have been made using the other samples and similar results are obtained. For 100 mV output signal, calculated values of $n\varepsilon$ are given below.

Sample	% $n\varepsilon = \frac{\Delta V_1}{V_{out}}$	% $n\varepsilon = \frac{\Delta V_1 + \Delta V_2}{V_{out}}$
1A	4.70 ∓ 0.25	5.00 ∓ 0.35
1B	4.50 ∓ 0.25	4.80 ∓ 0.35
2A	4.30 ∓ 0.25	4.60 ∓ 0.35
2B	4.60 ∓ 0.25	4.90 ∓ 0.35

It is found that by applying a small amount of dc bias (fat zero), $n\varepsilon$ can be decreased. The decrease of $n\varepsilon$ by dc bias is shown in Fig. 13 for Sample 1A at a transport clock frequency of 0.5 MHz. Most of the decrease of $n\varepsilon$ takes place for the first 10 percent bias value ($n\varepsilon$ decreases roughly 50 percent). Above 10 percent increase of dc bias, the decrease in $n\varepsilon$ is very small.

The measured values of $n\varepsilon$ versus frequency for Sample 1A are given in Fig. 14. No noticeable change in $n\varepsilon$ has been found in the frequency range of 0.5-10 MHz.

At 10 MHz, $n\varepsilon$ values of the other samples have been measured; it is found that the measured values are in agreement with the values given in the table above.

Dark Current Measurements

It is found that the shift in the baseline due to the dark current is linear. Because a constant-temperature chamber was not available, no precise dark-current measurements have been taken. But at normal room temperatures the measured dark current was always the value of 1 mV/msec given in the data sheet.

Results of Measurements on the Fairchild CCD 321

A block diagram of the internal organization of the Fairchild CCD 321 is shown in Fig. 15. The charge injection part consists of two gates and a diode. During the operation, ϕ_S is clocked to sample the input signal

that is applied at the V_I input. V_R is a dc reference potential, and the injected charge which is stored into the first well of the 455 cell register will be roughly proportional to V_R-V_I.

Registers are operated in the one and one-half phase mode, where one phase is a clock and the other is V_2, a dc potential. Charge packets that have transferred through the entire analog shift register are applied to the output amplifier; the output amplifier consists of three source-follower stages with constant-current source bias. A sample and hold transistor is located between the second and third stages. If ϕ_R, reset clock, is connected to V_{DD}, output drain voltage, an output in a pulse modulated form will be obtained; otherwise a continuous output waveform will be obtained. The sampled input voltage between t = o and t = t_c appears at the output terminal V_0 at t = 910 t_c.

Measurements were made on four samples of Fairchild CCD 321 to determine linearity, transfer inefficiency, and noise. During the measurements, the values given below are kept constant (see Fig. 16).

$V_{\phi L}$ = Analog shift register transport clocks low = 0V

$V_{\phi H}$ = Analog shift register transport clocks high = 17V

$V_{\phi SL}$ = Input sampling clocks low = 0V

$V_{\phi SH}$ = Input sampling clocks high = 16V

V_{DD} = Output drain voltage = 17V

V_2 = Analog shift register dc transport = 8.5V

Symmetrical clock pulses with about 7 nsec rise and fall times were used. Rise and fall times of the sample pulse were about 7 nsec.

Linearity Measurements

Linearity measurements have been made using the four samples; similar results were obtained. Figure 17 shows the linearity measurements of

Sample 1 for different values of V_R (analog reference input), and V_I (analog input bias) for a transport clock frequency of 1 MHz. (In the data sheets, it is noted that to obtain proper operation, V_R and V_I may be adjusted within the range of 8-13V.) It is noticed that for low values of V_R, linearity is better. Similar results have been obtained with the other samples.

Figure 18 gives the linearity measurements for the four samples for V_R = 9V and a transport clock frequency. No output was obtained for V_I>8.15V with Sample 2. For Sample 3, no output was obtained for V_I>8.40V.

All the samples except Sample 3 gave about the same gain (3 db) and a one volt dynamic range for positive-going pulses.

Figure 19(a) (positive-going signals) and Fig. 19(b) (negative-going signals) show the results of another experiment that was carried out using Sample 1 at a transport clock frequency of 1 MHz. Measurements show that if the V_I increases, the increased part of V_I can be considered as a part of the input signal and the output for different values of V_I can be plotted easily. By adjusting the V_I bias, the linear portions of the curves for both positive- and negative-going pulses can be adjusted.

Transfer Inefficiency Measurements

The measured transfer inefficiency product ($n\varepsilon$) versus output signal amplitude of Sample 1 is given in Fig. 20 for a transport frequency of 1 MHz. It can be shown that neglecting the high order deficits (ΔV_4, ΔV_5, ...) causes a negligible error in the calculated values of $n\varepsilon$. For this reason, only the calculated $n\varepsilon$ values from considerations of the first one, the first two, and the first three deficits are given in Fig. 20. For output signals of 500 mV, the corresponding $n\varepsilon$ values are:

$\frac{\Delta V1}{V_{out}}$ = 8.40 ∓ 0.50%; $\frac{\Delta V1 + \Delta V2}{V_{out}}$ = 9.40 ∓ 0.7%; and $\frac{\Delta V1 + \Delta V2 + \Delta V3}{V_{out}}$ =

9.60 $\mp$ 0.90%. These correspond to (9.23 $\mp$ 0.55) x 10^{-5}; (10.33 $\mp$ 0.77) x 10^{-5}; and (10.55 $\mp$ 0.389) x 10^{-5} loss per transfer, respectively.

It was found that $n\varepsilon$ varies with (V_R-V_I). The lowest values of $n\varepsilon$ were obtained at the highest values of (V_R-V_I).

Figure 21 shows the measured $n\varepsilon$ values versus frequency for Sample 1. There appears to be a slight increase of $n\varepsilon$ with frequency, but within the experimental errors, it could be considered constant. Figure 22 shows the normalized $n\varepsilon$ values versus frequency. Except for Sample 3, a slight increase with frequency has been noticed.

Figure 23 show the normalized frequency response of four samples. Above 10 MHz the gain of the CCDs decreases. At 20 MHz, the worst value is 0.75 for Sample 3. Sample 1 changed the least.

Noise Measurements

In Fig. 24, noise measurements versus frequency are given for the four samples. A slight increase in noise with frequency is found. At 15 MHz, the maximum measured noise is 1.71 mV (rms) for Sample 4, and the minimum is 1.66 mV (rms) for Sample 2. On the data sheet, signal-to-noise ratio is given at 55 db at 15 MHz. For an output of 1000 mV output, 55 db corresponds to 1.78 mV (rms) of noise. The signal-to-noise ratio in the data sheet is obtained using a noisemeter that has a bandwidth of 4.2 MHz.

Dark Current Measurements

It is found that the shift in the baseline due to dark current is linear. Although the dark current at 25°C is given as 10 mV/msec in the data sheet, present measurements at room temperature indicate that its value is larger than that. Because a constant temperature chamber was not available, no precise dark-current measurements were taken.

Timing Measurements

Requirements for timing between the transport and sample clocks to

obtain proper operation were investigated. Timing parameters are shown in Fig. 16, and measured maximum and minimum usable values are given in Table 1.

TABLE 1 TIMING REQUIREMENTS FOR TRANSPORT AND SAMPLE PULSE

Time	Given Typical Values in Data Sheet (nsec)	Measured Minimum Values (nsec)	Measured Maximum Values (nsec)
t_1	10	5	40 and up
t_2	10	5	40 and up
t_3	5.0	5	100 and up
t_4	5.0	5	100 and up
t_5	15	10	100 and up
t_6	5.0	5	40 and up
t_7	5.0	5	40 and up
t_8	5.0	5	40 and up

The following conclusions were reached.

1. It is found that in timing requirements only the minimum values are important; it is noticed that only the frequency will limit the maximum values (except Sample 3).
2. It is not necessary to use a symmetrical wave shape for the transport clock.
3. The change in the amplitude of the transport clock between 16 and 18V, and of the sampling pulse between 14 and 17V makes no noticeable change on the operation
4. To obtain a low n_ε at high frequencies (i.e., 20 MHz), the V_{DD} should not be less than 17V.

Theoretical Considerations

In this section, certain theoretical aspects of CCD technology are reviewed. Particular attention is given to those aspects related to the measurements described above.

Linearity

In a suitably designed and operated CCD, the transfer loss will be proportional to the signal charge. Therefore, non-linearities associated with the transfer of the charge packets should be negligible as compared to non-linearities related to the signal injection and detection.

For good linearity, the relation between the injected charge packets and the input signal must be stable and linear within the dynamic range of the device. The dependence on the threshold voltage must be as small as possible. The linearity of the voltage sensitive input using the "diode cutoff" method is limited by the changing depletion capacitance of the metering potential well and by charge redistribution effects during turn-off of the cutoff gate.[2] The quantity of charge carriers in the metering well follows the input signal while the input gate is open. However, if the gate is turned off rapidly, or if the cutoff point changes with time, a charge splashing takes place. If the sampling gate is closed slowly--that is, with a ramp function--a considerable change in the effective sampling momemt takes place and produces some additional non-linearities. This means the linearity of the CCD in a system depends in part on the control signal waveforms.

Another source of non-linearity is at the CCD output, where signal distortion can be introduced by the detection node. The change in the depletion capacitance around the sensing diode or around the potential well in which the signal will be detected produces a non-linear term.

By using an increased channel width in the sensing MOS-FET, this problem can be solved. This MOS-FET arrangement also lowers the output impedance.

Transfer Inefficiency

Transfer inefficiency is one of the most important parameters of a charge-coupled device, because it influences directly the fidelity of wave shapes of the signals. Transfer inefficiency, $\varepsilon = (1-\eta)$, was first defined by Joyce and Bertram.[3] In this equation η shows the transfer efficiency for a single transfer.[4,5] If ε is multiplied by the number of transfers, n, required to traverse the device, the transfer inefficiency product, $n\varepsilon$ is obtained.

In a buried-channel CCD (BCCD), there are two sources of transfer inefficiency. First, charge carriers may be inhibited from moving because of the local regions of lower potential energy. This problem is related with the design of a particular device. Recent advances in CCD technology have considerably reduced the importance of this problem. Second, the operation frequency may be so high that there is not enough time for all the charge carriers to follow the movement of the potential wells.

If ε is a constant fraction and independent of signal charge, the product, $n\varepsilon$, increases linearly with the number of transfers.

If CCD is operated without a fat zero (which means the zero signal is represented by a truly empty well), the leading edge of a pulse train experiences some additonal loss. A certain amount of charge, δ, in the leading edge of the pulse train goes to fill the interface states of bulk traps (BCCD). If the first charge packet cannot provide enough charge to fill the traps and interface states, the second charge packet will provide additional charge, and so on.

In the CCD, the total transfer loss can be described with the combination of these two losses. First, a fraction loss, ε, proportional to the

signal; second, a constant loss, δ, which is independent of the signal and increases with the number of preceding empty packets.

Noise

Three sources contribute to BCCD noise: input noise, transfer noise, and output noise. Various mechanisms internal to the BCCD give rise to these three noise sources.

It should be carefully noted that, with the exception of the output amplifier noise, all noise sources contribute to noise, or uncertainties, in the output signal levels. Consider for a moment an output amplifier that is noise free. Also imagine that a constant voltage is applied to the signal input of the CCD. Then, during each transfer-clock period, a constant voltage level will appear at the signal output of the CCD; however, the levels will vary from one clock period to the next because of the internal noise sources. If we now consider the output amplifier to be noisy, a certain amount of "real-time" noise is added--that is, there will now be random fluctuations in the output signal during each clock period. The latter are usually smaller than the fluctuations from one level to the next arising from the internal noise sources.

Input Noise

The noise that comes from the input of a CCD largely depends on the charge-injection procedure. The charge injection from source diffusion into a potential well is a random process because of the thermal noise in the resistance of the input circuit. For this reason, the number of injected carriers is a random variable.

In the "diode cutoff" method, the noise that comes from the insertion of the carriers may be higher. This results from the excessive fluctuations associated with the dynamic setting of charge and the random fluctuations in the voltage levels and pulse jitter of the clocking pulses.

In the case where the sampling gate is pulsed, the turn-off of the input channel also produces some additional noise fluctuations due to the partitioning of the input channel charge between the input diode and the first potential well.

Transfer Noise

In a BCCD, a certain amount of charge is left behind at each transfer as charge packets travel along the CCD. These charges left behind show random fluctuations, and therefore introduce noise. Due to the correlation of the incomplete charge transfer fluctuations in the neighboring charge packets, the spectral density of the transfer noise is suppressed at low frequencies.[6,7] There are two sources contributing to the transfer noise in BCCD's: bulk state noise and dark-current noise.

Bulk state noise--because of the trapping and emission of bulk states, the transfer of carriers from one site to another shows fluctuations and therefore introduces noise in the signal traveling along the BCCD.[8,9] Because of the discrete trap levels in the bulk, the associated noise is frequency dependent. This noise is also dependent on the signal size. If the signal charge decreases in size, its occupied volume will also decrease. This means that the number of bulk states it interacts with will also decrease.[9]

Dark current noise--the intrinsic generation of the hole electron pairs in the depleted silicone substrate, the diffusion of minority carriers from the neutral bulk, and the carriers generated in the depleted region by recombination-generation centers are the main sources of dark current. All these phenomena are random.

Although current densities as low as 5nA cm^{-2} are obtained at room temperature, some cells may have local current densities of several hundred nanoampere per square centimeter. The high local current densities

result from the presence of certain impurities in the bulk; these impurities create the necessary midband recombination centers.

If the transport clock frequency is changed during the operation of a CCD, (as in the application described above) the amount of dark current in the individual cells is different, and a fixed pattern of noise will be observed at the output of the CCD. By cooling the CCD, both dark current and the dark current noise can be reduced.

Output noise--there are two sources of CCD output noise: reset noise and output amplifier noise.

Reset noise: If the CCD read out involves the charging of a capacitance through a switch (reset), another noise contribution appears. Due to thermal noise in the reset circuit, the reset level is a random variable.

Output amplifier noise: The output voltage due to the various noise sources of the output amplifier is a random variable.

If the total experimental noise is considered, other noise sources such as the quantization noise at the Analog-to-Digital Converter should be considered. The ADC unit used in the experimental set up introduced a noise which can be called quantization noise. Since it was a 10-bit ADC unit, a quantization noise which corresponds 60 db signal-to-noise ratio was introduced by this unit.

Other amplifier units used after the CCD will also introduce noise.

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6. M. F. Tompsett "The quantitative effects of interface states on the performance of charge coupled devices," IEEE Transactions on Electron Devices, Ed.-20, 1973, pp. 45-55.

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8. A. M. Mohsen and M. F. Tompsett "The effects of bulk traps on the performance of bulk channel charge coupled devices," International Conference, Edinburgh, 1974, pp. 67-74.

9. A. M. Mohsen and M. F. Tompsett "The effects of bulk traps on the performance of bulk channel charge coupled devices," IEEE Transactions on Electron Devices, Ed.-21, 1974, pp. 701-712.

Work performed under the auspices of the U. S. Energy Research and Development Administration.

Captions

Fig. 1. A schematic representation of a typical CCD.

Fig. 2. Simplified block diagram of a portion of a chamber read-out system using CCDs. Sixteen chamber wire signal channels are shown.

Fig. 3. This shows the effects of CCD dark current at the output of the CCD during a read-in/read-out sequence. This input (wire) signal is assumed to be held continuously at its zero level.

Fig. 4. Block diagram of the system used to measure the CCD characteristics.

Fig. 5. Waveform at output of CCD when a pulse of the order of ten clock periods wide is applied to the input. This shows the deficits on leading and trailing edges caused by transfer inefficiency, and the baseline shift caused by dark current. The effect of internally generated noise on the baseline is also shown.

Fig. 6. Internal organization of Fairchild CCD 311.

Fig. 7. Result of linearity measurements on Sample 1A of Fairchild 311 for (a) positive-going pulses and (b) negative-going pulses.

Fig. 8. Results of linearity measurements on four channels of CCD 311. All at a dc bias of OV.

Fig. 9. Results of linearity measurements on one channel of CCD 311 at three transport clock frequencies.

Fig. 10. Transport clock frequency responses of four samples of CCD 311. For each sample, the output is normalized at 10 MHz.

Fig. 11. RMS output noise as a function of transport clock frequency for CCD 311.

Fig. 12. Transfer inefficiency product (upper curves) as a function of output signal amplitude, together with experimental errors (lower curves) for CCD 311.

Fig. 13. Transfer inefficiency product versus bias charge for CCD 311.

Fig. 14. Transfer inefficiency product versus transport clock frequency for CCD 311.

Fig. 15. Internal organization of Fairchild CCD 321.

Fig. 16. Transport clock and sampling clock parameters.

Fig. 17. Output versus input for Sample 1 of the Fairchild 321 for four bias conditions.

Fig. 18. Output versus input for four samples of Fairchild 321.

Fig. 19. Output versus input for (a) positive-going signals, and (b) for negative-going signals for CCD 321 Sample 1 for four values of V_I.

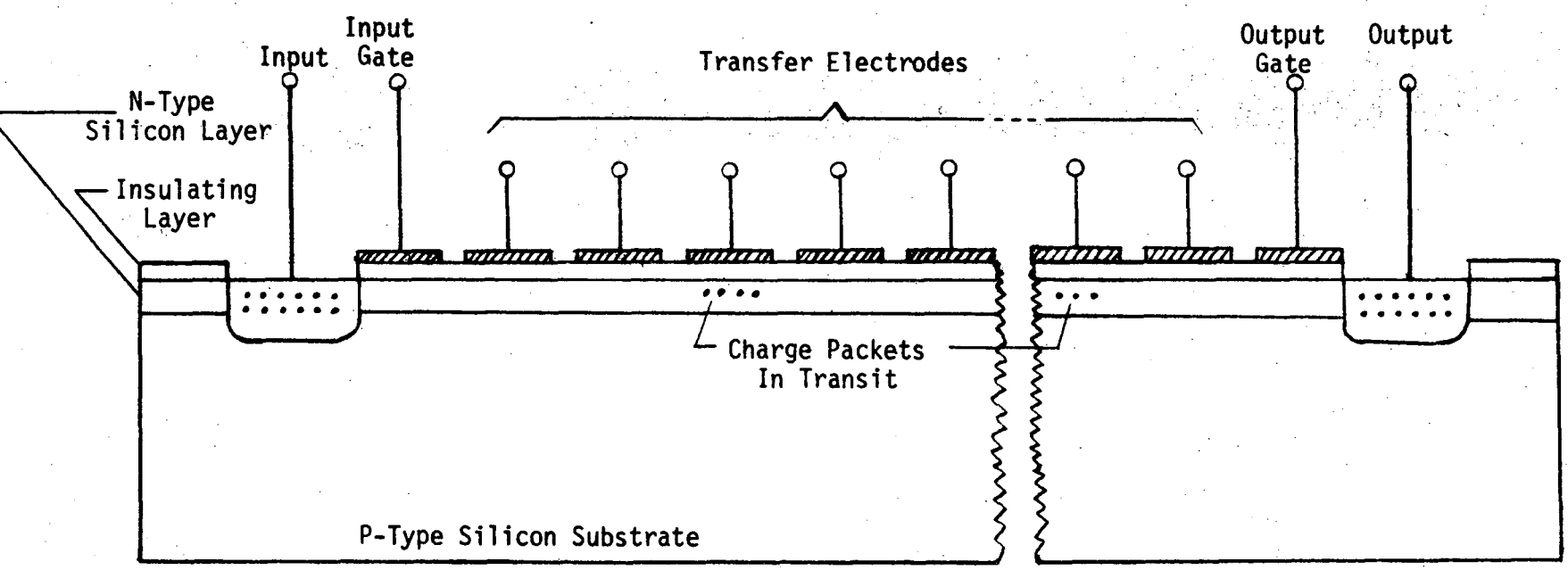
Fig. 20. Transfer inefficiency product (upper points) and measurement errors (lower points) as a function of output signal amplitude for CCD 321.

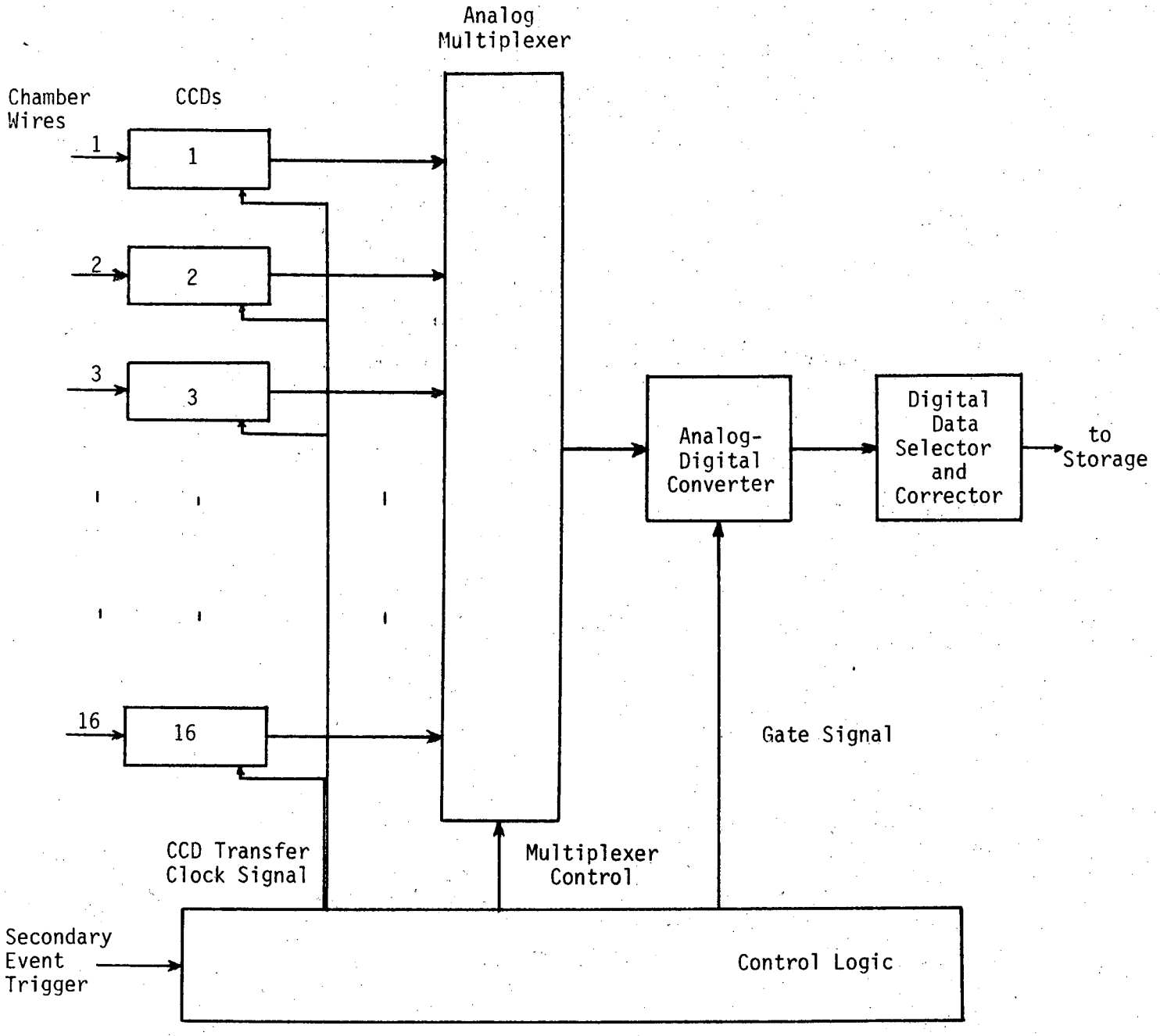
Fig. 21. Transfer inefficiency product as a function of transport clock frequency for Sample 1 of CCD 321.

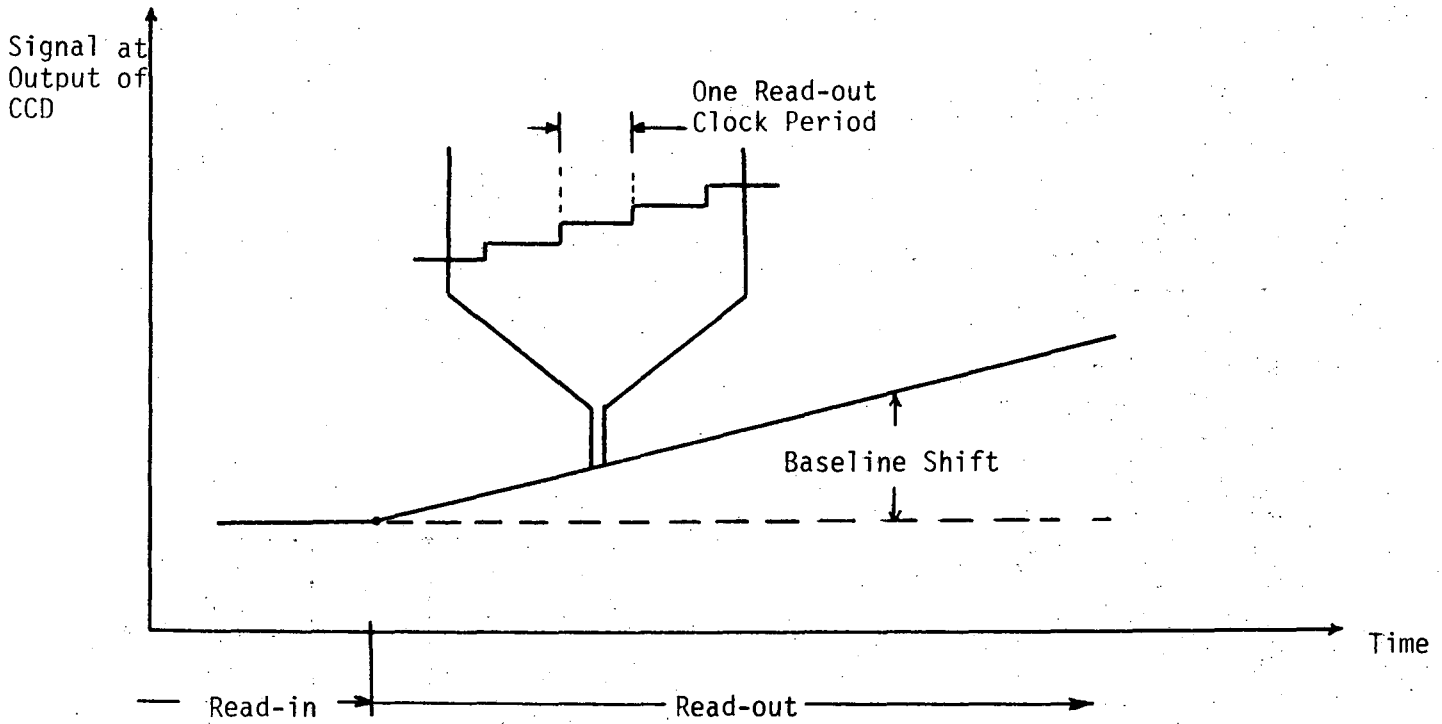
Fig. 22. Normalized transfer inefficiency product versus frequency CCD 321.

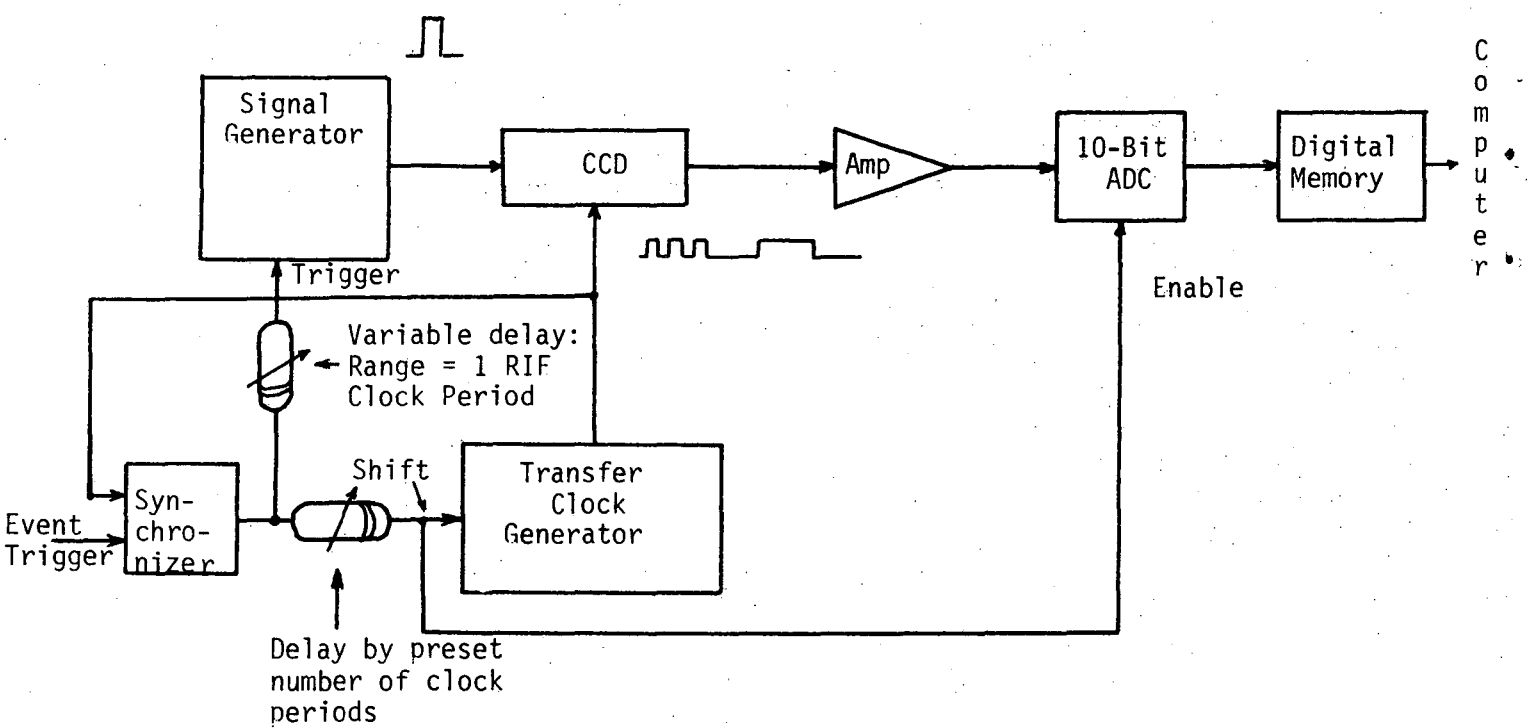
Fig. 23. Normalized output response versus transport clock frequency for CCD 321.

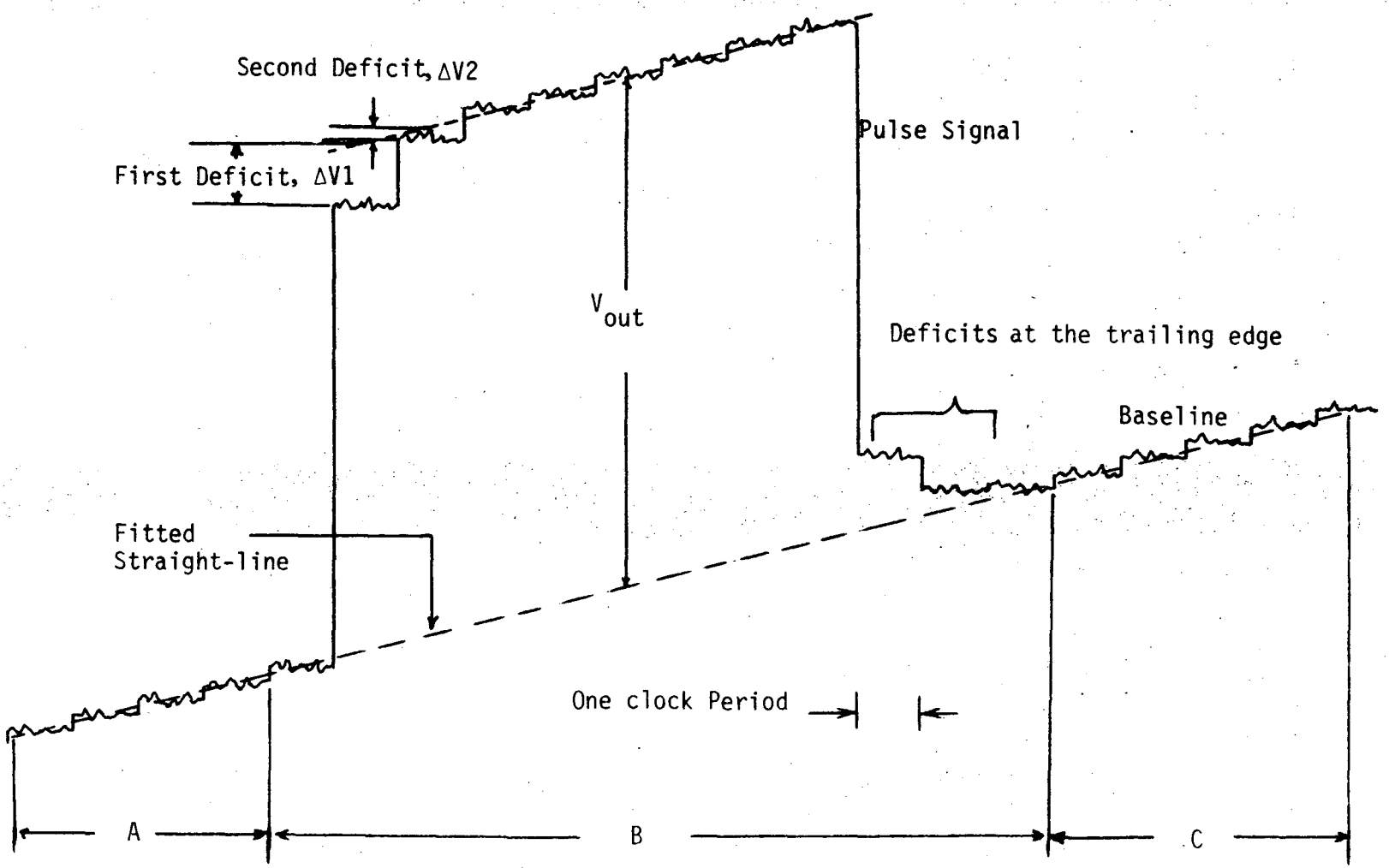
Fig. 24. Output noise versus transport clock frequency for CCD 321.

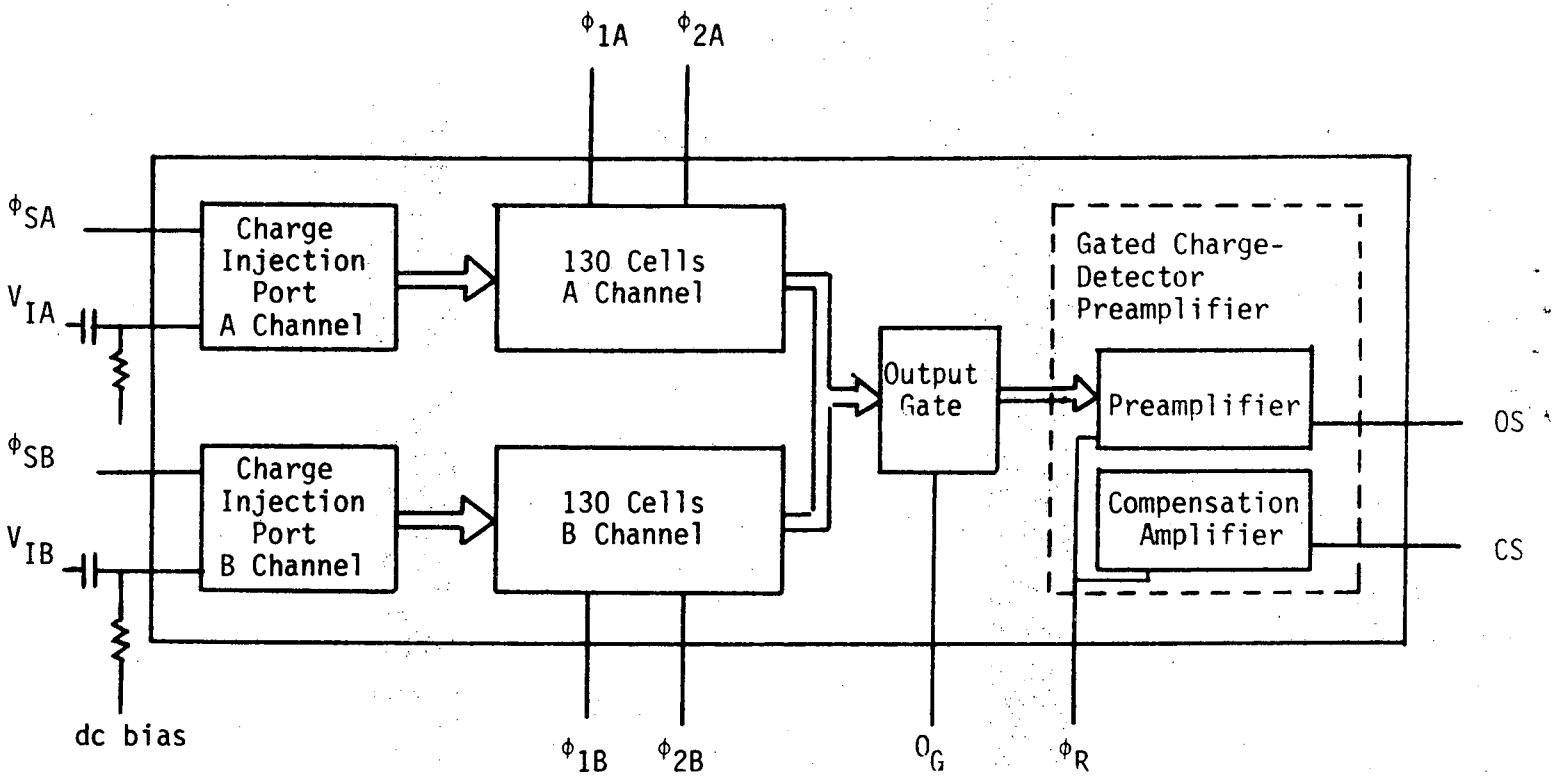

Input
Input Gate
Transfer Electrodes
Output Gate
Output
N-Type Silicon Layer
Insulating Layer
Charge Packets In Transit
P-Type Silicon Substrate

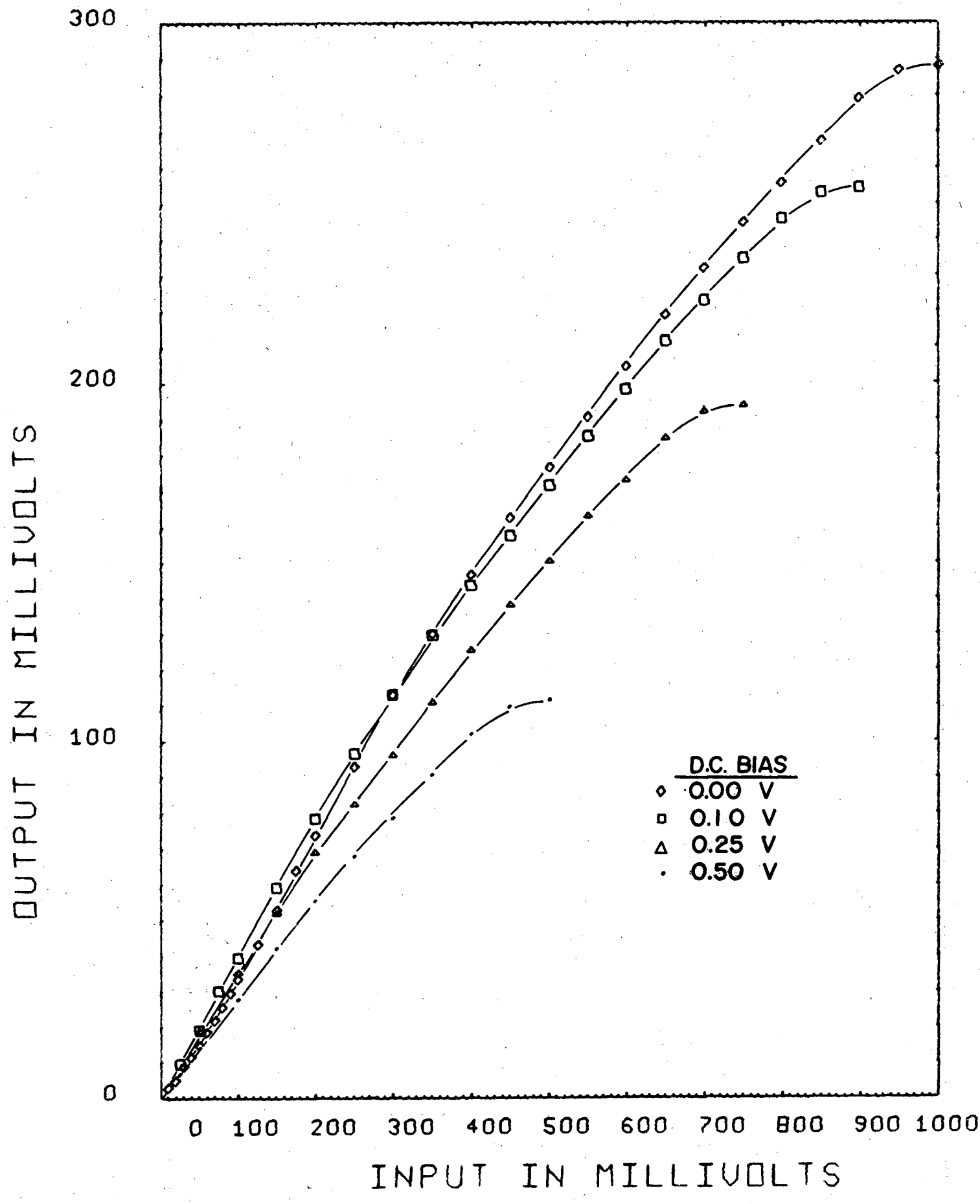


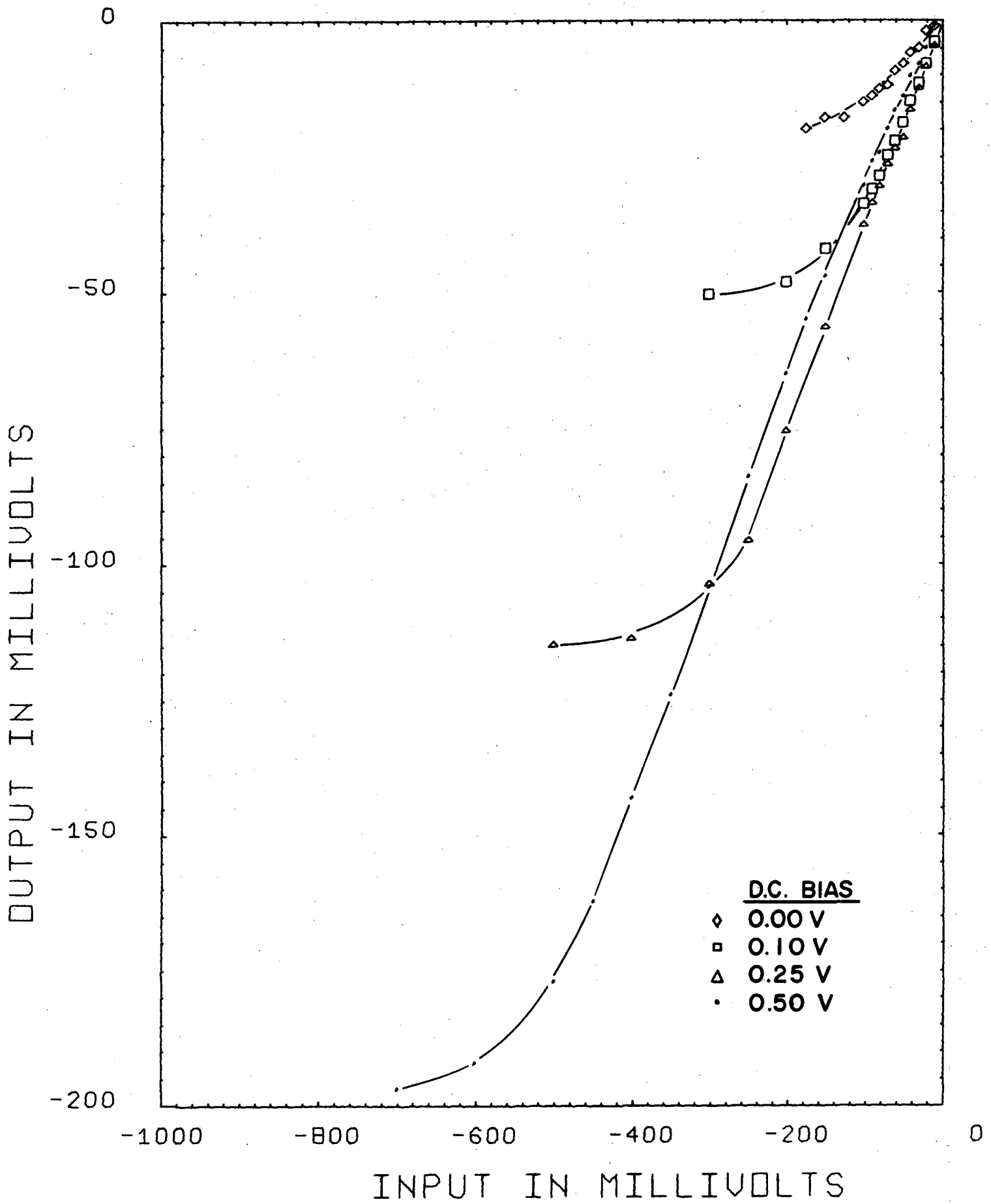

Signal at Output of CCD
One Read-out Clock Period
Baseline Shift
Time
Read-in
Read-out

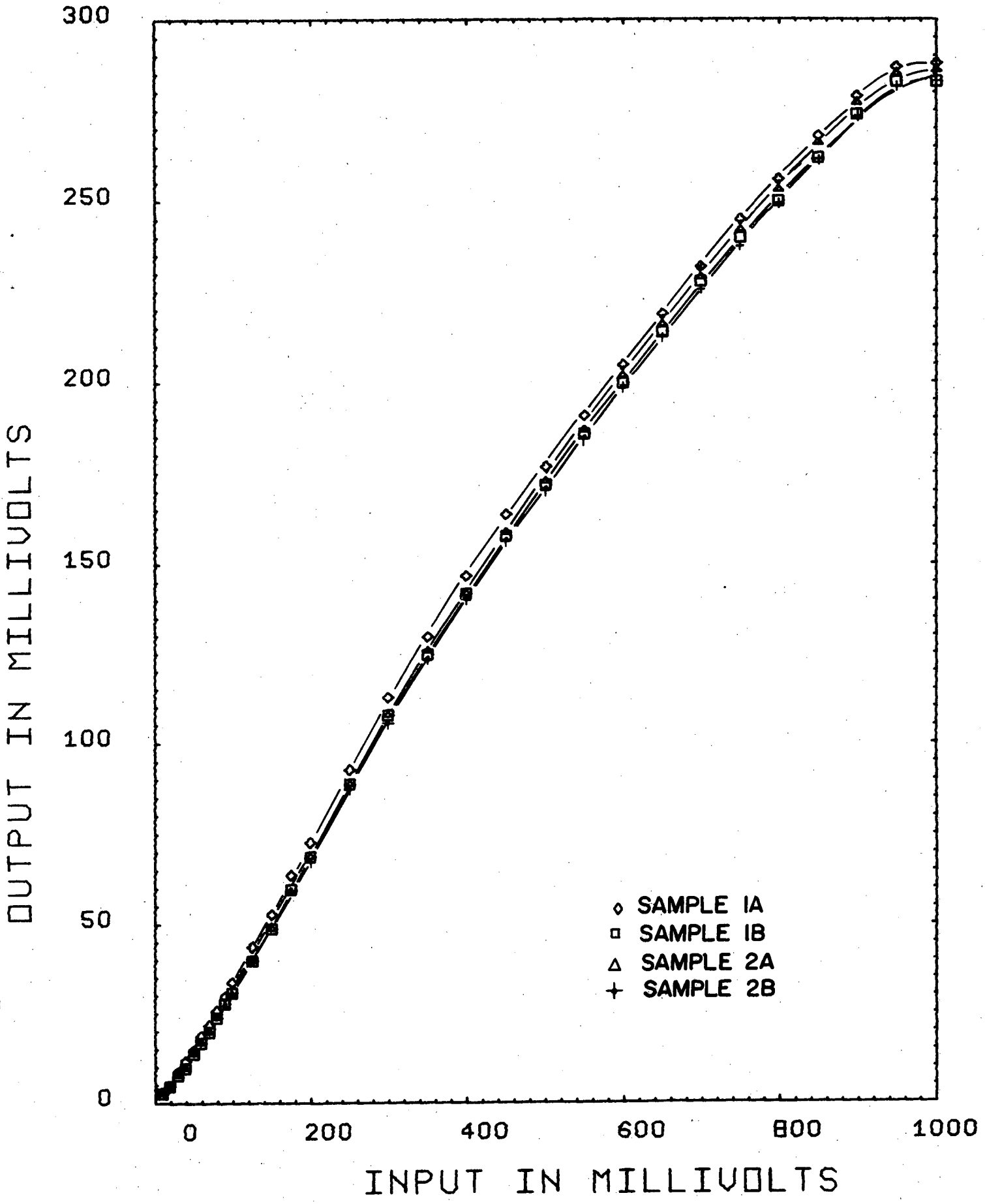

Signal Generator
CCD
Amp
10-Bit ADC
Digital Memory
Computer
Trigger
Enable
Variable delay: Range = 1 RIF Clock Period
Shift
Transfer Clock Generator
Event Trigger
Syn-chro-nizer
Delay by preset number of clock periods

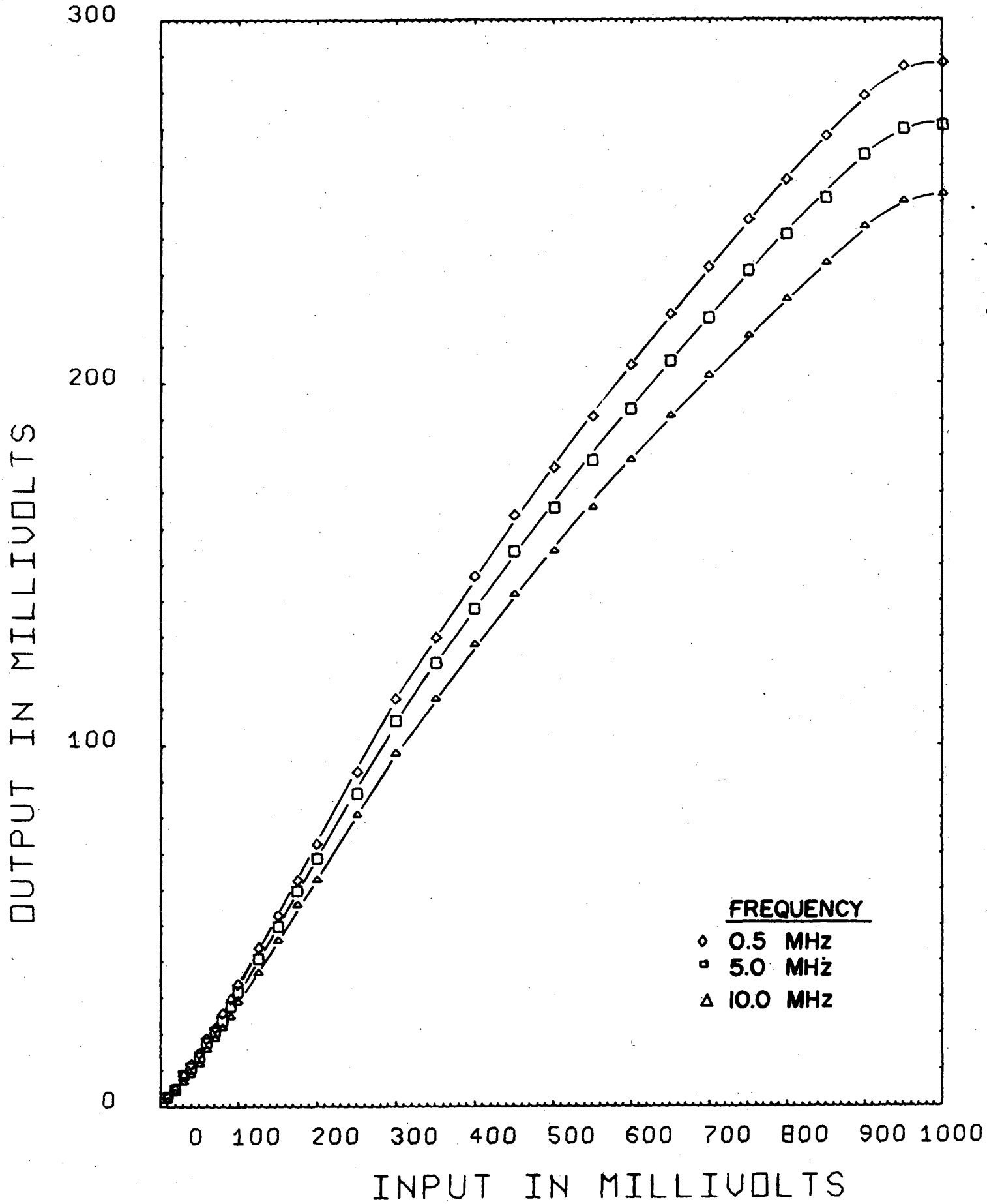

Second Deficit, ΔV2
First Deficit, ΔV1
Pulse Signal
V_{out}
Deficits at the trailing edge
Baseline
Fitted
Straight-line
One clock Period
A
B
C

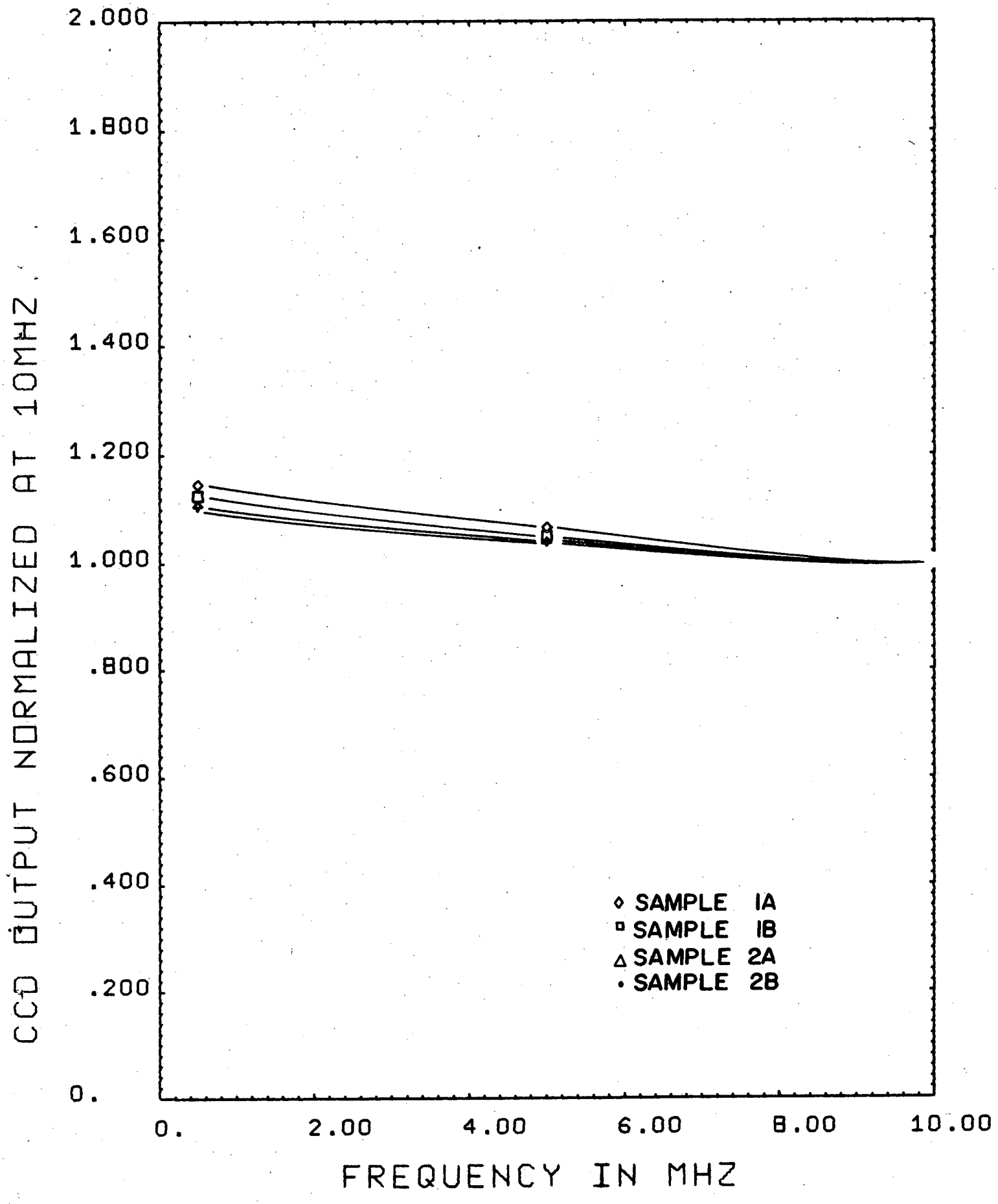

ϕ_{1A}
ϕ_{2A}
ϕ_{SA}
V_{IA}
Charge Injection Port A Channel
130 Cells A Channel
Gated Charge-Detector Preamplifier
Output Gate
Preamplifier
OS
ϕ_{SB}
V_{IB}
Charge Injection Port B Channel
130 Cells B Channel
Compensation Amplifier
CS
dc bias
ϕ_{1B}
ϕ_{2B}
O_G
ϕ_R

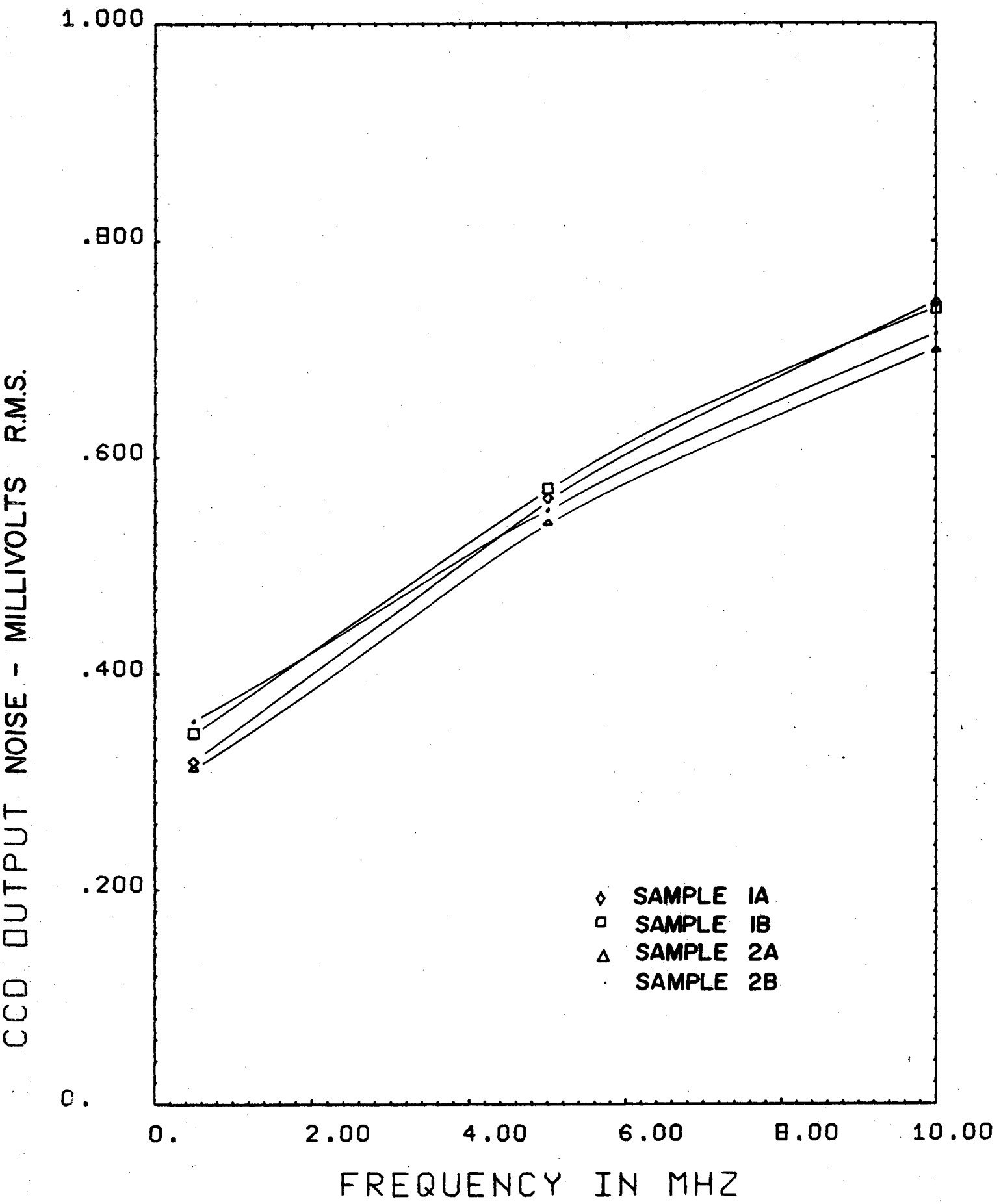


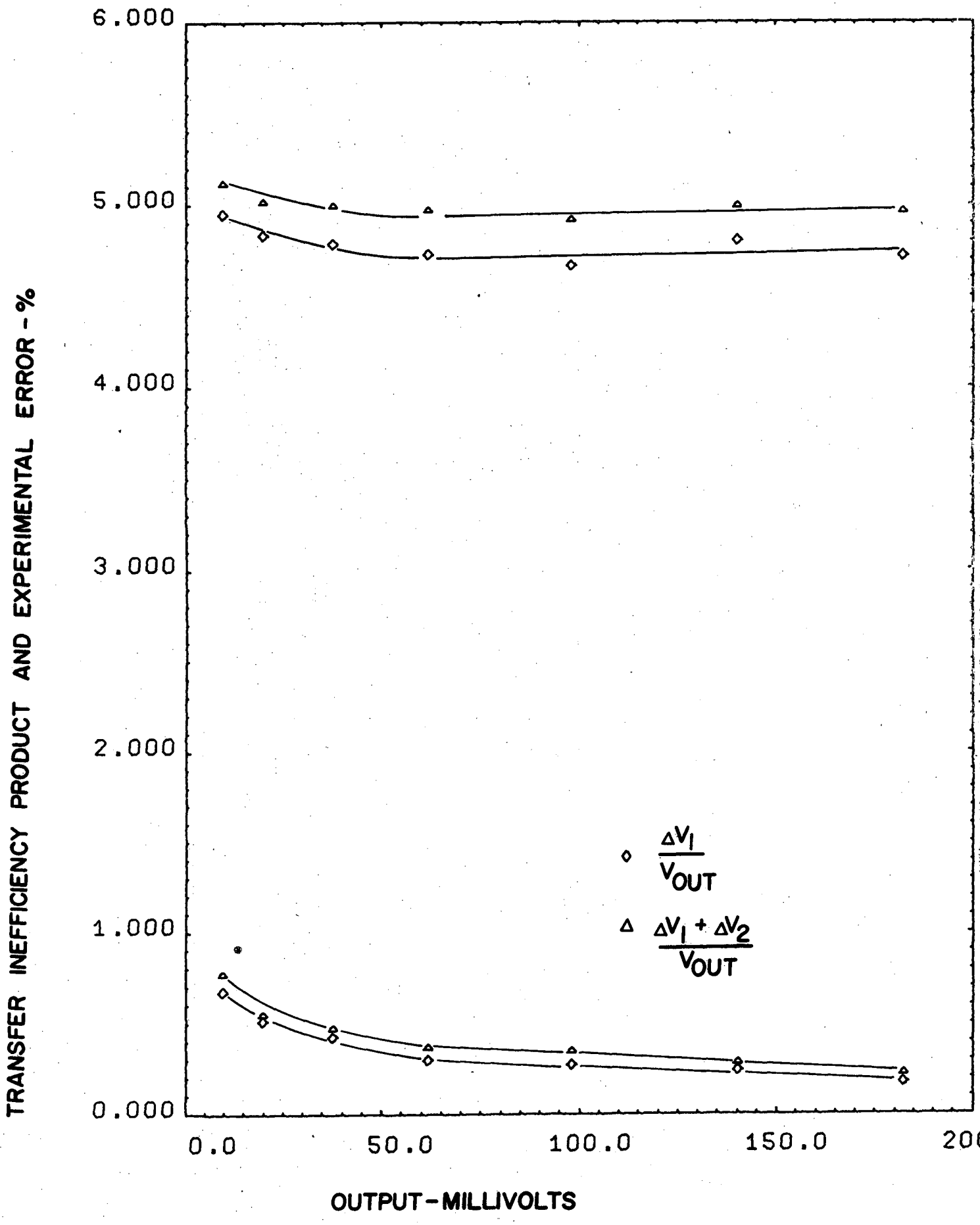

0
-50
-100
-150
-200
OUTPUT IN MILLIVOLTS
-1000
-800
-600
-400
-200
0
INPUT IN MILLIVOLTS
D.C. BIAS
0.00 V
0.10 V
0.25 V
0.50 V

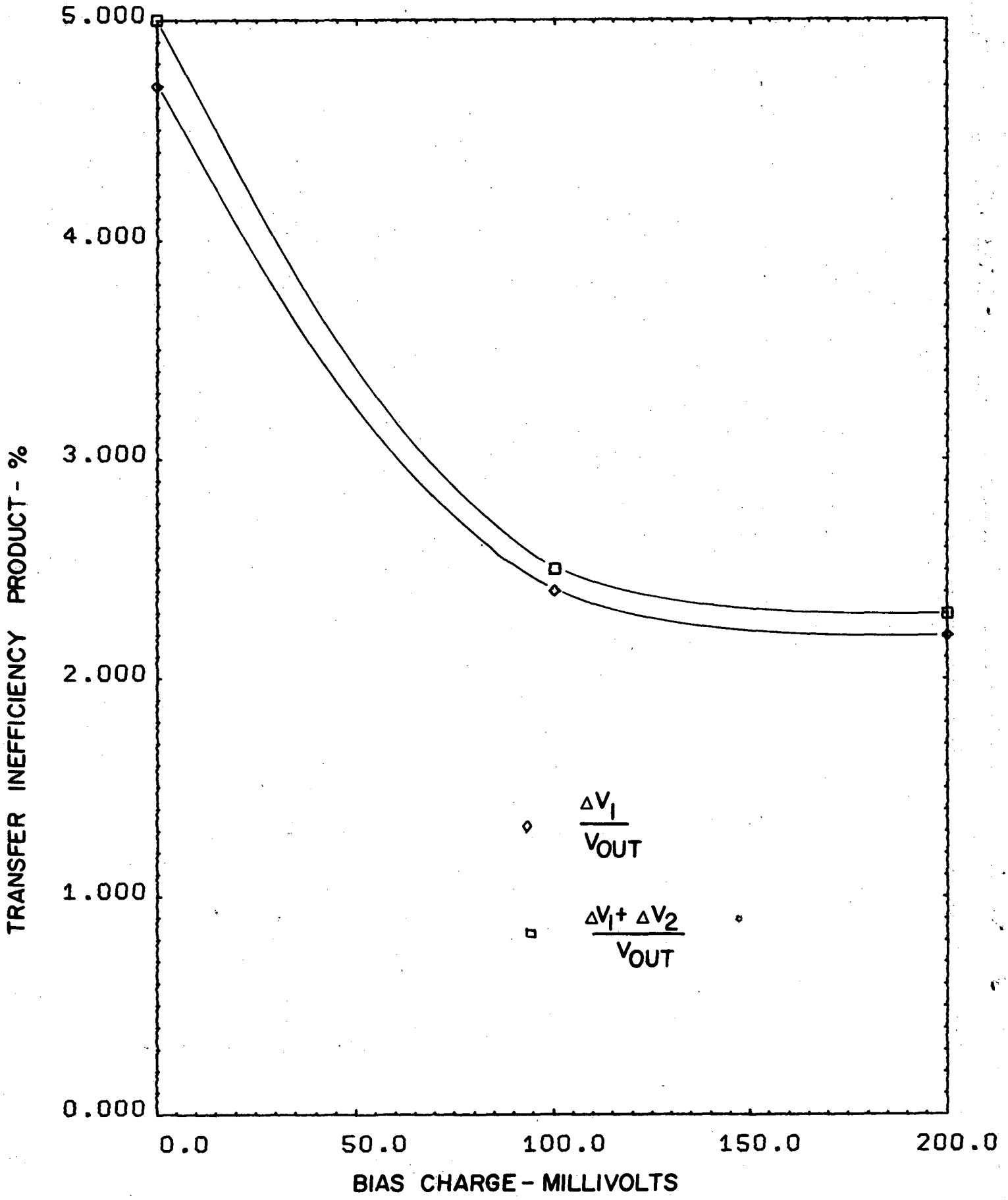


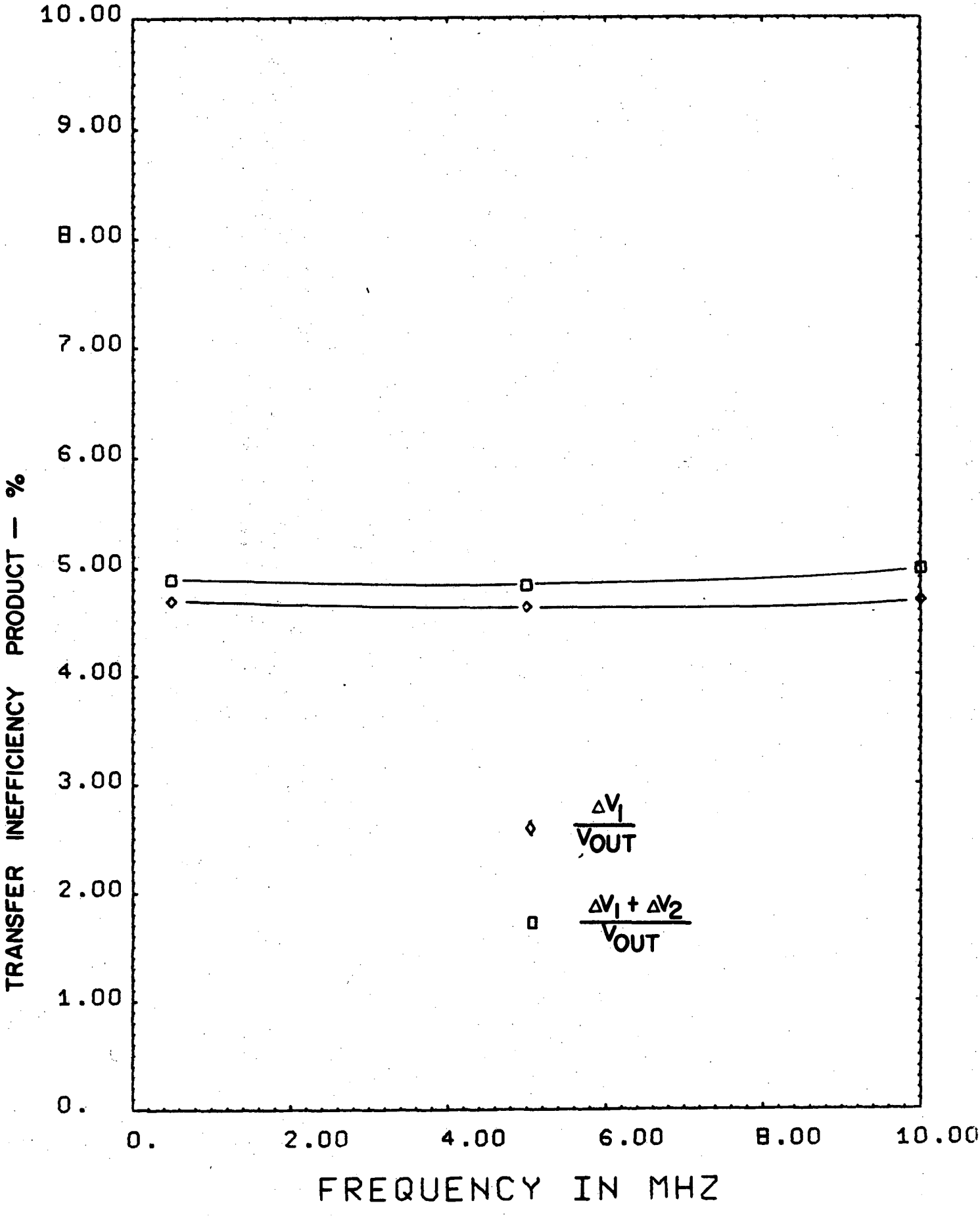

300
200
100
0
OUTPUT IN MILLIVOLTS
0 100 200 300 400 500 600 700 800 900 1000
INPUT IN MILLIVOLTS
FREQUENCY
0.5 MHz
5.0 MHz
10.0 MHz

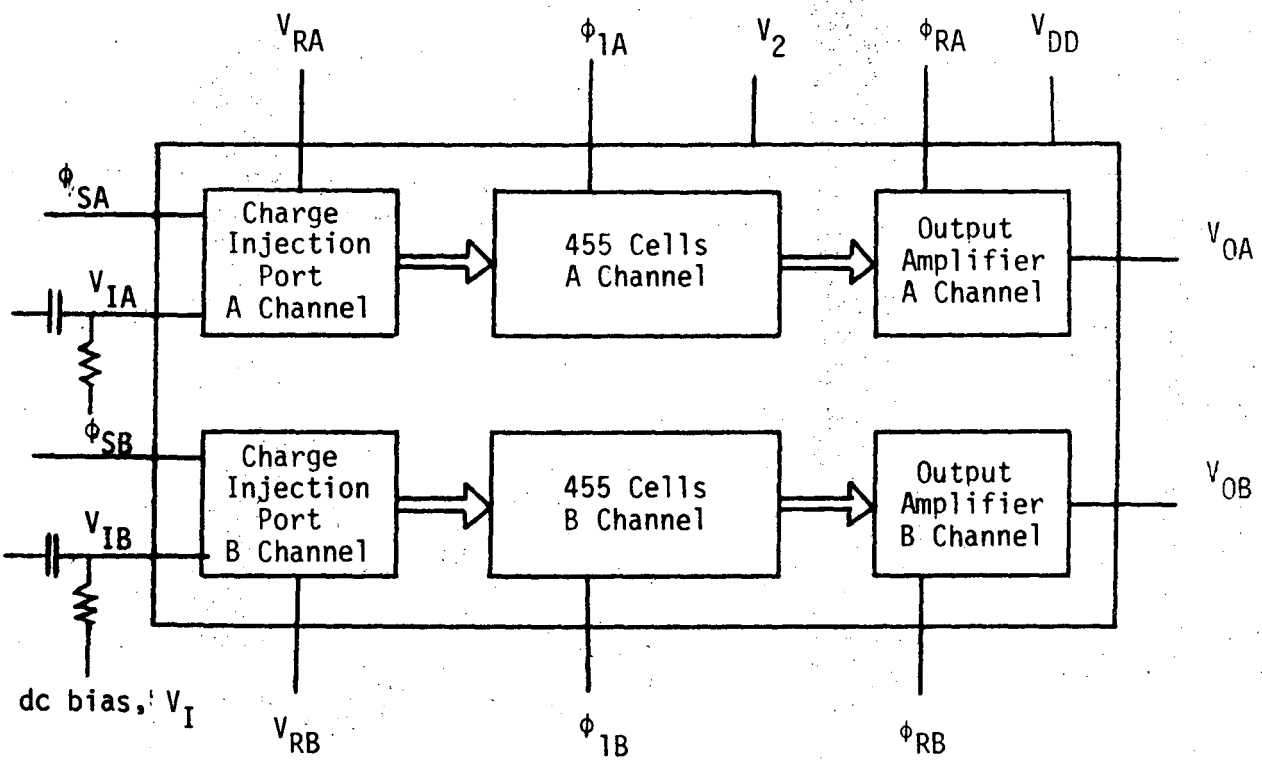


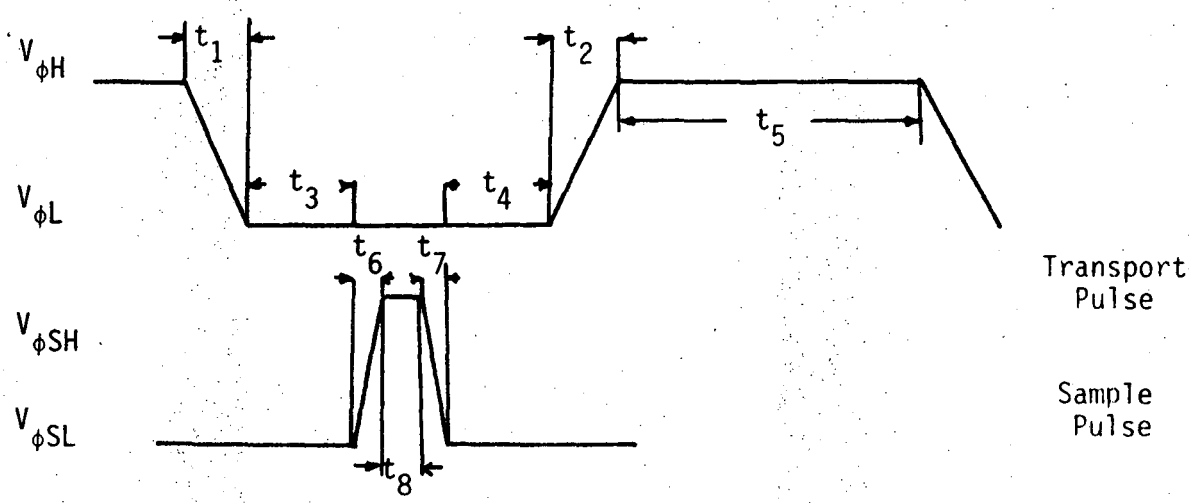

1.000
.800
.600
.400
.200
0.
CCD OUTPUT NOISE - MILLIVOLTS R.M.S.
SAMPLE 1A
SAMPLE 1B
SAMPLE 2A
SAMPLE 2B
0.
2.00
4.00
6.00
8.00
10.00
FREQUENCY IN MHZ

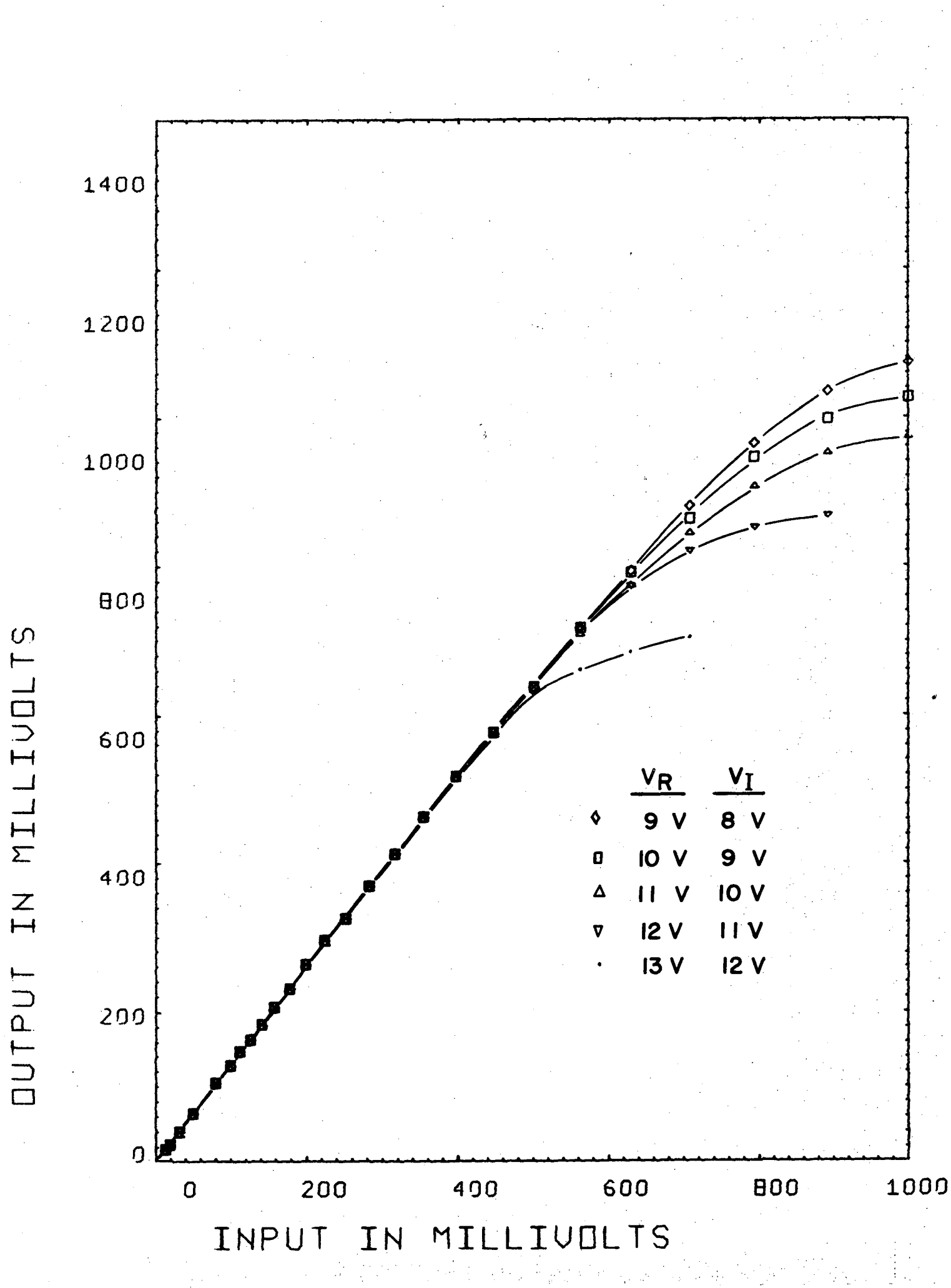


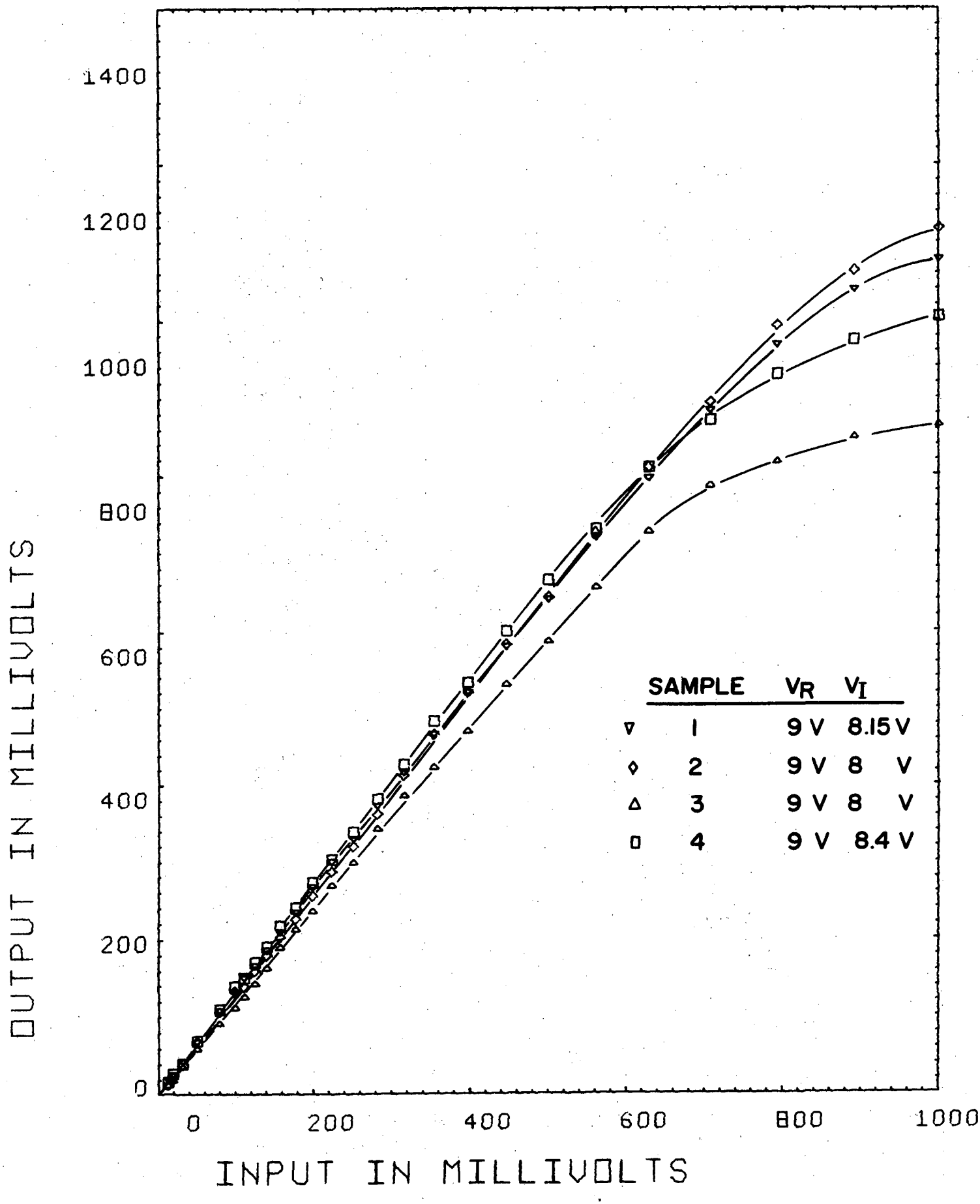

5.000
4.000
3.000
2.000
1.000
0.000
TRANSFER INEFFICIENCY PRODUCT - %
0.0
50.0
100.0
150.0
200.0
BIAS CHARGE - MILLIVOLTS
$\frac{\Delta V_1}{V_{OUT}}$
$\frac{\Delta V_1 + \Delta V_2}{V_{OUT}}$

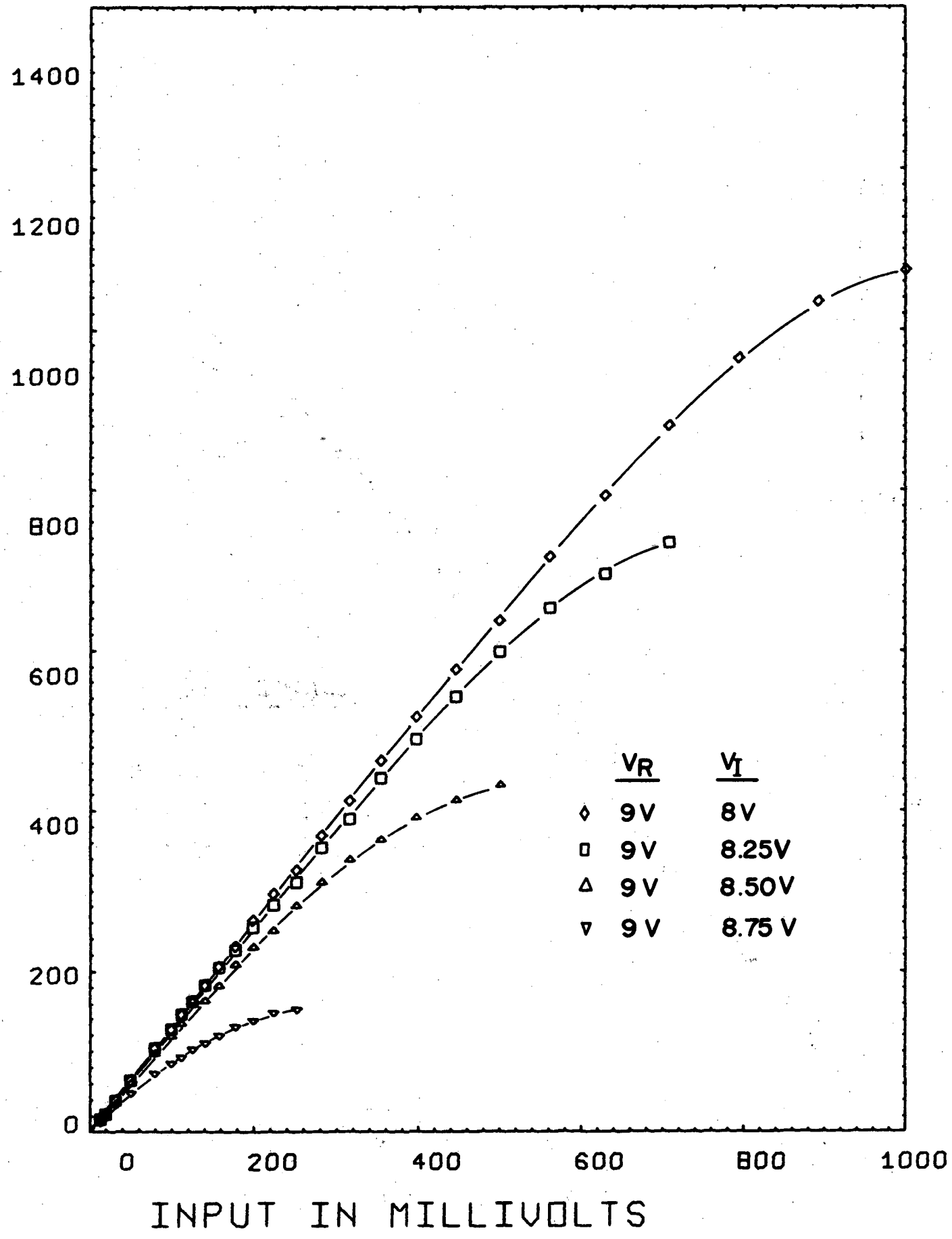


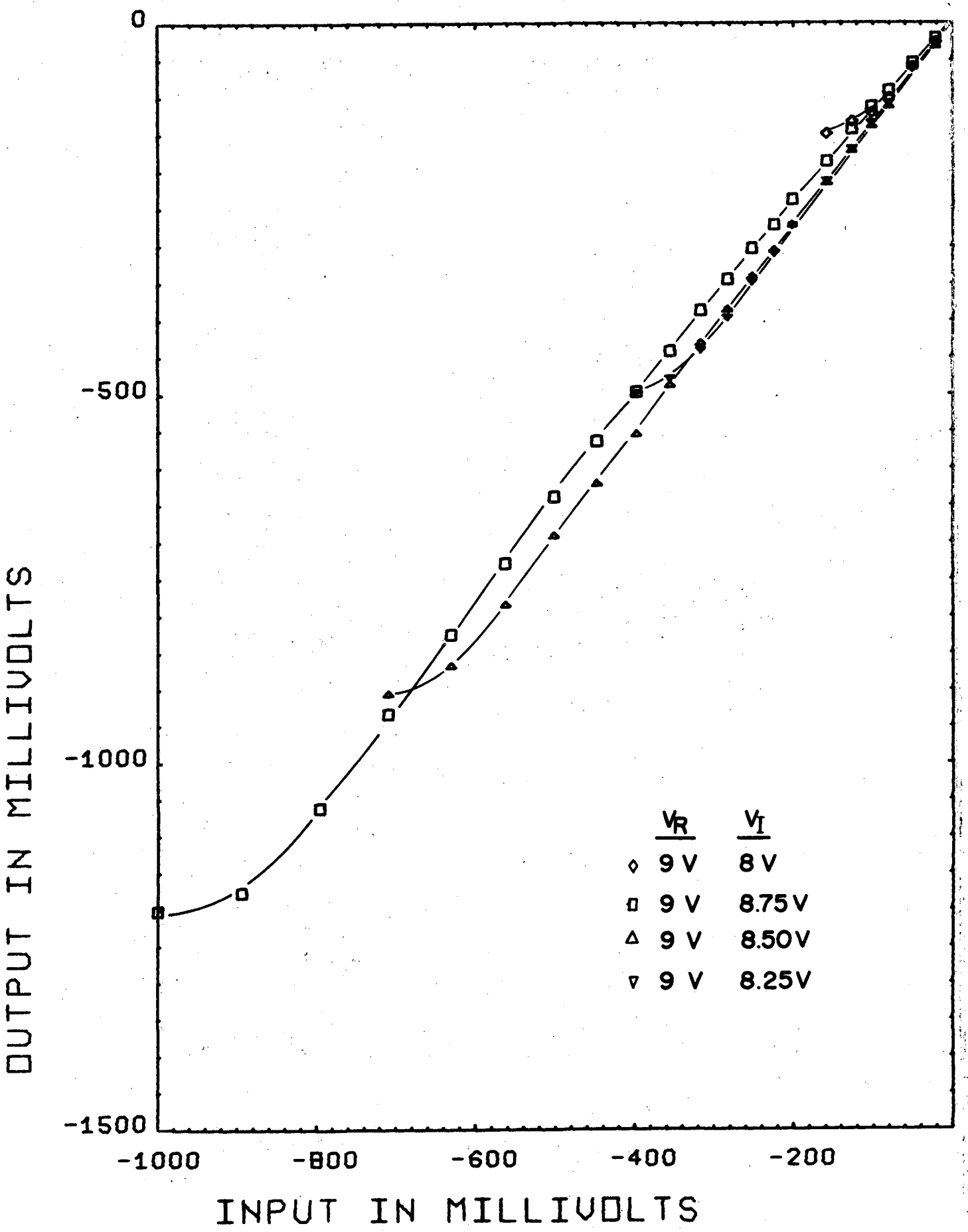

V_{RA}
ϕ_{1A}
V_2
ϕ_{RA}
V_{DD}
ϕ_{SA}
V_{IA}
Charge Injection Port A Channel
455 Cells A Channel
Output Amplifier A Channel
V_{OA}
ϕ_{SB}
V_{IB}
Charge Injection Port B Channel
455 Cells B Channel
Output Amplifier B Channel
V_{OB}
dc bias, V_I
V_{RB}
ϕ_{1B}
ϕ_{RB}

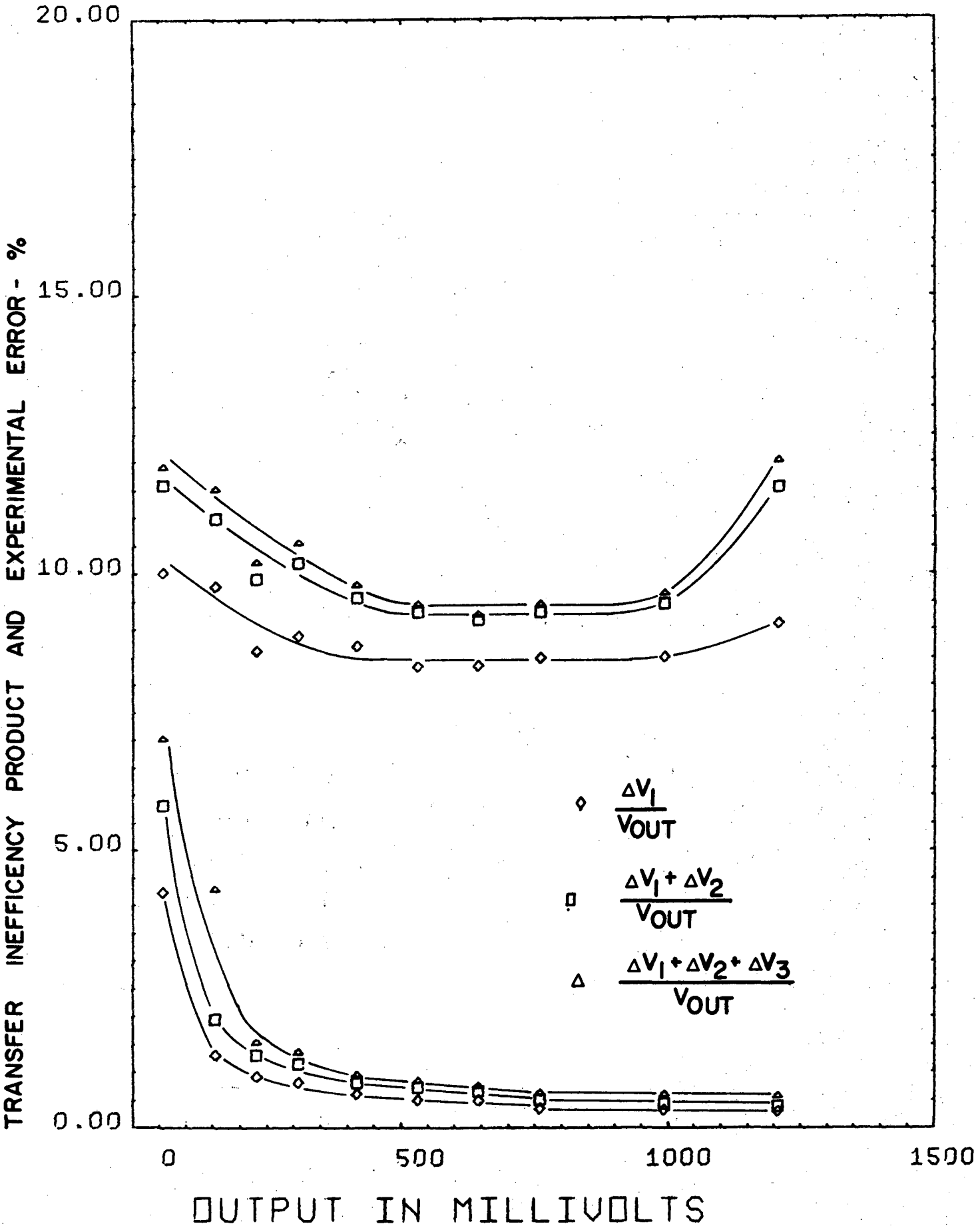


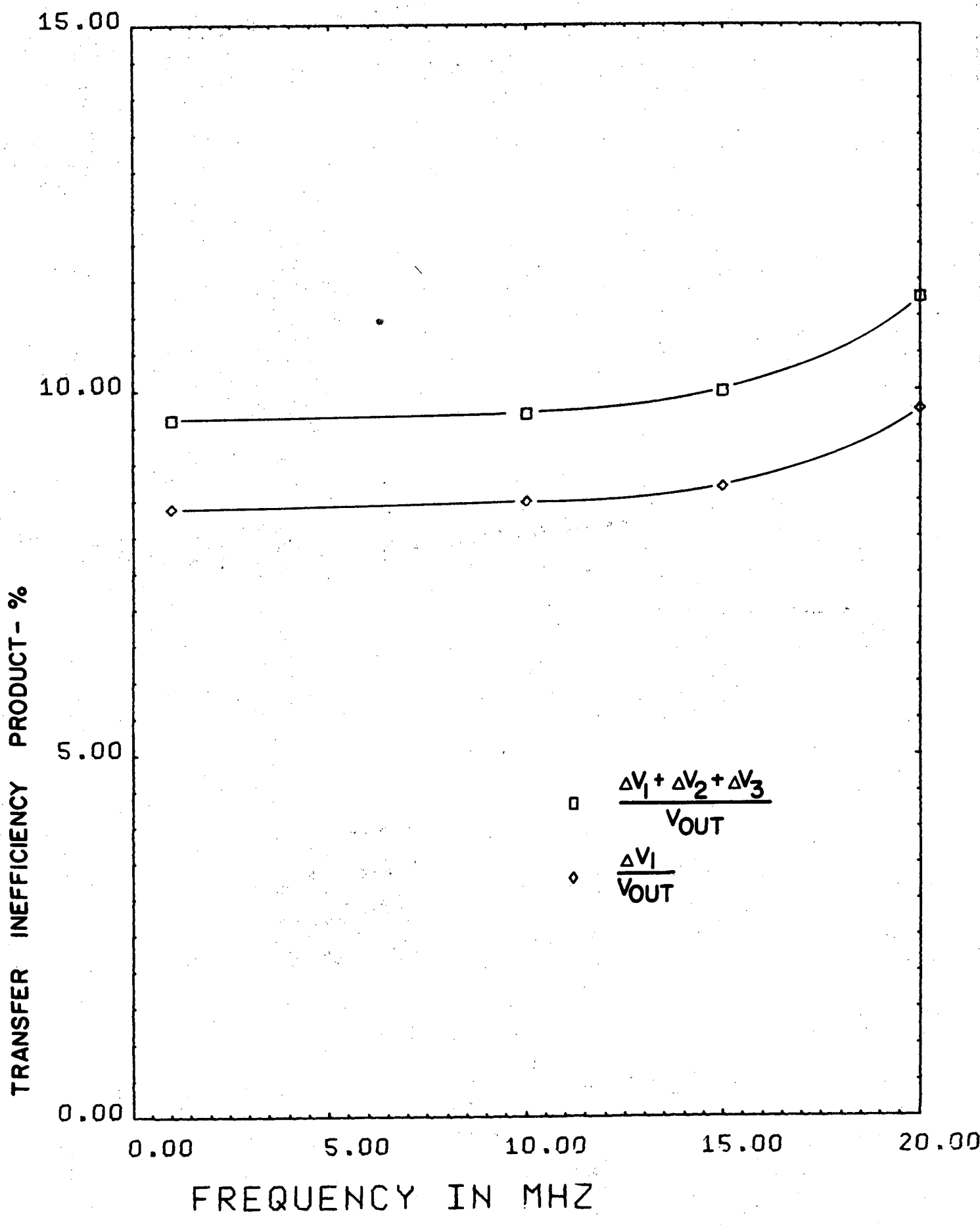

1400
1200
1000
800
600
400
200
0
OUTPUT IN MILLIVOLTS
0
200
400
600
800
1000
INPUT IN MILLIVOLTS
VR
VI
9 V
8 V
10 V
9 V
11 V
10 V
12 V
11 V
13 V
12 V

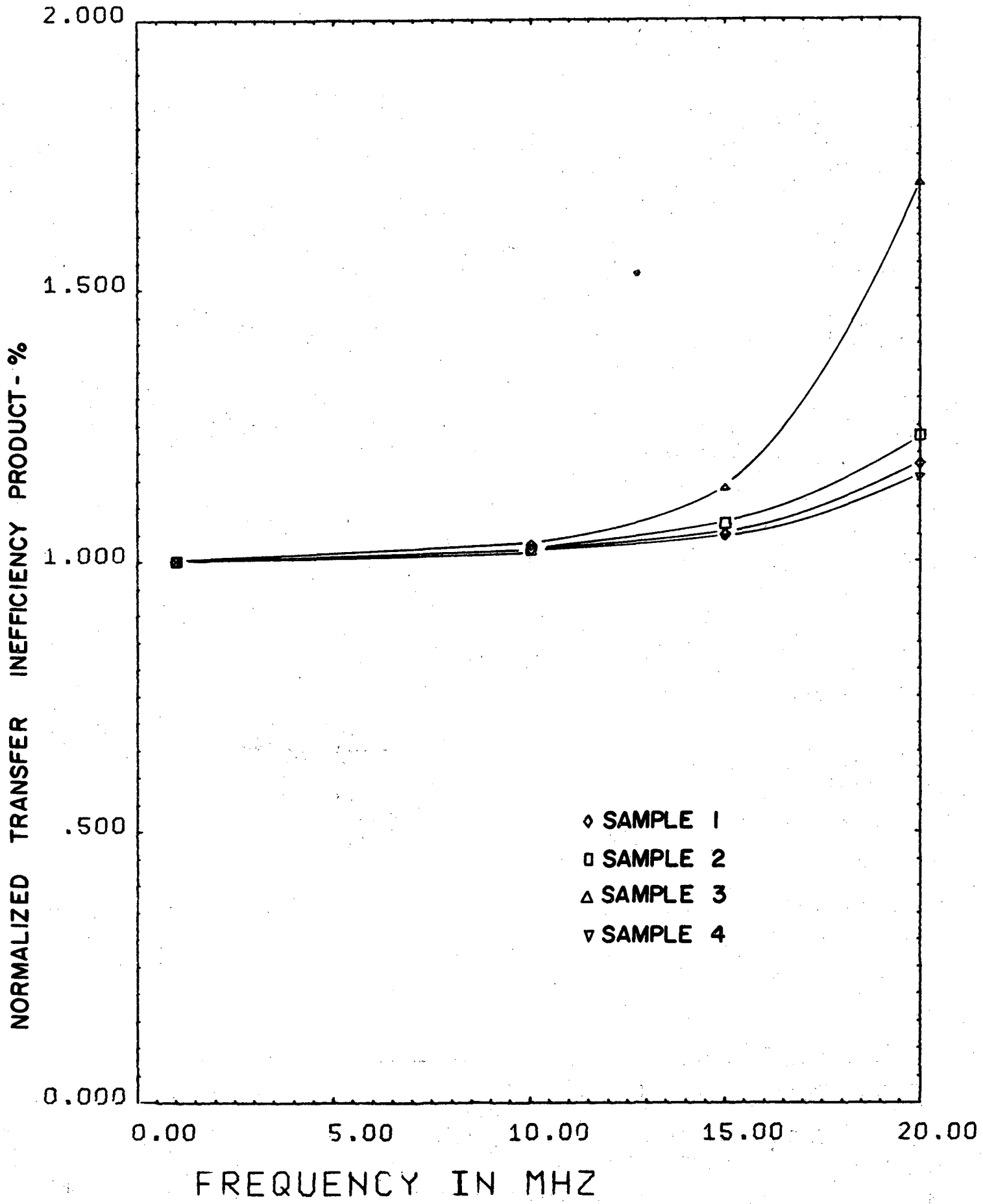

1400
1200
1000
800
600
400
200
0
OUTPUT IN MILLIVOLTS
0
200
400
600
800
1000
INPUT IN MILLIVOLTS
SAMPLE VR VI
1 9 V 8.15 V
2 9 V 8 V
3 9 V 8 V
4 9 V 8.4 V

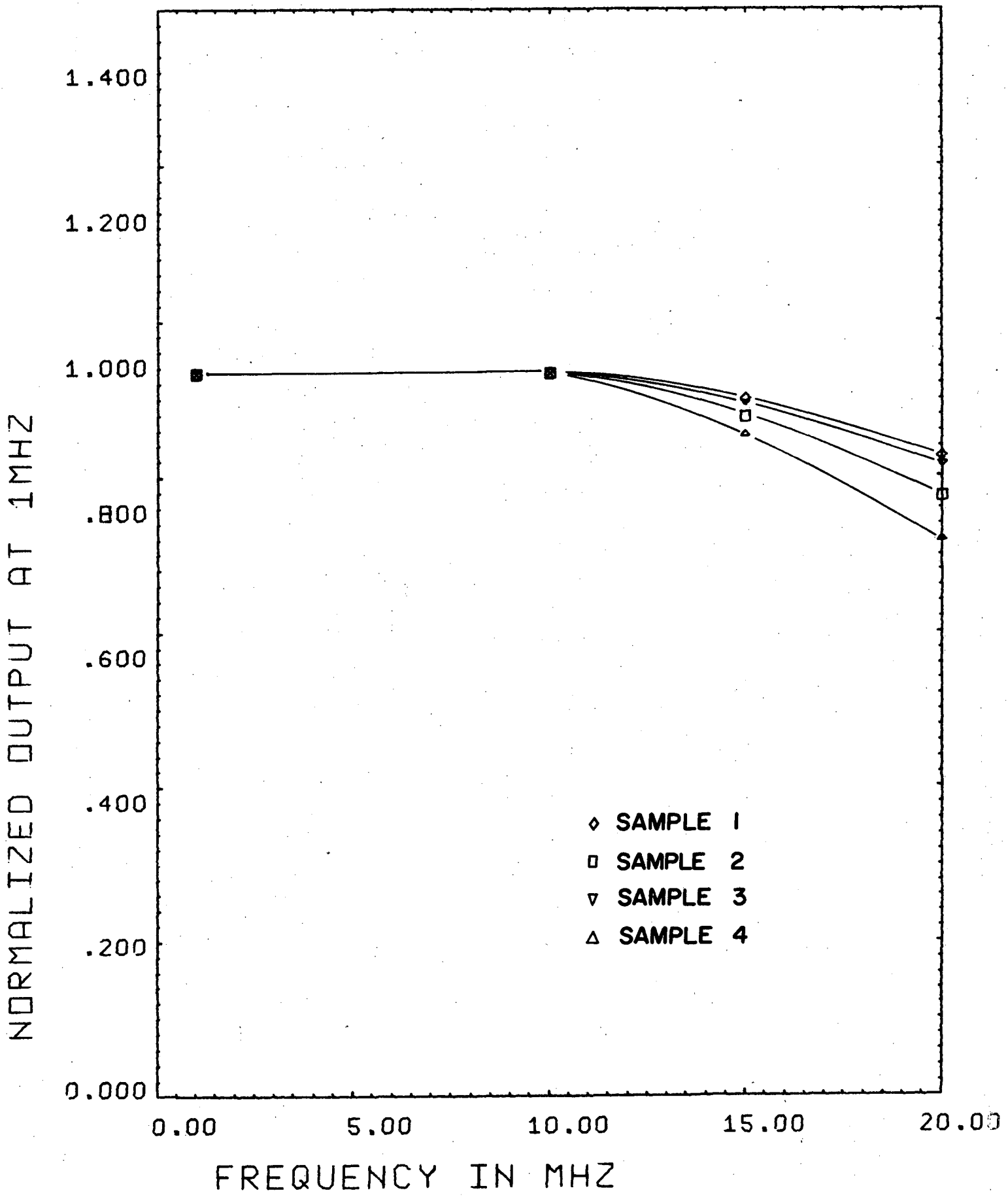

1400
1200
1000
800
600
400
200
0
0
200
400
600
800
1000
INPUT IN MILLIVOLTS
VR
VI
9V
8V
9V
8.25V
9V
8.50V
9V
8.75V

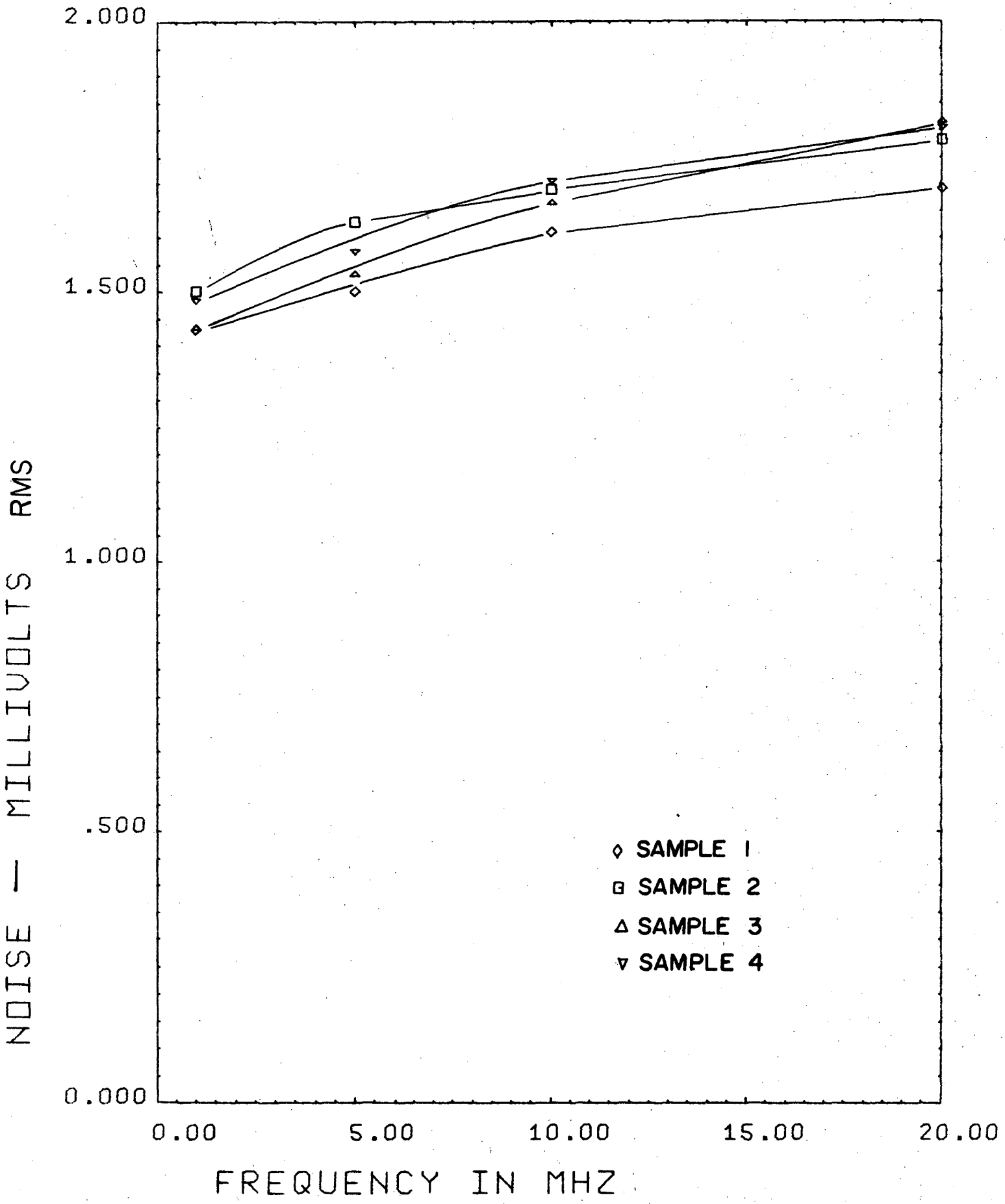



20.00
15.00
10.00
5.00
0.00
TRANSFER INEFFICENCY PRODUCT AND EXPERIMENTAL ERROR - %
0
500
1000
1500
OUTPUT IN MILLIVOLTS
$\frac{\Delta V_1}{V_{OUT}}$
$\frac{\Delta V_1 + \Delta V_2}{V_{OUT}}$
$\frac{\Delta V_1 + \Delta V_2 + \Delta V_3}{V_{OUT}}$




2.000
1.500
1.000
.500
0.000
NORMALIZED TRANSFER INEFFICIENCY PRODUCT - %
0.00
5.00
10.00
15.00
20.00
FREQUENCY IN MHZ
◇ SAMPLE 1
□ SAMPLE 2
△ SAMPLE 3
▽ SAMPLE 4


1.400
1.200
1.000
.800
.600
.400
.200
0.000
NORMALIZED OUTPUT AT 1MHZ
0.00
5.00
10.00
15.00
20.00
FREQUENCY IN MHZ
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4


2.000
1.500
1.000
.500
0.000
NOISE — MILLIVOLTS RMS
0.00
5.00
10.00
15.00
20.00
FREQUENCY IN MHZ
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4

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