CHARACTERIZATION OF DOUBLE-LAYER CAPACITORS FOR POWER ELECTRONICS APPLICATIONS

BY

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GRADUATE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

UNIVERSITY OF TORONTO

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ABSTRACT

A new kind of capacitor, with large capacitance and high energy density, has become available in the last few years. These high energy capacitors are based on the double-layer technology. They have higher power handling capability and energy density compared to electrolytic power capacitors.

So far, almost no research has been published with respect to the use of these capacitors; in addition, the information supplied by the manufacturer is not enough to establish an accurate model and to understand the operation of the capacitors.

This thesis deals with the selection, identification and verification of a simple and accurate model for the double-layer capacitors. The model is based on the terminal behavior of the double-layer capacitors; therefore, the identification is given by a specific and repetitive process based on electrical measurements.

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CHAPTER 1

INTRODUCTION

The fast, reliable and efficient storage and recovery of energy is an important requirement in many power electronics applications. The batteries, which have been the traditional storage devices, should not only be able to store large amounts of energy, but also to draw that energy at high rates. However, the fast advance in the electronic devices and systems has not been accompanied by the same rate of improvement in the batteries' performance. Further, the battery performance is the main obstacle in many designs and applications.

The development of a new kind of capacitor, with larger value of capacitance and higher energy density, may open a wide range of possible applications in the power electronics field, not only as an energy storage element, but also as a fast energy delivery device.

Several kinds of power capacitors with different construction technologies have been developed since 1989. Most of them are still in the laboratory research stage. The PANASONIC power capacitor is one of the first carbon-based double-layer capacitors available commercially, and several prototypes are available at the University of Toronto for experimental testing; therefore, this device will be the object of this research.

The PANASONIC capacitors are based on the electrical double-layer principle. They are available in two ratings; 470 F and 1500 F. The double-layer capacitors present several characteristics which are very attractive to the power electronics field; among them are high power, energy density more than ten times greater than that of the

electrolytic capacitors, low internal resistance and very high capacitance.

Modeling the double-layer capacitors with a single resistive capacitive circuit is insufficient to describe the device behavior. Furthermore, so far, almost no research regarding the use of the double-layer capacitors has been published, and the information supplied by the manufacturer is not enough to develop a more accurate model and to understand the operation of the capacitors. Moreover, the first experimental results have shown inconsistent results that suggest the study of those devices is not a simple task.

The general objective of this research is the characterization of the double-layer capacitors through the development of an equivalent model that should be based on the terminal behavior of the device. This objective includes the selection of an adequate model, the determination of a procedure for calculating the model parameters, and in general, the understanding of the double-layer capacitors terminal performance. The presence of extremely long transient phenomena inside the double-layer capacitors makes it very difficult to conduct repeatable experiments; therefore, the development of a standard procedure to secure the same known initial conditions in every experiment is required.

The characterization will be completed by studying the losses and energy inside the double-layer capacitor and the performance of the capacitors connected in series.

This research is the fundamental starting point for future research and one important reference for the utilization of the double-layer capacitors in power electronics applications.

In the next section, a brief description of the main research

goals is presented. The main objective of the thesis is explained in detail, and the contribution of this research is emphasized. In addition, other goals that complete the understanding of the double-layer capacitors are presented and described.

1.1 THESIS OBJECTIVES

1.1.1 *Modeling of Double-Layer Capacitors*

One of the ways to obtain a better understanding of the performance and characteristics of new systems or devices is to model the system under study. The use of simple and well-known elements to represent a more complex device enables any engineer or scientist to become familiar in a short time with the properties of the device. In addition, the equivalent model makes possible the use of conventional mathematical techniques and simulation tools to study the device and its applications.

Modeling the double-layer capacitors using a single resistance and a single capacitance is insufficient to represent adequately the electrical behavior of the devices. Figure 1.1 shows the comparison between the experimental and simulated results of the terminal voltage when a simple RC series circuit is used to model the DLC. In this experiment a constant current of thirty amperes was used to charge the DLC; then, one hundred seconds pass without current application, and finally, the capacitor was discharged using a constant current of thirty amperes.

The deviation between the simulation and experiment demonstrates the presence of a more complex response and internal transients and therefore the inadequacy of this elementary model.

The main general objective of this research is the development

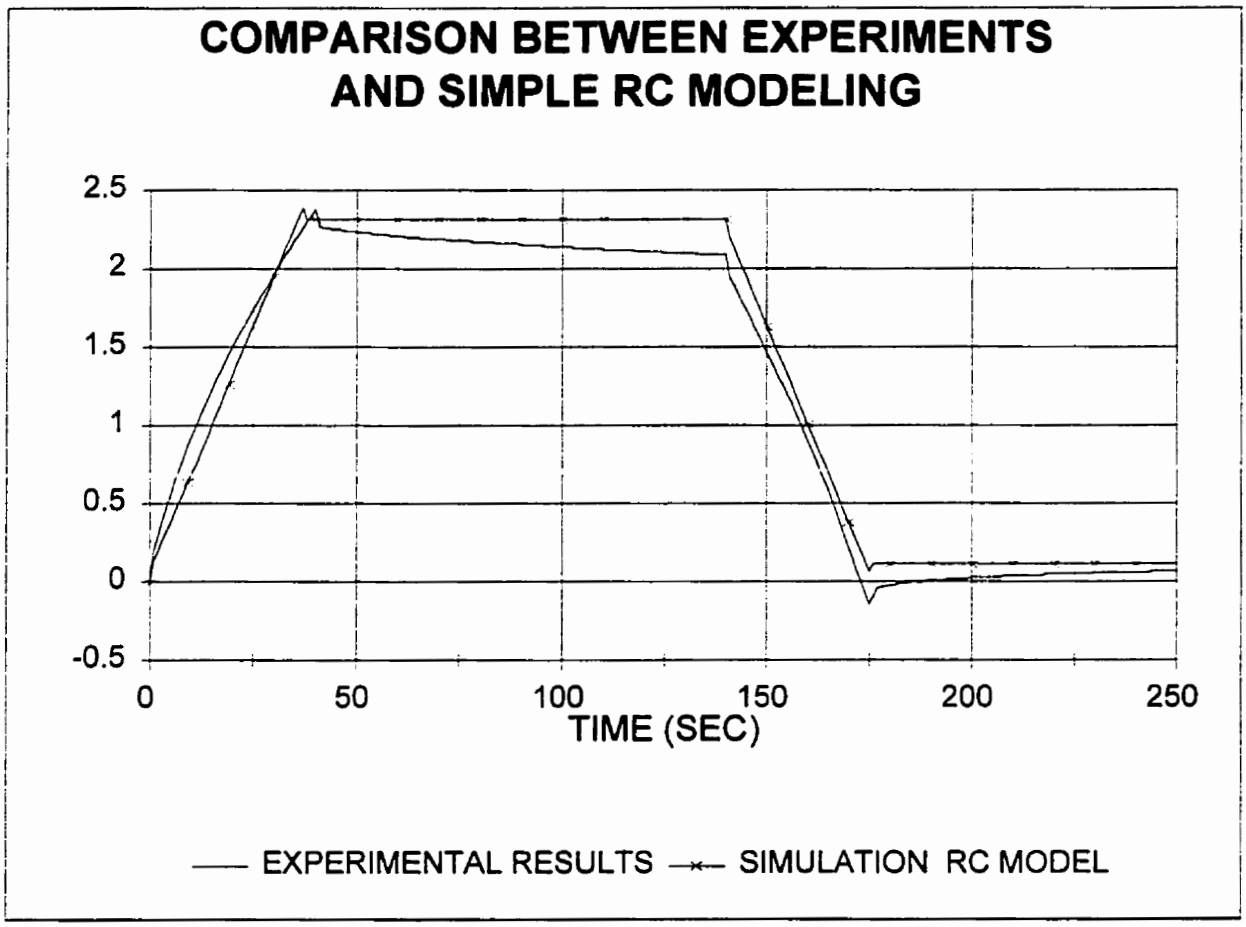


FIGURE 1.1 SIMPLE RC MODELING.

of an equivalent model for the DLC that should be based on two criteria: First, the model should be as simple as possible but describing the terminal behavior, over a time span of 30 minutes, accurately enough for design and application purposes. Second, the model parameters should be calculated based on the results of a series of measurements at the device terminals in a repeatable and clear procedure. Although there are equivalent models based on the physics of the double-layer, those models are not convenient for the design and analysis of double-layer capacitors applications in power electronics applications.

An equivalent model based on measurable electrical terminal parameters has several advantages:

First, the model parameters can be easily measured and verified several times using a simple experimental setup.

Second, because the fast advance of the technology makes almost certain the appearance of new improved devices, the proposed measurable model approach may be extended easily to future devices similar to those studied here.

Third, as the model uses typical electrical devices in its structure, that model is much easier to understand and analyze by engineers. Therefore, an accurate equivalent model provides the designer with the tools sufficient to integrate the DLC's in future designs.

Fourth, the availability of an equivalent model makes it possible to use simulation tools in order to anticipate the performance of the double-layer capacitors in specific applications, thus saving time and money.

1.1.2 *Energy Considerations*

The general utilization of the double-layer capacitors in commercial applications depends on the adequate utilization of the energy by the devices. In this direction, a study of the energetic needs, losses, and efficiency is fundamental in order to complete the characterization.

The study includes the calculation of the losses in the double-layer capacitor when it is subject to charge and discharge sequences. The energy study uses the proposed equivalent model and it is performed using simulation tools.

In addition, a study of the efficiency of the capacitor, based on the amount of energy that can be taken out of the capacitor with respect to the energy stored previously, is presented. Because of the long time constant present in the DLC response, the definition of efficiency is not a simple relation, and it will be a function of the time, so that it is necessary to define a cycle of charge in time that is the base for the efficiency study. In fact, the study should be defined as an energy interchange study for power electronics applications more than a traditional efficiency analysis.

1.1.3 *Series Connection*

Because the rated voltage of the PANASONIC double-layer capacitors is only 2.3 V., the series connection study should be included as one necessary action in order to reach the voltage needed in most applications. In traditional capacitor banks, a resistance or another electronic device is placed externally in parallel with each capacitor in order to maintain a voltage balance among the capacitors. However, due to the DLC's high capacitance, which leads to long time

constants, and to the frequent current source applications in the power electronics field, the connection of external devices to balance the voltages in each capacitor is not useful.

Therefore, it is fundamental to study the performance of capacitors connected in series, giving special attention to the voltage drift when the capacitors are subject of several charge and discharge actions in sequence. The performance of the capacitors in the series test will show if it is necessary to design a more complicated system in order to balance the voltages and use the double-layer capacitors in series.

1.2 THESIS OUTLINE

After the brief introduction and the clear definition and justification of the thesis objectives presented in the first part of this chapter, it is necessary to define the structure of the following chapters.

Chapter two presents a review of the double-layer background and double-layer capacitor construction. Furthermore, some possible applications for the double-layer capacitors are presented.

Chapter three introduces the selected double-layer capacitor equivalent model. First, the theoretical concepts and practical observations on which the selection of the model was based are discussed. Then, the different sections and elements of the model are defined and justified.

Chapter four introduces the procedure proposed for the identification of the equivalent model parameters.

Chapter five deals with the measurement of the equivalent model parameters. First, the general features of the experimental setup are

presented. Second, the measurement techniques needed in order to get trustworthy and accurate results are defined; this section includes the introduction of the automated test programs and the necessary normalization procedure. Third, the measurement results are presented. Finally, a discussion of the results is offered.

Chapter six uses the equivalent model and simulation tools in order to compare the model performance with the experimental results for several different tests. The simulations use the program SAM4 developed at the University of Toronto.

Chapter seven is a study of the losses and energy interchange inside the capacitor. This study uses the simulation software PSPICE and the verified equivalent model.

Chapter eight presents the results of an experimental study on the DLC series connection. Voltage drift among the capacitors, total capacitance, and the performance in short and long tests are the main points considered under research.

Chapter nine concludes with the results of the thesis and gives an overview of possible future research in this field.

CHAPTER 2

BACKGROUND OF DOUBLE-LAYER CAPACITORS

The electric double-layer phenomenon, described initially by H. von Helmholtz in 1879, was the starting point that led, almost one century later, to the development of large energy density capacitors. The electric double-layer capacitor was developed initially by Boss in 1971; since then, this kind of capacitor has been studied and developed by several corporations reaching capacitance and energy density levels which open a wide range of possible applications in power electronics, not only as energy storage device, but mostly as a fast energy delivery element. Although the double-layer capacitors have lower energy density than batteries, they can release that energy at high power level because of their low internal resistance.

Electric double-layer capacitors can be cycled many times, can operate over a wide temperature range, and are expected to reduce their cost as the manufacturing technology improves. On the other hand, the engineering information available is not enough to encourage the massive use of these devices in applications.

Several different names have been given to the high energy density capacitors; among them are: Supercapacitors, Pseudo-capacitors, and Ultracapacitors. The more general name of double-layer capacitors (DLC's) will be used during this report with reference to the high energy density capacitors.

The initial point of interest is to obtain a good understanding of the technology upon which the DLC's are based. This aspect will be introduced in the next section.

2.1 ELECTRICAL DOUBLE-LAYER TECHNOLOGY

A double-layer charge distribution is formed when two different phases, solid/liquid in the DLC's case, are in contact, and charge separation occurs at the boundary. The formation of the double-layer can be explained in the following way: when two phases are brought into contact, ions, which are assumed to be positively charged, migrate from one phase, in which the escaping tendency is larger, to the other phase. Because of this ionic migration, one phase becomes positively charged and the other negatively charged producing a double-layer charge distribution structure [1].

The reason for this chemical process, in which ions migrate from one phase to the other, is the difference in the inner potential between the two phases. When the superficial contact is established, the inner potential difference produces a force which transfers the particles across the interface.

The double-layer charge distribution generates an electric field, and subsequently an interface's potential. That electric field will hinder further migration of the ions as it compensates for the inner potential difference between the phases. Therefore, after a certain number of ions have migrated, a state of equilibrium is reached.

The double-layer effect behaves like an electric capacitor in that it is capable of storing energy. If a comparison with a parallel plate capacitor is done, the charge is stored in the double-layer formed across the interface. However, in this case, the distance between the plates (phases) is very small producing a device with high specific capacitance [2].

When the electric charge distributes itself throughout one of the phases, as occurs in the liquid, the double-layer is called

"diffused". As the solid structure does not allow much of a charge distribution, the charge produced in the solid phase is a surface charge. The surface charge at the solid phase generate a dipole orientation which generates another effect called "bound" double-layer. This bound double-layer is extremely thin, probably one molecule thick, and can be said to form a molecular capacitor. In the bound double-layer the charges neither move nor separate from the surface [1]. The capacitances of the two kinds of double-layer mentioned can be assumed to be in series, and they will produce the capacitor effect used in the double-layer capacitors.

Figure 2.1 represents the double-layer effect resultant in the interface between a liquid and a solid.

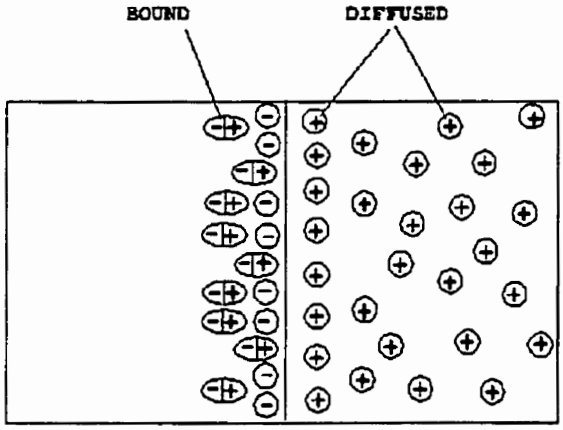


FIGURE 2.1 DOUBLE-LAYER FORMATION

If an external voltage is applied to the double-layer, the potential difference between the phases is increased or decreased depending on the sign of the applied voltage and the number of charges needed to establish the equilibrium is modified. The relation between the charge stored in the double-layer and the external voltage will

define the capacitance for the double-layer interface.

Figure 2.2 presents the potential curve at the interface including the effect that the external potential applied has on the charge stored at the double-layer. In the figure ϕs is the inner potential at the solid, ϕL is the inner potential at the liquid, X is the position and V is the external voltage applied. A positive external voltage increases the space charge at the interface. Also note in the right section of figure 2.2 the effect of the diffused double-layer that produces a curve in the potential characteristic.

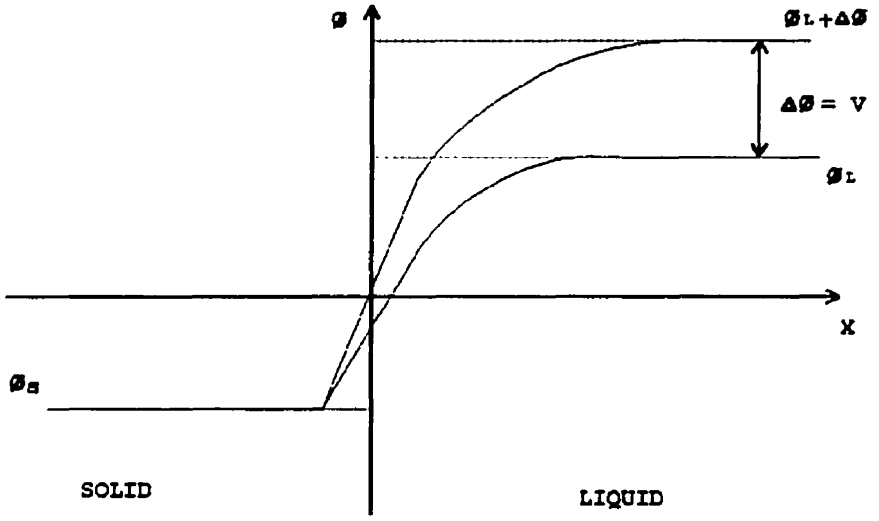


FIGURE 2.2 POTENTIAL OF THE DOUBLE-LAYER CHARGE DISTRIBUTION

Previous studies in interfacial electrochemistry reported that the interface can never be represented simply by a parallel plate capacitor [1],[2],[3]. The more complex representation of the double-layer capacitor is mainly due to the following factors: First, all double-layer capacitors can be self discharged by electrochemical reactions taking place across the interface. Second, the charge held by the capacitor is not a linear function of the potential across it.

Third, the double-layer capacitance was found to depend not only on the composition of the solution but also on the concentration of the electrolyte in a given system [2].

The second factor introduced in the previous paragraph establishes that the total charge stored in the two layers is not linearly related to the potential difference between the layers; therefore, the capacitance of the double-layer is not a constant but depends on the potential difference.

The capacitance is generally defined as the ratio between the charge and the voltage. Because of the non-constant capacitance in the double-layer distribution, the previous definition is insufficient to represent appropriately the double-layer capacitance; therefore, a more adequate definition is used:

The differential capacitance (C_{diff}) is defined as the derivative of the charge with respect to the potential difference between the phases:

$$C_{diff} = \frac{dQ}{dE} \quad (2.1)$$

The double-layer charge distribution is physically studied through the so called interfacial tension. The interfacial tension is developed at the contact surface between phases and it is given by the force per unit of length at the interface; this quantity is also a function of the potential difference. Based on the interfacial tension definition, the curve of interfacial tension vs potential difference has been measured using different solutes and electrolytes in the formation of the double-layer [1],[2],[4]. This curve is called the electrocapillarity curve and the results have been concordant with the fact that the capillarity curve can be modelled,

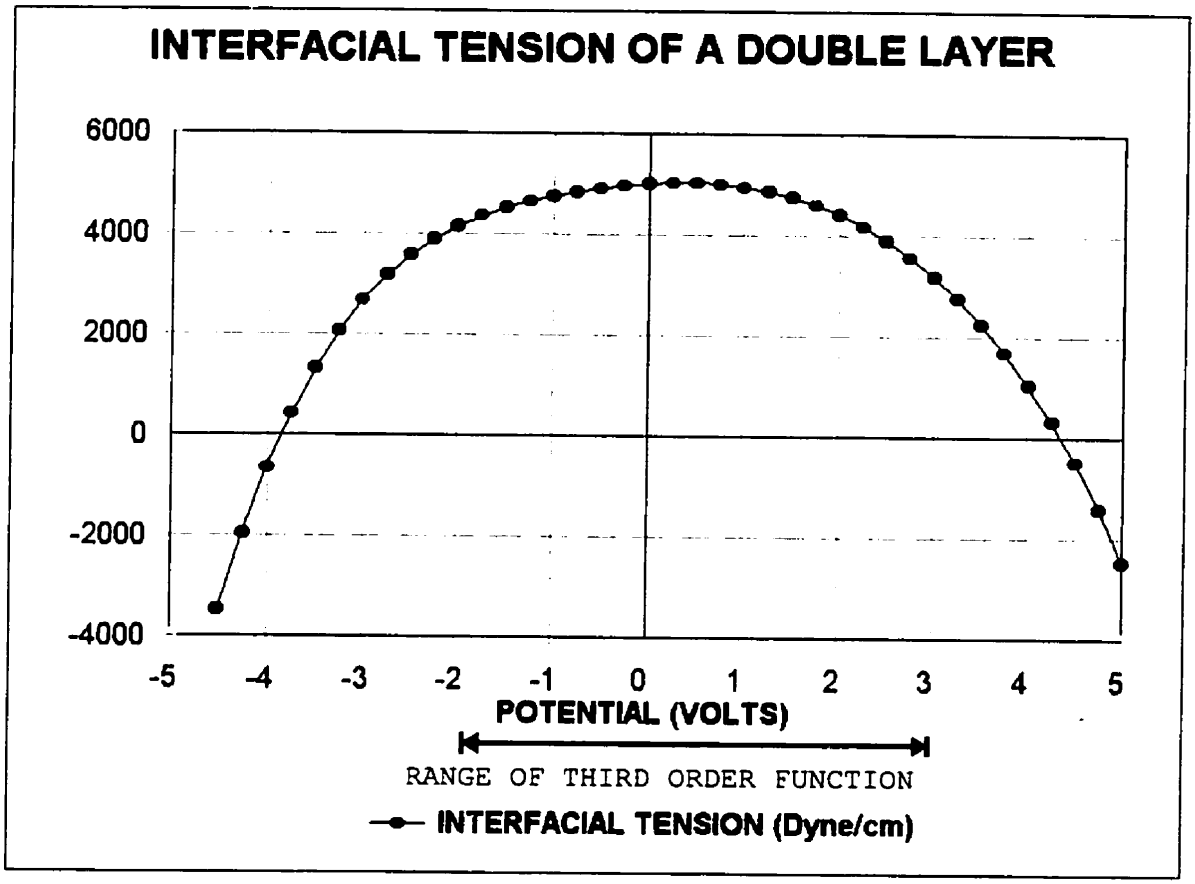


FIGURE 2.3 TYPICAL ELECTROCAPILLARITY CURVE.

at least for potential differences close to zero volts, as a third order function. Using different non ionic solutes, the location of the curve may be affected but not its general shape.

Figure 2.3 represents the general form of the capillarity curve and the approximate range of voltage used in the double-layer capacitors.

Based on the capillarity curve, the so-called capillarity equation is developed. In the capillarity equation, the interfacial tension (γ) is related to the electric potential difference across the phases (E) and to the surface charge (σ).

A number of more or less equivalent derivations of the electrocapillarity equation have been given [2]. One of the simplest is the Lippmann derivation which is based on the supposition that the interface is analogous to a parallel plate condenser, so that the reversible work dG, associated with changes in area and in charge, is given by:

$$dG = \gamma dA + \Delta\phi dq \quad (2.2)$$

where q is the total charge and $\Delta\phi$ is the difference in potential. The second term on the right gives the work needed to increase the charge in a condenser. Integration of the last equation keeping γ and $\Delta\phi$ constants gives:

$$G = \gamma A + \Delta\phi q \quad (2.3)$$

The last equation may now be redifferentiated with respect to different variables (γ and $\Delta\phi$):

$$0 = A d\gamma + q d(\Delta\phi) \quad (2.4)$$

It should be noted that E in the electrocapillarity equation

refers to the externally measured potential difference, while $\Delta\phi$ in the deduced equation is the difference in potential between the two phases in question. These two quantities are not the same, but generally they differ by some constant involving the nature of the electrodes and other junctions in the system; so that changes in both are equal, and dE may be substituted for $d(\Delta\phi)$. Substituting $d(\Delta\phi)$ and using the charge density (σ = q/A) instead of the total charge (q), the last equation represents the electrocapillarity equation:

$$\left(\frac{d\gamma}{dE}\right)_{\mu} = -\sigma \quad (2.5)$$

where the parameter μ is the called electrochemical potential which depends on the solution composition, and it is constant for the same capacitor materials.

A more detailed study of the electrocapillarity equation is presented by Adamson [4].

Using the defined differential capacitance presented in equation 2.1 and the capillarity equation (2.5), the capacitance of the double-layer is related to the interfacial tension through the following equation:

$$C_{diff} = \left(\frac{dQ}{dE}\right) = K\frac{d}{dE}\left(\frac{d\gamma}{dE}\right) \quad (2.6)$$

As the capillarity curve can be represented by a third order equation in the region close to zero volts, the differential capacitance expected in this region results in a linear function of the potential difference after the double differentiation indicated in equation 2.6. Figure 2.4 presents the double-layer charge and double-layer capacitance calculated from figure 2.3. The region of interest for the double-layer capacitors is again indicated.

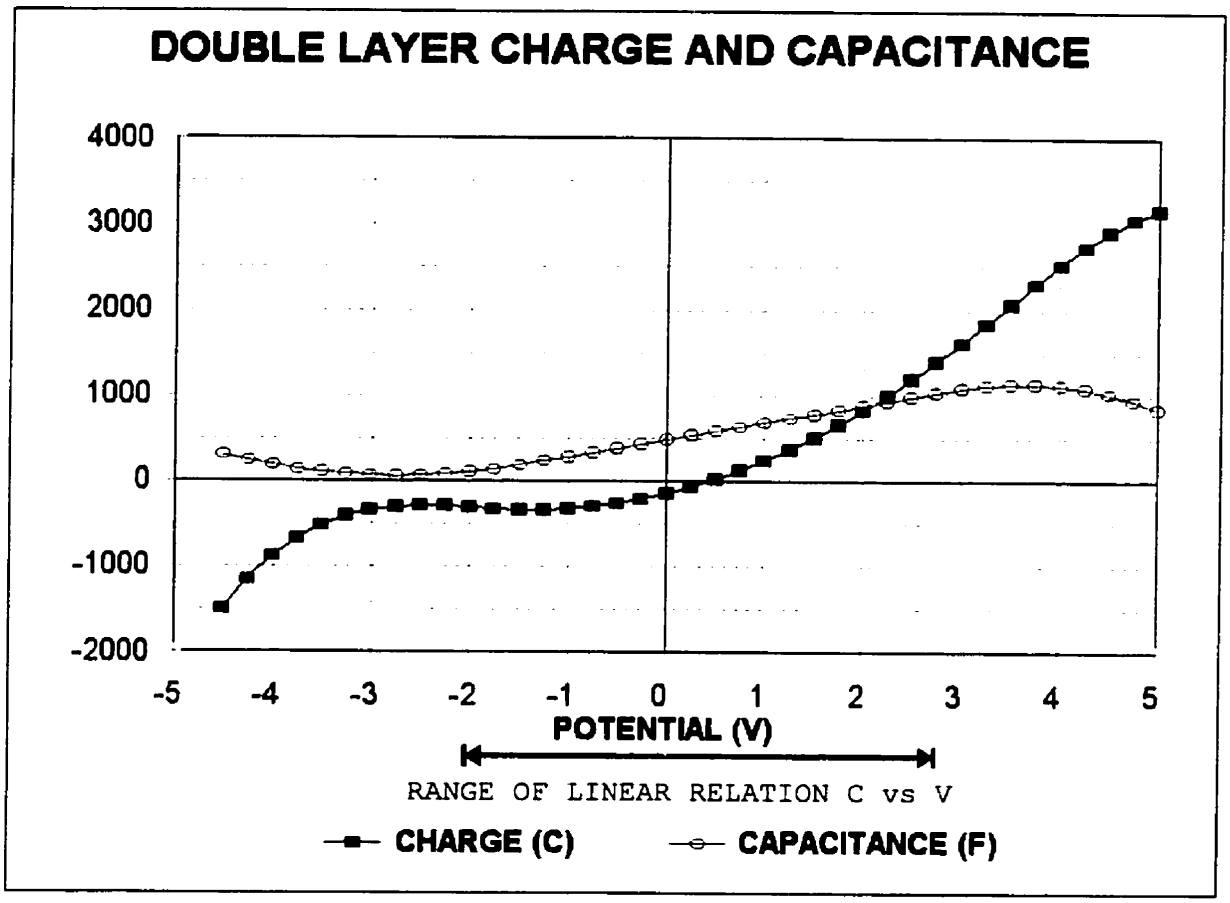


FIGURE 2.4 TYPICAL DOUBLE-LAYER CHARGE AND CAPACITANCE CURVE.

2.2 DOUBLE-LAYER CAPACITORS DEVELOPMENT

The first group of double-layer capacitors, developed in the eighties, was mostly the result of the increasing demand for miniaturization of devices used in the backup of memories and microcomputers. In general, they had capacitance values lower than 1 F, and very small dimensions as was dictated by the desired application [5].

Since then, several studies have been carried out to improve the capacitor characteristics by modifying the material of the polarizable electrodes, pore size distribution, packaging, and electrolyte material. In the early nineties, the development of a very high capacitance and low DC resistance capacitor was reported [6]. That capacitor, with greater dimensions, suitable for charging and discharging at high current levels, and with higher energy density, was the base in which PANASONIC developed and commercialized a double-layer capacitor which is rated 2.3 volts and 470 F. or 1500 F. These PANASONIC devices are the objects of study in this research.

Recently, other large capacitance devices with values up to 1000 F. and 5.5 volts using several cells in series have been reported [7]. Those devices, not available commercially, show the fast improvement in the characteristics of the double-layer capacitors, and give a good perspective into the future use of these devices in power applications.

2.3 DOUBLE-LAYER CAPACITOR CONSTRUCTION

The basic general structure of the double-layer capacitor consists of a pair of polarizable electrodes. The electrodes are

formed by solid colloids suspended in an electrolytic solution, a separator between the electrodes, two collector electrodes as solid contacts, and a pair of leads used to charge and discharge the capacitor [6],[8].

Figure 2.5 shows the basic structure of a double-layer cell.

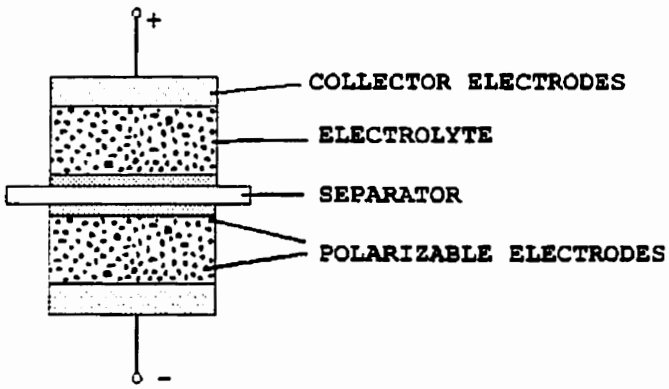


FIGURE 2.5 STRUCTURE OF THE ELECTRIC DOUBLE-LAYER CELL

The PANASONIC double-layer capacitor employs aluminum coils as collector electrodes, activated carbons as polarizable electrodes, binding material in the aluminum foils, and polypropylene separators. A mixture of activated carbons with particle size of 10μm, the organic binder and the solvent were coated on an aluminum foil. After removal of the solvent, a pair of aluminum foils with activated carbon layers were wound in spiral with polypropylene separators. The electrode wounds were immersed in an electrolytic solution, and then, the final compound was assembled in an aluminum case to form the capacitor [6].

The electrolytic solution is a mixture of tetraethyl-ammonium, tetrafluoroborate and propylene carbonate. Aluminum rods were used as connection terminals in order to support high current and obtain low resistance [6].

The reason for using activated carbons as polarizable electrodes

is the high specific surface area and high chemical stability of the carbon particles. As was explained, the capacitor effect is produced by the interface between two different phases, so that the surface of the carbon particles gives the possibility of obtaining greater value of capacitance per volume unit. In addition, the activated carbon electrodes have features of low sheet resistance and high density of carbon particles, which help to improve the characteristics of the device.

Figure 2.6 represents the structure and dimensions in centimetres of the PANASONIC 470 F double-layer capacitor.

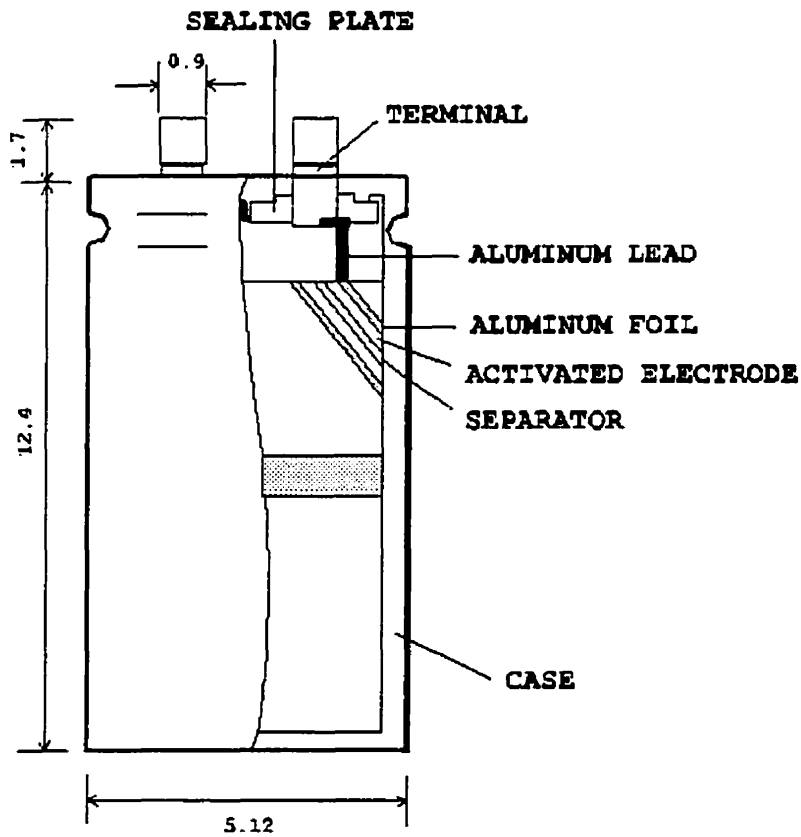


FIGURE 2.6 CONSTRUCTION OF THE PANASONIC DOUBLE-LAYER CAPACITOR

Among the main features of the 470 F. capacitor given by the manufacturer are the following:

- High values of capacitance.
- Small temperature dependence of the capacitance value.
- Small internal resistance of the device.
- High energy density.
- Large values of current are supported by the device.

Table 2.1 shows quantitative and structural characteristics of the 470 F device given by the manufacturer.

RATED VOLTAGE	2.3 V
RATED CAPACITANCE	470 F
DIAMETER	5.12 cm
LENGTH	12.4 cm
VOLUME	255 cm^3
WEIGHT	330 gm
ENERGY DENSITY	1.05 Wh/kg or 1.35 Wh/l
ENERGY STORED	1241 W.sec
TECHNOLOGY	SINGLE SPIRAL CELL
MATERIALS	CARBON BASED, NON AQUEOUS ELECTROLYTE

TABLE 2.1

The data sheet given by the manufacturer in reference to the double-layer capacitors that are the objects of this research is presented in Appendix A.

2.4 COMPARISON BETWEEN DOUBLE-LAYER AND ELECTROLYTIC POWER CAPACITORS

The innovation that the double-layer capacitors may represent in the electronics field may be visualized in a better way if their rated characteristics are compared with a classical electrolytic capacitor used in many power electronics applications. Table 2.2 compare the manufacturer information of the 1500 F double-layer capacitor with an electrolytic power capacitor of similar physical dimensions.

PARAMETER	D-L CAPACITOR	ELECTROLYTIC CAP.
RATED VOLTAGE	2.3 V	350 V
CAPACITANCE	1500 F	4800 μF
VOLUME	610 cm^3	885 cm^3
WEIGHT	800 gm	1000 gm
ENERGY DENSITY	1.39 Wh/kg	0.081 Wh/kg
ENERGY STORED	4000 W.sec	294 W.sec

TABLE 2.2

The table 2.1 shows the notorious advantages of the DLC's in energy stored, device weight, volume and mainly in energy density.

It should be especially noted that the energy density of the DLC's is seventeen times higher than that of the electrolytic capacitor. In addition, an increase in the energy density of the double-layer capacitors by a factor of at least two is expected in the near future [9].

The only rating in which the electrolytic capacitor surpasses the double-layer capacitor is in the rated voltage. No appreciable improvements in the double-layer capacitor rated voltage are expected. That is because the use of higher voltage in this kind of device would produce irreversible chemical reactions, in particular the dissociation of the electrolyte solution.

The last condition makes it necessary to study in detail the double-layer capacitors connected in series. The connection of several double-layer capacitor cells in series inside the same case has already been reported [7].

2.5 DOUBLE-LAYER CAPACITORS APPLICATIONS

There is a large spectrum of possible applications for the DLC's. Most of them depend on the increase in the knowledge about the characteristics and performance of the devices. In the next pages, some of the potential applications that in the short term are of interest are presented.

2.5.1 *Electric and Hybrid Vehicle Applications*

The average power that must be supplied by the battery in an all electric vehicle is relatively low depending on the driving mode and grade[9]. However, the peak power pulses during some periods are much higher due to the sudden acceleration and passing actions. Some studies have shown that the ratio between the peak power and the average power could be 16:1 or more [9]. If only a battery is used to supply the instant energy to the vehicle, the battery should be rated for the peak values increasing its weight, size, and cost.

The use of double-layer capacitors gives the possibility of

decoupling the peak power requirements from the average power. In this direction, the DLC's would meet the peak power requirements and the battery would supply the average power. Figure 2.7 shows the possible use of DLC's in an electric vehicle.

In addition, a study for the use of double-layer capacitors as energy source in hybrid vehicles instead of a battery has been reported [10]. In this study, the ratings with regard to the energy content and capacity needed to use the DLC's in hybrid vehicles are determined.

The main improvement needed to fulfill the requirements for this application is the increase in the energy density of the capacitor, up to at least 5 Wh/kg, in order to limit the space occupied by the double-layer capacitors [9],[10].

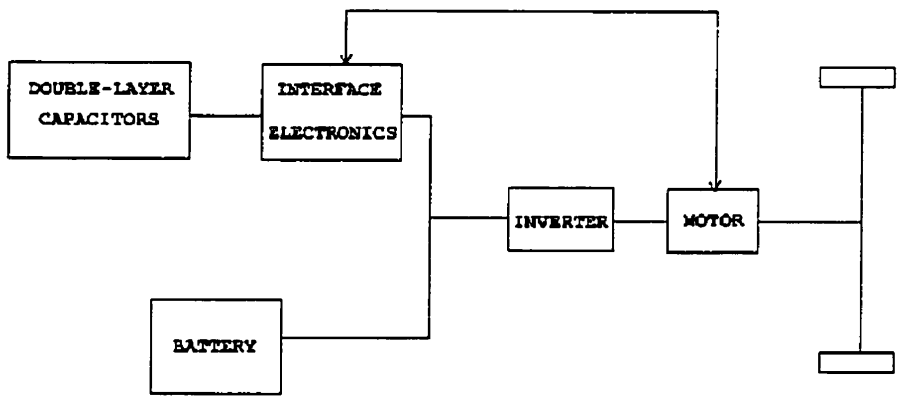


FIGURE 2.6 ELECTRIC VEHICLE APPLICATION

2.5.2 *Electrically Heated Catalyst*

A catalyst can be used in order to reduce the emissions from traditional vehicles. It has been reported that much higher levels of emission occur during the engine start and in the early stages; that

is, when the system is still cold [9].

Using the energy stored in the DLC's, the catalyst could be heated up just prior to or during the engine start. The levels of power required to heat the catalyst are high but the amount of energy is relatively small, therefore, this appears to be a potential example for the use of double-layer capacitors.

2.5.3 *Vehicle Accessories*

Some automotive accessories, such as power steering and power brakes, require intermittent high power levels for their operation. Currently, these accessories utilize a hydraulically actuated or a vacuum actuated drive and accumulators for the energy supply. Double-layer capacitors would be adequate to supply the peak power and reduce the stress on the battery during periods of great demand.

2.5.4 *Uninterruptible Power Supplies*

The objective of an electric supply is to provide a wide range and variety of customers with electrical energy. In practice, it is totally impossible to safeguard the electricity supply network against sporadic system failures.

However, there are many systems with critical loads which should have permanent power in order to protect the equipment involved. In addition, the presence of sensitive loads, typically computers, which may be seriously affected by relatively small disturbances, makes it necessary to maintain the quality of the power supply during disturbances[11].

Therefore, it is necessary not only to provide standby power in the event of supply failure, but also to make certain that the

electrical input is pure, clean, and continuous.

Uninterruptible power supplies are designed and implemented in order to fulfill the previous conditions. They usually use a source of stored energy such as a battery which will give the energy during the main power failure.

Many of the power interruptions or disturbances only last a few seconds; in those cases, the energy required is relatively small but the power requirements may be high and that increases the size and cost of the battery.

The DLC's may be an adequate and reliable source of energy for these short backup power needs. They should reduce the size, increase the efficiency, and eventually reduce the cost of the UPS system.

2.5.5 *Other Applications*

There are unlimited possible applications for the double-layer capacitors: in medical equipment, in some military applications, in soldering equipment, in industrial electrical drives, as a memory backup for computers and other digital equipment, etc.

Not all of the applications mentioned earlier require and are adequate for the 470 F. PANASONIC capacitor. Some of them require lower levels of energy and capacitance but also make possible the use of smaller device sizes. In this direction, several other double-layer capacitors with different ratings and sizes are being developed by several corporations around the world [5],[8],[12].

CHAPTER 3

EQUIVALENT MODEL PROPOSAL

This chapter deals with the selection of an equivalent model which satisfies the general objectives of the thesis; that is, based on the double-layer capacitor terminal behavior and composed of general electrical components such as resistors, capacitors and inductors.

The selection of the equivalent model is based on two criteria: physical reasons related to the double-layer and the DLC construction and practical considerations resulting from the terminal model objective. The physical arguments are introduced in the following section.

3.1 PHYSICAL FACTS LEADING TO THE MODEL

3.1.1 *Time Behavior of the Double-Layer Capacitors*

Chapter one presented the fact that electrical charge is stored in the double-layer when external voltage is applied. The flow of charges across the interface is not an instantaneous process. It depends on the ion mobility, environmental conditions and several other factors. In addition, the cross of electrical charges is followed by a series of charge distribution processes, and dipole orientations which take a considerably long time.

Based on the last factor, the capacitance of the double-layer is physically represented by a model which consists of an infinite number of parallel branches each one composed of a resistor and a capacitor in series. The time constant of each branch is longer with respect to

the previous one producing a general device with a complicate internal behavior.

Figure 3.1 presents the general model for the double-layer capacitance.

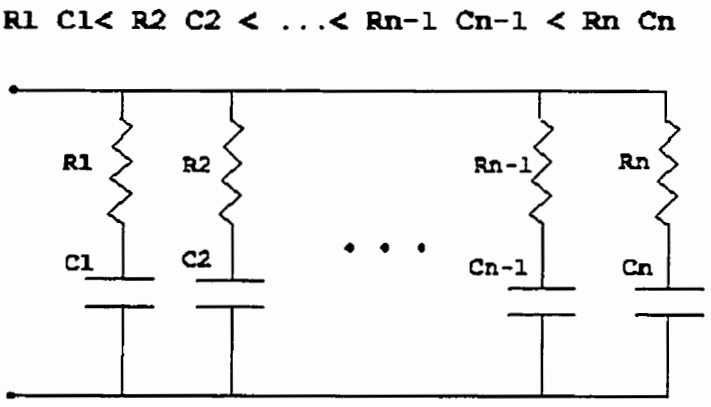


FIGURE 3.1 GENERAL DOUBLE-LAYER CAPACITANCE MODEL

This model as a representation of the double-layer has several factors favorable to the objective of this research:

- Use of simple electrical components to describe the double-layer (Resistors and Capacitors).
- Representation of the double-layer as a terminal device.

Unfortunately, this representation of the DLC is not adequate for the characterization due to the following reasons:

- The presence of an infinite number or even a very large number of branches makes the model too complex for practical use and excessive effort is necessary to represent the model mathematically.
- The parameter calculation of so many branches based on

current and voltage measurements is difficult, arbitrary and inaccurate. In addition, physical data for the parameters values of the above equivalent model is not available.

Based on the previous considerations, the selected model will use the RC structure of the model in figure 3.1 but with a finite number of branches. The number of branches should be the smallest number possible keeping a good level of accuracy when the capacitor performance is simulated.

3.1.2 *Dependence of the Capacitance on the Potential Difference*

In chapter one, the study of the physics of the double-layer showed that the capacitance of the double-layer is not a constant but depends on the potential difference. This has to be included in the equivalent model in order to get accurate results.

The conclusion reached in Chapter two after the physical study of the double-layer is that the differential capacitance is linearly dependent on the potential. Therefore, the capacitance of the DLC model will include a fixed capacitor Co in parallel with a variable capacitor (C_1) linearly dependant on the voltage.

$$C_{diff}(V) = Co + C_1 * V \quad (3.1)$$

Based on the differential capacitance, an integral capacitance C_K may be defined as the ratio between the total charge delivered to the capacitor to the voltage across the capacitor terminals.

$$C_K = \frac{Q_{tot}}{V_c} \quad (3.2)$$

Note that this definition uses the total charge referred to the zero voltage condition and it cannot be calculated from a different initial charge. The integral capacitance may be calculated from the differential capacitance in the following way:

$$C_K = \frac{1}{V}\int_0^V C_{diff}\, dV \quad (3.3)$$

In terms of Co and C_1 the integral capacitance can be expressed as:

$$C_K = Co + \frac{C_1}{2} V \quad (3.4)$$

Although the integral capacitance appears to be the definition used in the specification of the capacitor value for the PANASONIC double-layer capacitor, the differential capacitance (C_{diff}) of the DLC will be the definition used in the modeling of the double-layer capacitors. That is because the differential capacitance defines the "instantaneous" capacitance of the DLC during any charge action independently of the previous charge cycles applied.

3.1.3 *Double-Layer Leakage*

Another characteristic of the double-layer mentioned in chapter one is the self discharge process present in the capacitor as a result of electrochemical reactions occurring across the interface when charge separation is present. This self-discharge or leakage means that part of the charge stored in the double-layer is lost internally and may not be recovered.

The leakage effect is represented in the equivalent model by a resistance in parallel with the resistance-capacitance branches already mentioned in the previous two sections. This resistance from now will be called R_{lea}.

3.1.4 *Inductive Effect in the Capacitor*

Although specific details of the DLC construction are not available, the general construction process explained in chapter one mentioned that the aluminum foils are wound in spiral. Thus, it is possible to have some inductance inside the device which may affect the slew rate performance of the device. Therefore, a series inductance is included in the equivalent model.

Based on the previous physical reasoning, the general structure of the equivalent model as shown in figure 3.2 is now proposed. Further properties of the proposed model are based on extensive experimentation and the conclusions of this experimentation will be presented in the next section.

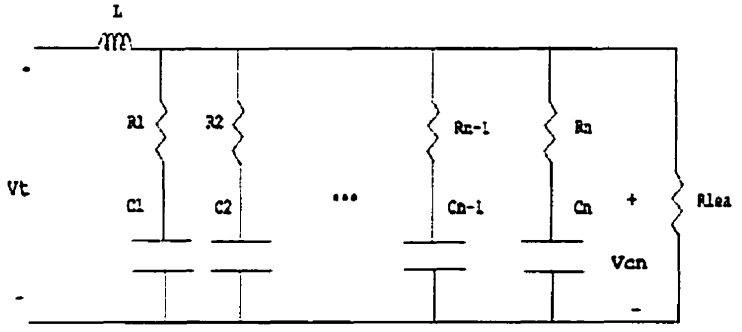


FIGURE 3.2 PROPOSED MODEL STRUCTURE

3.2 PRACTICAL CONSIDERATIONS

With the general structure of the equivalent model selected, the question about the number of branches needed to represent accurately the double-layer capacitor should be answered. For a practical model, the number of branches should be limited to the smallest number possible. The use of three branches to represent the DLC behavior is proposed.

Extensive experimental observations have influenced the selection of the number of branches of the equivalent model and in the model structure; these observations are commented on next:

1) Charging a fully discharged capacitor (all the equivalent internal capacitances with zero voltage) with controlled constant current up to the rated voltage and measuring the time required to this charge allow to calculate an integral capacitance of the device. The integral capacitance measured hardly changes if currents in the ratio of 1 to 10 are used for charging. This result indicates that the fastest branch may be assumed to have a very short time constant compared to further branches. The selection of a much bigger time constant for one branch in respect to the previous one makes the identification and calculation of the parameters simpler.

2) Although the internal time behavior of the double-layer capacitor may include processes with time constants of hours, the interest in power electronics is restricted to relatively short time or high power applications; so that the model selected should follow with greater accuracy the capacitor response thirty minutes after the start of a charge or discharge process.

3) The physical model composed by an infinite number of branches with different time constants gives a clear impression that reactions

with time constants between a few seconds and several hours occur inside the device. Observing the terminal voltage after a charge cycle confirms the previous impression and indicates that the charge is redistributed among the different branches. This distribution over the time of interest (30 minutes) should be represented in the model by the response of additional branches. One branch is insufficient to match the capacitor behavior in this wide time span; therefore, two branches with different time constant are proposed to represent the internal charge distribution. The second branch has a time constant in the order of few minutes and the third branch has a time constant in the order of tens of minutes.

4) The selection of the three voltage dependant branches increases the complexity of the parameter identification. In addition, extensive measurements of the internal charge distribution process at different voltages indicate that the assumption of only one branch voltage dependant does not introduces an appreciable error if the capacitor voltage is kept over 1.5 volts. As in the power applications the DLC's will not be discharged to very low voltages the dependence of the capacitance with the voltage is assigned to the first branch only.

Based on the previous physical and experimental observations, the proposed model consists of three branches in parallel each one composed of the connection in series of a resistor and a capacitor. In addition, the model includes a leakage resistor in parallel with the three branches and a series inductor in the input. The capacitance of the first branch is divided in a fixed part and a voltage dependant part.

The first branch has the smallest time constant. The time constant will be given by the capacitor response to a fast charge process, in other words a charge action with high current. Using the rated values given by the manufacturer, the time constant expected for this branch is in the order of few seconds. From this point the first branch and its components (R and C) will be named "immediate" and denoted with the letter 'i'. The name "immediate" is given because this branch will respond immediately to the charge action.

The second branch has a medium time constant. The time constant selected for this branch is between one and five minutes. That means that the time constant for the second branch is at least ten times larger than the time constant for the immediate branch. From this point the second branch will be named "delayed" branch and its elements denoted with the letter 'd'.

The third branch will be named "long term" branch and denoted with the letter 'l'. This branch has a time constant of more than 10 minutes which makes it much slower than the delayed branch.

Figure 3.3 presents the detailed proposed model of the carbon-based double-layer capacitor.

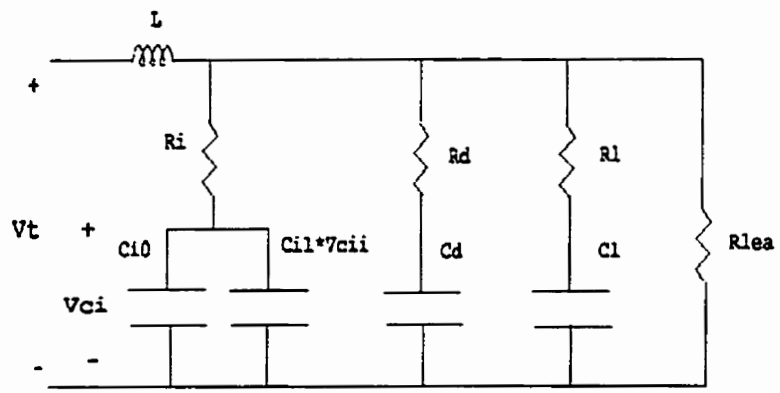


FIGURE 3.3 DETAILED PROPOSED MODEL

CHAPTER 4

IDENTIFICATION OF EQUIVALENT MODEL PARAMETERS

This chapter presents the principles on which the identification of the equivalent model parameters is based. With the principles clearly defined, the detailed parameter identification procedure is explained.

The measurement procedure is based on a test facility that consists of a controlled current source and a voltage measurement system. The test facility and the techniques used in the measurement of the parameters are presented in chapter five. However, it is convenient to indicate now that the current source has a very short maximum rise time compared with the typical charge times for the double-layer capacitors. Furthermore, the current source can be turned on or off at precise intervals in time, by mean of the controller board timing, or by the instant at which the double-layer capacitor terminals reach some pre-fixed value.

The identification of nine model parameters using only two measurable variables (terminal voltage and input current) has an infinite number of possible solutions, and therefore is in general arbitrary. However, based on the justified assumption of three branches with distinct time constants the principles of the parameter identification process are now proposed:

- The double-layer capacitor to be modeled should be in a fully discharged state; that is, all the equivalent internal capacitances have zero voltage. To achieve this state of full

discharge, a "normalization" process was developed and is presented in chapter five.

- The capacitances to be assigned to the equivalent model are given by the differential definition presented in chapter three. This definition gives the possibility to know the instantaneous capacitance of the device at any moment of any test sequence.

- The identification of the immediate branch equivalent model parameters is based on the charge of the capacitor up to the rated voltage with high current and the continuous measurement of the terminal voltage. The use of high current reduces the effect of the other two branches in the measurements.

- When the terminal voltage reaches the rated value, the current source is turned off and an internal charge distribution process among the different branches begins. Continuous voltage measurement during that charge distribution is used to identify the delayed and long term equivalent circuit parameters.

- The leakage resistance is identified using a capacitor whose voltage is equal across all the internal equivalent capacitances. In other words, no charge distribution process is occurring inside the device. Under this condition, the change in terminal voltage is only a result of the equivalent model leakage resistance.

- The DLC input inductance is calculated using the slope of the current transient at the instant that a fully charged capacitor is suddenly short-circuited.

In the above paragraphs only the general principles used in the identification were presented. A detailed description of the identification of each parameter is given in the following pages.

4.1 IDENTIFICATION OF IMMEDIATE BRANCH PARAMETERS

The immediate branch parameters are measured by applying a fast charge to the capacitor. The higher the value of current the lower the charge introduced into the delayed and long term branches; therefore, the current should be as high as possible; however, the devices available for the experimental facility are limited to fifty amperes. For these reasons, the current was selected as 5% of the rated short circuit current of the double-layer capacitor or 45 Amp. The rated short circuit current is defined as the ratio between the rated voltage and the rated internal resistance of the capacitor.

The resistance of the immediate branch is determined from the voltage drop produced at the terminals when the current is applied to the capacitor. The DLC terminal voltage is measured at the time t0 before the application of the current. At some time t1 after the turn on of the current source, the terminal voltage is measured again. The time t1 is equal to the maximum rise time of the current source, which is also greater than the di/dt of the device; at this time, the current has reached the desired value but the energy stored in the equivalent capacitance is very low. Therefore, the measured voltage step (ΔV) is due to the equivalent resistance of the immediate branch and the value of the resistance is calculated using equation 4.1. In equation 4.1, I is the controlled current applied, R_i is the immediate branch resistance and ΔV is the difference between the voltage measured at t1 and the voltage measured at t0:

$$R_i = \frac{\Delta V}{I} \quad (4.1)$$

The voltage measured at the time t1 is used as a starting point

for the capacitance calculation. The fixed part of the immediate capacitance (C_{i0}) is measured based on the defined differential capacitance at the start of the charge action according to the following equation:

$$C_{i0} = \frac{dQ}{dV}\Big|_{Vci=0} = \frac{I\,dt}{dV}\Big|_{Vci=0} = \frac{I}{dV/dt}\Big|_{Vci=0} \quad (4.2)$$

As the current magnitude is constant, the voltage drop across the immediate resistance is constant; therefore, the dv/dt of the terminal voltage curve as a function of the time is equal to the dv/dt of the voltage curve at the immediate branch capacitance. The slope of the terminal voltage versus time curve is measured at the first instants after the current has been established. This value is used in conjunction with the known value of the current and C_{i0} is determined.

The slope of the curve (dV/dt) is measured in the following form: The terminal voltage is measured continuously. When the terminal voltage has increased a value ΔV with respect to the voltage measured at t1, the time t2 is measured. The time change Δt corresponding to this ΔV is equal to t2-t1. In this form the dv/dt of the terminal voltage curve in time is measured and its value is used in equation 4.2. The size of the voltage step ΔV is selected to provide good resolution in the calculation.

The voltage dependant immediate capacitance (C_{i1}) may be calculated using the definition of differential capacitance or integral capacitance. As the integral capacitance definition does not need to measure the slope of the terminal voltage curve, this method is more accurate and will be implemented. The time t3 at which the capacitor reaches the rated value is measured. At this time the

equivalent integral capacitance of the immediate branch is given by the following relation:

$$C_K = \frac{Q_{tot}}{\Delta V} = \frac{I(t3-t1)}{V_{(t3)} - V_{(t1)}} \quad (4.3)$$

where t1 is the time at the start of the charge already mentioned in the calculations of Ri and C_{i0}, and $V_{(tn)}$ represents the terminal voltage at the time tn.

With the value of the integral capacitance calculated, equation 3.4 is used to relate the integral capacitance with the differential capacitance. Using equation 3.4 the value of C_{i1} is calculated:

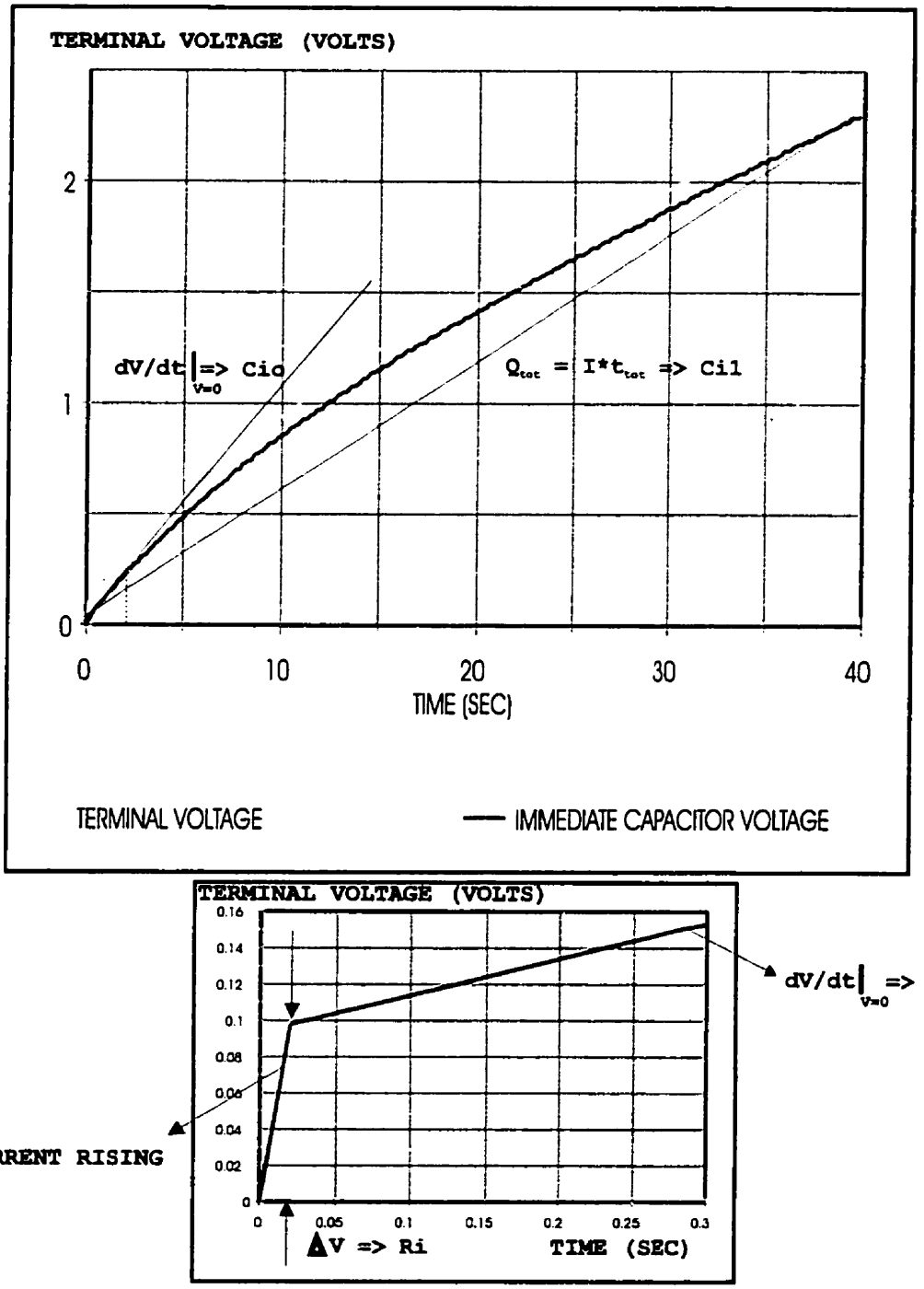
$$C_{i1} = \frac{2(C_K - C_{i0})}{V_{t3} - V_{t1}} \quad (4.4)$$

Figure 4.1 presents a typical curve of voltage vs time for a simple charge action with constant current. This figure summarizes the calculation of the immediate branch parameters.

4.2 IDENTIFICATION OF DELAYED BRANCH PARAMETERS

When the terminal voltage reaches the rated value, the current source is turned off and the redistribution of charge between the immediate and the delayed branch is the predominant action inside the capacitor. At this point the calculation of the delayed branch parameters begins.

The assumption made for the calculation is that the voltage at the delayed branch is zero volts when the current is removed; in other words, the time constant of the delayed branch is much higher than the



INITIAL INSTANTS SCALE ZOOM

FIGURE 4.1 IDENTIFICATION OF IMMEDIATE BRANCH PARAMETERS

charge time of the immediate branch.

The equivalent circuit in figure 4.2 represents the capacitor during that redistribution process

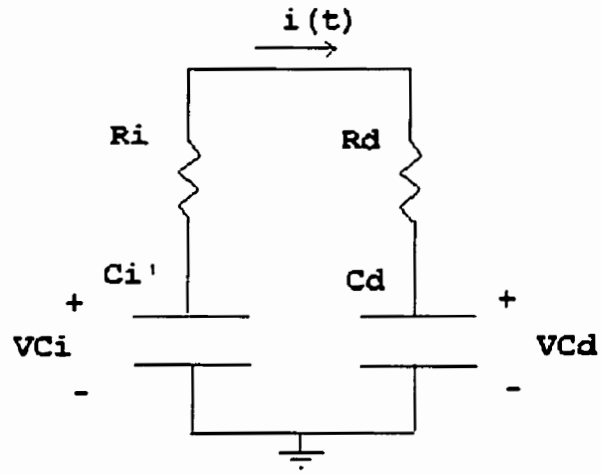


FIGURE 4.2 CHARGE REDISTRIBUTION EQUIVALENT CIRCUIT

In this figure, Ci' is the value of the immediate branch capacitance at the corresponding voltage, and Ri is the immediate branch resistance. The initial current flowing through the circuit when the current falls to zero and Vcd is zero (t4), is given by:

$$i_{(t4)} = \frac{Vci}{Ri+Rd} \quad (4.5)$$

In addition, the following relation between the capacitor current and its voltage is valid at this instant:

$$i_{(t4)} = C' \frac{dVci}{dt} \quad (4.6)$$

The time t4, accordingly to the current source characteristics, is equal to the time during which the current source was turned off plus the maximum fall time of the current. The terminal voltage at t4

is measured, and then the voltage is continuously measured until it has dropped a fixed value ΔV. This point determines the instant t5. With these two points of time and voltage the value of dV/dt = ΔV/Δt is determined.

Assuming Rd >> Ri, Vci is approximately equal to the terminal voltage. Therefore, measuring the terminal voltage and dVci/dt, Rd can be calculated through the following equation deduced from 4.5 and 4.6:

$$Rd = \frac{Vci}{C' * dVci/dt} \quad (4.7)$$

The value of Vci and C' used in the calculation of Rd is the terminal voltage and the immediate branch capacitance at the medium point of the dV/dt calculation. (See figure 4.3)

Using the same equivalent circuit shown in figure 4.2 at some instant (t6) where Vcd is different from zero, the value of Cd can be calculated. As the delayed branch was selected to represent the capacitor behavior up to five minutes after the charge action, the calculation of the delayed branch capacitance is done three minutes after the end of the charge action (t6 = 180 sec + t3).

At this instant the current flowing from the immediate to the delayed branch is given by:

$$i(t6) = C' \frac{dVci}{dt} \quad (4.8)$$

Furthermore, the total charge equilibrium equation that represents the interchange of charge between Ci and Cd is given by:

$$\Delta Q = Vci(t4) * C_K(t4) - Vci(t6) * C_K(t6) = Vd(t6) * Cd \quad (4.9)$$

The integral capacitance value, needed in the previous equation, may be easily calculated from the differential capacitance as

explained in chapter three. The value of Vcd at t=t6 is calculated from figure 4.2 as:

$$Vci(t6) = i(Rd+Ri) + Vcd(t6) \quad (4.10)$$

Using equations 4.8 to 4.10 the value of Cd is calculated:

$$Cd = \frac{\Delta Q}{Vci(t6) - C' * \frac{dVci}{dt}\Big|_{t6} * (Ri+Rd)} \quad (4.11)$$

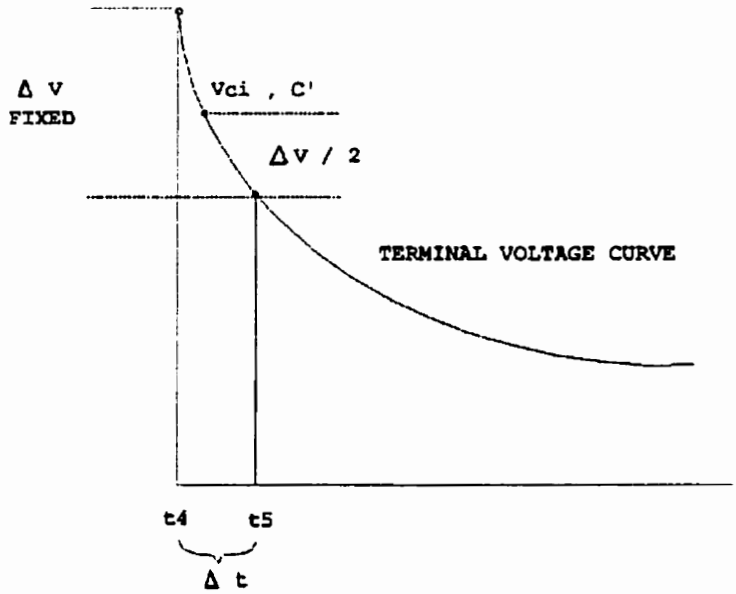


FIGURE 4.3 dV/dt CALCULATION

A second proposal for the delayed branch capacitance calculation based only in the charge equilibrium is now presented. In this second possible identification, the time constant for the delayed branch is previously assumed. After three time constants of the delayed branch, the voltages across the immediate and delayed branches are practically equal, and the equation 4.9 for the charge equilibrium is applied with Vcd = Vci. This procedure has the advantage to save the calculation of dv/dt which is in general inaccurate. On the other hand, this

second proposal needs more time for the computation of the parameter Cd because the calculation is done when the voltages in both branches are considered equal.

4.3 IDENTIFICATION OF LONG TERM BRANCH PARAMETERS

The long term branch parameters' calculation follows similar steps to those for the delayed branch. In this case, the delayed capacitance is assumed with equal voltage to the immediate branch and the long term capacitance is assumed fully discharged. To make these assumptions valid, the start time for the calculation of the long term branch should be at least three times the delayed branch time constant. This criterion assures that the delayed voltage is within 95% of the immediate branch voltage.

The equivalent circuit for the charge transfer to the long term branch is shown in figure 4.4.

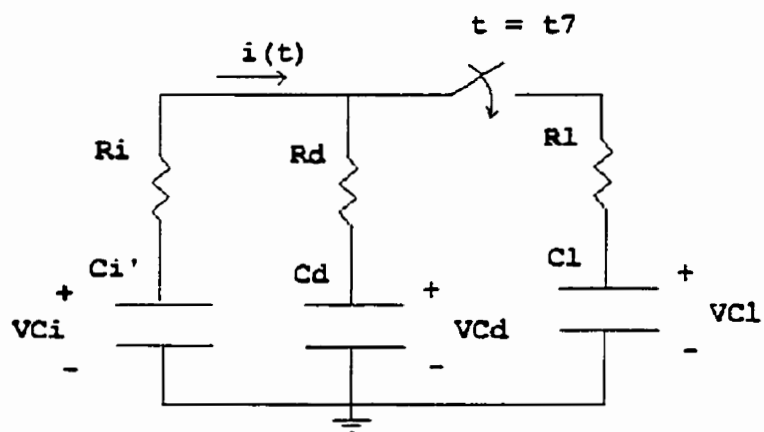


FIGURE 4.4 EQUIVALENT CIRCUIT FOR CHARGE DISTRIBUTION TO Cl

The switch S1 is closed at the instant t7 in which the voltages at the immediate and delayed branches are almost equal. In this instant most of the charge transference occurs between the immediate branch and the long term branch because the value of Ri is much lower than Rd. Therefore, Rl is calculated using equation 4.7 three delayed branch time constants after the instant at which the current was turned off. The calculation of the dV/dt used in equation 4.7 is done in the same form explained for the delayed branch.

The capacitance Cl is calculated using the same procedure explained for the delayed branch but now the capacitance C' in equations 4.8 to 4.11 is equal to the capacitance of the immediate branch in parallel with the capacitance of the delayed branch. The instant of calculation for Cl is thirty minutes after the termination of the current source.

As was done for the delayed branch, the dv/dt of the terminal voltage versus time curve is measured and the equations mentioned for the case of the delayed branch are applied to the results.

In the calculation of the long term branch capacitance it is also possible to use a second identification procedure. In this method, the time constant for the long term branch is previously assumed and the equation for the charge equilibrium is applied after three times the selected time constant. This method saves the calculation of dV/dt that for this case is very difficult because the transient is very slow. However, the time needed to calculate the parameter is longer.

4.4 IDENTIFICATION OF LEAKAGE RESISTANCE

The leakage resistance is identified by measuring the decrease

in the capacitor terminal voltage over a period of 24 hours. The capacitor used for the leakage resistance determination was previously normalized to 2 volts. After the normalization, it is expected that all the internal capacitances in the equivalent model are charged to the same voltage and the voltage decrease as function of time can be attributed to the equivalent leakage resistance. The duration of the test (24 hours) is much greater than the time constants of the three equivalent model branches; therefore, the capacitor is assumed as the parallel equivalent of the three branches and the resultant circuit is an RC circuit. The analysis of a simple RC circuit gives:

$$Vc(t) = Vo\, e^{-t/R_{lea}Ct} \quad (4.12)$$

where Ct is the parallel equivalent capacitance, Vc is the double-layer capacitor terminal voltage and Vo is the initial voltage for the discharge, or in other words the terminal voltage after the normalization. In the previous equation the value of the leakage resistance is assumed to be much larger than the resistance of the three branches. Using the series approximation for the previous equation with t << Rlea*Ct gives:

$$Vc(t) = Vo(1-t/RpC_{lea}) \quad (4.13)$$

Defining ΔVc as the decrease in terminal voltage after the 24 hours test, the following relation is produced

$$R_{lea} = \frac{Vo\ \Delta t}{\Delta Vc\ Ct} \quad (4.14)$$

In the previous relation Vo is two volts, ΔVc is measured after 24 hours, Ct is known from the previous identification of the internal capacitances and Δt is equal to 24 hours.

4.5 IDENTIFICATION OF DOUBLE-LAYER CAPACITOR INDUCTANCE

The measurement of the capacitor inductance will be done with a DLC precharged to the rated voltage. The precharged DLC is then connected as is shown in figure 4.5. In this figure R is the total loop resistance and Vd is the on state voltage drop of a PN junction. Then, a trigger pulse of 10 msec is applied to the switch and the current waveform in the circuit is measured.

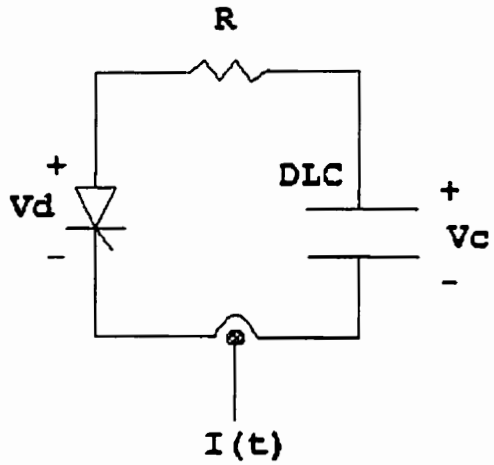


FIGURE 4.5 IDENTIFICATION OF CAPACITOR INDUCTANCE

The voltage Vc may be assumed as constant during the transient because of the long time constant involved in its variation, the final current after the transient results in:

$$I(\infty) = \frac{Vc - Vd}{R} \quad (4.15)$$

The analysis of the circuit gives:

The solution of the previous differential equation is:

$$L\frac{di}{dt} + iR = Vc - Vd \quad (4.16)$$

$$i(t) = I(\infty)\,(1-e^{-t/\tau}) \quad (4.17)$$

where $\tau = L/R$. If the slope of the curve of i vs t is measured, the final value of I ($I(\infty)$) is calculated, and the current for some time t' during the transient is known, then L could be calculated.

This measured inductance includes all the inductance in the loop; therefore, the inductance of the other components should be estimated and then subtracted from the total inductance calculated. The result of the identification is only an approximation.

CHAPTER 5

MEASUREMENT OF EQUIVALENT MODEL PARAMETERS

In this chapter, the experimental techniques used in the measurements and calculations are presented; these techniques assure that all the factors that may affect the accuracy of the measurements are controlled. In addition, results of the parameters measurements are presented and a brief discussion of these results is given. First, it is important to introduce the test facilities used in the double-layer capacitor test and in the parameters measurements.

5.1 TEST AND MEASUREMENT FACILITIES

Chapter 4 presented the procedure for the identification of the equivalent model parameters. The identification of the immediate branch parameters is based on the application of a controlled current source. The main function of the experimental setup is the generation of the controlled current source. Figure 5.1 shows the experimental setup used in the DLC test and the following pages include a brief explanation of the main functions of each element in the experimental setup.

The host computer is an IBM compatible system running under WINDOWS that is used to facilitate the user interface during the tests. The main functions of the computer are: programming of the controller, adjusting of the settings used in the different tests, and data processing. The computer is connected through the serial port to the control processor. Continuous interchange of data between the

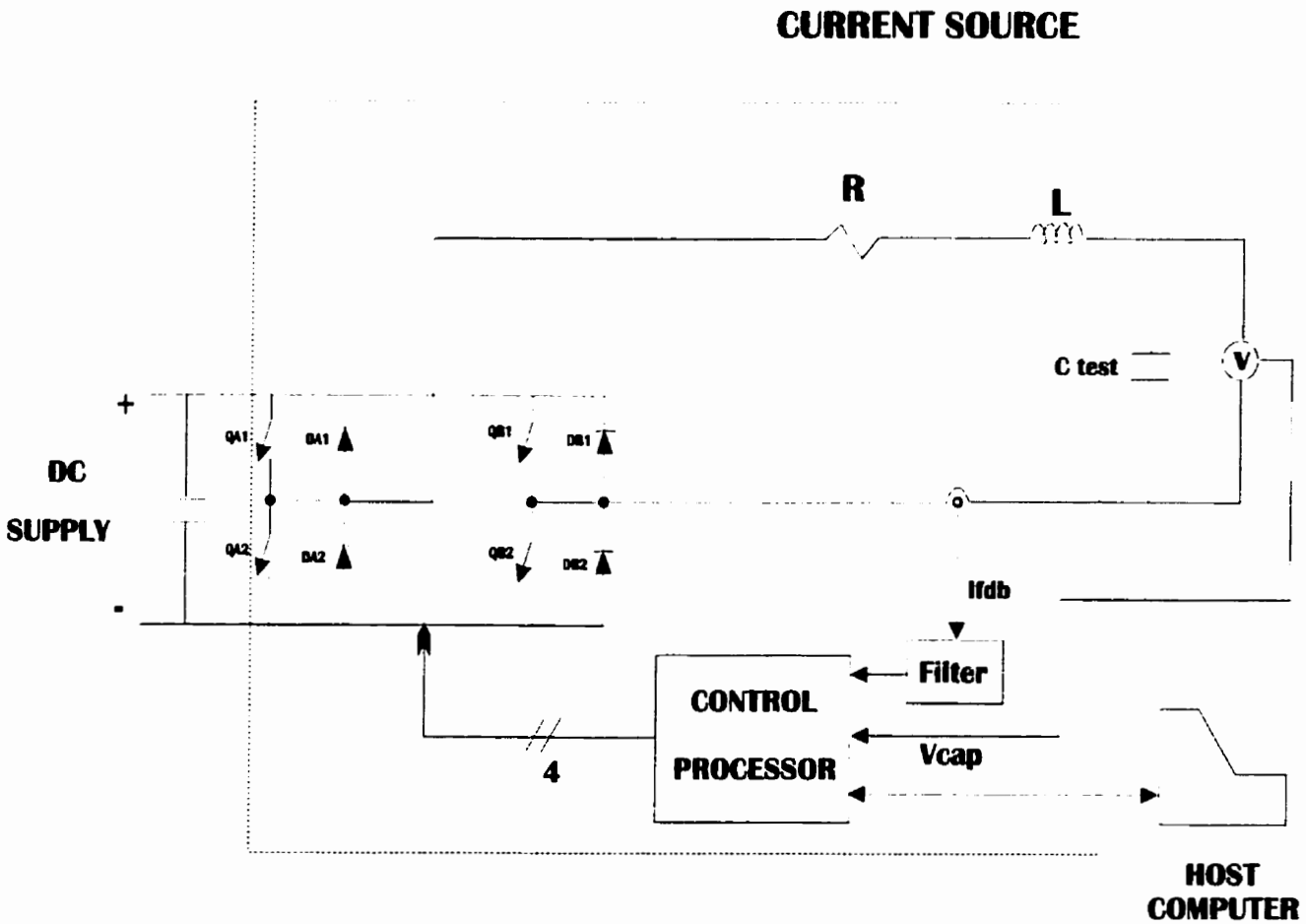


FIGURE 5.1 DLC TEST FACILITY

computer and the control processor is possible.

The control processor, a general purpose controller board for real time control, is the platform used for the control of the DC/DC converter, and for the different tests of the DLC's. The board is based on the microcontroller MC68332, which uses the 68020 CPU. Beside having the typical microcontroller features, the M68332 includes a time processing unit, which has many independently timed pulse channels. Those channels are used to control the state of the DC/DC converter switches.

The use of the microcontroller mounted in a business computer card makes it possible to use the system connected to a terminal or host computer. Therefore, the processor is programmed in C language on the host computer, compiled, and then the resultant file is transferred to the control board. Eight analog inputs and eight analog outputs are available for the signal feedback and monitoring as well as a 16-bit parallel port.

The main tasks of the control processor are: control of the current source, timing of the charge cycles, data acquisition, and control and execution of the programs for normalization and parameter calculation. The details are presented in the next section.

The controlled current source is generated by the four quadrant DC/DC converter, the R-L output circuit, and the controller. The DC/DC converter is a power circuit capable of operating in any of the four quadrants of the Vo vs Io. Four quadrant operation is necessary in the DLC study to guarantee regeneration and reversal of the supply to the load circuit. The converter can provide a charge and discharge current between -45 and 45 Amp in steps of 0.1 Amp.

The current source is controlled through the switching of the

power switches at a frequency of 4 KHz. The value of the inductance in conjunction with the supply voltage and the switching frequency of the devices produces a ripple in the current. The current ripple is 5 Amp peak to peak but the average value is precisely controlled. The resistance R and the inductance L in conjunction determine the time constant of the system. This time constant is needed in the design of the proportional integral control (see Appendix B).

The data acquisition is governed by the control processor; the analog feedback signals, current and voltage, are sampled with a period of 2 msec. The feedback signals have a range of -5 to +5 volts and the analog to digital converter in the controller has a resolution of 11 bits plus the sign bit. A data collection system, programmed in PASCAL and run on the PC, is used to store the measured voltage in a file that may be used later for data processing.

The switching frequency of the DC/DC converter is higher than the sampling frequency of the data acquisition unit. Therefore, the sampling theorem is not fulfilled and the sampled current may not be representative of the average current in the system. That factor makes it necessary to pre-filter the current signal from the sensor before the use of that signal in the digital system.

The anti-aliasing filter should be designed in order to attenuate the ripple frequency (4 KHz) and to keep without appreciable attenuation the sampling frequency (500 Hz). A second order filter was designed to accomplish that. The frequency response of the designed filter is shown in figure 5.2. Details about the structure and design of the filter are presented in Appendix B.

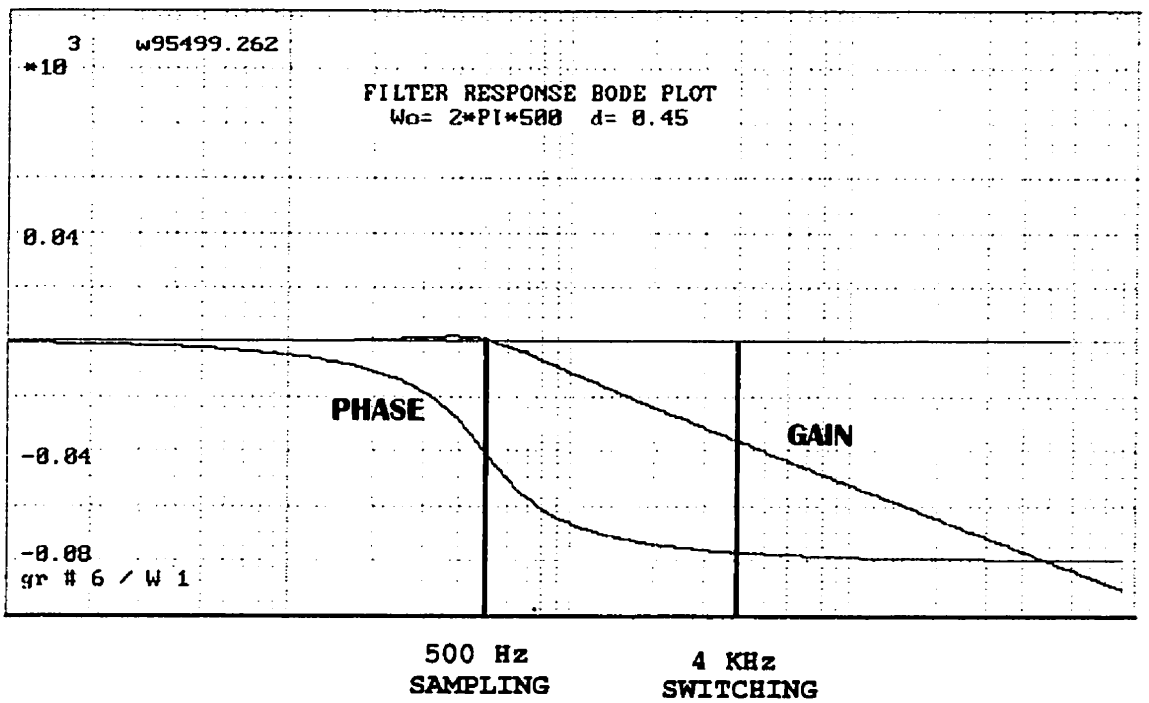


FIGURE 5.2 FILTER RESPONSE BODE PLOT

5.2 MEASUREMENT TECHNIQUES

This section introduces the different techniques implemented in order to control the factors that may affect the measurements if they are not controlled carefully. The development of techniques to govern these factors is necessary to get repeatable results in the experiments. These factors are:

- Control of the charge fed into the capacitor.
- Automatic measurements.
- Initial charge present inside the capacitor.

In the following pages each one of these factors and the corresponding techniques used in their control are analyzed in detail.

5.2.1 *Control of the Charge in the Capacitor*

The capacitance is given by a relation between the charge delivered to the capacitor and the voltage across its terminals; therefore, the accuracy in the capacitance measurements depends on the control of the charge introduced in the capacitor and the adequate sensing of the voltage.

The test of the capacitors is based on the application of constant current into the device. The total charge under this condition is given by the following integral:

$$Q = \int_0^t i\,dt = I\int_0^t dt \qquad (5.1)$$

In the previous relation two factors are involved in the charge control; the exactness of the current magnitude (I), and the precise timing of the current source. Those two factors should be exactly controlled during the experiments.

As was explained in the previous section, the test facility produces a controlled current with an average value precisely fixed according to the control input. The controller uses a proportional integral control of the current to get high accuracy in the magnitude of the current source.

In addition, the response of the controller should be fast enough to neglect the effect of the waveform when the current is rising or falling to the desired value. The controller adjusts the current in such a way to reach the desired value in less than 20 msec; furthermore, the current rises or falls monotonously. This transient time is small enough compared to the time of a typical DLC charge action that is in the order of seconds, and the current waveform may be considered as a step to the desired value.

The second factor involved in the control of the charge is the timing of the current source. The current source is precisely timed inside the control processor in order to know exactly how much time current was applied to the capacitor, and this allows accurate calculation of the total charge delivered to the capacitor.

Therefore, the two factors involved in the total charge delivered to the capacitor are carefully controlled during the experiments.

5.2.2 *Automated Measurement Procedures*

The second parameter, beside the charge, which is important in the measurement of the capacitance is the capacitor voltage. As the time constants for the delayed and long time branches are in the order of minutes, the process of measuring the parameters takes considerable time. In addition, as was mentioned before, it is necessary to control the current source timing, sample the terminal voltage with a

fixed frequency of up to 10 times per second, and in some cases synchronize the current source with the terminal voltage measurements in order to get accurately the charge introduced into the capacitor. Therefore, measurements fully automated in the short and long time are needed to produce repeatable results.

The automated measurement procedures allow the possibility of making all the measurements accurately, using the maximum resolution of the digital system, and eliminating the human participation and its inaccuracy. In this form, the automated measurements save time and reduce the sources of error.

Two automated measurements systems were developed:

- Data Acquisition System.
- Automated Parameter Calculation.

DATA ACQUISITION SYSTEM

The data acquisition system is an automated measurement procedure that samples the double-layer capacitor voltage in synchronization with the current source timing and produces a file with the total time that the current has been applied along with the correspondent terminal voltage. This system assures that the charge introduced into the capacitor and the voltage are measured simultaneously. The sampling frequency is up to 100 samples per second and the system allows the read values to be saved in a file facilitating the use of analytic and graphical tools with the collected data.

The data acquisition system consists of two independent parts: the first is a computer program that enables the data collection process, collects the data, and stores it in a file. This program was written in PASCAL. The second part consists of the inclusion of a

routine in the control board which can respond to the signal received from the PC and send, with a desired frequency, the read data back to the PC.

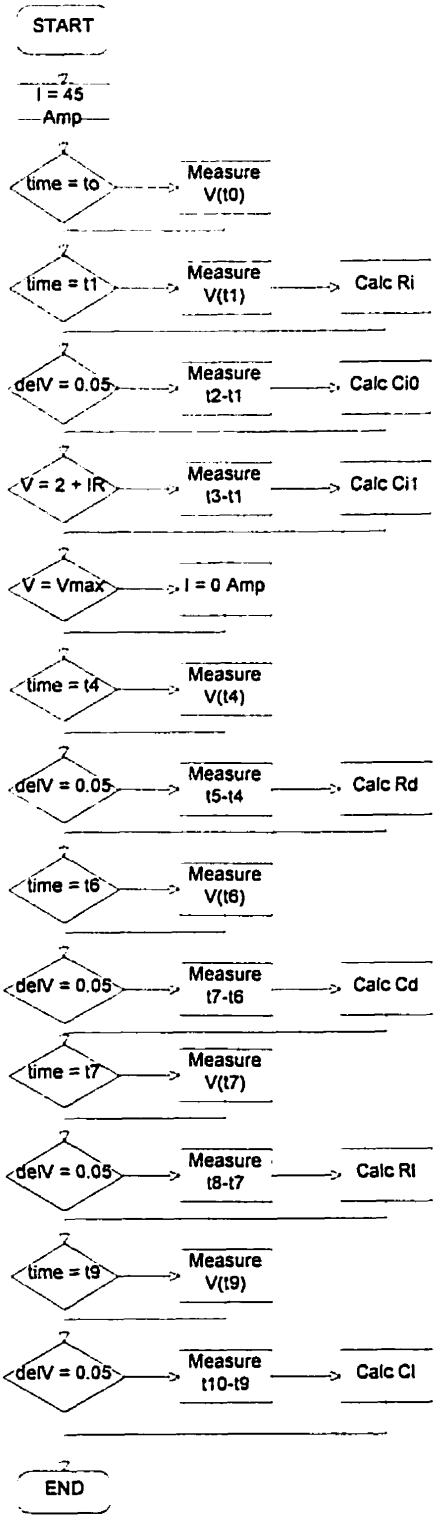
AUTOMATED CALCULATION OF PARAMETERS

The automated process of parameter calculation has as its objective the calculation of the equivalent model parameters directly inside of the microprocessor based control board. The availability of this program allows one to make use of the maximum resolution available in the digital control system, and gives consistency in the sequence of steps and timing of the parameter calculation. This program calculates the parameters of the immediate, delayed and long term branches.

The main properties of the parameter calculation program are the following:

- A fully discharged DLC should be used in the identification.
- Takes approximately thirty five minutes to calculate the immediate, delayed and long term parameters.
- Indicates the results on the computer screen if a monitor program is being used.

Details about the methodology used in identifying the equivalent model parameters were presented in chapter 4. Figure 5.3 summarizes the sequence of steps followed by the automated parameter measurement program. The list of the automatic calculation program is included in the general double-layer capacitor test program (CAP1.C) presented in appendix C.



V(tn) refers to terminal voltage at tn

I refers to external current source value

del V = terminal voltage change in volts

FIGURE 5.3 AUTOMATIC PARAMETERS MEASUREMENT FLOW CHART.

5.2.3 *Double-Layer Capacitor Initial Conditions*

One problem found experimentally when repeated experiments were applied to the capacitor was the effect of the charge present in the capacitor at the start of the test. In the first set of experiments, the capacitor under test was discharged by applying a short circuit across its terminals for several hours. However, the results were not consistent.

Then, a study of the charge remaining in the capacitor after several hours of short circuit was performed. That test revealed that even after twenty-four hours of short circuit, there is enough charge stored in the capacitor to increase the terminal voltage up to 20% of the initial voltage. Short circuit condition for about one month is necessary to fully discharge the capacitor; this makes experiments in an acceptable time frame almost impossible.

The remaining charge inside the capacitor is responsible for the differences in experimental results. Therefore, it is necessary to develop a procedure to fully discharge the DLC in a shorter time. A capacitor fully discharged is defined as one with voltage lower than 1% of the rated voltage in all the internal capacitances .

In addition, for the leakage resistance and input inductance measurement and for future applications with DLC's, it is necessary to precharge the capacitors to a predetermined and fixed voltage. The precharge of the capacitor implies the charge of all the branches in the equivalent model to the same voltage. Therefore, it is also necessary to develop a procedure to equalize the double-layer capacitor voltage to any desired level. An equalized voltage is defined as a DLC terminal voltage that changes less than 1% of the rated voltage in 24 hours if the leakage effect mentioned in chapter

three is compensated.

The discharge or precharge procedures are called "Normalization Process" and are explained in the following pages.

NORMALIZATION PROCESS

Repeatable measurements of the capacitor properties are only possible if the voltage across all internal capacitances of the proposed model is the same and if all the tests are applied to capacitors with the same initial conditions. The previous results about the charge remaining in the capacitor showed the difficulties in reaching the fully discharged condition in the capacitors.

First, it is important to understand the reason behind those differences in the results. The general equivalent model of a double-layer capacitance, presented in chapter three, consists of an infinite number of parallel RC branches with different time constants between a few seconds and several hours. Using this model, the behavior of the capacitor under discharge is explained: When the capacitor is discharged, either using a short circuit or applying a negative current, only the charge stored in the fast branches is removed. The terminal voltage falls to zero but large amounts of charge are still inside the capacitor. This charge will redistribute itself throughout the capacitor, thus increasing the terminal voltage. The charge distribution process takes hours or even several days. It is clear that the longer the short circuit time, the larger the amount of charge removed. This fact explains the appreciable differences in results if the discharge method and initial voltage are not controlled.

The goal to be reached is to take a capacitor with any initial

charge, and to precharge or discharge it completely in the shortest time possible. From this point, the description of the normalization process will discuss to the capacitor discharge; the precharge follows similar steps but shifting the voltage reference to the desired precharge voltage. Several principles are used in the proposed normalization process to fulfill the previous goal:

- Utilization of negative capacitor terminal voltage but limited only to 15% of the rated voltage because the capacitors are asymmetrical and the use of high negative voltages may produce damage in the devices.

- The selection and justification of the normalization process selected based on the three branch equivalent model presented in chapter three.

- According to the two points mentioned before, the normalization involves the introduction of charge producing a negative voltage in the immediate branch to accelerate the internal charge redistribution process.

- In general the normalization process consists of the application of a discharge current, followed by a wait time in which the internal charge redistribution process increases the terminal voltage. This discharge cycle is repeated several times until the total charge in the capacitor is approximately equal to the zero voltage charge.

After the selection of the general normalization process, several specific decisions were made to optimize the procedure. These decisions are based on experimental results, and they refer to the current levels, voltage set points, and number of cycles. The decisions are the following:

- The results of the parameter identification process, to be presented later in this chapter, indicate that the capacitance of the delayed and long term branches together are similar in magnitude to the fixed capacitance of the immediate branch. Using this observation, if the DLC voltage before the normalization process is lower than 10% of the rated value, the normalization consists simply in discharging the capacitor to a negative voltage equal to the one before the normalization. Therefore, the opposite charge introduced in the immediate branch is compensated by the charge still present in the other two branches and the total charge is approximately the zero voltage charge. This conclusion is valid only in the discharge process as in the precharge the immediate branch capacitance depends on the desired voltage.

- When the normalization process begins, the current is made high to remove the charge faster. In subsequent discharge cycles, the current is decreased to reduce the effect of the immediate resistance voltage drop and optimize the amount of charge removed. The discharge current in the first three discharge cycles is 30 Amp, 10 Amp, 5 Amp; in all the subsequent cycles a discharge current of 2 Amp is used.

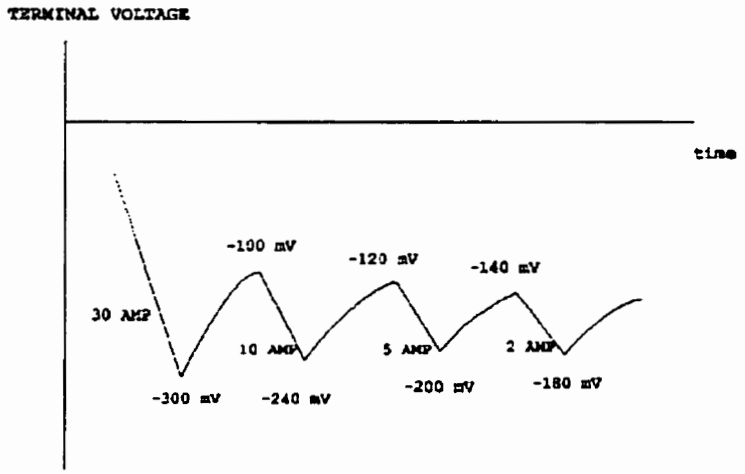


FIGURE 5.4 DISCHARGE CYCLES DURING NORMALIZATION.

- The negative terminal voltage reached during each discharge cycle (-0.3 volts for the first cycle) is decreased in magnitude for subsequent cycles. Similarly, the voltage up to which the capacitor voltage increases by the internal charge distribution is negative and is increased in magnitude for subsequent cycles. These two conditions reduce the time between discharge cycles and accelerate the normalization process. Figure 5.4 presents a typical voltage vs time curve during the normalization process in which the current used in each discharge cycle and the voltage set points are indicated.

- The normalization procedure should be applied for 90 minutes to a single capacitor in the first day; then, the procedure is repeated 24 hours later for another 60 minutes to remove the charge initially stored in the long term branch. 24 hours later, the terminal voltage and the internal equivalent capacitances will be equalized to approximately zero volts.

The normalization program was tested several times with different initial voltages and for different capacitors. The results indicate that a program run of 90 minutes could remove between 80 and 90% of the initial charge stored in a capacitor with initial terminal voltage close to the rated value. 24 hours after the second normalization action, the capacitor voltage is lower than 20 millivolts and this voltage does not grow more than 5 millivolts in the following days. Capacitors with low initial voltage were normalized in 24 hours, after the application of a single discharge.

Figure 5.5 presents the simplified flow chart for the discharge normalization program. The precharge normalization program follows similar steps except for the alternative procedure for initial low voltage that can not be implemented.

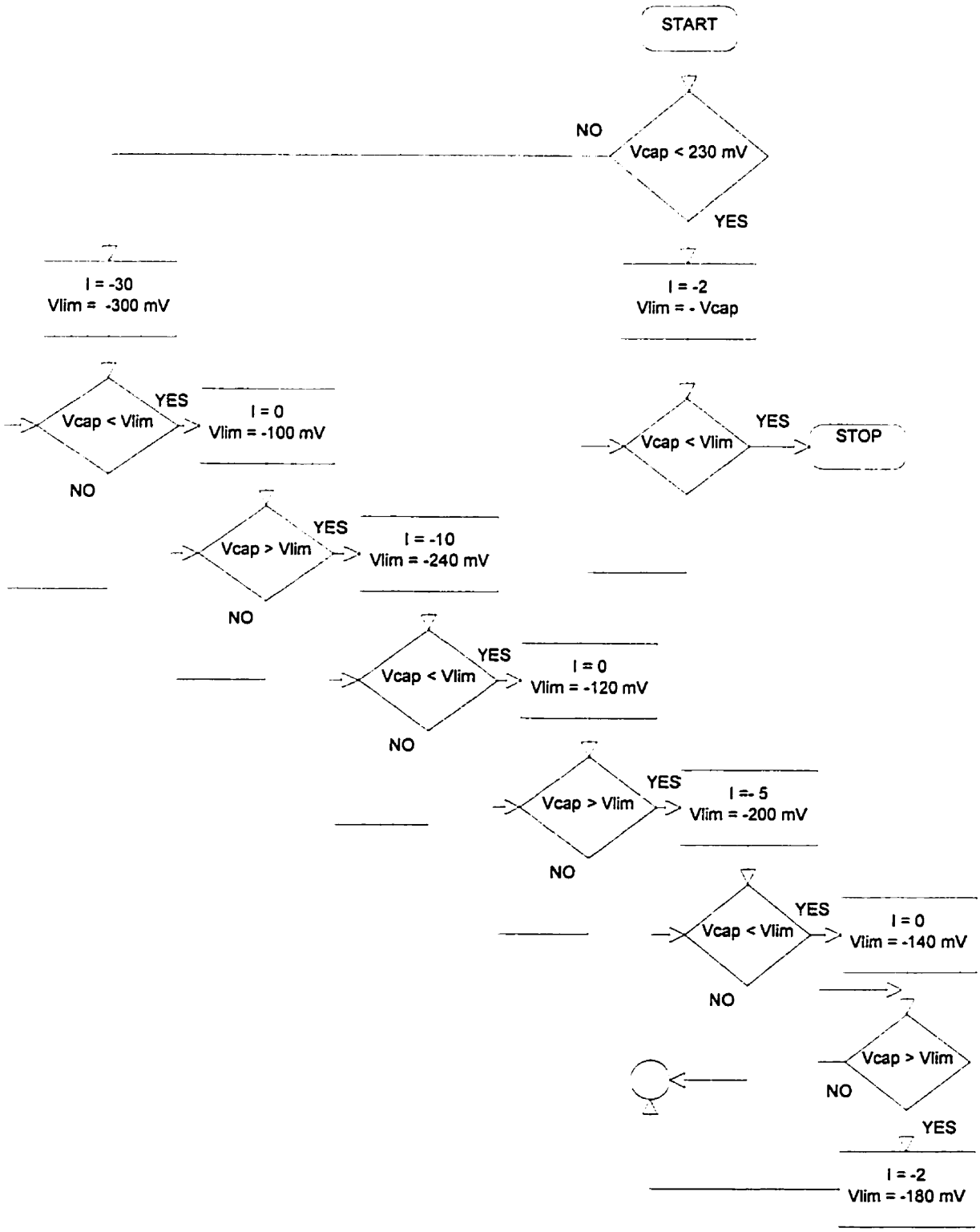


FIGURE 5.5 NORMALIZATION PROCESS FLOW CHART.

With the techniques needed to get repeatable measurements clearly established, the next section presents the identification and measurement of the equivalent model parameters.

5.3 MEASUREMENT OF PARAMETERS

With the clear definition of the procedure for the parameter calculation and the development of the automated parameter measurement program, the parameters values may now be measured. The following table summarizes the average results of the parameters measurements:

PARAMETERS	PANASONIC 470 F	PANASONIC 1500 F
Ri	2.5 mΩ	1.5 mΩ
Ci0	270 F	900 F
Ci1	190 F/V	600 F/V
Rd	0.9 Ω	0.4 Ω
Cd	100 F	200 F
Rl	5.2 Ω	3.2 Ω
Cl	220 F	330 F

TABLE 5.1

The parameters were measured for ten different 470 F capacitors and six 1500 F capacitors and the differences among the measured parameters were lower than 10%.

Figure 5.6 presents the equivalent model with the parameter values for the 470 F double-layer capacitor.

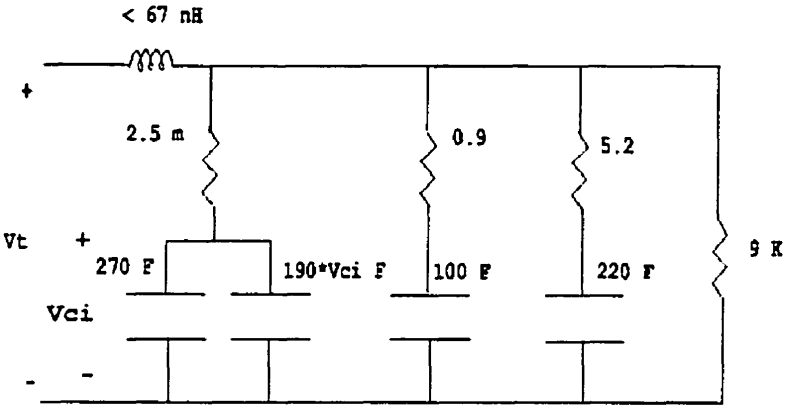


FIGURE 5.6 MEASURED EQUIVALENT MODEL FOR THE 470 F DOUBLE-LAYER CAPACITOR

The next step is a study of the consistency of the automatic parameter calculation program. In this direction, the program was run five times to the same normalized DLC and the results were compared. Table 5.2 summarizes the results.

PARAMETER	MAXIMUM VALUE	MINIMUM VALUE	ERROR (%)
Ri	2.353 mΩ	2.251 mΩ	4.43 %
Ci0	281 F	269 F	3.94 %
Ci1	205 F/V	189 F/V	8.51 %
Rd	0.925 Ω	0.842 Ω	9.22 %
Cd	109 F	102 F	6.67 %
Rl	5.252 Ω	4.951 Ω	6.05 %
Cl	238 F	222 F	6.96 %

TABLE 5.2

The per cent error among the five measurements was calculated as the maximum value minus the minimum value divided by the average value of each parameter.

The results show the consistency in the results of the automatic parameters measurement system with an error under 10% for all the measurements.

The measured average leakage resistance for the 470 F DLC was 9 KΩ.

The total measured loop inductance is about 167 nH. The inductance of the loop without the capacitor is estimated to be at least 100 nH. That gives an estimated capacitor inductance lower than 67 nH for the 470 F DLC. Although this value is only an approximation, it is small enough to assume a neglectable capacitor inductance for most if not all power electronics applications.

5.4 DISCUSSION OF MEASUREMENTS

There are several important observations that result from the parameters calculations; among them are the following:

- The capacitance of the immediate branch increases with an increase in terminal voltage; therefore, most of the energy is stored in the higher voltage levels. This observation is an advantage in power electronics because the capacitor will provide most of the energy without the necessity to discharge it to very low voltages.

- The capacitance of the delayed and long term branches together is approximately equal to the fixed capacitance of the immediate branch. This is a considerable amount of energy that can not be removed quickly from the capacitor. This relation between the capacitance of the different branches is an important factor that was

used in the normalization program.

- The time constant of the immediate branch depends on the voltage and its range is between 0.5 sec and 2 sec. The time constant of the delayed branch is about 90 sec; therefore, it is considerably higher than the immediate branch time constant and the assumptions of independent time behavior are correct.

- The long term branch parameters were calculated five minutes after the charge action, that is more than three times the delayed branch time constant. The long term branch time constant was about 1265 sec; therefore, again this value is considerably higher than the time constant for the delayed branch and the assumption is correct.

- The integral capacitance appears to be the definition used by the manufacturer in the DLC rating. However, a higher value of capacitance is obtained at potentials over 1.5 volts which is the range of interest in power electronics.

- Although there are differences in the parameter values among the ten capacitors available, those differences are lower than 10% with respect to the experimental results presented in table 5.1. In other words, the 470 F DLC may be modeled with the values of table 5.1 without an appreciable error.

In the next chapter the mathematical equations directing the behavior of the equivalent model are introduced in a simulation program and the results obtained with the simulator are verified with the experimental data available.

CHAPTER 6

EQUIVALENT MODEL VERIFICATION

The purpose of this chapter is to provide a comparison between the experimental results and the results of simulations using the proposed equivalent model. The chapter includes the development of a simulation routine, the validation of the principal assumptions used in the model development, and the verification of the model accuracy under different tests.

The software to be used is the program SAM4 developed at the Power Group of the Electrical and Computer Engineering Department at the University of Toronto. In this simulation tool, the system to be simulated is represented by the differential equations that govern the response of the system. The program solves the differential equations using the Runge-Kunta method. In addition, the program gives a graphical and tabular output of the state variables and any other variable previously defined.

Based on the model of the double-layer capacitor presented previously, the program SAM4 was chosen for the following reasons:

- Easy representation of the equivalent model in differential equations.
- The program allows the user to stop the simulation task at any point, change the parameters, and continue the simulation. This feature makes it possible to simulate changes in the conditions of the device during the test.
- Good graphical representation of the output simulated variables.
- Easy graphical representation of several output variables

simultaneously.

- The program can store the output variables in a file coherent with the data acquisition previously described. In this way, the experimental and simulated results may be easily represented in the same graph.

6.1 MATHEMATICAL REPRESENTATION OF THE EQUIVALENT MODEL

The equivalent model used for simulations has one difference with respect to the complete model calculated in chapter 5. The calculated inductance at the input of the double-layer capacitor is neglected under current levels of tens of amperes such as the set of experiments simulated in this chapter.

Therefore, the equivalent model to be simulated consists of three parallel RC branches in series and a parallel leakage resistance. The immediate branch capacitor value is linearly dependant on the voltage across its terminals.

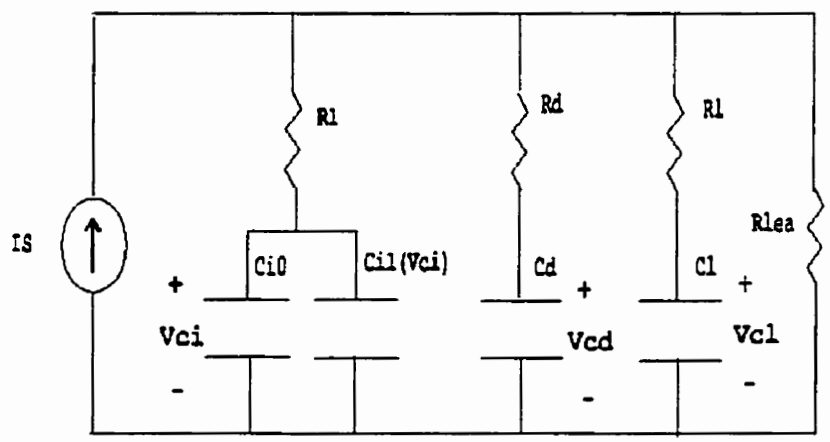


FIGURE 6.1 EQUIVALENT MODEL FOR SIMULATIONS.

Figure 6.1 shows the equivalent model used for the simulation. Based on this equivalent circuit, the differential equations that define the system will be calculated next.

The current source is an ideal DC source and the values of the different model parameters are the ones calculated in chapter 5 for the 470 F double-layer capacitor. The three state variables used to formulate the differential equations are the voltages in each one of the equivalent capacitors (VCi, VCd and VCl). The determination of the differential equations is based on the relation for the differential capacitance presented in chapter three:

$$C_n = \frac{dQ}{dV} = \frac{i_n(t)\,dt}{dV} \qquad (6.1)$$

Where n represents each one of the equivalent model branches. From equation 6.1, the relation between the change in the capacitor voltage and the current flowing through it is deduced:

$$i_n = C_n \frac{dVc_n}{dt} \qquad (6.2)$$

In the immediate branch, the value of Ci depends on the state variable VCn as was explained in chapter three:

$$C_i = C_{i0} + C_{i1} * Vc_i \qquad (6.3)$$

In addition, the currents flowing through each branch are related to the terminal voltage of the capacitor (Vt) through the following equation:

$$i_n = \frac{Vt - Vc_n}{R_n} \qquad (6.4)$$

Using the equations 6.2, 6.3 and 6.4 for each branch to eliminate the branch current that is not known, the differential equations are

determined:

$$\frac{dVc_i}{dt} = \frac{Vt - Vc_i}{R_i * (C_{i0} + C_{i1} * Vc_i)} \quad (6.5)$$

$$\frac{dVc_d}{dt} = \frac{Vt - Vc_d}{R_d * C_d} \quad (6.6)$$

$$\frac{dVc_l}{dt} = \frac{Vt - Vc_l}{R_l * C_l} \quad (6.7)$$

Finally, a relation between the terminal voltage (Vt), not controlled in the experimental setup, and the controlled variable (Is) should be determined:

$$Vt = \frac{Is + V_i/R_i + V_d/R_d + V_l/R_l}{1/R_i + 1/R_d + 1/R_l + 1/R_{leq}} \quad (6.8)$$

The last four equations will represent mathematically the equivalent model of the DLC. Appendix C presents the main program CAPASAM.PAS, used for the capacitor performance simulation.

6.2 VERIFICATION OF EQUIVALENT MODEL ASSUMPTIONS

In the selection of the double-layer capacitor model several assumptions based on physics facts or experimental results were made. This section presents the verification of the two principal assumptions in the equivalent model: the linear dependence of the immediate branch capacitance on the voltage and the distinct time constant of the different branches.

6.2.1 *Experimental Dependence of the Capacitance on the Voltage*

Whereas the physics of the double-layer indicates that a linear relation between the capacitance and the voltage exists at least in some region of voltage, this relation should be confirmed experimentally in the operating range of the capacitor. The immediate branch differential capacitance of a double-layer capacitor was calculated from the experimental data between zero volts and the rated voltage. Figure 6.2 shows the measured curve of differential capacitance vs voltage.

In this figure, the increase in the capacitance value as the voltage is increased is confirmed. Although in fact the curve is not a perfectly straight line, the assumption of a straight line as is shown is a good approximation of the relation between Ci and Vci.

6.2.2 *Distinct Time Behavior of the Branches*

Figure 6.3 shows the simulation of a simple charge and self charge distribution action. In the figure, the voltages in each of the three equivalent capacitors have been included. The point A shows the instant at which the current source is turned off and the delayed branch begins to be calculated. At this point, the voltage in the delayed branch is lower than 20% of the rated voltage, which means the energy stored in this branch is lower than 4% of the maximum energy in the branch. This result validates the assumption of no charge at the start of the delayed branch calculation used in the parameters identification.

Point B shows the point of the delayed capacitance calculation. Point C shows the start of the long term branch calculation. Note in

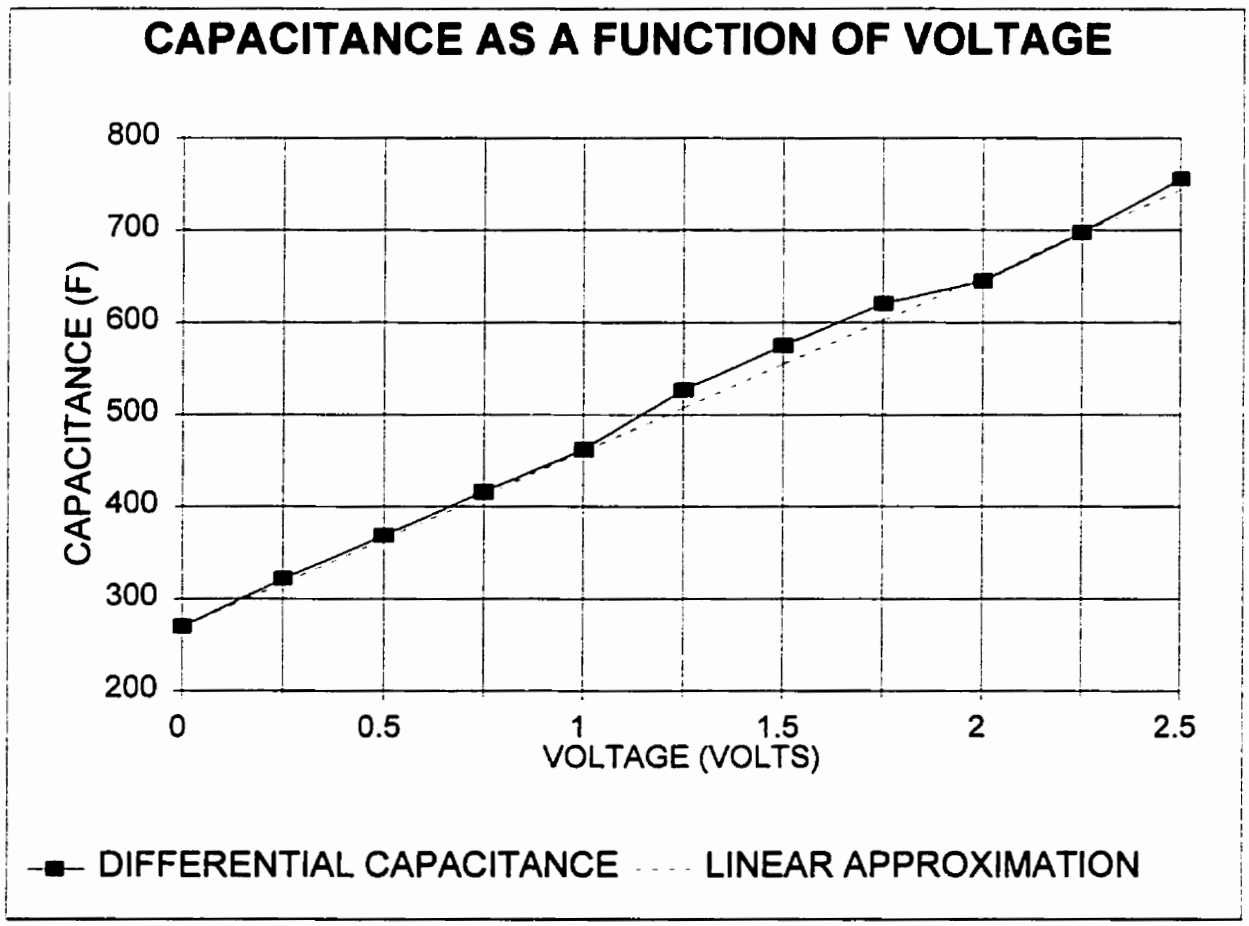


FIGURE 6.2 EXPERIMENTAL RELATION BETWEEN THE DLC CAPACITANCE AND THE VOLTAGE.

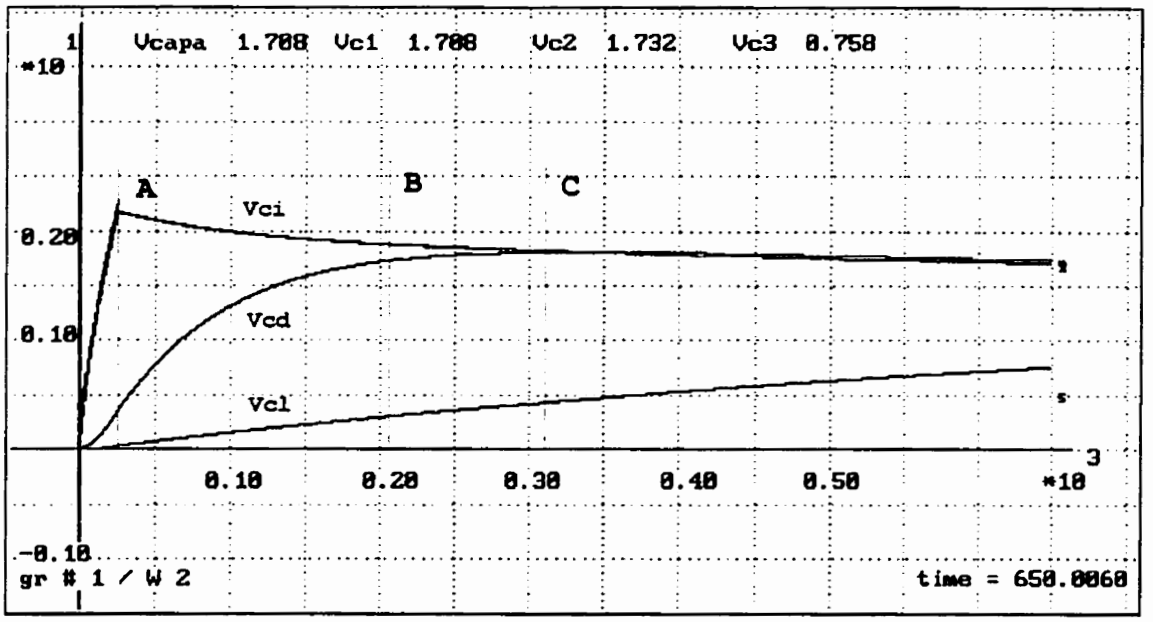


FIGURE 6.3 VERIFICATION OF THE PARAMETER IDENTIFICATION ASSUMPTIONS.

this point the almost equalized voltage in the immediate and delayed branches and the low voltage present in the long term branch at this point. Those two observations confirm the validity of the supposition of independent time behavior of the long term branch with respect to the delayed one.

6.3 COMPARISON BETWEEN EXPERIMENTAL AND SIMULATED RESULTS

Figures 6.4 to 6.9 represent the comparison between the experimental and simulated results for five different tests.

Figure 6.4 shows the terminal voltage during the charge action with constant current and the first minutes of the internal charge distribution process. This graphic presents the first three minutes of the capacitor response to a charge action. In other words, the figure compares the experimental results with the simulation during the time that the immediate and delayed branches predominate in the capacitor behavior. The experimental and simulated results are in a very good agreement with each other.

Figure 6.5 shows a more extensive representation of the internal charge distribution process. Again a constant current of 30 amperes was applied to a normalized capacitor but now the graphic indicates up to 30 minutes after the charge action application. This comparison gives the possibility of evaluating the long term branch of the equivalent model. A small difference in the simulated and experimental results exists mainly in the interval between the delayed and long term branches; however, the difference is always less than two per cent of the rated voltage which is an acceptable value. Also note, the fit between the curves in the two points given by the instants of

parameter calculations.

Figure 6.6 is a representation of the double-layer capacitor terminal voltage during a charge action with very low current. As the parameters of the equivalent model were calculated using 45 amperes, it is important to verify how accurate the model is with lower charge current. This curve permits to conclude that the model is accurate independently of the magnitud of the current applied to the capacitor.

Figure 6.7 is a complete representation of the charge and discharge cycle in a DLC. This curve assures that the model is equally adequate for discharge actions. It is important to recall that the differences in the parameter values among DLC's are up to 10% of the average values shown in table 5.1. As the average values of that table are used in all the simulations, some curves fit better than other; however, in all the simulations, the results are under the acceptable limits (error < 2%).

Figure 6.8 presents a more complex charging cycle in which the capacitor is charged until the rated voltage. Then, thirty seconds pass without any current application. After that, the capacitor is discharged until the voltage across the immediate and delayed branches are at approximately equal. Finally, the current is turned off again and the change in terminal voltage thereafter is very low since that change is given only by the long term branch. Again the experimental and simulated results are very close.

Figure 6.9 presents the capacitor response to a charge up to one volt and the first ten minutes of the self discharge process. In this case the differences between the experimental and simulated results are greater than in the previous simulations. These differences are due to the simplification of the equivalent model specifically the

assumption of only one branche voltage dependent. Note that the experimentally measured voltage decrease faster during the first seconds of the self-charge distribution but the final simulated voltage is lower than the experimental one. This indicates that the time constant of the delayed branch at this voltage is smaller; therefore, the delayed capacitance is lower. The trade off between model simplicity and accuracy is now evident; however, in most of the DLC applications, the devices are not discharged to very low voltages and the mentioned error has less effect. Furthermore, even for this small charge voltage the error in the simulation is lower than 5% of the rated voltage. This is still an acceptable value.

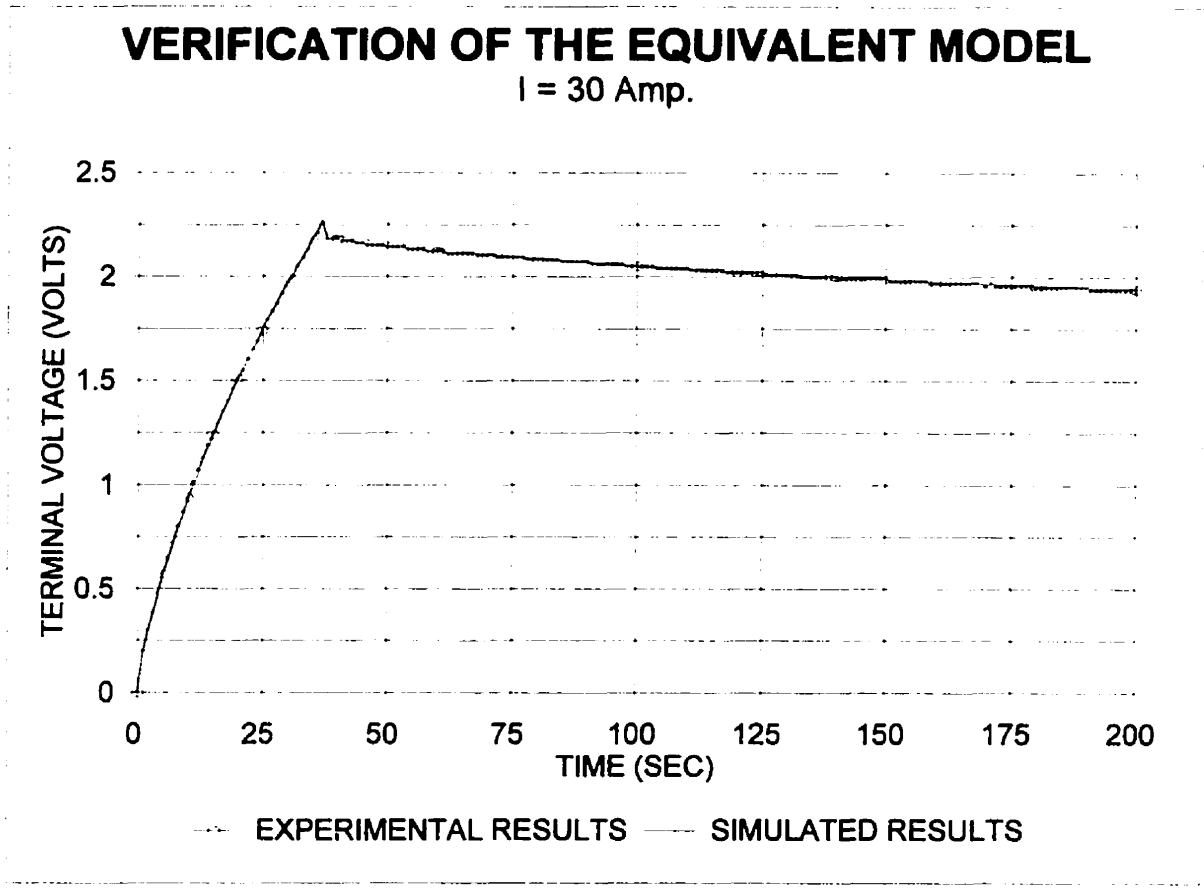


FIGURE 6.4 IMMEDIATE AND DELAYED BRANCHES VERIFICATION.

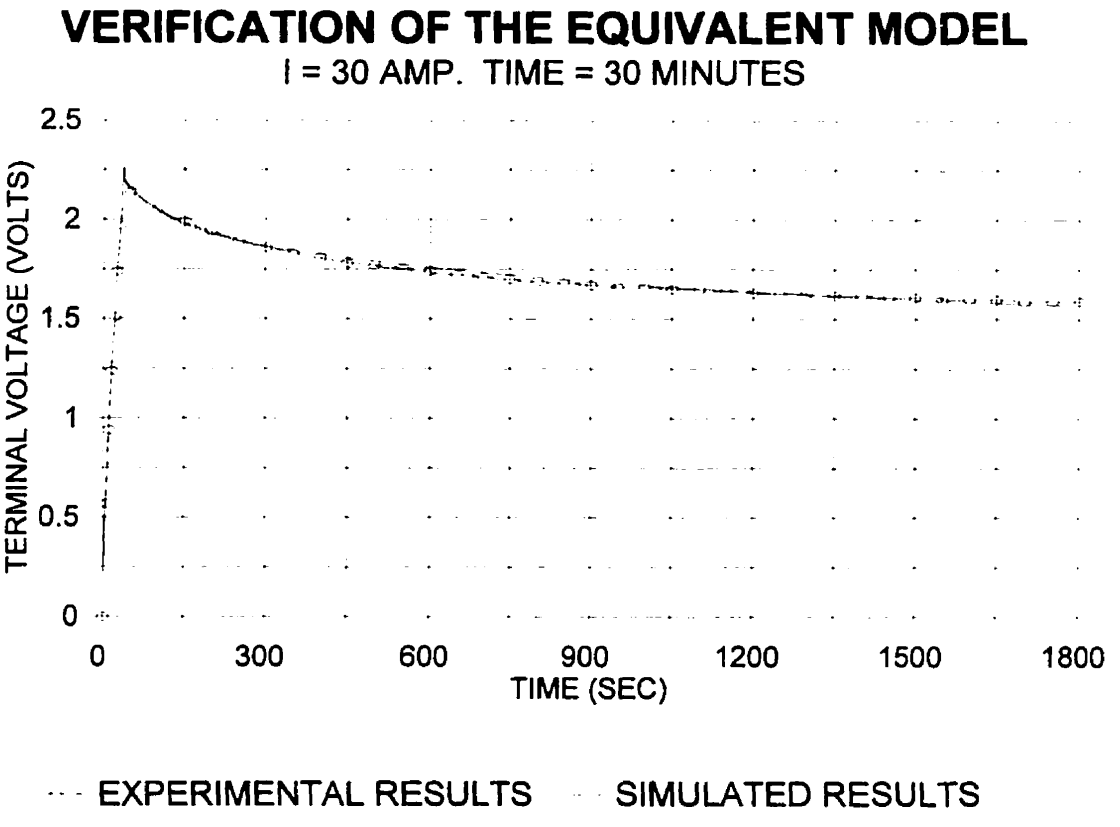


FIGURE 6.5 VERIFICATION OF THE LONG TERM BRANCH.

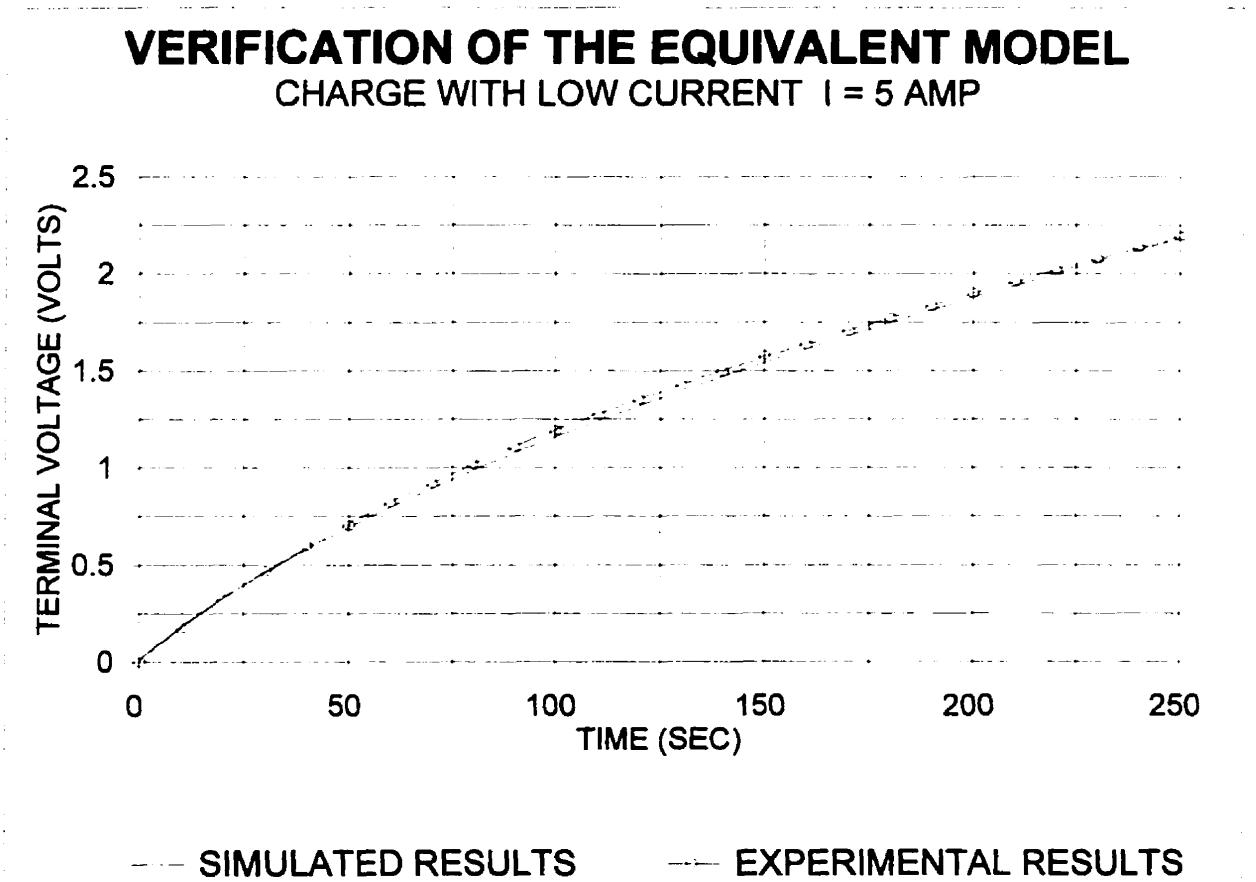


FIGURE 6.6 VERIFICATION OF THE EQUIVALENT MODEL. LOW CURRENT CHARGE.

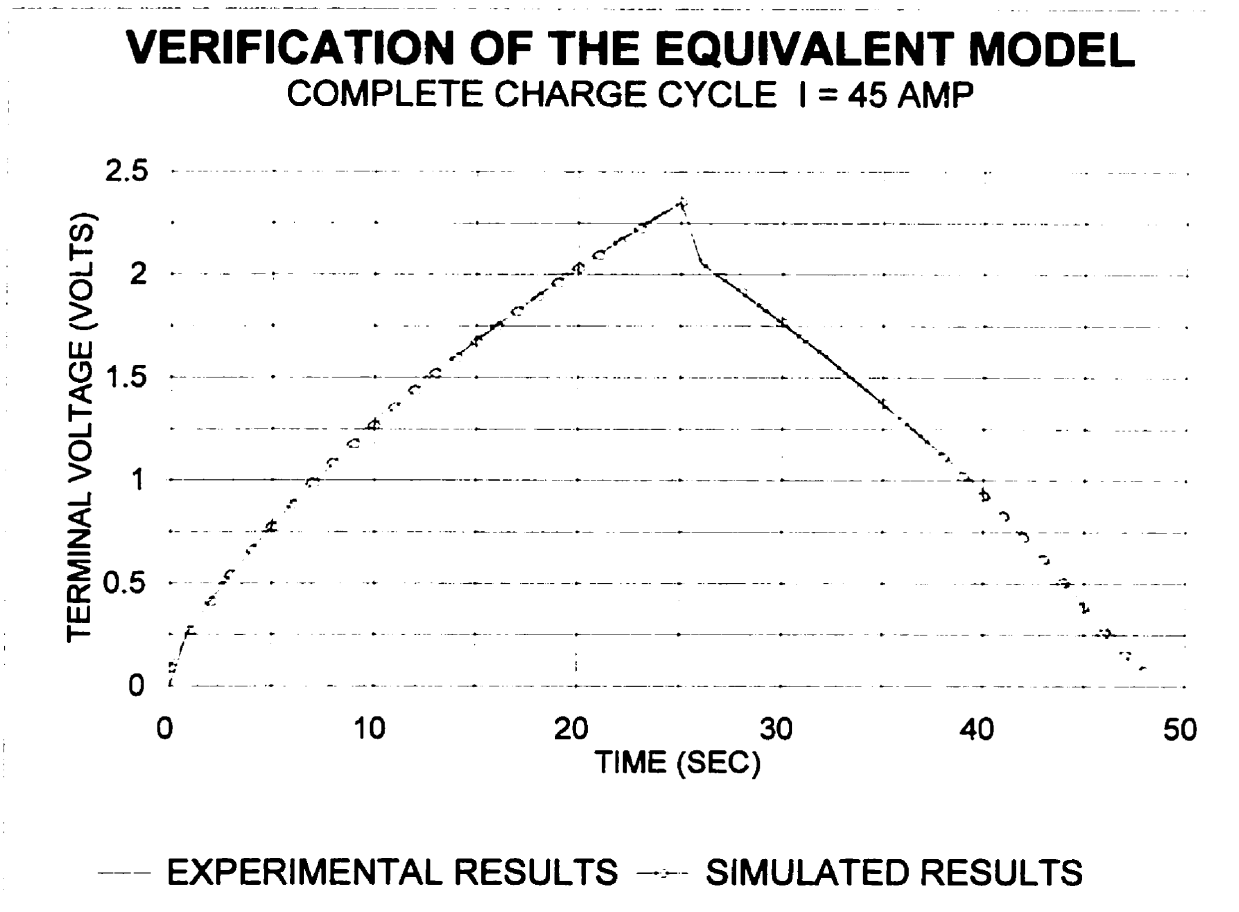


FIGURE 6.7 VERIFICATION OF THE EQUIVALENT MODEL. CHARGE AND DISCHARGE.

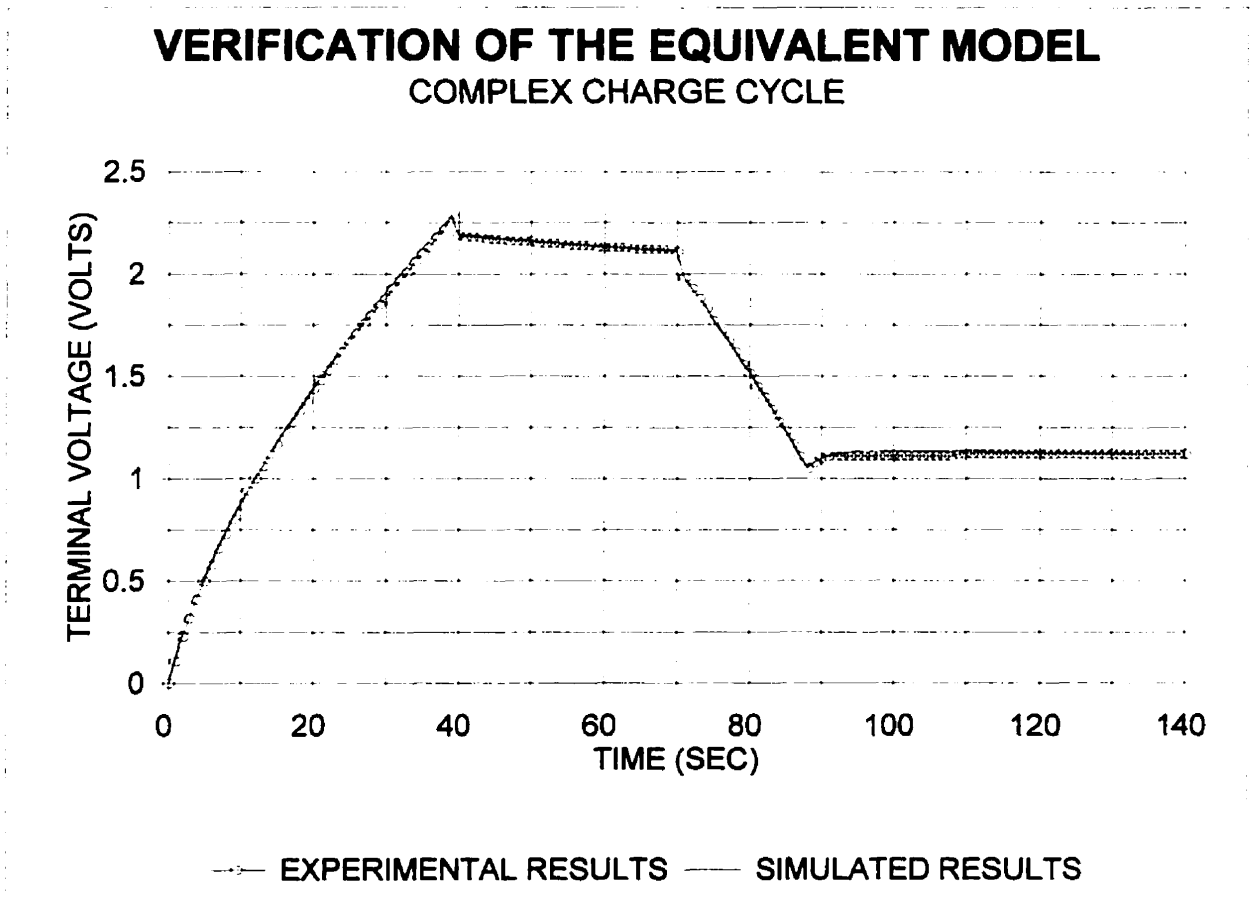


FIGURE 6.8 VERIFICATION OF THE EQUIVALENT MODEL. COMPLEX CHARGE CYCLE.

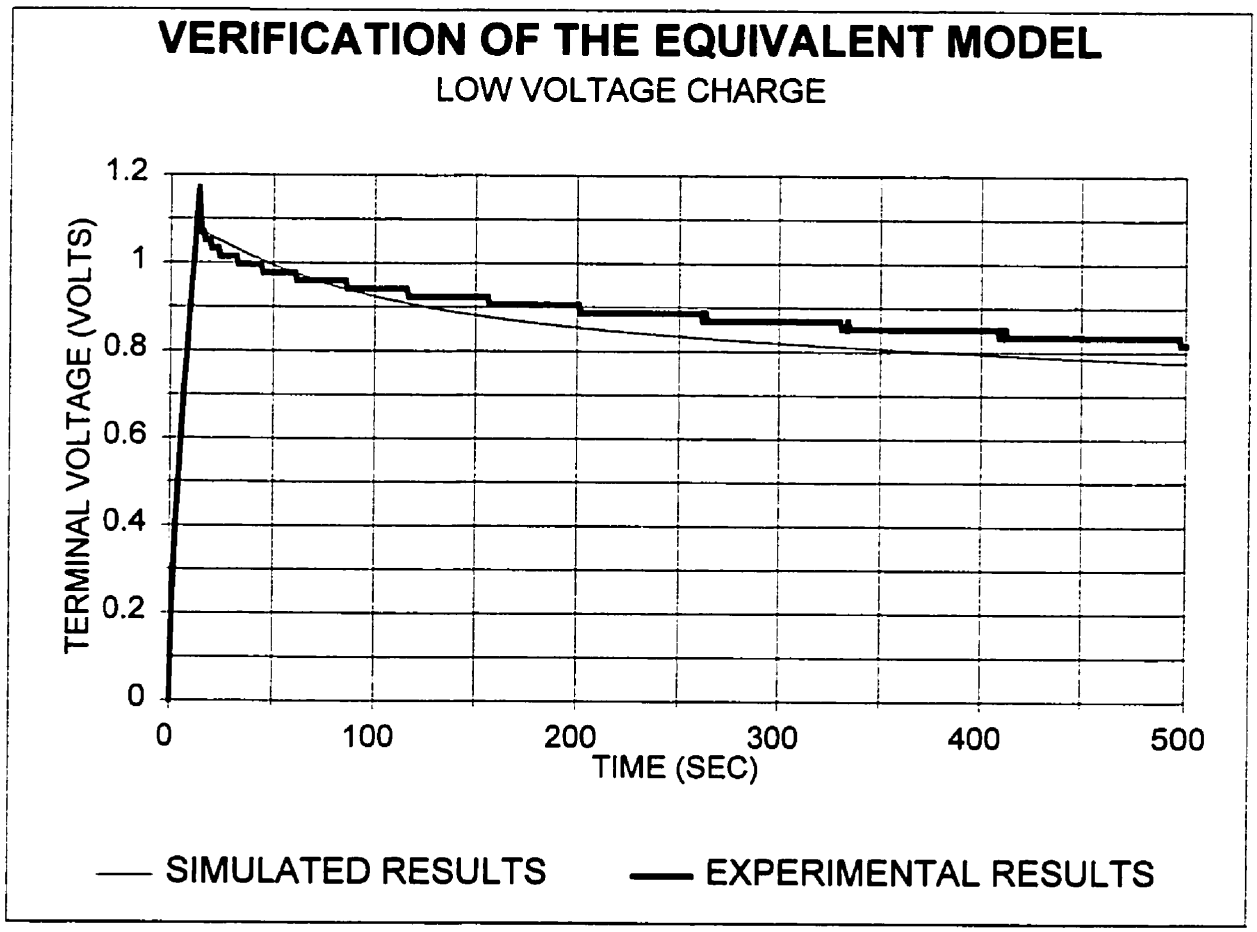


FIGURE 6.9 EQUIVALENT MODEL VERIFICATION. LOW VOLTAGE CHARGE.

CHAPTER 7

ENERGY CONSIDERATIONS

One of the most important aspects in the design of power electronics systems is the adequate use of the energy. The losses in the electronic devices represent energy that can not be transferred to the load and as a results is not useful in practice. Therefore, it is necessary to study the losses and energy efficiency inside the double-layer capacitor to complete the device characterization.

The energy study will be performed using the simulation software PSPICE. The simulation uses the equivalent model defined, calculated and verified previously. Different charge and discharge actions are applied to the model and the results are used to calculate power and energy. The study is divided in three parts; first, the losses in the capacitor equivalent model are calculated when a normal charge action is applied; second, the energy stored in the capacitor is calculated and some observations about the results are discussed; finally, a factor of energy utilization in a full charge cycle is determined.

7.1 DOUBLE-LAYER CAPACITOR LOSSES

As was concluded in previous chapters, the DLC presents an appreciable internal resistance given by the materials used in the device construction. This resistance produces losses every time that charge is fed into the capacitor. Even after the charge actions, when the internal charge distribution process is taking place, the flow of charges inside the capacitor produces additional losses.

The losses are studied by applying a charge action with constant current to the DLC model. The losses in each branch are calculated as

the product of the voltage and the current in the equivalent resistance of the correspondent branch.

$$P = V_{Rn} * I_n = I_n^2 * R_n \quad (7.1)$$

The charge action continues until the capacitor reaches the rated voltage. Then, the current is removed but the losses are calculated for a few more seconds in order to observe the losses during the internal charge distribution process.

Figure 7.1 shows the losses in each branch of the equivalent circuit during the charge action. As was expected, at the start of the charge action the losses occur mostly in the immediate branch because the resistance in that branch is much lower than in the other two and the current flows primarily through that branch.

As the terminal voltage is increased, more current flows through the other two branches, especially through the delayed branch, thus reducing the losses in the immediate branch. Therefore, the losses in the second and third branch are increased proportionally to the terminal voltage, and the losses in the immediate branch are reduced.

When the current is removed, the losses are reduced suddenly; that reduction is more appreciable in the immediate branch. However, some losses still occur as a result of the internal charge redistribution process. Those losses are higher in the delayed and long term branches because of the higher resistances in those branches.

Note that there is a section of the charge cycle in which the losses in the delayed branch are comparable and even greater than the losses in the immediate branch. If the capacitor is initially discharged, this interval is at the end of the charge cycle because

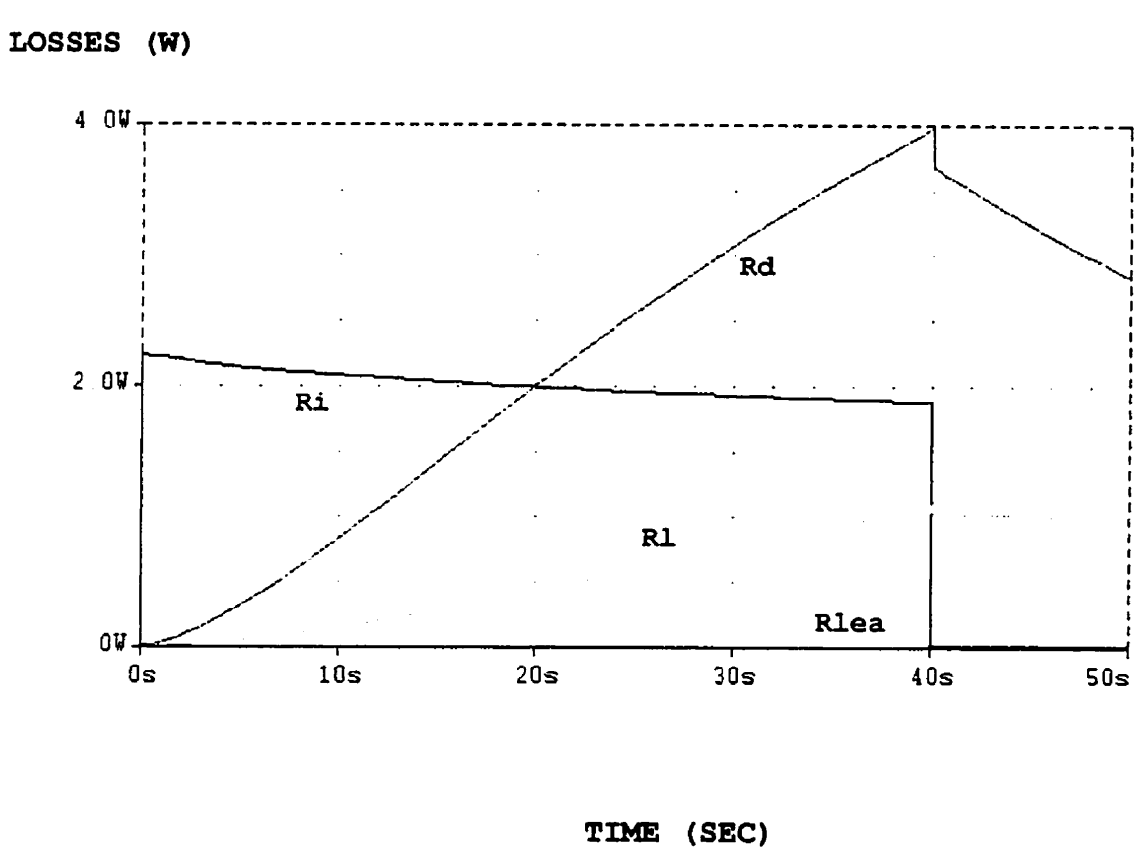


FIGURE 7.1 LOSSES PER BRANCH. CAPACITOR NORMALIZED

the difference in potential between the immediate and delayed branch is greater in that interval. Also note that the losses in the long term branch are about 40% of the losses in the immediate branch at the end of the charge cycle. The importance of the long term branch losses is higher during the self charge distribution process. On the other hand, the losses in the leakage resistance are very low and may be neglected in most cases.

If the capacitor has initially some charge stored in the delayed and long term branches, the curve of the losses will have modifications but still the three branches will have appreciable influence during some part of the charge action. Figure 7.2 present the losses for the same kind of charge action but this time the delayed and long term branches have been precharged to 50% of the rated voltage; the maximum losses in the delayed and long term branch have been reduced but now the losses in those branches are higher in the beginning of the charge action. In conclusion, the three branches should be always considered in any energy study even in high power applications.

The observation mentioned in the last two paragraphs give the indication that, if the specific application of the double-layer capacitors is limited to some range of voltage, then it is convenient to precharge the DLC to the middle point of the range of voltage to be used. In this form, the average difference of voltage of the delayed and long term branches with respect to the immediate branch is reduced and the losses in the delayed and long term branch are lower.

It is clear that the current level affects the total losses in the capacitor. However, this effect occurs mainly in the immediate branch because the current in the delayed and long term branches is

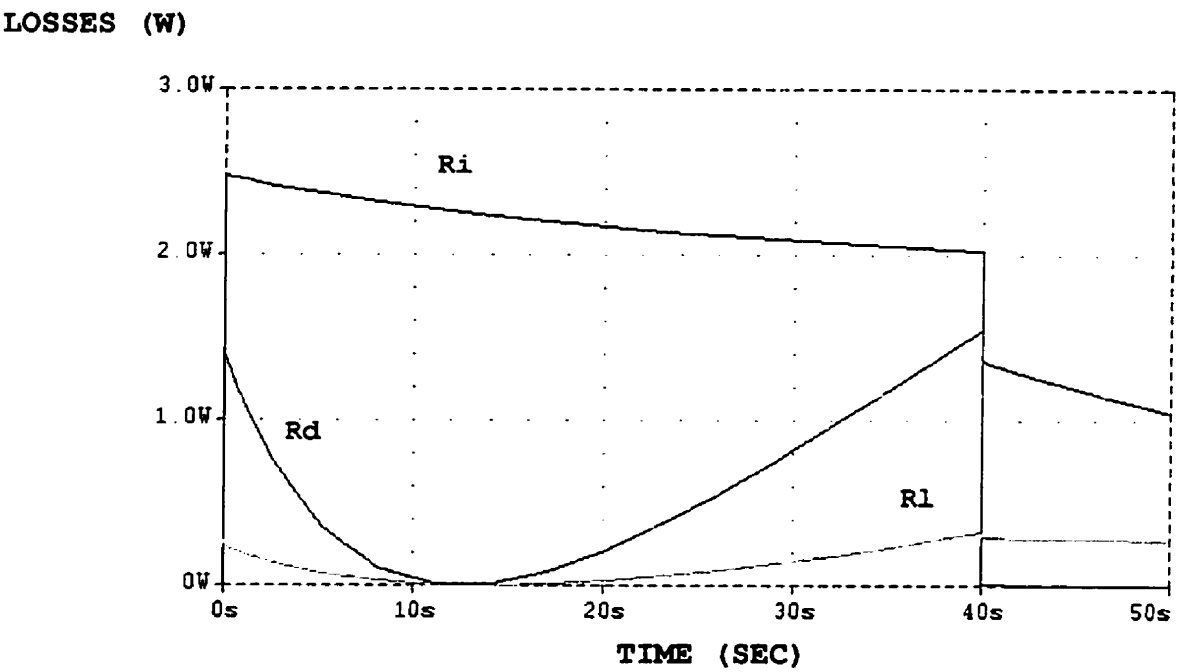
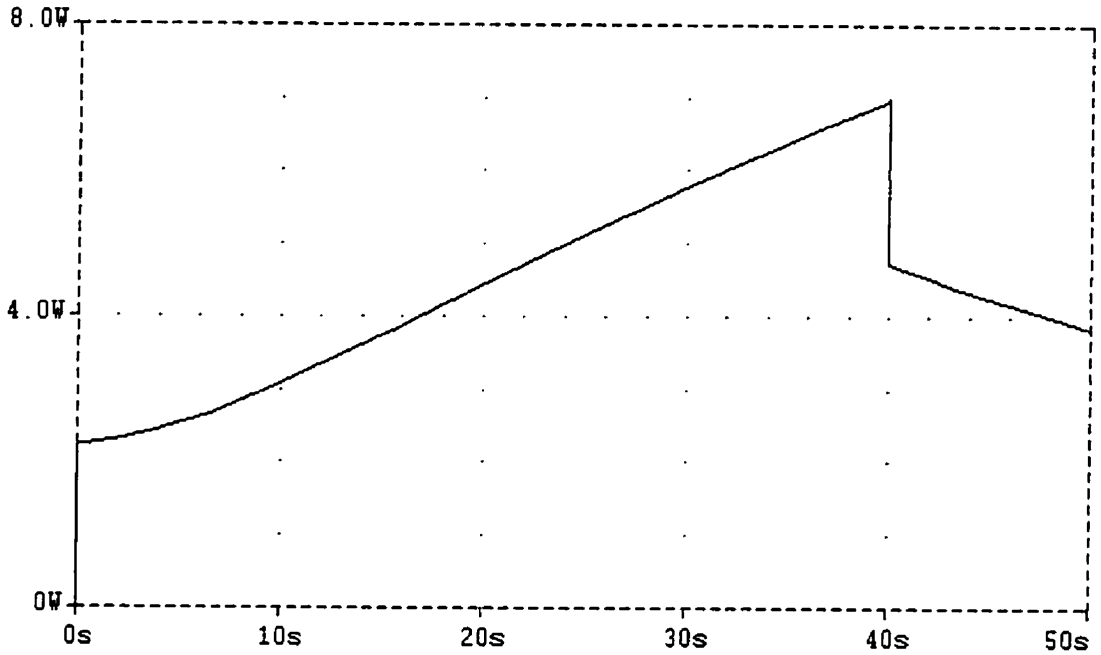


FIGURE 7.2 LOSSES PER BRANCH CAPACITOR PRECHARGED TO 1.2 V.
I = 30 AMP

LOSSES (W)



TIME (SEC)

FIGURE 7.3 TOTAL LOSSES IN A SINGLE CHARGE CAPACITOR NORMALIZED I = 30 AMP

given by the terminal voltage of the capacitor and not for the external current source.

Figure 7.3 represents the total losses during the charge action of a normalized capacitor. It can be seen that the losses under these conditions are higher at the end of the charge process.

Also it is convenient to compare the losses in the DLC with the losses in the electrolytic power capacitor presented in chapter one. In a double-layer capacitor charged with 30 Amp the maximum losses are lower than 8 W. The electrolytic capacitor, used for comparison in table 1.1, has a rated internal series resistance of 0.044 Ω ; this value gives about 30 W in losses if the device is charged with the same current used in the DLC simulation. That is about 4 times the maximum losses in the DLC charge cycle.

7.2 ENERGY IN THE IMMEDIATE BRANCH OF THE DOUBLE-LAYER CAPACITOR

The energy delivered to the DLC is initially stored in the immediate branch, and then is transferred to the delayed and long term branches. However, the energy that may be removed quickly from the capacitor is limited to the energy stored in the immediate branch. Therefore, it is important to know the amount of energy and the energy distribution in the immediate branch.

The energy introduced in the capacitor is given by the integral of the power during the time of charge and is defined by the following expression:

$$E = \int_0^t p(t)\,dt = \int_0^t v_t(t)\,i(t)\,dt \quad (7.2)$$

If the charge current is constant, equation 7.2 results in:

$$E = \int_0^t v_t(t)\,I\,dt \quad (7.3)$$

From the definition of differential capacitance the following relation for the immediate branch is deduced:

$$C(Vci) = \frac{dQ}{dVci} = \frac{I\,dt}{dVci} \Rightarrow I\,dt = C(Vci)\,dVci \quad (7.4)$$

And the terminal voltage v_t for a constant charge current is related to the immediate branch capacitance voltage Vci by the following relation:

$$v_t(t) = Vci + IRi \quad (7.5)$$

Substituting equation 7.4 and 7.5 into 7.3 the total energy supplied to the capacitor as function of the immediate capacitance voltage is calculated:

$$E = \int_0^{Vci} C(Vci)\,Vci\,dVci + \int_0^{Vci} IRi\,C(vci)\,dVci \quad (7.6)$$

The second term in the last equation represents the energy dissipated in the internal resistance and the first term the energy stored in the capacitor.

Solving the first integral in equation 7.6 for an arbitrary voltage Vci with C(Vci)= Cio+Ci1*Vci gives the following equation:

$$E = Cio\frac{Vci^2}{2} + Ci1\frac{Vci^3}{3} \quad (7.7)$$

The last equation is used to calculate the energy stored in the

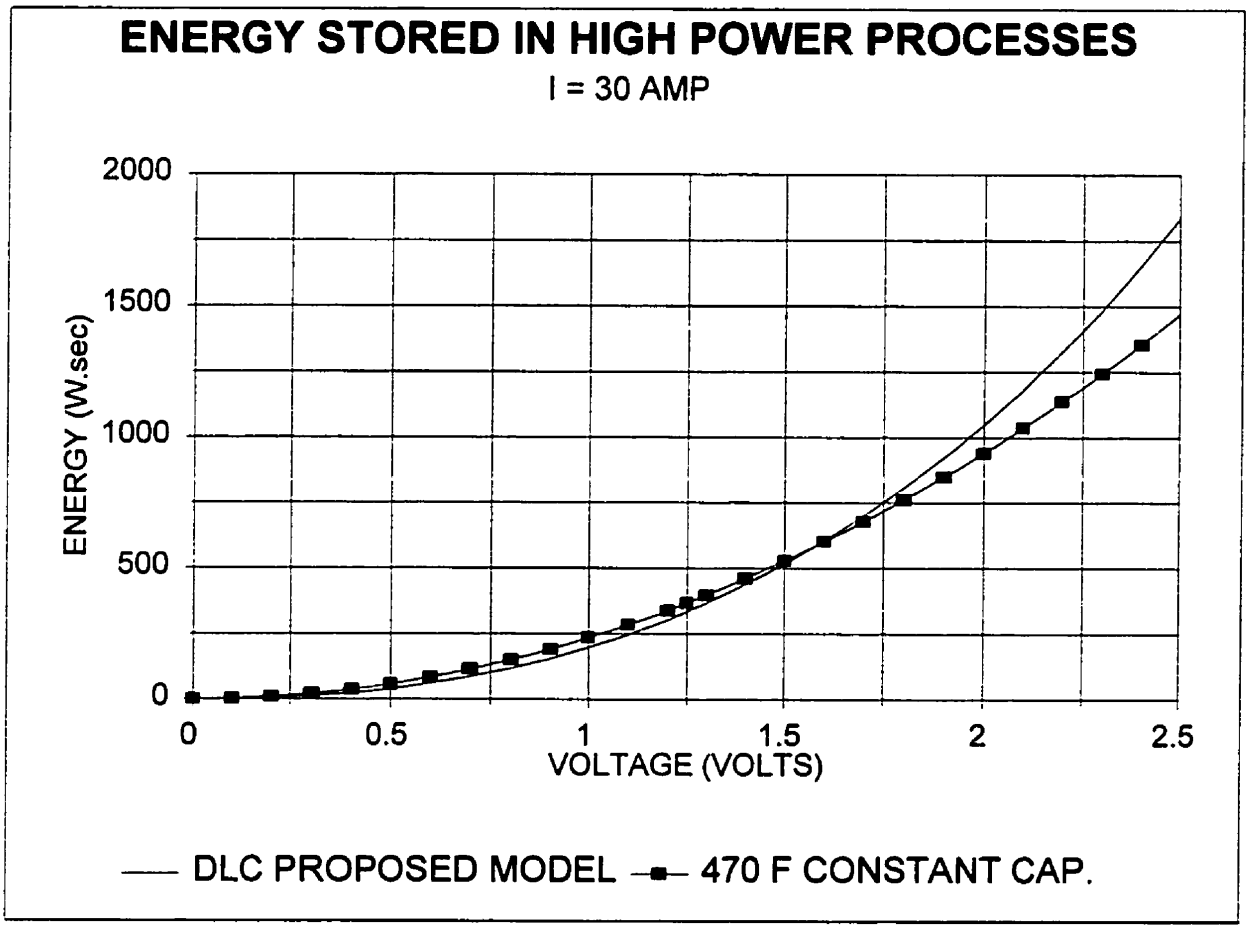


FIGURE 7.4 ENERGY STORED IN HIGH POWER CHARGE ACTIONS.

immediate branch capacitance at any voltage VCi.

Figure 7.4 presents the curve of energy vs voltage for the DLC. In this figure, the curve of energy for a capacitor with constant capacitance of 470 F (rated value) has been included. Two important conclusion result from this figure: first, the real energy stored in the double-layer capacitor at 2.5 volts is 25% higher than the theoretical energy calculated using the rated capacitance. Second, the energy is stored mainly at the higher voltage levels of the DLC. This is an important conclusion because if the capacitor is discharged up to 50% of the initial voltage, the energy that is removed from the capacitor is 81.72% from the total immediate branch energy and not the 75% that is calculated using the constant 470 F model.

7.3 ENERGY INTERCHANGE DEFINITION

The definition of efficiency for this kind of device in which time constants in the order of hours are present is not simple. The capacitor may be charged and immediately discharged or some time may elapse between the charge and discharge actions; in addition, the capacitor may be initially discharged or may have some charge in the delayed and long term branches. Therefore, the efficiency is a function of the time and this factor should be considered.

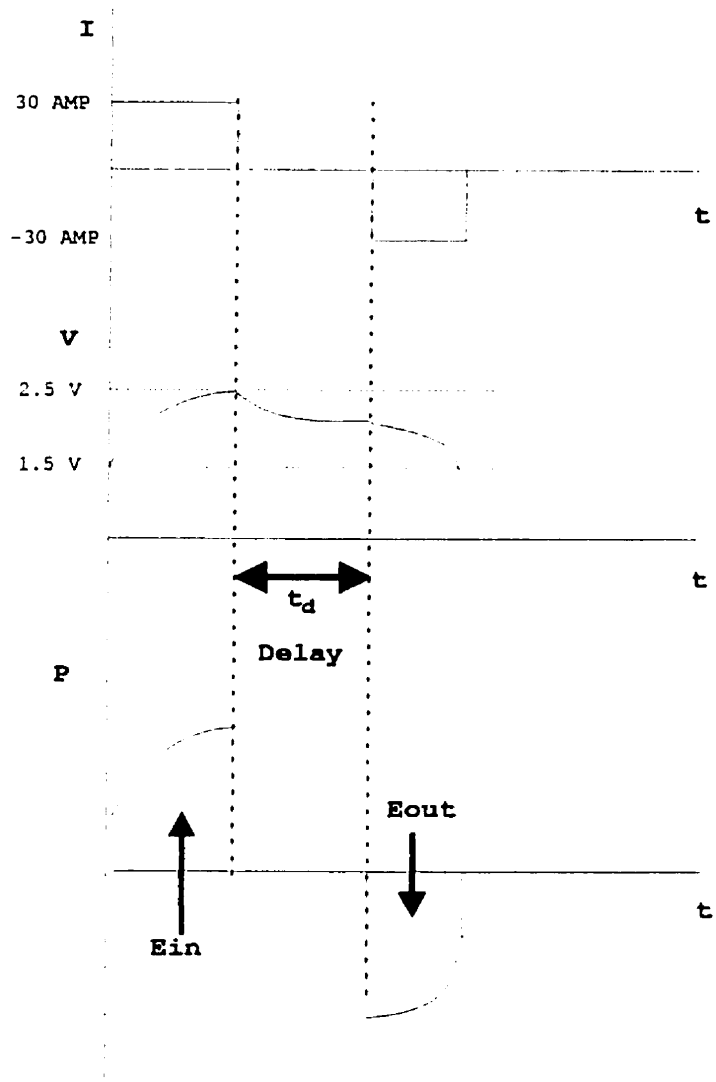
A definition of efficiency for high current charge and discharge processes is now proposed. Although the study does not go deep in the consideration of all possible factors affecting the devices efficiency, this definition provides a basic information for power electronics applications.

The energy interchange cycle consists of three parts: First, the DLC is precharged to 1.5 volts using a constant current until the

terminal voltage reaches 2.5 volts. Second, a time delay, which is taken as a parameter, passes without any current application. Third, after the delay time, the capacitor is discharged up to 1.5 volts with a current value equal to the one used in the charge. The ratio between the energy taken out of the capacitor and the energy previously introduced represents the energy utilization for this specific delay. This definition is used to study the high power energy utilization of the capacitors in the range of application for power electronics.

It is clear that the energy utilization factor calculated using this definition is not given only by the losses inside the capacitor, but the definition indicates the percentage of energy that may be used in a fast discharge action. The energy interchange also depends on other factors such as changes in the initial charge stored in the capacitor and range of charge voltage swept in the charge action, those factors are not studied in this research.

Figure 7.5 represents the graphical explanation of the energy interchange definition. Figure 7.6 shows the calculated energy interchange as a function of the delay for three different charging currents. As was expected, for higher current the energy interchange is lower because of the increase in the immediate branch losses. Also note the reduction in the energy interchange as the time delay is increased; this reduction is because of the energy transferred to the delayed and long term branches.



$$E = \int P \, dt$$

Energy Interchange Factor = (Ein /Eout)*100

FIGURE 7.5 ENERGY INTERCHANGE DEFINITION

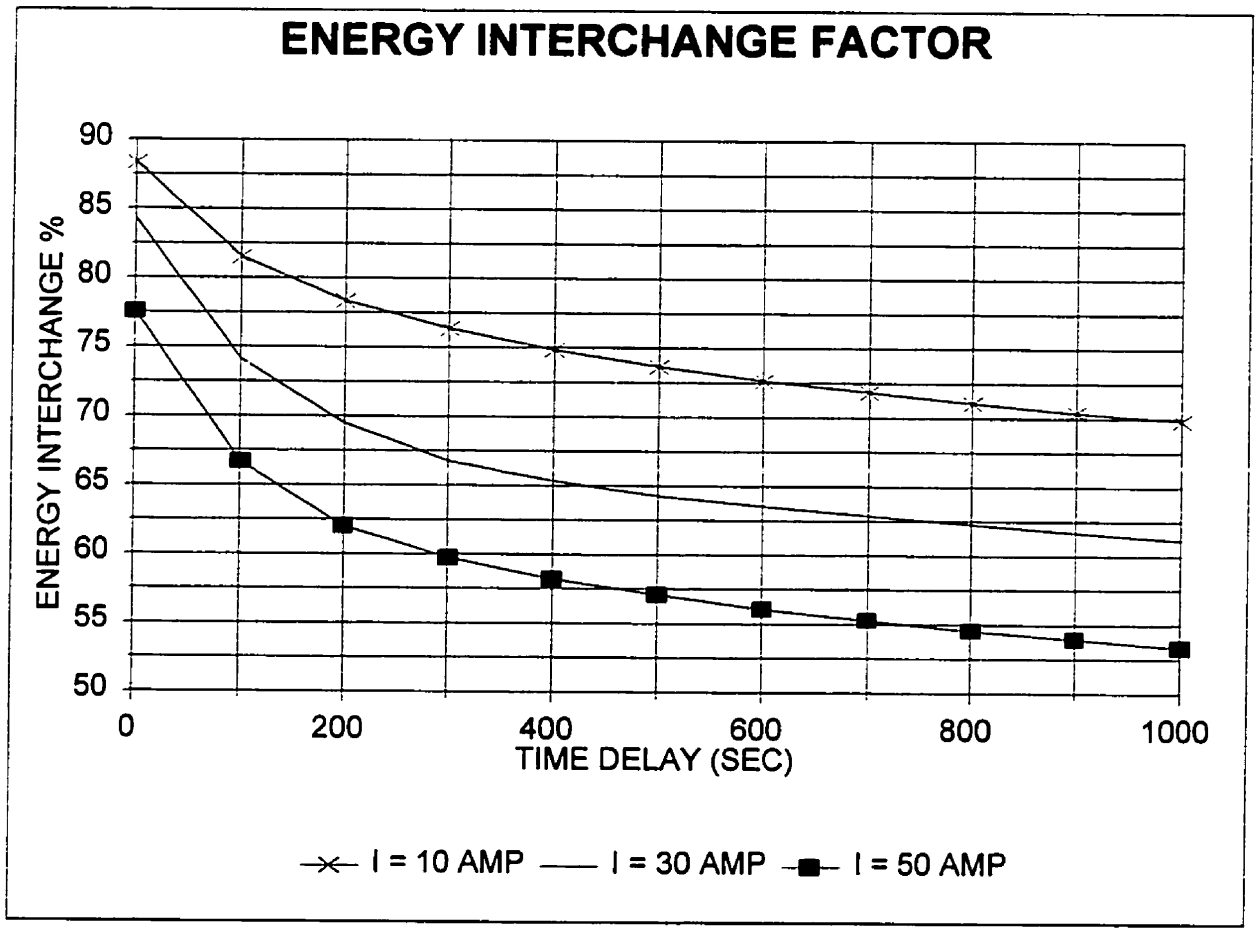


FIGURE 7.6 ENERGY INTERCHANGE FACTOR VS TIME DELAY.

CHAPTER 8

SERIES CONNECTION PERFORMANCE

The low rated voltage of the PANASONIC double-layer capacitors makes the series connection one necessary step in order to reach higher voltages. The use of capacitors in series extends the possible applications of the DLC's and it also produces a more versatile energetic device.

The series connection study will give conclusions about how far apart the practical response and the equivalent model parameter values of several similar devices are. Ten capacitors rated 470 F are connected in series and several tests are applied to them.

The results presented in this chapter make it possible to decide how simple is the utilization of double-layer capacitors connected in series and what differences in the performance among capacitors are expected when the capacitors are connected in series.

The study includes four different tests. Each one should reveal the relative differences among some of the equivalent model parameters of the ten DLC's.

8.1 FAST CHARGE TEST

This test has as its objective the study of the differences in the parameters of the immediate branch among the ten capacitors connected in series. As the immediate branch has a time constant in the order of a few seconds, the response of this branch is observed through the application of a high charging current. A current of 30 amperes is applied to ten normalized double-layer capacitors connected in series and the voltage in each capacitor is sensed frequently. In

this way, the voltage drift among the ten capacitors can be observed. The charging process continues until the terminal voltage across any capacitor reaches the rated value. This test permits one to observe the voltage differences across all range of voltages.

Figure 8.1 shows the plot of the voltage in each capacitor as a function of the time. The figure shows that the difference between the capacitor with the highest and the lowest voltage is less than 10 per cent of the rated voltage at any instant of the charging action. This result was expected from the results presented in chapter five that presented differences amongst capacitors lower than 10% in the equivalent model parameter values. A voltage difference lower than 10% is an acceptable result that gives the impression that the capacitors can be connected in series without any external device and without important disequilibrium in the voltages. However, it is important to verify if the differences in the parameter values of the other two branches produce an increase in the voltage drift among capacitors when several charge and discharge actions are applied to the capacitors.

8.2 TEN CONSECUTIVE CYCLES TEST

In order to observe the possible differences amongst the parameter values of the delayed branch, ten consecutive cycles of charge and discharge between -10% of the rated voltage and the rated voltage are applied to ten normalized double-layer capacitors connected in series. As the delayed branch has a time constant of approximately 90 seconds, its effect is observable in the ten charge and discharge cycles. The total duration of the test is more than 5 minutes

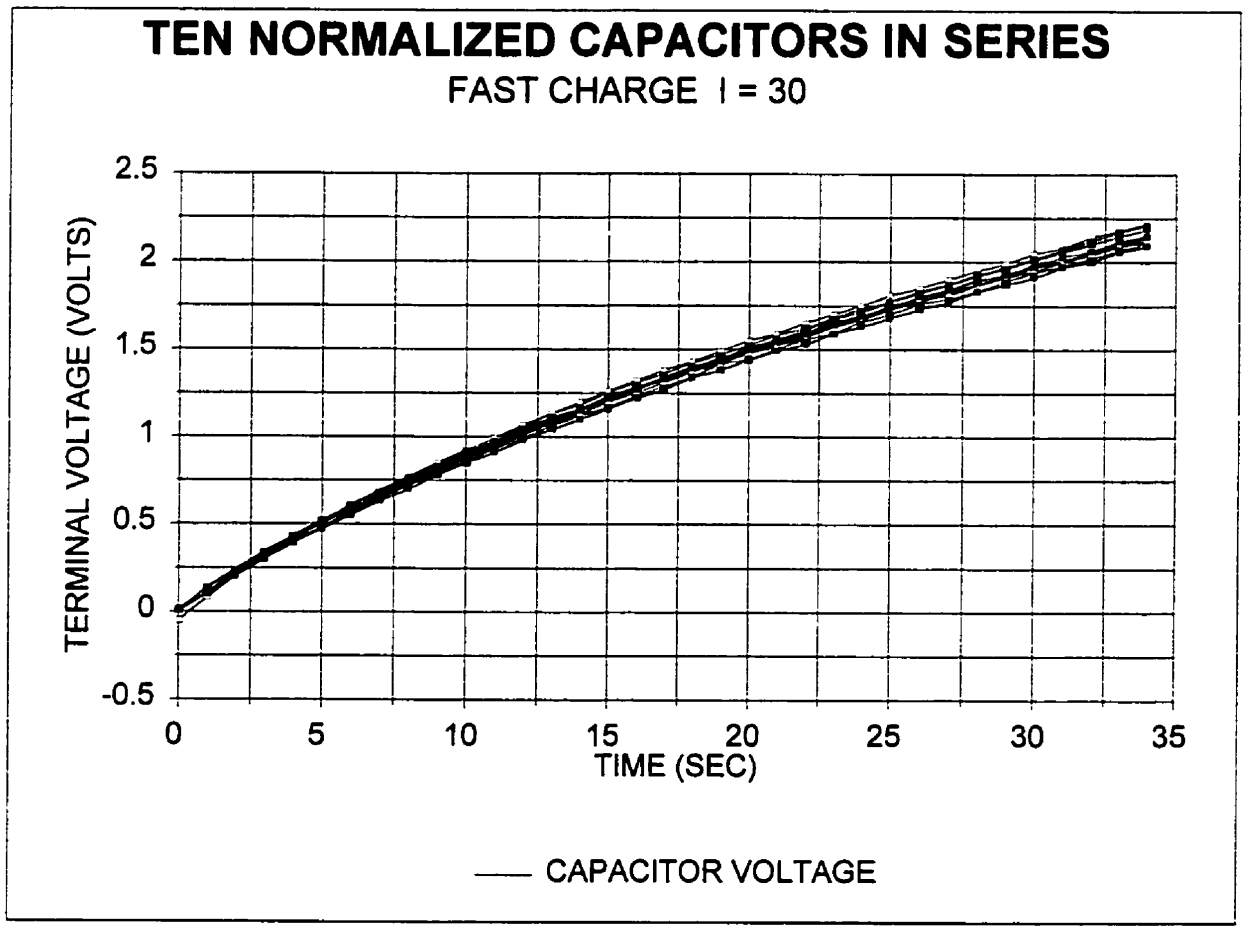


FIGURE 8.1 VOLTAGE DRIFT AMONG NORMALIZED CAPACITORS IN SERIES.

Table 8.1 represents the voltage across each capacitor at each positive and negative peak and the percentile difference of voltage between the capacitor with the highest and the lowest voltage. The percentage is calculated using the DLC rated voltage as a base through the following relation:

$$\%Drift = \frac{V_{highest} - V_{lowest}}{V_{rated}} * 100 \quad (8.1)$$

That table leads to two important conclusions: first, the difference in voltage amongst the capacitors is not increased appreciably in the subsequent cycles. Second, the difference in voltages are always lower than 10% of the rated voltage.

In other words, after 10 complete cycles of charge and discharge the capacitors are still behaving very close in their response to the charging action.

8.3 FIVE HUNDRED CONSECUTIVE CYCLES TEST

This study has as its purpose the study of the differences in the long term parameters of the double-layer capacitors. Five hundred charge and discharge cycles with 45 amperes are applied to ten normalized capacitors and the difference in the voltage amongst the ten capacitors is measured. Table 8.2 presents the results of this test at five different instants of the experiment. The table presents the voltages of the ten capacitors measured each hour after the start of the experiment; in addition, the last column indicates the DLC voltages after 500 cycles. The total duration of the experiment is 5 hours and 37 minutes.

Again the results are favourable as the difference in voltage among the capacitors not only is not increased in additional cycles

CYCLE	CAP1	CAP2	CAP3	CAP4	CAP5	CAP6	CAP7	CAP8	CAP9	CAP10	% OF DRIFT
0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.5	2.10	2.12	2.11	2.14	2.12	2.20	2.16	2.18	2.14	2.14	4.35
1	-0.24	-0.20	-0.23	-0.26	-0.24	-0.28	-0.26	-0.23	-0.26	-0.24	3.48
1.5	2.16	2.14	2.15	2.15	2.15	2.20	2.19	2.23	2.15	2.14	3.91
2	-0.24	-0.20	-0.23	-0.26	-0.24	-0.27	-0.27	-0.22	-0.28	-0.24	3.48
2.5	2.12	2.16	2.13	2.16	2.16	2.21	2.17	2.20	2.15	2.15	3.91
3	-0.24	-0.21	-0.25	-0.28	-0.24	-0.28	-0.29	-0.23	-0.29	-0.26	3.48
3.5	2.12	2.17	2.13	2.16	2.16	2.21	2.17	2.19	2.15	2.16	3.91
4	-0.24	-0.21	-0.25	-0.28	-0.25	-0.28	-0.29	-0.22	-0.30	-0.25	3.91
4.5	2.13	2.11	2.11	2.12	2.12	2.18	2.16	2.19	2.11	2.12	3.48
5	-0.22	-0.20	-0.23	-0.26	-0.22	-0.26	-0.27	-0.19	-0.28	-0.23	3.91
5.5	2.08	2.14	2.09	2.12	2.12	2.17	2.13	2.16	2.10	2.12	3.91
6	-0.23	-0.19	-0.23	-0.26	-0.24	-0.27	-0.23	-0.18	-0.24	-0.17	4.35
6.5	2.12	2.15	2.13	2.15	2.15	2.20	2.20	2.21	2.13	2.14	3.91
7	-0.19	-0.17	-0.20	-0.23	-0.20	-0.24	-0.25	-0.18	-0.27	-0.21	4.35
7.5	2.10	2.14	2.10	2.13	2.12	2.17	2.18	2.20	2.10	2.13	4.35
8	-0.18	-0.15	-0.18	-0.21	-0.18	-0.23	-0.24	-0.20	-0.26	-0.19	4.78
8.5	2.11	2.14	2.10	2.13	2.12	2.16	2.23	2.19	2.09	2.12	6.09
9	-0.18	-0.17	-0.18	-0.22	-0.18	-0.24	-0.24	-0.14	-0.26	-0.20	5.22
9.5	2.11	2.14	2.12	2.14	2.14	2.18	2.20	2.24	2.12	2.13	5.65
10	-0.21	-0.17	-0.22	-0.25	-0.22	-0.24	-0.22	-0.18	-0.24	-0.24	3.48

but in fact is reduced. In other words, the experiment leads one to conclude that the differences in the parameters values of the first two branches are balanced by the differences in the parameters of the long term branch.

CAPACITOR NUMBER	1 HOUR	2 HOUR	3 HOUR	4 HOUR	500 CYCLES
1084	2.04	1.19	1.73	0.65	70 mV
1226	2.06	1.21	1.73	0.64	65 mV
1100	2.08	1.22	1.74	0.64	60 mV
1156	2.03	1.19	1.71	0.63	58 mV
1192	2.06	1.20	1.72	0.63	51 mV
1066	2.10	1.24	1.75	0.64	58 mV
1193	2.04	1.19	1.70	0.62	54 mV
1090	2.09	1.23	1.72	0.61	50 mV
1074	2.02	1.18	1.72	0.64	61 mV
1151	2.05	1.20	1.72	0.62	55 mV

TABLE 8.2

The three previous experiments have studied the voltage drift amongst capacitors in the short, medium and long term. During no instant of the almost six continuous hours of charge and discharge did the differences reach values that would indicate appreciable disequilibrium in the performance of the different capacitors.

However, those experiments were applied to normalized double-layer capacitors, the next section present the results of experiments with non-normalized capacitors.

8.4 SERIES CONNECTION OF NON-NORMALIZED CAPACITORS

The fast charge experiment and the ten cycle experiment were repeated with no normalized capacitors; that is, with capacitors that have differences in their initial voltage. The differences in initial voltage amongst capacitors were limited to 20% of the rated voltage.

Figure 8.2 presents the results of the fast charge test. This figure indicates that the initial differences amongst voltages has not been increased during the charge cycle.

The results of the ten cycles of charge and discharge also confirms that the differences amongst voltages in the following cycles have not increased.

8.5 SERIES CONNECTION SELF-CHARGE DISTRIBUTION TEST

The three previous series test showed that the difference in voltage amongst any pair of capacitors is lower than 10% under different number of charge actions. However, it is important to verify if the same results are produced in the self charge distribution process internal to the DLC.

Ten normalized capacitors are charged to a voltage of 2.2 volts, and the voltage in each one is measured frequently during several minutes after the charging action. As was expected, the voltage fell down as a result of the internal distribution of the charge. Table 8.3 indicates the voltage in each capacitor at several instants after the charge.

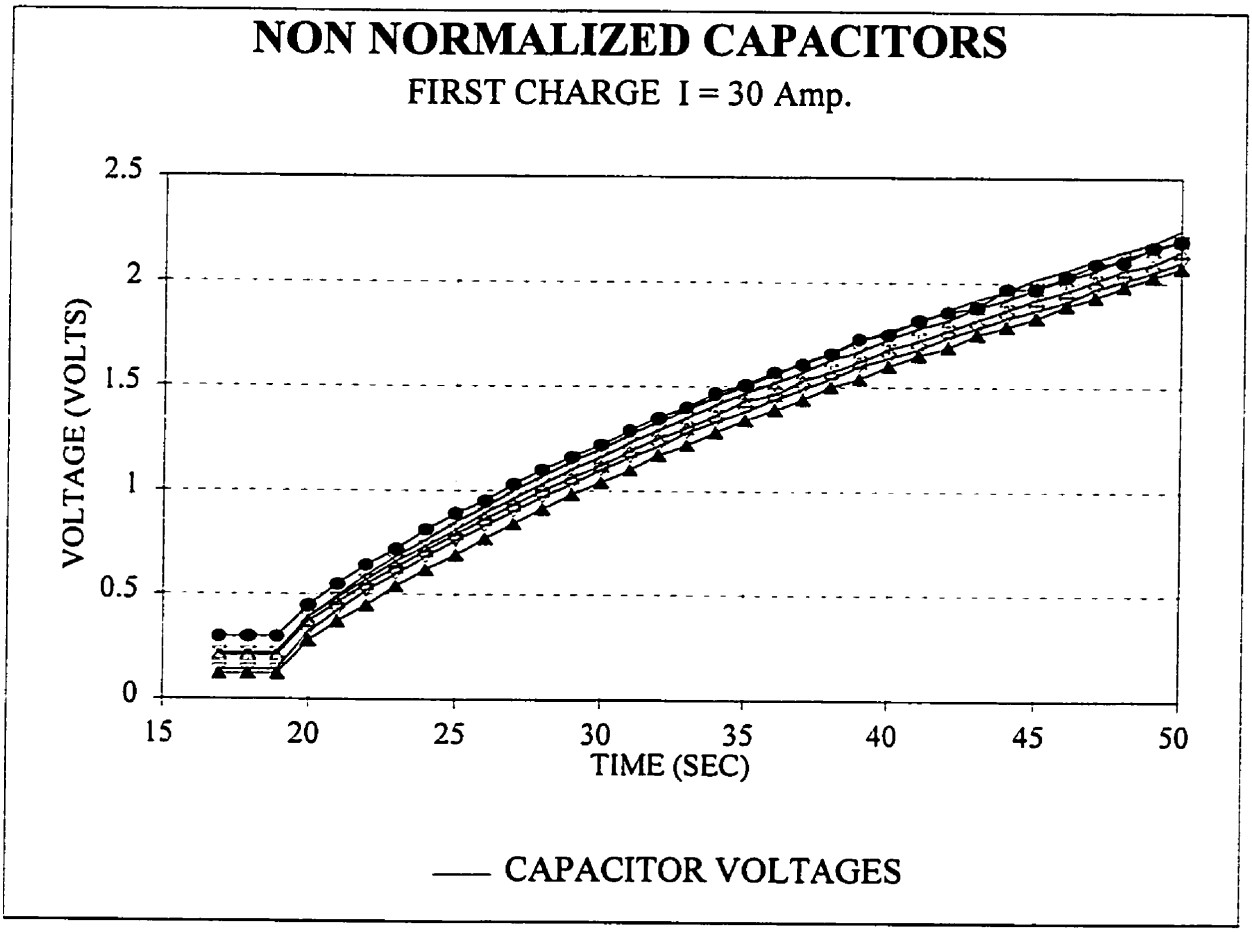


FIGURE 8.2 VOLTAGE DRIFT AMONG NON-NORMALIZED CAPACITORS IN SERIES.

CAP #	15 min	30 min	45 min	75 min	120 min
1084	1.562	1.452	1.421	1.378	1.298
1226	1.608	1.506	1.480	1.438	1.323
1100	1.597	1.493	1.465	1.419	1.307
1156	1.585	1.480	1.446	1.395	1.313
1192	1.531	1.412	1.374	1.316	1.286
1066	1.572	1.451	1.413	1.353	1.299
1193	1.557	1.448	1.398	1.310	1.259
1090	1.550	1.426	1.379	1.337	1.265
1074	1.560	1.437	1.405	1.351	1.280
1151	1.534	1.459	1.406	1.318	1.271

TABLE 8.3

This table indicates that no higher differences in voltage are produced during the self charge distribution process. In fact, the highest difference in voltage is still less than 10% of the rated voltage.

In conclusion, no indication of appreciable differences amongst capacitors connected in series were observed in several different experiments. Those experiments involved short, medium and long time tests as well as the internal charge redistribution process.

CHAPTER 9

CONCLUSIONS

The characterization of the PANASONIC double-layer capacitors was performed and the thesis objectives were satisfied. The following conclusions can be stated:

- The double-layer capacitors present several advantages with respect to the traditional electrolytic capacitors, thus making these devices attractive in the power electronics field.

- The physics of the double layer, which is based on the double-layer capacitor effect, justifies the selection of a more complex equivalent model instead of a simple capacitance-resistance series element.

- An equivalent model composed of capacitors, resistors and inductors and based on the physics of the double-layer and in experimental considerations may be used to represent the double-layer capacitor. This model is composed of three RC branches connected in parallel, one leakage resistance and one input inductance.

- The equivalent model parameters are identified throughout the measurement of the two electrical accessible variables of the double-layer capacitor: terminal voltage and current. Therefore, the equivalent model is based on the terminal behavior of the capacitor and may be easily recalculated any time.

- The double-layer capacitor time behavior can be represented by independent sections in the equivalent model. Based on the above fact, a repeatable and unambiguous procedure for the parameters identification was proposed and automatized.

- The physics of the double-layer suggests that the

capacitance of the device is voltage dependant. To keep the model simple, only the immediate branch is voltage dependant and its value is increased linearly with an increase in the terminal voltage.

- The delayed and long term capacitances, whose energy may not be used in high power applications, have together a value comparable with the fixed capacitance of the immediate.

- The equivalent model was verified using simulation tools and was found to be in agreement with experimental results. An error under 3% of the rated voltage for up to 30 minutes simulations was found. However, it is necessary to emphasize that the model is designed for power electronics applications and it follows with greater accuracy the capacitor response for a voltage higher than 50% of the rated value and for up to 30 minutes. For lower voltages or a longer time, the differences between experimental and simulated response increases.

- The differences in the parameter values among several double-layer capacitors are lower than 10% of the average parameter value. Therefore, good consistency in the electrical characteristics exists between similar devices.

- The losses in the three RC branches of the equivalent model should be considered in any energy study because in a complete charge cycle the three losses have an appreciable effect.

- The total energy that may be stored in the immediate branch of the double-layer capacitor is higher than the indication given by the rated capacitance value. In addition, because of the linear increase of the capacitance with the voltage most of the energy is stored at the higher voltage levels.

- An interchange of energy definition was proposed. This

definition is a function of the time and indicates the ratio of the energy introduced in the capacitor that may be used in high power applications.

- The series connection of double-layer capacitors was studied through the connection of ten cells to obtain a 23 volts, 47 F capacitor. The voltage drift amongst capacitors was lower than 10% of the rated voltage at any instant of the 500 charge and discharge cycles.
- If the double-layer capacitors connected in series have small differences in their initial voltages, those differences are not appreciably increased in successive charge and discharge cycles.
- The energy interchange factor decreases as the delay between the charge and the discharge is increased because of the charge redistribution inside the capacitor.

The double-layer capacitors have been characterized with an accurate but still simple terminal model. The model appears to be adequate for most of the power electronics applications. Further studies should be directed to the design of specific applications using the double-layer capacitors. Another field of interest may be a more deep study of the efficiency inside the devices. However, a more adequate energy study depends on the specific application because of the many factors involved in the DLC efficiency.

If for some specific application the developed model results are insufficient, it may be extended to a greater number of branches and/or capacitance dependency on the voltage for all the branches. However, this focus will result in a much more complex model and a more complicated and inexact parameter identification procedure.

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APPENDIX A

APPENDIX B

SOFTWARE AND HARDWARE DESIGN DETAILS

B.1 FILTER DESIGN

Chapter four presented the test facility used in the double-layer capacitor test. The current waveform is a triangular wave with a frequency of 4 kHz. This frequency is equal to the switching frequency used in the DC/DC converter. However, the time needed to read the analog inputs makes it impossible to use the same frequency for the sampling process. The analog to digital sampling frequency used is 500 Hz. Therefore, the analog to digital conversion does not satisfy the sampling theorem and the current value sampled may not represent the average current in the system. This factor makes it necessary to use an anti-aliasing filter in the signal measured at the sensor before the sampling and digital conversion process.

The filter should be designed to attenuate the ripple frequency (4 kHz) and to limit the attenuation of the sampling frequency (500 Hz). The structure of the second order filter is shown in the figure B.1.

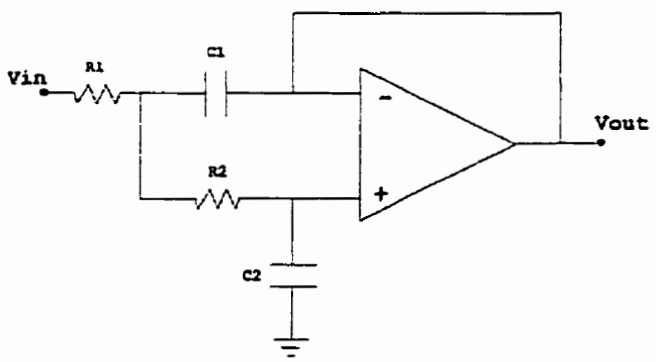


FIGURE B.1 FILTER SCHEMATIC

The natural frequency of that circuit is given by:

$$\omega_o = \frac{1}{\sqrt{R1*R2*C1*C2}} \quad (B.1)$$

And the damping constant is given by:

$$d = \omega_o * C2 * (R1+R2)/2 \quad (B.2)$$

The damping of the filter should be selected in such way that the gain at the sampling frequency is one and the attenuation at 4 kHz is as large as possible. Figure 5.2 presented the Bode plot for the filter response with fo = 500 Hz and d = 0.45. In that figure it can be seen that at 500 Hz the gain is close to 0 DB and the attenuation at 4 kHz is 10^{-4} DB.

Using the equations for the damping and taking R1 = R2 = 33 KΩ C2 can be calculated: C2= 4.34 nF.

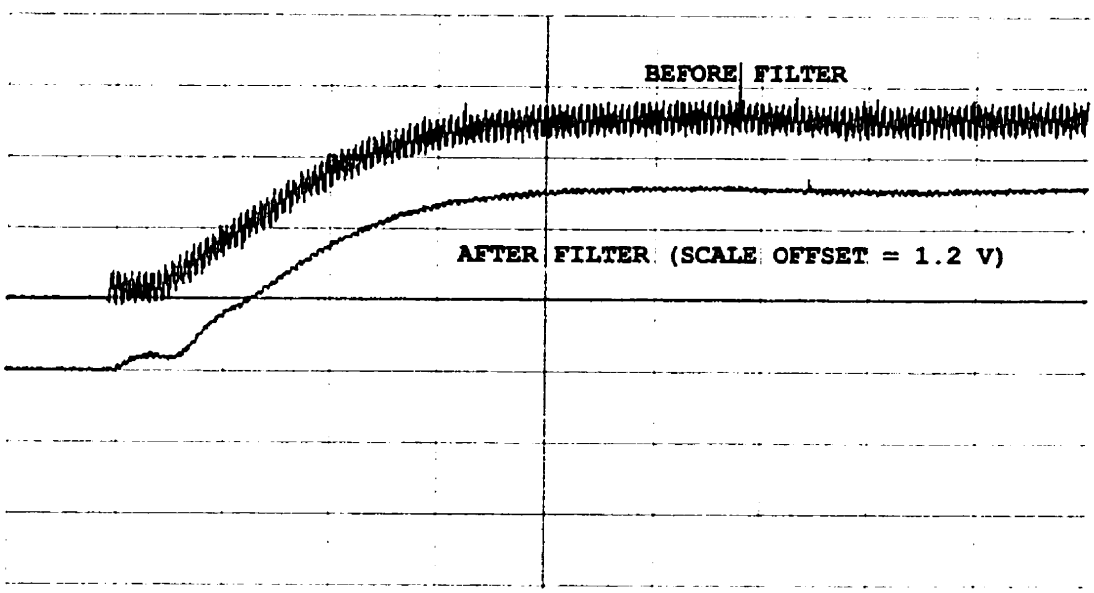
Using the equation of ωo and the values previously defined, the value of C1 can be calculated: C1 = 21.44 nF.

The commercial values used are C2 = 4.7 nF and C1= 20 nF.

Figure B.2 shows the current waveform before and after the filter.

B.2 CURRENT CONTROL

In a DC/DC converter, the average DC output voltage is controlled by the switch on and switch off interval durations. The method used for controlling the output voltage is switching at constant frequency, and adjusting the duration of the on state to control the average output voltage. Figure B.3 shows the basic pulse width modulation operation for two different output voltages. There can be seen that a control signal proportional to the desired average output should be



TIME BASE = 4 msec/div VOLTAGE BASE = 1.2 V/div

FIGURE B.2 CHARGE CURRENT BEFORE AND AFTER THE FILTER.

used as an input.

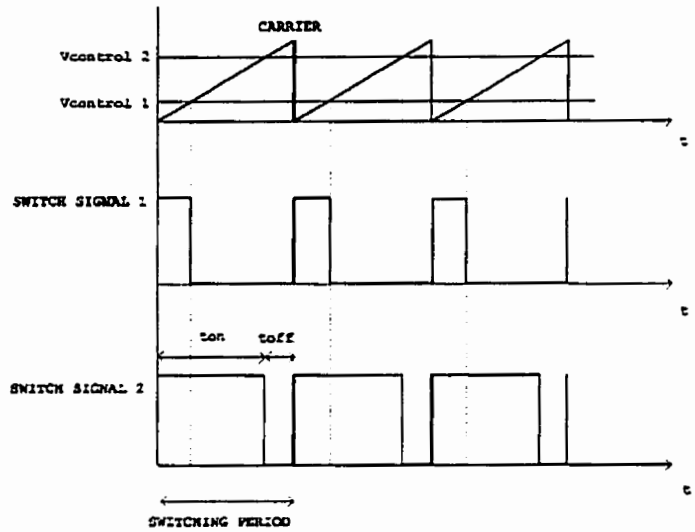


FIGURE B.3 PULSE WIDTH MODULATION

The control board, used in the DLC tests, gives the possibility of doing a PWM control giving as input only the control signal. As a current control is the goal, the current flowing through the circuit is measured and compared with a reference. Using a proportional integral control, the control signal is generated and used to produce the PWM signals.

In a proportional-integral controller, the control signal is generated as the addition of two different terms; the first one is called the gain, and it is proportional to the error signal. The second one is the time related term which is proportional to the integral of the error over a fixed time. Therefore, the equation of a PI controller is given by:

$$u(t) = kp * e(t) + \frac{kp}{Tr}\int_{o}^{t} e(t)\,dt \quad (B.3)$$

where Tr is the time constant of the system and Kp is a constant. The last equation may be presented as a transfer function:

$$\frac{u}{e} = kp\left(1+\frac{1}{TrS}\right) \quad (B.4)$$

As the control is implemented using a digital system, the transfer function should be adjusted using a digital transformation. Here, the bilinear transformation is used:

$$S=\frac{2}{T_s}\frac{1-Z^{-1}}{1+Z^{-1}} \quad (B.5)$$

where Ts represents the sampling frequency of the digital system. Substituting equation B.5 in B.4 the following relation results:

$$\frac{u}{e} = kp+\frac{kpTs(1-Z^{-1})}{2Tr(1-Z^{-1})} \quad (B.6)$$

Transforming from the Z domain to the time domain the equation B.6 results in:

$$u(T) = kp\left(1+\frac{Ts}{2Tr}\right)e(T) - kp\left(1-\frac{Ts}{2Tr}\right)e(T-1) + u(T-1) \quad (B.7)$$

The last equation could be written in the following form:

$$u(T) = K1(e(T) - K2e(T-1)) + u(T-1) \quad (B.8)$$

In the last equation K1 and K2 are given by:

$$K2=\frac{\left(1-\frac{Ts}{2Tr}\right)}{\left(1+\frac{Ts}{2Tr}\right)} \quad (B.9)$$

$$K1=kp\left(1+\frac{Ts}{2Tr}\right) \quad (B.10)$$

In the hardware setup mentioned earlier Tr = 15 msec. In addition, the sampling period used in the setup is 2 msec.

Substituting the values of Ts and Tr in equation B.9, K2 results in:

$$K2 = 0.875 = E00_H \text{ (4.12 system)}$$

The value of K1 is chosen experimentally to get a monotonic current change. The best performance was observed with:

$$K1 = 0.64 = A3D$$

B.3 DATA ACQUISITION SOFTWARE

The data acquisition presented in chapter five is an automated system of voltage measurement needed to get repeatable and accurate results. The two constituent parts of the system are discussed in detail in the following pages:

B.3.1 *PC Data Collection Program*

The PC data collection program has three basic functions:

- Send, using the serial port, a mark to start the interchange of data.
- Collect the data sent by the controller board and save it in a structured way.
- Send, using the serial port, a mark to stop the interchange of data.

In order to fulfil those requirements, a program in PASCAL was developed. The program begins by opening the file in which the data is going to be saved; second, it initializes the serial port of the PC and enables it to interface with the controller board (GPC); third, the program starts the data collection by sending the ASCII code for the letter 'd' which should be understood for the GPC; then, the PASCAL software starts to collect the ASCII codes received from the GPC, checks the received value for errors and if it is correct, saves

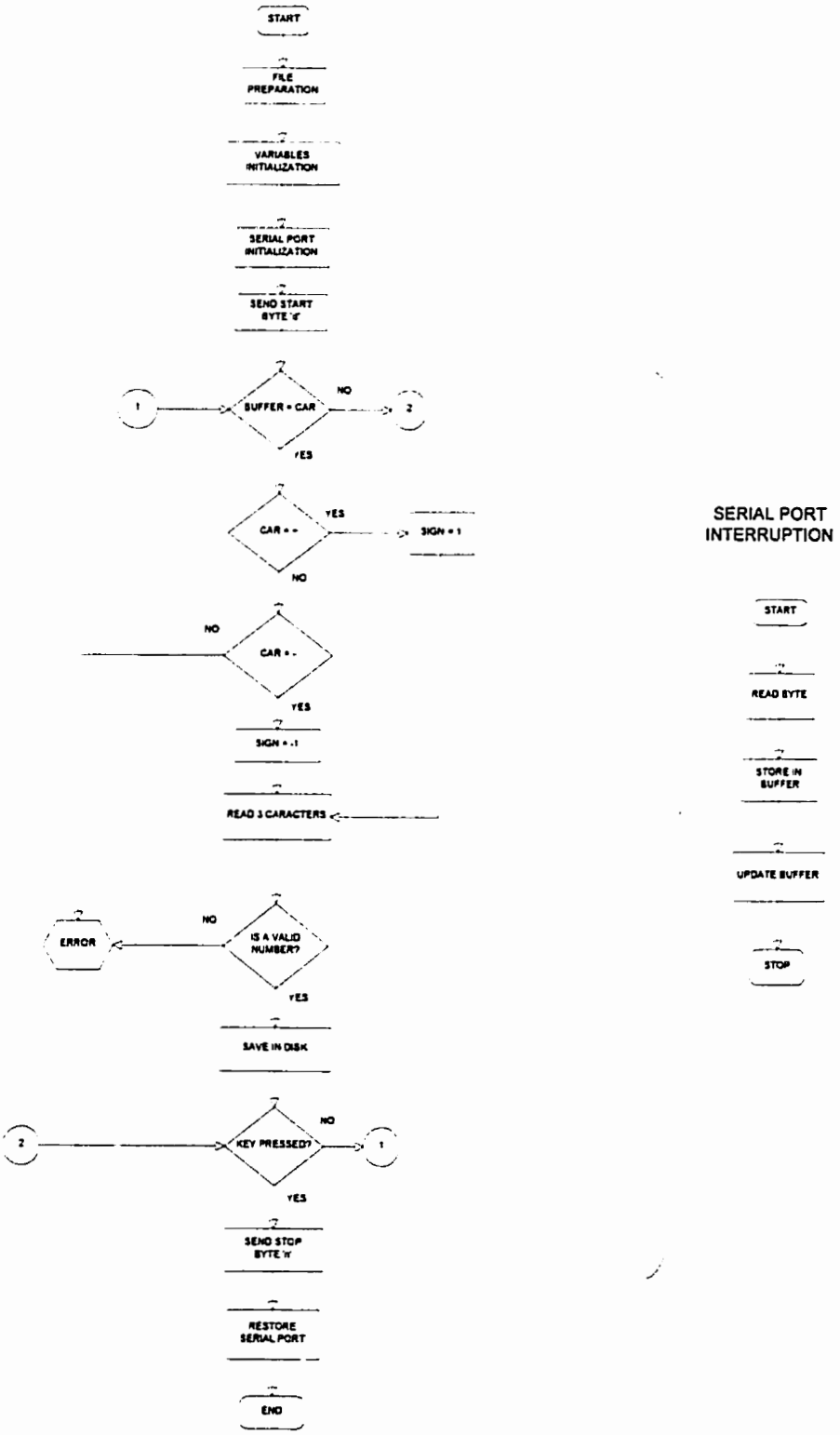


FIGURE B.4 PC DATA ADQUISICION PROGRAM

the data in the output file. Finally, the program sends the ASCII code for the letter 'n' to stop the data transmission.

Figure B.4 is a flow chart for the PC data collection program.

B.3.2 *Data Transmission Routine*

The GPC should be able to perform the following actions:

- Detect and understand the ASCII code for the letter 'd' as the signal to start the data transmission.
- Detect and understand the ASCII code for the letter 'n' as the signal to stop the data collection.
- Convert the per unit values, used for the internal processing of the GPC, to the equivalent real values of the reading.
- Send the ASCII value, which corresponds to the read value, to the PC every time that the synchronizing process indicates it.
- Synchronize the transmission data to send data with a fixed frequency.

The first two points were done through the modification of the general keyboard interface routine. The original routine key_io.c set the flag keyflg to the hex value AA each time that a valid input is introduced through the keyboard. The keyboard sequence should follow a specific sequence and should be confirmed by the letter 'Y' in order to be valid.

In the new version, which is named key1_io.c, when the input received through the serial port is the letter 'd', the routine does not wait for confirmation, instead, the variable kbflg is immediately set to a different value to indicate the start of transmission.

In similar way, when the letter received is an 'n', the variable kbflg is returned to the value HEX 55 that means do nothing.

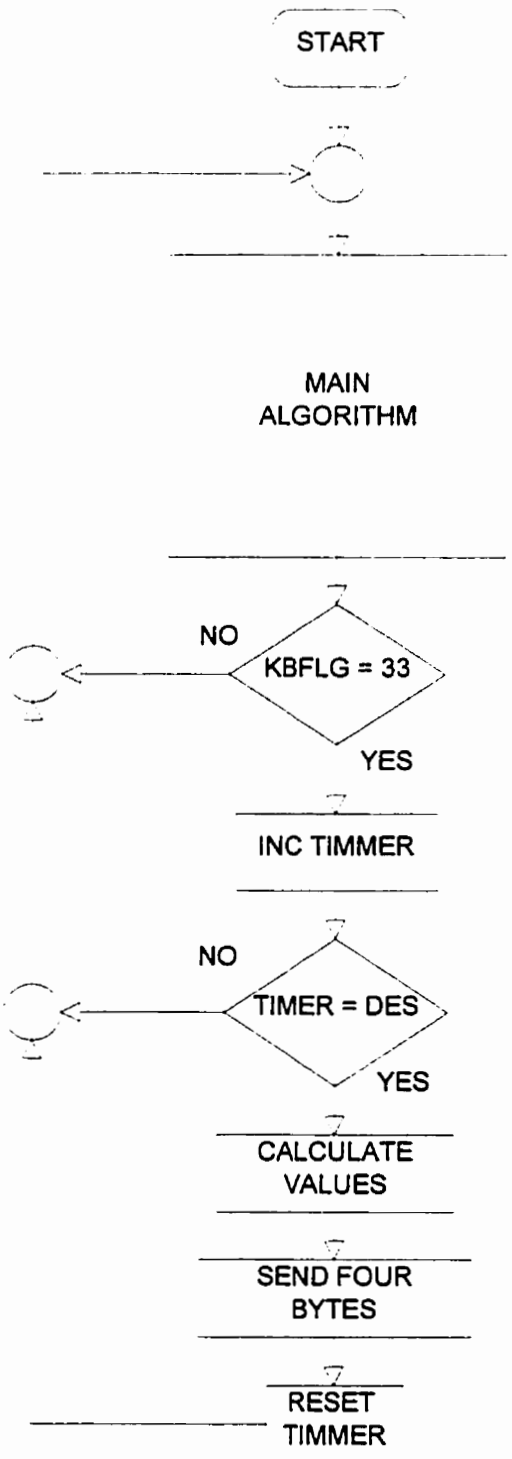


FIGURE B.5 CONTROLLER BOARD DATA ADQUISICION RESPONSE

The other functions were done through a routine which is included in the main program. The flow chart of this subroutine is included in figure B.5.

B.4 SERIES CONNECTION HARDWARE AND SOFTWARE MODIFICATIONS

In the series connection ten double-layer capacitors are charged simultaneously; therefore, sensing the voltage in all the capacitors is necessary to avoid over voltage in any of them. The voltages can be measured using independent sensors and each output can be taken into a different input of the controller board. However, the limit in the number of analog inputs of the controller board and the inadequate use of ten voltage sensors makes it necessary to develop a more elaborated system for voltage sensing.

An analog voltage multiplexer was designed and implemented to sense consecutively the voltage across each capacitor and multiplex those voltages in a single analog output. The multiplexer is based on high resistance values for isolation, differential amplifiers and analog switches.

The multiplexer should fulfill some requirements:

- Recognition of the signals coming from the parallel port of the control board as controlling signals.
- Good rejection of the noise introduced by the switching pattern occurring at the DC/DC converter.
- High accuracy in the measurement.

The system is composed of a high impedance attenuator to reduce the voltage to the levels used in the electronics, ten differential

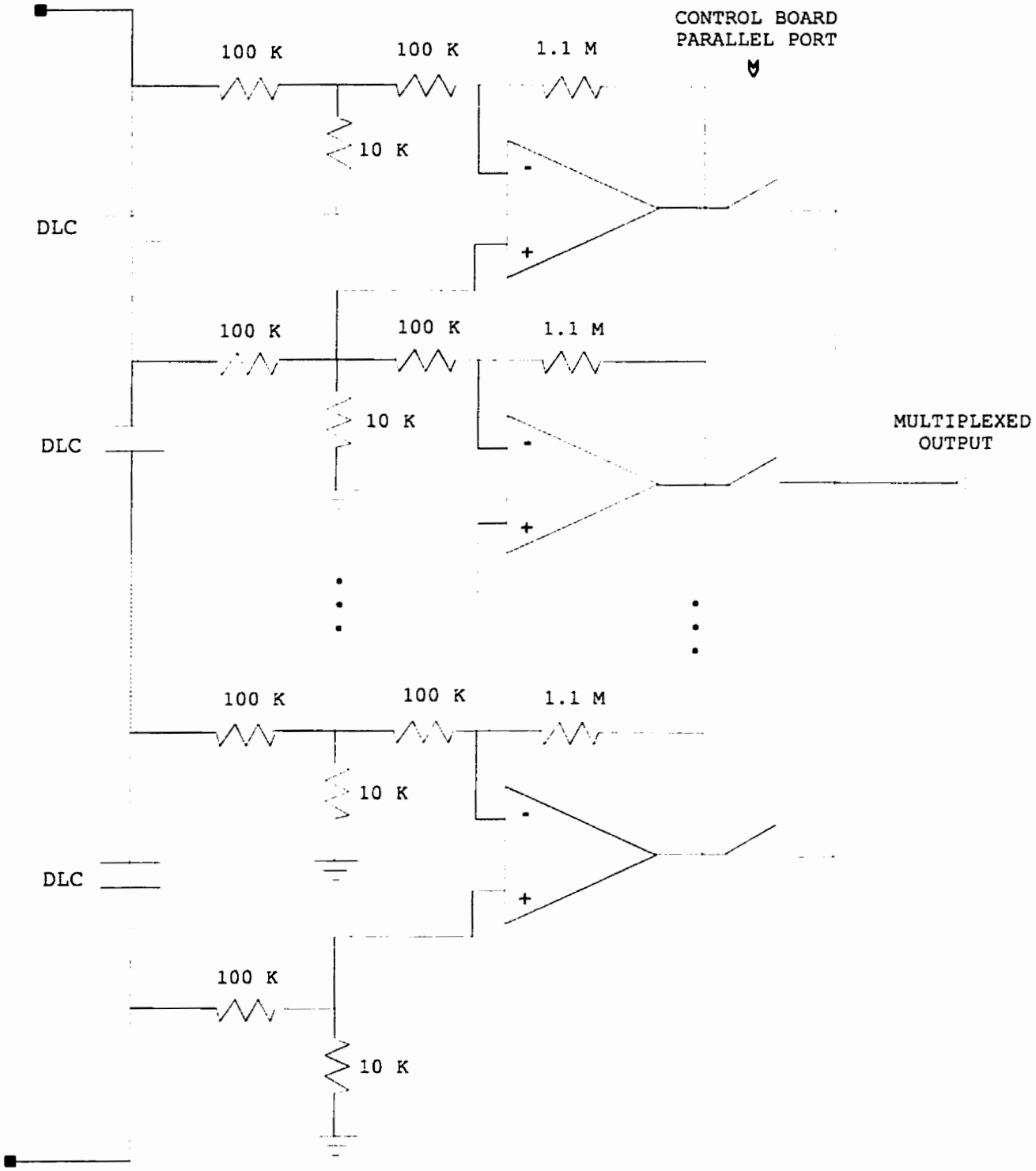


FIGURE B.6 MULTIPLEXER SYSTEM

amplifiers, one for each capacitor, and a group of ten analog switches with an output open collector to obtain the multiplexer effect when they are connected directly.

The figure B.6 shows the multiplexer system.

The attenuator and the following differential amplifier should be perfectly calibrated to get good accuracy in the sensor. Therefore, it is necessary to use high precision resistors and to calibrate carefully the system.

In addition, high resistance values at the attenuator are necessary to get high input impedance.

The presence of a new voltage sensing system makes it necessary to make some modifications in the control program. The file SERCAPA.C was developed to perform the test of the series capacitors. This program is based in the initial CAP1.C used for the general DLC test but some modification should be mentioned:

- The parallel port, which was not used in CAP1.C, is now used. Ten lines of the parallel port are activated in sequence each one during 2 msec, and those lines activate the analog switches of the multiplexer.

- The charge and discharge actions are started and stopped when any of the ten capacitors reach the limit voltage. In other words, a new pair of variables representing the highest and lowest voltage are implemented.

- The subroutine used to send the data in response to the data acquisition program sends the ten DLC voltages each period.

- The program will not include the normalization and automatic parameter calculation routines.

Appendix C include the list of the serial capacitor test.

APPENDIX C

LIST OF PROGRAMS

C.1 GENERAL CAPACITOR TEST PROGRAM

```
/* cap1.c */
/* 1/2/96  R.Bonert    */
/* 1/8/96  L.Zubieta   */
/* program
   ultra capacitor testing
   uses 4Q chopper (4qch.c), fsw 4 kHz, Tsa 2 msec
   with VSI module : switches S1,S4 and S5,S2 used

   switch names                TPU channels
   1o  2o       -> s1  s5  -> ch2  ch6
   11  21          s4  s2     ch3  ch7
   ch 0 switch period
   ch 1 interrupt period
   ch 2,3 & 6,7 gating channels
   ch 8-D DIO out

   data I/O :
   in  : ifdb current feedback          ch7
         vcap total capacitor voltage   ch6
         vcap*10 (for model accuracy)   ch5
   out : iref  ch9
         pwcon ch8
         ifdb  ch7
         vcap  ch6

   program operation :
   there are five basic modes selected by keyb Mxxx
   1    capacitor testing (default)
   21   chopper test pw control, man & sine
   22   chopper test current loop (20ms), man & sine
   3    capacitor discharge or normalization
   4    capacitor charge normalization until reach desired voltage
   5    model parameters calculation

   keyb controls :
   Mxx     mode selection 1,21,22,3,4 or 5.
   G       gating on/off G11 = on, Gx = off
   R       run  inverter (switch signal DIO ch 8 = 1)
   S       stop  DIO ch8 = 0 and gating off

   in chopper test mode
   p       pw control in %  +100 to -100, keyb input
   a,f     automatic control of pw, sine f = 0.1..100Hz
           a 0..100%, pw = p +  sine
           in test mode 22 current control
           p,a,f provide the per unit current reference

   parameter input for charge control :
   v      ?x  v-1.y  y selects parameter to be set
          ?0  vxxx.xx  ibase in A
```

```
          ?1  vxxx.xx  icharge in A
          ?2  vxxx.xx  idischarge in A
          ?3  vxxx.xx  vbase in V
          ?4  vxxx.xx  vmax in V
          ?5  vxxx.xx  vmin in V (negative)
          ?6  vxxx.xx  capacitor voltage desired in mode 4
          ?7  vxxx.xx  number of cycles
          ?8  vxxx.xx  pause in sec
          ?9  vxxx.xx  charge time in sec

   in capacitor test mode
   gxx     0   iref =0, gating off
          10   charge to vmax
          20   discharge to vmin
          30   timed charge, max vmax
          40   timed discharge, min vmin
          50   cycled charging vmax,vmin
          60   charge to vmax after pause delay

   in mode 3 and 4 (dis)charge cycle and currents prefixed, run 1 or 2 hours
   in mode 5 use a normalized capacitor, values are prefixed
*/
#include "memap332.h"                    /* hardware memory map  */
#include "tabsin.h"                      /* table sine function 0-360 */

/* ======================== GLOBAL VARIABLES ======================== */
  /* ---- variables for data transfer and interrupt routines ---- */
unsigned short ka, loopflg;
unsigned short ilpcnt;
signed int     in0,in1,in2,in3,in4,in5,in6,in7,
               out3,out4,out5,out6,out7,out8,out9;
unsigned int   swlocnt,sw1lcnt;

  /* ----------------- variables for table look up --------------- */
unsigned int   tabpos;
signed short   tabres;

/* ======================== EXTERNAL FUNCTIONS ====================== */
extern void    tepsa4(),tepla4(),pp_setup(),qsms870(),keyb1_io();

/* ================== FUNCTIONS & INTERRUPT ROUTINES ================ */
  /* ------------------------ INT TPU CH 1 ------------------------ */
#pragma interrupt()
void dio_samp()
{
        /* interrupt TPU ch 1 for transfer of pwm data for next
           interval timing of sampling and I/O through QSPI analog
           input last cycle, analog output and telegrams in next cycle.
           analog I/O data format:
           for fxp 1.0 p.u. ->  signed short var = *pRXDF >> 3;
           write fxp to ch# *pTXD# = (signed short var fxp) >> 1;

           if program QSMs870 is used, then :
               analog in : ch 7,..6,..5,..4,..3,..2,..1,..0
                           *pRXD F,..C,..9,..6,..4,..2,..1,..0
               analog out : ch 7..6..5..4..3..9..8
                           *pTXD E..D..B..A..7..5..8
        */

        ilpcnt = ilpcnt + 1;
        switch(ilpcnt)
        {
```

```
                case 4 :                    /* start QSM single shot */
                tepsa4();
                *pSPCR1  = 0x901A;
                break;

                case 6 :                    /* start QSM again to provide data */
                *pSPCR1  = 0x901A;          /* sampled in the last 0.5 msec */
                break;

                case 8 :                    /* Tloop 2 msec */
  /* ---------------------- pwm data transfer ------------------ */
                *pCH2p46  = swlocnt;        /* switch data next per */
                *pCH3p46  = swllcnt;        /* coherent write */
                *pCH6p46  = swllcnt;
                *pCH7p46  = swlocnt;

  /* ------------------------ analog inputs -------------------- */
                in7 = *pRXDF >> 3;          /* ch7 ifdb */
                in6 = *pRXDC >> 3;          /* ch6 vcap total */
                in5 = *pRXD9 >> 3;          /* ch5 10*vcap */

  /* ------------------------ analog outputs ------------------- */
                *pTXD5 = out9 >> 1;         /* iref out to ch 9 */
                *pTXD8 = out8 >> 1;         /* pwcon out to ch 8 */
                *pTXDE = out7 >> 1;         /* ifdb out to ch 7 */
                *pTXDD = out6 >> 1;         /* vcap out to ch 6 */
                *pTXDB = out5 >> 1;         /* ichpu ch 5 */

  /* --------------------- set start flag algorithm loop -------- */
                loopflg = 0x1111;
                ilpcnt = 0;
                break;
        }                                   /* end switch ilpcnt */
        ka = *pCISR; *pCISR = 0xFFFD;       /* clear int ch1 */
        tepsa4();
}                                           /* end dio_samp */

/* ======================== PROGRAM SETUP ========================== */
main(void)
{
  /* ------------ VARIABLES GENERAL INFRAESTRUCTURE ------------- */

  /* --------------------- for keyboard input -------------------- */
static unsigned char  letter;
static unsigned char  kbflg = 0x55;
static signed int     val,valf;
static unsigned short kbstat;
static unsigned short parout;

  /* -------------------------- for loop ----------------------- */
static unsigned int   mlo,fsa10;
static unsigned short TEflg;

  /* --------------------variables spec. program ----------------*/
static unsigned int   swpercnt,swotcnt,fsmax,pwlcnt,phi1,phiincr,
                      modesel,fsel,nextfsel,gstcnt,cnt31,cnt55,cnt56;
static signed int     pwcon,vav1,vav2,vav3,ams,amax,x1,aux;

  /* --------------------- for current control ------------------- */
static unsigned int   kscu,ksc;
static signed int     ifdb,SLUcu,SLLcu,uncu,u0cu,encu,e0cu,k1cu,k2cu,
                      LPcu,LNcu;
```

```
  /* -------------------- for parameters input ------------------ */
static unsigned int   param,nbcyc,pause,paucnt,chrgtime,chtcnt,cntp;
static signed int     iref,ibase,ichrg,idischrg,vbase,vmax,vmin,ichpu,
                      idispu,vmaxpu,vminpu,vdes,vdespu;

  /* --------------------- for normalization -------------------- */
static unsigned int   ciclo,ciclo1;
static signed int     factor,vlim,vcap,vcapo;

  /* ---------------- for serial data adquisicion --------------- */
static unsigned int   cont,timmer,sent,datcol;
static signed int     ser1,ser2,ser3,ser4,ser5,vcaps;

  /* -------------------- for model calculation ----------------- */
static unsigned int   cntmod,model,scrmod,elem;
static signed int     vmod0,vmod1,vmod2,r1,r2,r3,c0,c1,c2,c3,cv,cv2,
                      rb1,rb2,rb3,rb4,rb5,rb6,rb7,fac1,env;
static unsigned char  ch1,ch2;

  /* ------------------ SET UP - START INFRASTRUCTURE ----------- */
        *pPfpar = 0x00F0;                   /* set pin 3-0 up as port F */
        *pDdrf  = 0x000F;                   /* pin 3-0 out  */
                                            /* IRQ 7-4 still operative */

  /* ------------- setup parallel port M68230 on GPC-board ------ */
        pp_setup();                         /* PA out,PB in,PC out for PLD */

  /* ---- program of PLD U14 controls of ch2..D see chopper ----- */
        *pPortf = 0x01;                     /* gating off, 0x0D -> gating on */
        *pPCDR = 0x99;

  /* ------------------- initialize and start QSM --------------- */
        qsms870();                          /* Ts=180+byte*9.5, byte>=9 */

  /* ------ init D/A output data,run one cycle to set flag ------ */
        *pTXDE = 0;       *pTXDD = 0;       *pTXDB = 0;
        *pTXD8 = 0;       *pTXD7 = 0;       *pTXD5 = 0;
        *pTXDA = 0;
        *pSPCR1  = 0x901A;

  /* ---------- start QSM, Ts = 427usec < Tsa = 500 usec -------- */
        fsa10 = 50;                         /* algorithm frequency/10 */
        TEflg = *pSPSR;                     /* test end of QSM cycle */
        while ((TEflg & 0x80) == 0 )
               { TEflg = *pSPSR;}

  /* --------------- PWM & CONTROL INITIALIZATION --------------- */
        swpercnt = 1048;                    /* 4194 = 1 kHz = fsw
                                               2097 = 2 kHz, 1048 = 4 kHz
                                               1398 = 3 kHz, 466 = 9 kHz */
        fsmax = 100;                        /* in Hz fmax < fsw/15 */
        amax = 0x0EA0;                      /* <- estimate for 4 kHz
                                               3 kHz 0x0F09
                                               9 kHz 0x0DEB
                                               1 kHz 0x0FAD */
        phi1 = 0;                           /* phi per unit = 0xFFFF due to
                                               table structure */
        x1 = (0x00041852*2) >> 16;          /* x1 = 0.2% pu */

        phiincr =(((swpercnt*4*x1) >> 12) * fsmax) >> 8;
                                            /* start frequency 0.2 % of fmax
```

```
                                        incr = 0xFFFF * Tsw * fsine */
      phiincr = phiincr * 8;            /* Tsa/Tsw = 8 */

      x1 = (0x0028F333*1) >> 16;        /* x1 = 1% pu */
      ams = (amax * x1) >> 12;          /* start amplitude 1% of amax */
      swotcnt = 26;                     /* 7 usec switch over time */

/* -------------- initial chopper PWM calculation ------------- */
      vav1 = ams; vav2 = ams; vav3 = ams;

      pw1cnt =  (swpercnt * ( 0x0FFF + vav1)) >>13;
                                        /* (swpercnt * (1+vav1)/2) >> 12 */

      sw1ocnt = ((pw1cnt - swotcnt) << 16)
                + ((swpercnt-pw1cnt+swotcnt) >> 1);

      sw11cnt = ((pw1cnt + swotcnt) << 16)
                + ((swpercnt-pw1cnt-swotcnt) >> 1);

/* --------------------- TPU SET UP AND INIT ------------------ */
      *pTMCR = 0x00C1;                  /* 0.24 usec; int ID $1, presc = 1
                                           -> 16.777216 MHz/4 */
      *pTICR = 0x0640;                  /* int 6, intv $4x -> $100 offset */
                                        /* CAUTION 332Bug trap at $108 ! */

      /* description of channel functions :
         ch 0 SPWM mode 2 links
         ch 1 SPWM mode 0 or 1 sync to ch 0
         ch 2,3  & 6,7 SPWM mode 1
         ch 4,5 DIO set to zero !
         ch 8..D DIO
      */

/* ---------- ch0 SPWM mode 2 , switch interval timing -------- */
      *pCH0pr0  =  0x0092;              /* f low, TCR1 */
      *pCH0p46 = ((swpercnt >> 1) << 16) + swpercnt;
                                        /* hightime = swpercnt/2 */
      *pCH0pr8  =  0x660E;              /* L st L cnt, dummy adr */
      *pCH0prA  =  0;                   /* delay, only on start */

/* ---------- ch1 SPWM mode 1 , QSM algorithm timing ---------- */
      *pCH1pr0  =  0x0092;              /* f low, TCR1 */
                                        /* Tch4 = Tch5 */
      *pCH1p46  = ( 0x00640000 + (swpercnt-200));
                                        /* hightime 25 usec, del -50 usec
                                           check whether int finishes before
                                           ch0 rising edge */
      *pCH1pr8  =  0x0200;              /* adr 1, adr 2 ch 0 */

/* ---------- ch2 = switch 1o, SPWM mode 1 linked ------------- */
      *pCH2pr0  =  0x0092;              /* f low, TCR1 */
      *pCH2p46  = sw1ocnt;              /* coherent write , pw, del */
      *pCH2pr8  =  0x0200;              /* adr1, adr2 of ch 0 */

/* ---------- ch3 = switch 11, SPWM mode 1 linked ------------- */
      *pCH3pr0  =  0x0092;              /* f low, TCR1 */
      *pCH3p46  = sw11cnt;              /* coherent write, pw, del */
      *pCH3pr8  =  0x0200;              /* adr1, adr2 of ch 0 */

/* ---------- ch6 = switch 3o, SPWM mode 1 linked ------------- */
      *pCH6pr0  =  0x0092;              /* f low, TCR1 */
      *pCH6p46  = sw11cnt;              /* coherent write , pw, del */
```

```
      *pCH6pr8  =  0x0200;              /* adr1, adr2 of ch 0 */

/* ---------- ch7 = switch 31, SPWM mode 1 linked ------------ */
      *pCH7pr0  =  0x0092;              /* f low, TCR1 */
      *pCH7p46  = swlocnt;              /* coherent write, pw, del */
      *pCH7pr8  =  0x0200;              /* adr1, adr2 of ch 0 */

/* ---------- ch 4,5  9..D DIO,  no parameter reg. ---------- */

/* -------- channel function registers group ch F..8 ---------- */
      *pCFSR0 = 0x0088;                 /* ch D,C DIO */
      *pCFSR1 = 0x8888;                 /* ch B..8 DIO */
      *pCPR0  = 0x0555;                 /* ch D..8 low pri */
      *pHSQR0 = 0x0AAA;                 /* ch D..8 upd on HSR */

/* -------- channel function registers group ch 7..0 ---------- */
      *pCFSR2  =  0x7788;               /* ch 7,6 SPWM 5,4 DIO */
      *pCFSR3  =  0x7777;               /* ch 3..0 SPWM */
      *pCPR1   =  0xF5FF;               /* ch 7,6 3..0  hi prio */
      *pHSQR1  =  0x5A56;               /* ch7,6 3..1 m 1,ch0 m2 */

/* ------------------- init discret outputs ------------------- */
      *pHSRR0 = 0x0002;                 /* Stop inverter, ch8 DIO low,
                                           gating must be set off */

      *pHSRR1 = 0x0600;                 /* set ch5,4 low no gating,
                                           caution ch5 inv  */

      *pHSRR0 = 0x0FFF;                 /* init,start ch D..8 */

      *pHSRR1  =  0xAFAA;               /* init,start ch 7..0 */

/* -------------------- set up int -> ch1 ---------------------- */
      ka = *pCISR;
      *pCISR = 0xFFFD;                  /* clear int bit ch1 */
      *pCIER   =  0x0002;               /* enable ch1 int */
      asm("  move.w  #$2500,SR ");      /* int ch1 offset 0x41*4 = 0x104 */

/* ------------------ OTHER INITIALIZATIONS ------------------- */
        loopflg = 0x8888; ilpcnt = 0;   /* interrupt loop */
        modesel = 1;                    /* capacitor test mode*/

        cntp = 0; fsel = 0; ciclo = 0;  ciclo1 = 0; cont = 0;
        cntmod = 0; model = 0; scrmod = 0; elem = 0;
                                        /* all the switch variables */
        param = 1; timmer = 1;
        sent = 1; datcol = 1;           /* synchronization variables */

/* --------------- init PI regulator high res ----------------- */
         u0cu = 0; uncu = 0; e0cu = 0; encu = 0;
         k1cu =  0x049D;                /* gain 12*Tr, Tr 0.015, Ts 2 msec */
         k2cu =  0x0D90;
         kscu =  0;
         SLUcu = 0x02000000; SLLcu = 0xFE000000;
         LPcu = amax << 12;             /* old 0x0F80000;  96%  */
         LNcu = (-amax) << 12;          /* old 0xFF800000;  -54% */

      /* init parameters non dangerous, in case input forgotten ! */

/* ======================== PROGRAM LOOP ========================== */
mlo = 2;                                /* LOOP */
while (mlo == 2)
```

```
{
        while (loopflg == 0X8888) { }     /* test for end of int */
        loopflg = 0x8888;
        tepla4();                         /* loop length indicator */

        TEflg = *pSPSR;                   /* test end of QSI cycle */
        if ((TEflg & 0x80) == 0 )
        { letter = 'E'; }                 /* exit to monitor */
        *pSPSR = 0x7F;

  /* ---------------------- PARAMETERS INPUT ---------------------- */
        if (param == 7)                   /* do if keyboard 'v' */
        {
        param = 1;
        if (val<0)
             {
                cntp = -1*valf;           /* start input from param valf */
                parout = 0x30+cntp;       /* ASCII code for valf */
                kbstat = *pSCSR;          /* test port status */
                if (kbstat & 0x0100) { *pSCDR = parout; }
             }
        else
             {
                switch(cntp)
                {
                case 0 :                  /* i base input */
                    *pSCDR = '1';
                    ibase = val*10+valf;
                    cntp = cntp + 1;
                break;

                case 1 :                  /* i charge input */
                    *pSCDR = '2';
                    ichrg = (val*10+valf) << 16;
                    ichpu = (ichrg/ibase) >> 4;
                    cntp = cntp + 1;
                break;

                case 2 :                  /* i discharge input */
                    *pSCDR = '3';
                    idischrg = (val*10+valf) << 16;
                    idispu = (idischrg/ibase) >> 4;
                    cntp = cntp + 1;
                break;

                case 3 :                  /* v base input */
                    *pSCDR = '4';
                    vbase = val*10+valf;
                    cntp = cntp + 1;
                break;

                case 4 :                  /* v max input */
                    *pSCDR = '5';
                    vmax = (val*10+valf) << 16;
                    vmaxpu = (vmax/vbase) >> 4;
                    cntp = cntp + 1;
                break;

                case 5 :                  /* v min (negative) input */
                    *pSCDR = '6';
                    vmin = (val*10+valf) << 16;
                    vminpu = (-1*vmin/vbase) >> 4;
```

```
                cntp = cntp + 1;
            break;

            case 6 :                    /* v desired input (mode 4) */
                *pSCDR = '7';
                vdes = (val*10+valf) << 16;
                vdespu = (vdes/vbase) >> 4;
                cntp = cntp + 1;
            break;

            case 7 :                    /* number of cycles input */
                *pSCDR = '8';
                nbcyc = val;
                cntp = cntp + 1;
            break;

            case 8 :                    /* pause time input */
                *pSCDR = '9';
                pause = val*10+valf;
                paucnt = pause*fsa10;
                cntp = cntp + 1;
            break;

            case 9 :                    /* time of (dis)charge input */
                *pSCDR = '0';
                chrgtime = val*10+valf;
                chtcnt = chrgtime*fsa10;
                cntp = 0;
            break;
            }                           /* end switch cntp */
        }                               /* end else */
    }                                   /* end parameter input */

/* ----------------- MODE 1 CAPACITOR TEST OPTIONS ------------ */
    if (modesel==1)                     /* do if mode=1 */
    {
        switch(fsel)                    /* input fsel gives kind of test */
            {
            case 0 :                    /* gating delayed off */
                iref = 0;
                fsel = 800;
                nextfsel = 210;
                gstcnt = 30;
            break;

/* -------------------- charge to vmax ------------------------ */
            case 10 :                   /* charge with icharge */
                *pPortf = 0x0D;
                iref = ichpu;
                fsel = 11;
            break;

            case 11 :                   /* terminate at v max */
                if (vcap > vmaxpu)
                  {
                  iref = 0;
                  gstcnt = 30;
                  fsel = 800;
                  nextfsel = 210;
                  }
            break;
```

```
/* -------------------- charge to vmin ------------------------ */
            case 20 :                   /* discharge to idischarge */
                *pPortf = 0x0D;
                iref = -idispu;
                fsel = 21;
            break;

            case 21 :                   /* terminate at v min */
                if (vcap < vminpu)
                  {
                  iref = 0;
                  gstcnt = 30;
                  fsel = 800;
                  nextfsel = 210;
                  }
            break;

/* ----------------- charge during fixed time ------------------ */
            case 30 :                   /* charge with icharge */
                *pPortf = 0x0D;
                iref = ichpu;
                cnt31 = chtcnt;
                fsel = 31;
            break;

            case 31 :                   /* terminate at chgtime or vmax */
                cnt31 = cnt31-1;
                if ((vcap > vmaxpu)||(cnt31==0))
                  {
                  iref = 0;
                  gstcnt = 30;
                  fsel = 800;
                  nextfsel = 210;
                  }
            break;

/* ----------------- discharge during fixed time --------------- */
            case 40 :                   /* discharge with idischarge */
                *pPortf = 0x0D;
                iref = -idispu;
                cnt31 = chtcnt;
                fsel = 41;
            break;

            case 41 :                   /* terminate at chgtime or vmin */
                cnt31 = cnt31-1;
                if ((vcap < vminpu)||(cnt31==0))
                  {
                  iref = 0;
                  gstcnt = 30;
                  fsel = 800;
                  nextfsel = 210;
                  }
            break;

/* ------------------- cycling between vmax,vmin ---------------- */
            case 50 :                   /* pause before start */
                iref = 0;
                cnt55 = paucnt;
                cnt55 = 1;              /* only if want no pause at start */
                fsel = 800;
                gstcnt = 30;
```

```
    nextfsel = 59;
    cnt56 = nbcyc;
break;

case 59 :                   /* pause delay */
    cnt55 = cnt55-1;
    if (cnt55 ==0)  { fsel = 58; }
break;

case 58 :                   /* charge with icharge */
    *pPortf = 0x0D;
    sent = 7;
    iref = ichpu;
    fsel = 51;
break;

case 51 :                   /* terminate at v max */
    if (vcap > vmaxpu)
      {
      iref = 0;
      gstcnt = 30;
      cnt55 = paucnt;
      cnt55 = 1;            /* only if want no pause */
      fsel = 800;
      nextfsel = 52;
      }
break;

case 52 :                   /* pause delay */
    cnt55 = cnt55-1;
    if (cnt55 ==0) { fsel = 53; }
break;

case 53 :                   /* discharge with idischarge */
    *pPortf = 0x0D;
    iref = -idispu;
    fsel = 54;
break;

case 54 :                   /* terminate at v min */
    if (vcap < vminpu)
      {
      iref = 0;
      gstcnt = 30;
      cnt55 = paucnt;
      cnt55 = 1;            /* only if want no pause */
      fsel = 800;
      nextfsel = 55;
      }
break;

case 55 :                   /* pause delay */
    cnt55 = cnt55-1;
    if (cnt55 ==0) { fsel = 56; }
break;

case 56 :                   /* cycle repetition nbcyc times */
    cnt56 = cnt56-1;
    if (cnt56 ==0) { fsel = 210; }
    else { fsel = 59; cnt55 = 1;}
break;
```

```
/* -------- charge to vmax after delay (for data acq) --------- */
              case 60 :                    /* delay of paucnt before charge */
                  iref = 0;
                  cnt55 = paucnt;
                  fsel = 800;
                  gstcnt = 30;
                  nextfsel = 61;
              break;

              case 61 :                    /* pause delay */
                  cnt55 = cnt55-1;
                  if (cnt55 ==0) {fsel = 62;}
              break;

              case 62 :                    /* charge with icharge */
                  *pPortf = 0x0D;
                  sent = 7;
                  iref = ichpu;
                  fsel = 63;
              break;

              case 63 :                    /* terminate at v max */
                  if (vcap > vmaxpu)
                    {
                    iref = 0;
                    gstcnt = 30;
                    fsel = 800;
                    nextfsel = 210;
                    }
              break;

              case 800 :                   /* gating delayed off */
                  gstcnt = gstcnt-1;
                  if (gstcnt==0)
                  {
                  *pPortf = 0x01;
                  fsel = nextfsel;
                  }
              break;

              case 210 :                   /* do nothing */
              break;
              }                            /* end switch fsel */
      }                                    /* end mode=1 */


/* ------------------ MODE 21 OR 22 CHOPPER TEST -------------- */
      if ((modesel==21)||(modesel==22))
      {
           phi1 = phi1 + phiincr;          /* phi 360 deg. -> FFFF */
           tabpos = phi1;                  /* read from table */
           asm( " move.l _tabpos,D0 " );
           asm( " TBLS.W _sintab,D0 " );
           asm( " move.w D0,_tabres " );
           vav2 = (ams * tabres) >> 12;
           vav1 = vav3+vav2;               /* calc based in p,a,f inputs */
           if (vav1 > amax)                /* vav1 must be limited to avoid */
             { vav1 = amax; }              /* malfunction of the pwm */
           if (vav1 < (-amax))
             { vav1 = (-amax); }
           if (modesel==21)                /* vav1 -> pwcon in mode 21 */
             { pwcon=vav1; iref=0; }
```

```
            if (modesel==22)              /* vav1 -> iref in mode 22 */
              { iref=vav1; pwcon=0; }
      }                                   /* end mode = 21,22 */

/* ------------------ CAPACITOR NORMALIZATION ----------------- */
      if (modesel==3)
      {
           switch (ciclo)                 /* gives normalization section */
              {
              case 0:                     /* -30 amps until -300 mv */
                  *pPortf = 0x0D;
                  iref = (-1*(300<<16)/ibase)>>4;
                  vlim = (-1*(3<<16)/(vbase))>>4;
                  ciclo = 1;
              break;

              case 1:                     /* self charge until -100 mv */
                  if (vcap < vlim)
                  {
                    *pPortf = 0x01;
                    iref = 0;
                    vlim = (-1*(1<<16)/(vbase))>>4;
                    ciclo = 2;
                  }
              break;

              case 2:                     /* -10 amps until -240 mv */
                  if (vcap > vlim)
                  {
                    *pPortf = 0x0D;
                    iref = (-1*(100<<16)/ibase)>>4;
                    vlim = (-1*(24<<16)/(10*vbase))>>4;
                    ciclo = 3;
                  }
              break;

              case 3:                     /* self charge until -120 mv */
                  if (vcap < vlim)
                  {
                    *pPortf = 0x01;
                    iref = 0;
                    vlim = (-1*(12<<16)/(10*vbase))>>4;
                    ciclo = 4;
                  }
              break;

              case 4:                     /* -5 amps until -200 mv */
                  if (vcap > vlim)
                  {
                    *pPortf = 0x0D;
                    iref = (-1*(50<<16)/ibase)>>4;
                    vlim = (-1*(2<<16)/(vbase))>>4;
                    ciclo = 5;
                  }
              break;

              case 5:                     /* self charge until -140 mv */
                  if (vcap < vlim)
                  {
                    *pPortf = 0x01;
                    iref = 0;
                    vlim = (-1*(14<<16)/(10*vbase))>>4;
```

```
                    ciclo = 6;
                }
            break;

            case 6:                     /* -2 amps until -180 mv */
                if (vcap > vlim)
                {
                  *pPortf = 0x0D; /* gating on */
                  iref = (-1*(20<<16)/ibase)>>4;
                  vlim = (-1*(18<<16)/(10*vbase))>>4;
                  ciclo = 5;
                }
            break;

            case 99 :                   /* if vcapo<250mv disch to -vcapo */
                 *pPortf = 0x0D;
                 iref = (-1*(20<<16)/ibase)>>4;
                 vlim = (-1.1*vcapo);
                 ciclo = 98;
            break;

            case 98 :                   /* terminate at -vcapo */
                if (vcap < vlim)
                {
                  *pPortf = 0x01;
                  iref = 0;
                  vlim = 0;
                  modesel=1;
                }
            break;
            }                           /* end switch ciclo */
    }                                   /* end mode = 3 */

/* --------------- CAPACITOR CHARGE TO FIXED VOLTAGE ----------- */
    if (modesel==4)
    {
        switch (ciclo1)                 /* gives charge process section */
        {
            case 0:                     /* 30 amps until vdes+300 mv */
                *pPortf = 0x0D;
                iref = (factor*(300<<16)/ibase)>>4;
                vlim = ((factor*(30<<16)/(10*vbase))>>4)+vdespu;
                ciclo1 = 1;
            break;

            case 1:                     /* self charge until vdes+100 mv */
                if (factor*vcap > factor*vlim)
                {
                  *pPortf = 0x01;
                  iref = 0;
                  vlim = ((factor*(1<<16)/(vbase))>>4)+vdespu;
                  ciclo1 = 2;
                }
            break;

            case 2:                     /* 10 amps until vdes+240 mv */
                if (factor*vcap < factor*vlim)
                {
                  *pPortf = 0x0D;
                  iref = (factor*(100<<16)/ibase)>>4;
                  vlim = ((factor*(24<<16)/(10*vbase))>>4)+vdespu;
                  ciclo1 = 3;
```

```
                }
            break;

            case 3:                     /* self charge until vdes+120 mv */
                if (factor*vcap > factor*vlim)
                {
                  *pPortf = 0x01;
                  iref = 0;
                  vlim = ((factor*(12<<16)/(vbase*10))>>4)+vdespu;
                  ciclo1 = 4;
                }
            break;

            case 4:                     /* 5 amps until vdes+200 mv */
                if (factor*vcap < factor*vlim)
                {
                  *pPortf = 0x0D;
                  iref = (factor*(50<<16)/ibase)>>4;
                  vlim = ((factor*(20<<16)/(10*vbase))>>4)+vdespu;
                  ciclo1 = 5;
                }
            break;

            case 5:                     /* self charge until vdes+140 mv */
                if (factor*vcap > factor*vlim)
                {
                  *pPortf = 0x01;
                  iref = 0;
                  vlim = ((factor*(14<<16)/(vbase*10))>>4)+vdespu;
                  ciclo1 = 6;
                }
            break;

            case 6:                     /* 2 amps until vdes+180mv */
                if (factor*vcap < factor*vlim)
                {
                  *pPortf = 0x0D;
                  iref = (factor*(20<<16)/ibase)>>4;
                  vlim = ((factor*(18<<16)/(10*vbase))>>4)+vdespu;
                  ciclo1 = 5;
                }
            break;
            }                           /* end switch ciclo1 */
      }                                 /* end mode = 4 */

/* ---------------- AUTOMATIC MODEL OBTENTION ---------------- */
      if (modesel==5)
      {
           cntmod = cntmod+1;
           switch (model)
           {
              case 0 :                  /* read init volt and i=45 A */
                  cntmod=0;
                  vmod0 = -in5;
                  *pPortf = 0x0D;
                  iref = ((450<<16)/ibase)>>4;
                  model = 1;
              break;

              case 1 :                  /* wait for transient, calc Ri */
                  if (cntmod==10)
                  {
```

```
    vmod1 = vcap;
    r1 = (((-in5 - vmod0)<<16)/iref)>>4;
    model = 2;
    cntmod = 0;
    }
break;

case 2 :                    /* after dV = 0.05 volts calc Ci0 */
    vmod2 = vcap;
    if ((vmod2-vmod1)>40)
    {
    c0 = ((((cntmod*iref)/500)<<16)/(vmod2 - vmod1))>>4;
    model = 3;
    }
break;

case 3 :                    /* when vol=2v calc Ci1 */
    if (vcap>((20*4095/vbase)+(vmod1-vmod0)))
    {
    vmod2 = vcap;
    c1 = ((((cntmod*iref)/500)<<12)/(vmod2 - vmod1))-c0;
    c1 = c1*1638/(vmod2 - vmod1);
    model = 4;
    }
break;

case 4 :                    /* stop current at vmax */
    if (vcap>vmaxpu)
    {
    iref = 0;
    *pPortf = 0x01;
    cntmod = 0;
    model = 5;
    }
break;

case 5 :                    /* wait transient, start calc Rd */
    if (cntmod==10)
    {
    vmod0 = vcap;
    cntmod = 0;
    model = 6;
    }
break;

case 6 :                    /* after dv = 0.05 volts calc Rd */
    vmod1 = vcap;
    if ((vmod0-vmod1)>40)
    {
    cv = c0 + ((c1*(vmod0+vmod1))/1638);
    fac1= (cv*(vmod0-vmod1))>>12;
    r2 = (((((vmod0+vmod1)*cntmod)/500)<<13)/fac1)>>2;
    model = 7;
    }
break;

case 7 :                    /* after 3 min start calc of Cd */
    if (cntmod==90000)
    {
    vmod1 = vcap;
    model = 8;
    }
```

```
break;

case 8 :                    /* after dV = 0.05 volts calc Cd */
    vmod2 = vcap;
    if ((vmod1-vmod2)> 40)
    {
    cv = c0 + ((c1*(vmod2+vmod1))/1638);
    fac1=(((cv*(vmod1-vmod2))/(cntmod-90000))*500)>>12;
    fac1=(fac1*r2)>>12;
    fac1=((vmod1+vmod2)>>1)-fac1;
    cv = c0 + ((c1*vmod0)/1638);
    cv2 = c0 + ((c1*vmod1)/1638);
    c2 = (vmod0*cv)-(vmod1*cv2);
    c2 = c2/fac1;
    model = 9;
    }
break;

case 9 :                   /* after 3 min start calc r1 */
    if (cntmod==150000)
    {
    vmod0 = vcap;
    model = 10;
    }
break;

case 10 :                  /* after dV = 0.05 volts calc r1 */
    vmod1 = vcap;
    if ((vmod0-vmod1)>40)
    {
    cv = c0 + ((c1*(vmod0+vmod1))/1638);
    fac1= (cv*(vmod0-vmod1))>>12;
    r3 = ((((vmod0+vmod1)*(cntmod-150000)/500)<<11)/fac1);
    model = 11;
    }
break;

case 11 :                   /* after 30 min calc C1 */
    if (cntmod==900000)
    {
    vmod1 = vcap;
    cv = c0 + ((c1*vmod0)/1638);
    cv2 = c0 + ((c1*vmod1)/1638);
    c3 = (vmod0*cv)-(vmod1*cv2);
    c3 = c3/vmod1;
    model = 90;
    env = r1*10000;
    ch1 = 'R';
    ch2 = '1';
    }
break;

case 90 :                   /* send parameters to screen */
  kbstat = *pSCSR;
  if (kbstat & 0x0100)
  {
    switch(scrmod)
    {
    case 0:                 /* calculate param in real values */
        rb1= env/4095;
        rb2= rb1/1000;
        rb3= rb1-(rb2*1000);
```

```
    rb4= rb3/100;
    rb5= rb3-(rb4*100);
    rb6= rb5/10;
    rb7= rb5-(rb6*10);
    *pSCDR = ch1;
    scrmod = 1;
break;

case 1:                 /* sent each digit in ASCII */
    *pSCDR = ch2;
    scrmod = 2;
break;

case 2:
    *pSCDR = '=';
    scrmod = 3;
break;

case 3:
    *pSCDR = 0x30+rb2;
    scrmod = 4;
break;

case 4 :
    *pSCDR = 0x30+rb4;
    scrmod = 5;
break;

case 5 :
    *pSCDR = 0x30+rb6;
    scrmod = 6;
break;

case 6 :
    *pSCDR = 0x30+rb7;
    scrmod = 7;
break;

case 7 :
    *pSCDR = 0x0D;
    scrmod = 8;
break;

case 8 :                /* go to next parameter and repeat */
    *pSCDR = 0x0A;
    scrmod = 0;
    switch(elem)        /* gives parameter identification */
    {
    case 0:
       env = c0*10;  /* factor is based on pu value*/
       elem=1;
       ch1='C';
       ch2='0';
    break;
    case 1:
       env = c1*10;
       elem = 2;
       ch1='C';
       ch2='1';
    break;
    case 2:
       env = r2*100;
```

```
                        elem = 3;
                        ch1='R';
                        ch2='2';
                    break;
                    case 3:
                        env = c2*10;
                        elem = 4;
                        ch1='C';
                        ch2='2';
                    break;
                    case 4:
                        env = r3*100;
                        elem = 5;
                        ch1='R';
                        ch2='3';
                    break;
                    case 5:
                        env = c3*10;
                        elem = 6;
                        ch1='C';
                        ch2='3';
                    break;
                    case 6:
                        elem = 0;
                        modesel =1;
                        model = 0;
                        cntmod = 0;
                    break;
                    }                       /* end switch elem */
                break;
                }                           /* end switch scrmod */
              }                             /* end if port status */
            break;
        }                                   /* end switch model */
    }                                       /* end mode = 5 */

/* ------------ MODE 1, 22, 3, 4 OR 5 CURRENT CONTROL --------- */
    vcap = in6;                             /* cap volt input to vcap */
    out7 = in7;                             /* ifdb output ch 7 */
    out6 = vcap;                            /* vcap output ch 6 */
    out9 = iref;                            /* iref output ch 9 */
    out8 = pwcon;                           /* pwcon output ch 8 */

    if ((modesel==1)||(modesel==22)||(modesel==3)
       ||(modesel==4)||(modesel==5))
    {
        ifdb = in7;                         /* current regulator */
        encu = iref - ifdb;
        aux = encu - ((k2cu*e0cu) >> 12);
        e0cu = encu;
        aux = (k1cu*aux);                   /* begin 8.24 section */
        ksc = kscu;
        while (((aux < SLUcu) && (aux > SLLcu)) && (ksc > 0))
        { aux = (aux << 1);  ksc = ksc - 1; }
        uncu = u0cu + aux;
        if (uncu > LPcu) { uncu = LPcu; }
        if (uncu < LNcu) { uncu = LNcu; }
        u0cu = uncu;                        /* end 8.24 section */
        pwcon = (uncu >> 12);
    }

/* ------------------- CHOPPER PULSEWIDTH --------------------- */
```

```
/* update chopper pulsewidth, f(pwcon) pwcon must be limited to
   +/- amax to avoid malfunction of pulse width modulator */

      pwlcnt =  (swpercnt * ( 0x0FFF + pwcon)) >>13;

      swlocnt = ((pwlcnt - swotcnt) << 16)
                + ((swpercnt-pwlcnt+swotcnt) >> 1);
      swllcnt = ((pwlcnt + swotcnt) << 16)
                + ((swpercnt-pwlcnt-swotcnt) >> 1);

/* ------------------- DATA ADQUISITION RESPONSE ------------- */
      if ((datcol==7)&&(sent==7))      /* synchronize data collection */
      {                                /* with current source */
        timmer = timmer+1;
        if (timmer > 500)              /* 1 samp per second (500 * 2ms) */
        {
           kbstat = *pSCSR;            /* read port status */
           if (kbstat & 0x0100)
           {
              switch (cont)
              {
                case 0 :               /* calculate real value */
                  if (vcap<0)          /* send sign */
                  {
                  vcaps=-1*vcap;
                  *pSCDR = '-';
                  }
                  else
                  {
                  vcaps=vcap;
                  *pSCDR = '+';
                  }
                  ser1 = vbase*10*vcaps/4096;
                  ser2 = ser1/100;
                  ser3 = ser1 -(ser2*100);
                  ser4 = ser3/10;
                  ser5 = ser3 - (10*ser4);
                  cont = 1;            /* only valid if truncate result */
                break;
                case 1:                /* send ASCII code LSB first */
                  *pSCDR = 0x30+ser5;
                  cont = 2;
                break;
                case 2:
                  *pSCDR = 0x30+ser4;
                  cont = 3;
                break;
                case 3:
                  *pSCDR = 0x30+ser2;
                  cont = 4;
                break;
                case 4:                /* reset timmer and cycle */
                  timmer = timmer - 500;
                  cont = 0;
                break;
              }                        /* end switch */
           }                           /* end if kbstat */
        }                              /* end if timmer */
      }                                /* end data transmision */

/* ----------------------- KEYBOARD INTERFACE --------------- */
      /* keyboard interface, input in succesive loop cycles keyboard
```

```
         input, req. time < 40 usec, placing at end of loop, means
         update of variables in next loop; it avoids cumulative extra
         loop time for keybl_io routine and update procedure
      */

      if ((kbflg == 0xAA)||(kbflg == 0x11)) { kbflg = 0x55; }
      keybl_io(&kbflg,&letter,&val,&valf);
      if (kbflg == 0x33)
            {datcol = 7;}              /* data colection start */
      if (kbflg == 0x11)
            {datcol = 1; sent = 1;}    /* data collection stop */
      if (kbflg == 0xAA)               /* kbflg given by keybl_io */
      {
         switch (letter)               /* letter pressed in keyboard */
         {
/* ---------------- parameter input selection ----------------- */
            case 'v':
            param = 7;
            break;

/* ----------------- kind of cap test input ------------------- */
            case 'g':
            u0cu = 0; uncu = 0; e0cu = 0; encu = 0;
            fsel = val;                /* letter g to test val selects */
            break;

/* -------------------- mode selection ------------------------ */
            case 'M':
            u0cu = 0; uncu = 0; e0cu = 0; encu = 0;
            modesel = val;
            if (val==4)                /* mode 4 setup */
            {
               ciclo1 = 0;
               if (vcap < vdespu)
               factor= 1;
               else if (vcap > vdespu)
               factor = -1;
               else factor = 0;
            }
            else if (val==3)           /* mode 3 setup */
            {
               ciclo = 0;
               vlim = ((25<<16)/(10*vbase))>>4;
               vcapo = vcap;
               if ((vcap < vlim) && (vcap > 0)) {ciclo = 99;}
            }
            break;

/* ---------------- pw input for modes 21 and 22 -------------- */

            case 'p':                  /* input in  xxx.x %  of pwmax */
            if (val > 100) { val = 100; }
            if (val < (-100)) { val = (-100); }
            x1 = ((0x0028F333*val) + (0x00041852*valf)) >> 16;
            vav3 = ( x1 * amax ) >> 12;
            break;

/* ------------------- sine frequency control ----------------- */
            case 'f':                  /* input in  xxx.x %  of fsmax */
            if (val > 100) { val = 100; }
            if (val < (-100)) { val = (-100); }
            x1 = ((0x0028F333*val) + (0x00041852*valf)) >> 16;
```

```
                phiincr =( ((swpercnt*4*x1) >> 12) *fsmax) >> 5;
                                        /* shift 5 because Tsa/Tsw = 8 */
                break;

   /* -------------------- sine amplitude control --------------- */
                case 'a':               /* input in  xxx.x %  of amax */
                if (val > 100) { val = 100; }
                if (val < (-100)) { val = (-100); }
                x1 = ((0x0028F333*val) + (0x00041852*valf)) >> 16;
                ams = ( x1 * amax ) >> 12;
                break;

   /* -------------------- gating control ---------------------- */
                case 'R':
                *pHSRR0 = 0x0001;       /* Run ch8 DIO high */
                break;

                case 'S':
                *pHSRR0 = 0x0002;       /* Stop ch8 DIO low */
                *pPortf = 0x01;         /* gating off,no inv */
                break;

                case 'G':
                *pPortf = 0x01;         /* gating off,no inv */
                if (val == 11)
                { *pPortf = 0x0D;}      /* gating on */
                break;
           }                            /* end switch letter */
        }                               /* end keyb input */

   /* ---------------------- PROGRAM EXIT ---------------------- */
        if (letter == 'E')
        {
             mlo = 0;
             letter = 0xEE;
             *pHSRR0 = 0x0002;          /* Stop ch8 DIO low */
             *pPortf = 0x01;            /* gating off,no inv */
        }
        tepla4();
  }                                     /* end program LOOP mlo == 2 */
}
/* ======================== END MAIN PROGRAM  ==================== */
```

C.2 SERIES CONNECTION TEST PROGRAM

```
/* sercap.c */
/* 10/8/96  R.Bonert,  L.Zubieta */

/* program
   up to 10 ultra capacitor connected in series testing
   uses 4Q chopper (4qch.c), fsw 4 kHz, Tsa 500 usec
   with VSI module : switches S1,S4 and S5,S2 used

   switch names                 TPU channels
   1o  2o       -> s1  s5  -> ch2  ch6
   1l  2l          s4  s2     ch3  ch7
   ch 0 switch period
   ch 1 interrupt period
```

```
    ch 2,3 & 6,7 gating channels
    ch 8-D DIO out

    data I/O :
    in  : ifdb current feedback                    ch7
          vcap(n) multiplexed capacitor voltage    ch6

    out : iref           ch9
          pwcon          ch8
          ifdb           ch7
          higher vcap    ch6

    program operation :
    there are three basic modes selected by keyb Mxxx
    1    capacitor testing (default)
    21   chopper test pw control, man & sine
    22   chopper test current loop (20ms), man & sine

    keyb controls :
    Mxx     mode selection 1,21,22.
    G       gating on/off G11 = on, Gx = off
    R       run   inverter (switch signal DIO ch 8 = 1)
    S       stop  DIO ch8 = 0 and gating off

    in chopper test mode
    p       pw control in %  +100 to -100, keyb input
    a,f     automatic control of pw, sine f = 0.1..100Hz
            a 0..100%, pw = p  +  sine
            in test mode 22 current control
            p,a,f provide the per unit current reference

    parameter input for charge control :
    v      ?x  v-1.y  y selects parameter to be set
           ?0  vxxx.xx  ibase in A
           ?1  vxxx.xx  icharge in A
           ?2  vxxx.xx  idischarge in A
           ?3  vxxx.xx  vbase in V
           ?4  vxxx.xx  vmax in V
           ?5  vxxx.xx  vmin in V (negative)
           ?6  vxxx.xx  number of capacitors in series
           ?7  vxxx.xx  number of cycles = xxx.xx
           ?8  vxxx.xx  pause in sec
           ?9  vxxx.xx  charge time in sec

    in capacitor test mode
    gxx     0   iref =0, gating off
           10   charge to vmax
           20   discharge to vmin
           30   timed charge, max vmax
           40   timed discharge, min vmin
           50   cycled charging vmax,vmin
           60   charge to vmax after pause delay
*/

#include "memap332.h"                    /* hardware memory map  */
#include "tabsin.h"                      /* table sine function 0-360 */

/* ==================== CONSTANTS, VARIABLES ====================== */

  /* --------------------- GLOBAL VARIABLES --------------------- */

  /* ----- variables for data transfer to interrupt routines ---- */
```

```
unsigned short ka, loopflg;
unsigned short ilpcnt, multi1, multi2;
signed int     in0,in1,in2,in3,in4,in5,in6,in7,
               out3,out4,out5,out6,out7,out8,out9;
unsigned int   swlocnt,swllcnt;

  /* ---------------- variables for table look up --------------- */
unsigned int   tabpos;
signed short   tabres;


/* ======================== EXTERNAL FUNCTIONS ==================== */

extern void    pp_setup(),qsms870(),keybl_io();

/* ================= FUNCTIONS & INTERRUPT ROUTINES ============== */

  /* ----------------------- INT TPU CH 1 ----------------------- */
#pragma interrupt()
void dio_samp()
{

        /* interrupt TPU ch 1 for transfer of pwm data for next
           interval timing of sampling and I/O through QSPI analog
           input last cycle, analog output and telegrams in next cycle.
           analog I/O data format:
           for fxp 1.0 p.u. ->  signed short var = *pRXDF >> 3;
           write fxp to ch  *pTXDE = (signed short var fxp) > 1;

           if program QSMs870 is used, then :
               analog in : ch 7,..6,..5,..4,..3,..2,..1,..0
                           *pRXD F,..C,..9,..6,..4,..2,..1,..0
               analog out : ch 7..6..5..4..3..9..8
                           *pTXD E..D..B..A..7..5..8
        */

        ilpcnt = ilpcnt + 1;
        switch(ilpcnt)
        {
                case 4 :                    /* start QSM single shot */
                *pSPCR1  = 0x901A;
                break;

                case 6 :                    /* start QSM again to provide data
                *pSPCR1  = 0x901A;             sampled the last 0.5 msec */
                break;

                case 8 :                    /* Tloop 2 msec */
                *pPADR = 0X00;              /* Parallel port reset overlap */
                *pPCDR = 0X00;
  /* ---------------------- pwm data transfer ------------------- */
                *pCH2p46  = swlocnt;        /* switch data next per */
                *pCH3p46  = swllcnt;        /* coherent write */
                *pCH6p46  = swllcnt;
                *pCH7p46  = swlocnt;

  /* ------------------------ analog inputs --------------------- */
                in7 = *pRXDF >> 3;          /* ch7 ifdb */
                in6 = *pRXDC >> 3;          /* ch6 vcap total */
                in5 = *pRXD9 >> 3;
                in4 = *pRXD6 >> 3;
                in3 = *pRXD4 >> 3;
```

```
  /* ------------------------ analog outputs ------------------- */
                *pTXD5 = out9 >> 1;       /* iref out to ch 9 */
                *pTXD8 = out8 >> 1;       /* pwcon out to ch 8 */
                *pTXDE = out7 >> 1;       /* ifdb out to ch 7 */
                *pTXDD = out6 >> 1;       /* vcap out to ch 6 */
                *pTXDB = out5 >> 1;       /* vcap2 ch 5 */
                *pTXDA = out4 >> 1;
                *pTXD7 = out3 >> 1;

                *pPADR = multi1;          /* Parallel port selection */
                *pPCDR = multi2;

  /* --------------------- set start flag algorithm loop -------- */
                loopflg = 0x1111;
                ilpcnt = 0;
                break;
        }                                 /* end switch ilpcnt */
        ka = *pCISR; *pCISR = 0xFFFD;     /* clear int ch1 */
}                                         /* end dio_samp */

/* ============================ PROGRAM ============================== */
main(void)
{
  /* ------------ VARIABLES GENERAL INFRAESTRUCTURE ------------- */

  /* -------------------- for keyboard input -------------------- */
static unsigned char  letter;
static unsigned char  kbflg = 0x55;
static signed int     val,valf,cont;
static unsigned short kbstat,cond;
static unsigned short parout;

  /* ------------------------- for loop ------------------------- */
static unsigned int   mlo,fsa10;
static unsigned short TEflg;

  /* --------------------variables spec. program ---------------*/
static unsigned int   swpercnt,swotcnt,fsmax,pwlcnt,phi1,phiincr,m1,m2,
                      cntdio,modesel,cntp,fsel,nextfsel,gstcnt,cnt31,
                      cnt41,cnt55,cnt56,kscu,ksc,ciclo,ciclo1,
                      nbcyc,pause,paucnt,chrgtime,chtcnt,capnum;
static signed int     pwcon,vav1,vav2,vav3,ams,amax,x1,x2,x3,x4,x5,aux,aux1,
                      aux2,iref,ifdb,SLUcu,SLLcu,ban,uncu,u0cu,encu,e0cu,
                      k1cu,k2cu,LPcu,LNcu,ibase,ichrg,idischrg,vbase,vmax,
                      vmin,vcap,ichpu,idispu,vmaxpu,vminpu,vlim,vdes,vdespu,
                      ser1,ser2,ser3,ser4,ser5,factor,vcaps,vcapo,vcapd;

  /* -------------------- for model obtention -------------------*/
static unsigned int   cntmod,model,scrmod,elem,vt;
static signed int     vmod0,vmod1,vmod2,r1,r2,r3,c0,c1,c2,c3,
                      rb1,rb2,rb3,rb4,rb5,rb6,rb7,fac1,env;
static unsigned char  ch1,ch2;

static unsigned short multi, numser,n,i,timmer;
static signed int     volt[16];

  /* ------------------ SET UP - START INFRASTRUCTURE ----------- */

        *pPfpar = 0x00F0;                 /* set pin 3-0 up as port F */
        *pDdrf  = 0x000F;                 /* pin 3-0 out  */
                                          /* IRQ 7-4 still operative */
```

```
  /* ------------- setup parallel port M68230 on GPC-board ------ */
       pp_setup();                          /* PA out,PB in,PC out for PLD */

  /* ---- program of PLD U14 controls of ch2..D see chopper ----- */
       *pPortf = 0x01;                      /* gating off, 0x0D -> gating on */
       *pPCDR = 0x99;

  /* ------------------- initialize and start QSM --------------- */
       qsms870();                           /* Ts=180+byte*9.5, byte>=9 */

  /* ------ init D/A output data,run one cycle to set flag ------ */
       *pTXDE = 0;       *pTXDD = 0;        *pTXDB = 0;
       *pTXD8 = 0;       *pTXD7 = 0;        *pTXD5 = 0;
       *pTXDA = 0;
       *pSPCR1  = 0x901A;
  /* ---------- start QSM, Ts = 427usec < Tsa = 500 usec -------- */
        fsa10 = 50;                        /* algorithm frequency/10 */
        TEflg = *pSPSR;                     /* test end of QSM cycle */
        while ((TEflg & 0x80) == 0 )
          { TEflg = *pSPSR;}


  /* --------------------- TPU SET UP --------------------------- */
       *pTMCR = 0x00C1;                     /* 0.24 usec; int ID $1, presc = 1
                                               -> 16.777216 MHz/4 */
       *pTICR = 0x0640;                     /* int 6, intv $4x -> $100 offset */
                                            /* CAUTION 332Bug trap at $108 ! */

/* description of channel functions :
        ch 0 SPWM mode 2 links
        ch 1 SPWM mode 0 or 1 sync to ch 0
        ch 2,3  & 6,7 SPWM mode 1
        ch 4,5 DIO set to zero !
        ch 8..D DIO  */

  /* ---- values for setup of timing pattern : PWM & control ---- */
       swpercnt = 1048;                     /* 4194 = 1 kHz = fsw
                                               2097 = 2 kHz, 1048 = 4 kHz
                                               1398 = 3 kHz, 466 = 9 kHz
                                               9 kHz very limited pw range */
       fsmax = 100;                         /* in Hz fmax < fsw/15 */
       amax = 0x0EA0;                       /* <- estimate for 4 kHz
                                               3 kHz 0x0F09
                                               9 kHz 0x0DEB
                                               1 kHz 0x0FAD */
       phi1 = 0;                            /* phi per unit = 0xFFFF due to
                                               table structure */
       x1 = (0x00041852*2) >> 16;
       phiincr =( ((swpercnt*4*x1) >> 12) *fsmax) >> 8;
                                            /* start frequency 0.2 % of fmax
                                               incr = 0xFFFF * Tsw * fsine */
       phiincr = phiincr * 2;               /* Tsa/Tsw = 2 */

       x2 = (0x0028F333*1) >> 16;
       ams = (amax * x2) >> 12;             /* start amplitude 1% of amax */

       swotcnt = 26;                        /* 7 usec switch over time */

      /* pw ideal, pwo upper sw, pwl lower sw, phases 1,2,3
           init average voltage vav 0.2 %
           phase 1 at zero crossing */
       vav1 = ams; vav2 = ams; vav3 = ams;
```

```
 pwlcnt =  (swpercnt * ( 0x0FFF + vavl)) >>13;
              /* (swpercnt * (1+vavl)/2) >> 12  */

 swlocnt = ((pwlcnt - swotcnt) << 16)
             + ((swpercnt-pwlcnt+swotcnt) >> 1);
 swllcnt = ((pwlcnt + swotcnt) << 16)
             + ((swpercnt-pwlcnt-swotcnt) >> 1);

  /* set up parameter registers */

  /* ch0 SPWM mode 2 , switch interval timing */
   *pCH0pr0  =  0x0092;   /* f low, TCR1 */
   *pCH0p46 = ((swpercnt >> 1) << 16) + swpercnt;
     /* coherent write, hightime = swpercnt/2 */
   *pCH0pr8  =  0x660E;   /* L st L cnt, dummy adr */
   *pCH0prA  =  0;        /* delay, only on start */

  /* ch1 SPWM mode 1 , QSM algorithm timing */
    *pCH1pr0  =  0x0092;   /* f low, TCR1 */
     /* Tch4 = Tch5 */
    *pCH1p46  = ( 0x00640000 + (swpercnt-200));
     /* coherent write, hightime 25 usec, del -50 usec
        check whether int finishes before ch0 rising edge */
    *pCH1pr8  =  0x0200;    /* adr 1, adr 2 ch 0 */

/* ch2 = switch 1o, SPWM mode 1 linked */
 *pCH2pr0  =  0x0092;   /* f low, TCR1 */
 *pCH2p46  = swlocnt;   /* coherent write , pw, del */
 *pCH2pr8  =  0x0200;   /* adr1, adr2 of ch 0 */

/* ch3 = switch 1l, SPWM mode 1 linked */
 *pCH3pr0  =  0x0092;   /* f low, TCR1 */
 *pCH3p46  = swllcnt;   /* coherent write, pw, del */
 *pCH3pr8  =  0x0200;   /* adr1, adr2 of ch 0 */

/* ch6 = switch 3o, SPWM mode 1 linked */
 *pCH6pr0  =  0x0092;   /* f low, TCR1 */
 *pCH6p46  = swllcnt;   /* coherent write , pw, del */
 *pCH6pr8  =  0x0200;   /* adr1, adr2 of ch 0 */

/* ch7 = switch 31, SPWM mode 1 linked */
 *pCH7pr0  =  0x0092;   /* f low, TCR1 */
 *pCH7p46  = swlocnt;   /* coherent write, pw, del */
 *pCH7pr8  =  0x0200;   /* adr1, adr2 of ch 0 */

/* ch 4,5  9..D DIO,  no parameter reg. */


 /* channel function registers group ch F..8 */
   *pCFSR0 = 0x0088;    /* ch D,C DIO */
   *pCFSR1 = 0x8888;    /* ch B..8 DIO */
   *pCPR0  = 0x0555;   /* ch D..8 low pri */
   *pHSQR0 = 0x0AAA;   /* ch D..8 upd on HSR */

 /* channel function registers group ch 7..0 */
   *pCFSR2  =  0x7788;   /* ch 7,6 SPWM 5,4 DIO */
   *pCFSR3  =  0x7777;   /* ch 3..0 SPWM */
   *pCPR1   =  0xF5FF;   /* ch 7,6 3..0  hi prio */
   *pHSQR1  =  0x5A56;   /* ch7,6 3..1 m 1,ch0 m2 */

   *pHSRR0 = 0x0002; /* Stop inverter, ch8 DIO low,
                        gating must be set off */
```

```
        /* set ch5,4 low no gating, caution ch5 inv */
           *pHSRR1 = 0x0600;

      /* set up int -> ch1 low-high (dio-samp) */
           ka = *pCISR; *pCISR = 0xFFFD; /* clear int bit ch1 */
           *pCIER   =  0x0002;   /* enable ch1 int */
           asm("  move.w  #$2500,SR ");
             /* int vec ch1 offset 0x41 * 4 = 0x104 */

        /* intialize/start  channel function reg ch F..8 */
          *pHSRR0 = 0x0FFF;  /* init ch D..8 */

        /* intialize/start  channel function reg ch 7..0 */
           *pHSRR1  =  0xAFAA;   /* init ch7..0 */


     /* =========  end init and set up TPU ================== */

     /* other initializations */
           loopflg = 0x8888; ilpcnt = 0; /* interrupt loop */
           cntdio = 0; cntp =0; fsel = 0;
           modesel = 21; /* chopper control by keyb */
           ciclo = 0;  ciclo1 = 0; vt = 1;
           cont = 0; cntmod = 0; model = 0; scrmod = 0; elem=0;
           capnum = 0; multi=1; multi1=0; multi2=0; numser=2;
           n=0; vdes=1; timmer=1;

      /* init PI regulator high res */
         u0cu = 0; uncu = 0; e0cu = 0; encu = 0;
         k1cu =  0x083D;   /* gain 12*Tr, Tr 0.015, Ts 2 msec */
         k2cu =  0x0F8C;   /* use pico to det const */
         kscu =  0;
         SLUcu = 0x02000000; SLLcu = 0xFE000000;
         LPcu = amax << 12;  /* old 0x0F80000;  96%  */
         LNcu = (-amax) << 12; /* old 0xFF800000;  -54% */

      /* init parameters non dangerous, in case input forgotten ! */


     /* ================================================  */

/* ========================== PROGRAM LOOP ======================== */
mlo = 2;   /* LOOP */
while (mlo == 2)
{
        while (loopflg == 0X8888) { }    /* test for end of int */
        loopflg = 0x8888;

        TEflg = *pSPSR;                  /* test end of QSI cycle */
        if ((TEflg & 0x80) == 0 )
        { letter = 'E'; }                /* exit to monitor */
        *pSPSR = 0x7F;


  /* --------------------- GATING CONTROL ---------------------- */
        if ((kbflg == 0xAA) && (letter == 'R'))
        { *pHSRR0 = 0x0001;}             /* Run ch8 DIO high */
        if ((kbflg == 0xAA) && (letter == 'S'))
        {
                *pHSRR0 = 0x0001;        /* Stop ch8 DIO low */
                *pPortf = 0x01;          /* gating off,no inv */
        }
```

```
        if ((kbflg == 0xAA) && (letter == 'G'))
        {
                *pPortf = 0x01;           /* gating off,no inv */
                if (val == 11)
                { *pPortf = 0x0D;}        /* gating on */
        }


/* ---------------------- MULTIPLEXED INPUT ---------------------- */
        multi = multi << 1;
        if (multi == numser)  {multi = 1;}
        multi1 = (multi & 0x00FF);
        multi2 = (multi & 0xFF00)>>8;
        out7 = in7;                       /* output ch 7 */
        out9 = iref;                      /* output ch 9 */
        out8 = pwcon;                     /* output ch 8 */
        if (n<(vdes-1))
        {volt[n]=in6;n=n+1;}
        else
        {
        volt[n]=in6;
        n=0;
        vcap=in6;
        out6=vcap;
        for (i=0;i<vdes;i++)
        {if (volt[i]>vcap)  { vcap=volt[i]; }}
        vcapd = in6;
        for (i=0;i<vdes;i++)
        {if (volt[i]<vcapd)  { vcapd=volt[i]; }}
        }

/* ---------------------- PARAMETERS INPUT ---------------------- */
        if ((kbflg == 0xAA) && (letter == 'v'))
        {
        if (val<0)
             {
                cntp = -valf;
                parout = 0x30+cntp;
                kbstat = *pSCSR;
                if (kbstat & 0x0100) { *pSCDR = parout; }
             }
        else
             {
                switch(cntp)
                {
                case 0 :                  /* i base input */
                    *pSCDR = '1';
                    ibase = val*10+valf;
                    cntp = cntp + 1;
                break;

                case 1 :                  /* i charge input */
                    *pSCDR = '2';
                    ichrg = (val*10+valf) << 16;
                    ichpu = (ichrg/ibase) >> 4;
                    cntp = cntp + 1;
                break;

                case 2 :                  /* i discharge input */
                    *pSCDR = '3';
                    idischrg = (val*10+valf) << 16;
                    idispu = (idischrg/ibase) >> 4;
```

```
                cntp = cntp + 1;
            break;

            case 3 :                    /* v base input */
                *pSCDR = '4';
                vbase = val*10+valf;
                cntp = cntp + 1;
            break;

            case 4 :                    /* v max input */
                *pSCDR = '5';
                vmax = (val*10+valf) << 16;
                vmaxpu = (vmax/vbase) >> 4;
                cntp = cntp + 1;
            break;

            case 5 :                    /* v min (negative) input */
                *pSCDR = '6';
                vmin = (val*10+valf) << 16;
                vminpu = (-1*vmin/vbase) >> 4;
                cntp = cntp + 1;
            break;

            case 6 :                    /* number of cap. in series */
                *pSCDR = '7';
                vdes = val;
                numser = 1 << vdes;
                cntp = cntp + 1;
            break;

            case 7 :                    /* number of cycles input */
                *pSCDR = '8';
                nbcyc = val;
                cntp = cntp + 1;
            break;

            case 8 :                    /* pause time input */
                *pSCDR = '9';
                pause = val*10+valf;
                paucnt = pause*fsa10;
                cntp = cntp + 1;
            break;

            case 9 :                    /* time of (dis)charge input */
                *pSCDR = '0';
                chrgtime = val*10+valf;
                chtcnt = chrgtime*fsa10;
                cntp = 0;
            break;
            }                           /* end switch cntp */
        }
    }


/* ----------------- MODE 1 CAPACITOR TEST OPTIONS ------------ */
    if (modesel==1)
    {
        if ((kbflg == 0xAA) && (letter == 'g'))
        { fsel = val; }
        switch(fsel)
            {
            case 0 :                    /* gating delayed off */
```

```
    iref = 0;
    fsel = 800;
    nextfsel = 210;
    gstcnt = 30;
break;

case 10 :                    /* charge to vmax */
    *pPortf = 0x0D;
    iref = ichpu;
    fsel = 11;
break;

case 11 :                    /* terminate at v max */
    if (vcap > vmaxpu)
      {
      iref = 0;
      gstcnt = 30;
      fsel = 800;
      nextfsel = 210;
      }
break;

case 20 :                    /* discharge to vmin */
    *pPortf = 0x0D;
    iref = -idispu;
    fsel = 21;
break;

case 21 :                    /* terminate at v min */
    if (vcapd < vminpu)
      {
      iref = 0;
      gstcnt = 30;
      fsel = 800;
      nextfsel = 210;
      }
break;

case 30 :                    /* timed charge */
    *pPortf = 0x0D;
    iref = ichpu;
    cnt31 = chtcnt;
    fsel = 31;
break;

case 31 :                    /* terminate at chgtime or v max */
    cnt31 = cnt31-1;
    if ((vcap > vmaxpu)||(cnt31==0))
      {
      iref = 0;
      gstcnt = 30;
      fsel = 800;
      nextfsel = 210;
      }
break;

case 40 :                    /* timed discharge */
    *pPortf = 0x0D;
    iref = -idispu;
    cnt41 = chtcnt;
    fsel = 41;
break;
```

```
case 41 :                    /* terminate at chgtime or vmin*/
    cnt41 = cnt41-1;
    if ((vcapd < vminpu)||(cnt41==0))
      {
      iref = 0;
      gstcnt = 30;
      fsel = 800;
      nextfsel = 210;
      }
break;

case 50 :                    /* cycling between vmax,vmin */
    iref = ichpu;
    *pPortf = 0x0D;
    cnt55 = 30000;
    fsel = 51;
    cnt56 = nbcyc;
break;

case 59 :                    /* pause delay */
    cnt55 = cnt55-1;
    if (cnt55 ==0)  { fsel = 58; }
break;

case 58 :                    /* charge to v max */
    *pPortf = 0x0D;
    iref = ichpu;
    fsel = 51;
break;

case 51 :                    /* terminate at v max */
    if (vcap > vmaxpu)
      {
      iref = 0;
      timmer = 600;
      gstcnt = 30;
      cnt55 = paucnt;
      cnt55 = 1;
      fsel = 800;
      nextfsel = 52;
      }
break;

case 52 :                    /* pause delay */
    cnt55 = cnt55-1;
    if (cnt55 ==0) { fsel = 53; }
break;

case 53 :                    /* discharge to vmin */
    *pPortf = 0x0D;
    iref = -idispu;
    fsel = 54;
break;

case 54 :                    /* terminate at v min */
    if (vcapd < vminpu)
      {
      iref = 0;
      gstcnt = 30;
      cnt55 = paucnt;
      cnt55 = 1;
      fsel = 800;
```

```
                    nextfsel = 55;
                    }
                break;

                case 55 :                   /* pause delay */
                    cnt55 = cnt55-1;
                    if (cnt55 ==0) { fsel = 56; }
                break;

                case 56 :                   /* cycle repetition */
                    cnt56 = cnt56-1;
                    if (cnt56 == 0) { fsel = 210; }
                    else { fsel = 58; }
                break;

                case 60 :                   /* charge to v max after delay */
                    iref = 0;
                    cnt55 = paucnt;
                    fsel = 800;
                    gstcnt = 30;
                    nextfsel = 61;
                break;

                case 61 :                   /* pause delay */
                    cnt55 = cnt55-1;
                    if (cnt55 ==0) {fsel = 62;}
                break;

                case 62 :                   /* charge to v max */
                    *pPortf = 0x0D;
                    iref = ichpu;
                    fsel = 63;
                break;

                case 63 :                   /* terminate at v max */
                    if (vcap > vmaxpu)
                      {
                      iref = 0;
                      gstcnt = 30;
                      fsel = 800;
                      nextfsel = 210;
                      }
                break;

                case 800 :                  /* gating delayed off */
                    gstcnt = gstcnt-1;
                    if (gstcnt==0)
                    {
                    *pPortf = 0x01;
                    fsel = nextfsel;
                    }
                break;

                case 210 :                  /* do nothing */
                break;
                }                           /* end switch fsel */
        }

/* ------------------ MODE 21 OR 22 CHOPPER TEST -------------- */
        if ((modesel==21)||(modesel==22))
        {
             if ((kbflg == 0xAA) && (letter == 'p'))
```

```
            {                                   /* input in  xxx.x %  of pwmax */
              if (val > 100) { val = 100; }
              if (val < (-100)) { val = (-100); }
              x1 = ((0x0028F333*val) + (0x00041852*valf)) >> 16;
              vav3 = ( x1 * amax ) >> 12;
            }
/* ------------------- sine frequency control ----------------- */
            if ((kbflg == 0xAA) && (letter == 'f'))
            {                                   /* input in  xxx.x %  of fsmax */
              if (val > 100) { val = 100; }
              if (val < (-100)) { val = (-100); }
              x1 = ((0x0028F333*val) + (0x00041852*valf)) >> 16;
              phiincr =( ((swpercnt*4*x1) >> 12) *fsmax) >> 7;
            }
/* -------------------- sine amplitude control ---------------- */
            if ((kbflg == 0xAA) && (letter == 'a'))
            {                                   /* input in  xxx.x %  of amax */
              if (val > 100) { val = 100; }
              if (val < (-100)) { val = (-100); }
              x1 = ((0x0028F333*val) + (0x00041852*valf)) >> 16;
              ams = ( x1 * amax ) >> 12;
            }
/* ---------------- getting sine functions from table --------- */
            phi1 = phi1 + phiincr;      /* phi 360 deg. -> FFFF */
            tabpos = phi1;
            asm( " move.l _tabpos,D0 " );
            asm( " TBLS.W _sintab,D0 " );
            asm( " move.w D0,_tabres" );
            vav2 = (ams * tabres) >> 12;
            vav1 = vav3+vav2;
            if (vav1 > amax) { vav1 = amax; }
            if (vav1 < (-amax)) { vav1 = (-amax); }
            if (modesel==21) { pwcon = vav1; iref = 0; }
            if (modesel==22) { iref = vav1; pwcon = 0; }
                                    /* vav1 -> pwcon in mode 21
                                       must be limited to avoid
                                       malfunction of the pwm */
                                    /* vav1 -> iref could be +/-
                                       1 p.u., but for test purposes
                                       vav1 is used */
      }


/* ------------ MODE 1, OR 22 CURRENT CONTROL --------- */


      if ((modesel==1)||(modesel==22))
      {

            ifdb = in7;                     /* current regulator */
            encu = iref - ifdb;
            aux = encu - ((k2cu*e0cu) >> 12);
            e0cu = encu;
            aux = (k1cu*aux);               /* begin 8.24 section */
            ksc = kscu;
            while (((aux < SLUcu) && (aux > SLLcu)) && (ksc > 0))
            { aux = (aux << 1);  ksc = ksc - 1; }
            uncu = u0cu + aux;
            if (uncu > LPcu) { uncu = LPcu; }
            if (uncu < LNcu) { uncu = LNcu; }
            u0cu = uncu;                    /* end 8.24 section */
            pwcon = (uncu >> 12);
```

```
      }


/* ------------------- CHOPPER PULSEWIDTH ---------------------- */
/* update chopper pulsewidth, f(pwcon) pwcon must be limited to
   +/- amax to avoid malfunction of pulse width modulator */

      pwlcnt =  (swpercnt * ( 0x0FFF + pwcon)) >>13;

      swlocnt = ((pwlcnt - swotcnt) << 16)
                + ((swpercnt-pwlcnt+swotcnt) >> 1);
      swllcnt = ((pwlcnt + swotcnt) << 16)
                + ((swpercnt-pwlcnt-swotcnt) >> 1);


/* -------------------- MODE SELECTION ------------------------ */
      if ((kbflg == 0xAA) && (letter == 'M'))
      { /* modesel 1 -> cap testing
                                21 -> man chopper control pw
                                22 -> man current loop test
                        for 21,22 cmd = keyb + sine(a,f) */
           if ((val==1)||(val==21)||(val==22))  {modesel = val;}
      }

/* ------------------- DATA ADQUISITION RESPONSE ------------- */
      if (kbflg == 0x33)
      {
      /*timmer = timmer+1;*/
      if (timmer > 500)
      {
           cond = *pSCSR;
           if (cond & 0x0100)
           {
              switch (cont)
              {
                case 0 :
                  if (capnum<vdes)
                  {
                  vcaps=volt[capnum];
                  if (vcaps<0)
                  {
                  vcaps=-1*vcaps;
                  *pSCDR = '-';
                  }
                  else
                  {
                  *pSCDR = '+';
                  }
                  ser1 = vbase*10*vcaps/4096;
                  ser2 = ser1/100;
                  ser3 = ser1 -(ser2*100);
                  ser4 = ser3/10;
                  ser5 = ser3 - (10*ser4);
                  capnum=capnum+1;
                  cont = 1;
                  }
                  else
                  {
                  timmer = timmer-500;
                  capnum = 0;
                  }
```

```
                    break;
                    case 1:
                      *pSCDR = 0x30+ser5;
                      cont = 2;
                    break;
                    case 2:
                      *pSCDR = 0x30+ser4;
                      cont = 3;
                    break;
                    case 3:
                      *pSCDR = 0x30+ser2;
                      cont = 0;
                    break;
                  }
               }
          }
          }

   /* ----------------------- PROGRAM EXIT ---------------------- */
          if (letter == 'E')
          {
               mlo = 0;
               letter = 0xEE;
               *pHSRR0 = 0x0001;          /* Stop ch8 DIO low */
               *pPortf = 0x01;            /* gating off,no inv */ }


   /* ------------------------ KEYBOARD INTERFACE ---------------- */
   /* keyboard interface, input in succesive loop cycles keyboard
      input, req. time < 40 usec, placing at end of loop, means
      update of variables in next loop; it avoids cumulative extra
      loop time for keyb1_io routine and! update procedure */

          if (kbflg == 0xAA) { kbflg = 0x55; }
          keyb1_io(&kbflg,&letter,&val,&valf);

 }                                        /* end program LOOP mlo == 2 */

}

/* ============================ END MAIN PROGRAM  ================== */
```

C.3 PASCAL PROGRAM FOR DATA ACQUISITION

```
{CAPA1.PAS}
{LUIS E. ZUBIETA  21/05/1996}
{GENERAL DATA ADQUISICION PROGRAM SINCHRONIZED BY THE GPC UNIT.
THE PROGRAM WAS DEVELOPED TO BE USED WITH THE GPC BOARD.
THE GPC SOFTWARE SHOULD USE KEYB1_IO.O IN ORDER TO RECOGNIZE THE INTERFASE}
{THE COMMUNICATION PROTOCOLE IS THE FOLLOWING:
THE PC SENDS A 'd' ASCII TO START THE DATA COLLECTION.
THE GPC SENDS EACH SECOND 4 ASCII VALUES; FIRST THE SIGN (+ OR -) AND THEN
THREE ASCII NUMERICAL DIGITS}

{$M 2000,0,0}
{$R-,S-,I-,D+,F+,V-,B-,N-,L+}
PROGRAM CAPA2;
USES CRT,DOS;
```

```
CONST
SEGMENTO:INTEGER=0;
DATOS=$02F8;
IER=$02F9;
LCR=$02FB;
MCR=$02FC;
LSR=$02FD;
MDM=$02FE;
INT=$21;
PARAMETROS=$E7;
LONBUF=128;

VAR
CARTOT,ENTRADA,SALIDA:WORD;
DATA:TEXT;
SEC,CADENA:INTEGER;
RXD,SIGN:INTEGER;
VOLT:REAL;
BUFFER:ARRAY[1..LONBUF] OF CHAR;
BUFF2:ARRAY[1..4] OF CHAR;
NUMERO:STRING[3];
VECTOR:POINTER;
REGS:REGISTERS;


{*************************************************************************
          THIS PROCEDURE STORE THE DATA IN THE FILE CAPA.DAT
*************************************************************************}
PROCEDURE ALMA;
BEGIN
     VOLT:= SIGN*RXD/100;
     WRITE(DATA,VOLT:2:2);
     WRITE(DATA,' , ');
     WRITELN(DATA,SEC);
END;

{*************************************************************************
        THIS PROCEDURE OBTAINS, USING THE SERIAL PORT, THE DATA
                          FROM THE  GPC
*************************************************************************}
PROCEDURE RECEPCION; INTERRUPT;
BEGIN
     INLINE($FB);
     IF (CARTOT < LONBUF) THEN
     BEGIN
          BUFFER[ENTRADA]:=CHAR(PORT[DATOS]);
          IF (ENTRADA < LONBUF) THEN INC(ENTRADA,1)
          ELSE ENTRADA := 1;
          INC(CARTOT,1);
     END;
     INLINE($FA);
     PORT[$20]:=$20;
END;

{*************************************************************************
        THIS PROCEDURE CONVERTS THE DATA COLLECTED IN THE NUMERICAL
                          REPRESENTATION
*************************************************************************}
PROCEDURE GENERATION;
VAR
DUDA:INTEGER;
BEGIN
```

```
     REPEAT
     IF (CARTOT > 0) THEN
     BEGIN
          BUFF2[CADENA] := BUFFER [SALIDA];
          IF (SALIDA < LONBUF) THEN INC(SALIDA,1)
          ELSE SALIDA:=1;
          DEC(CARTOT,1);
          IF ((CADENA = 1) AND (BUFF2[CADENA] = '+')) THEN SIGN:=1
          ELSE IF ((CADENA = 1) AND (BUFF2[CADENA] = '-')) THEN SIGN:=-1
          ELSE IF (CADENA = 1) THEN CADENA:=0;
          IF CADENA<>4 THEN INC(CADENA,1)
          ELSE
          BEGIN
               CADENA:=1;
               NUMERO:=BUFF2[4]+BUFF2[3]+BUFF2[2];
               WRITE(NUMERO,' ');
               VAL(NUMERO,RXD,DUDA);
               IF DUDA<>0 THEN WRITELN ('ERROR IN COMUNICATION');
               ALMA;
          END;
     END;
     UNTIL (KEYPRESSED)
END;

{*************************************************************************
   THIS PROCEDURE READJUST THE CONDITIONS OF THE SERIAL INTERRUPTION
                      WHEN THE PROGRAM IS ENDED
*************************************************************************}
PROCEDURE RECUPERAR;
VAR
B:BYTE;
BEGIN
     B:=PORT[INT];
     B:=B OR $10;
     PORT[INT]:=B;
     B:=PORT[LCR];
     B:=B AND $7F;
     PORT[LCR]:=B;
     PORT[IER]:=$0;
     PORT[MCR]:=$0;
     PORT[$20]:=$20;
     SETINTVEC($0B,VECTOR);
     MSDOS(REGS);
END;

{*************************************************************************
         THIS PROCEDURE PREPARE THE SERIAL PORT TO RECEIVE
                           THE DATA FROM THE GPC
*************************************************************************}
PROCEDURE PREPARATION;
VAR
B:BYTE;
BEGIN
     WITH REGS DO
     BEGIN
          DX:=1;
          AH:=0;
          AL:=PARAMETROS;
          FLAGS:=0;
          INTR($14,REGS);
     END;
     SEGMENTO:=DSEG;
```

```
      GETINTVEC($0B,VECTOR);
      SETINTVEC($0B,@RECEPCION);
      B:=PORT[INT];
      B:=B AND $0;
      PORT[INT]:=B;
      B:=PORT[LCR];
      B:=B AND $7F;
      PORT[LCR]:=B;
      PORT[IER]:=$01;
      PORT[MCR]:=$0B;
      PORT[MDM]:=$80;
      PORT[$20]:=$20;
END;

{*************************************************************************
               THIS PROCEDURE SENDS A BYTE TO THE GPC
*************************************************************************}
PROCEDURE ENVIO (B:BYTE);
BEGIN
     WHILE ((PORT[LSR] AND $20) <> $20) DO
     BEGIN
     END;
     PORT[DATOS]:=B;
END;


{*************************************************************************
            THIS PROCEDURE SENDS 'd' TO START DATA COLLECTION
*************************************************************************}
PROCEDURE TEMPO;
BEGIN
     ENVIO(ORD('d'));
END;

{************************** MAIN PROGRAM **************************}
BEGIN
     CLRSCR;
     ASSIGN(DATA,'CAPA.DAT');
     REWRITE(DATA);
     ENTRADA:=1;
     SALIDA:=1;
     CARTOT:=0;
     FILLCHAR(BUFFER,SIZEOF(BUFFER),0);
     CADENA:=1;
     CONT:=0;
     SEC:=0;
     PREPARATION;
     TEMPO;
     GENERATION;
     ENVIO(ORD('n'));
     RECUPERAR;
     CLOSE(DATA);
END.
```

C.4 PROGRAM FOR SIMULATION UNDER SAM4

```
{LUIS E. ZUBIETA  20/05/96}
{SIMULATION PROGRAM FOR THE PANASONIC CAPACITORS RATED 470 F. 2.3 v.
THE INITIAL PARAMETER VALUES WERE OBTAINED USING THE PROGRAM CAP1.C
IN THE MOTOROLA 68332 GPU.
```

```
THE EQUIVALENT MODEL USES THREE RC LEGS CONNECTED IN PARALEL AND ONE
PARALLEL LEAKAGE RESISTANCE. THE FIRST LEG CALLED IMMEDIATE
HAS CAPACITANCE VALUE AS FUNCTION OF THE TERMINAL VOLTAGE}

unit capadef;
  interface
    uses samtype;
                (   samtype defines only types, those are :
                    dim1r = array[1..20] of double;
                    dim1i = array[1..20] of integer;
                    name  = string[30];
                    dim1st = array[1..30] of name;     )

    const   om  = 376.99111848;
            pi3 = 1.0471976;

    var     inv,ouv : text;
            con: real;


{ *************** RUNGE KUTTA AND MATH. VARIABLES *************** }

            n,ist,ier,ierr,m1,m2,m55 : integer;
            x,h,hmax,hmin,tol : double;
            z,y : dim1r;
            errsam : integer;

{ *****************  VARIABLES SPEC. PROGRAM ******************** }

            R1,R2,R3,R4,Rlea,C0,C1,C2,C3,C4,Is,Ic1,Ic2,Ic3,Ic4,
            Vc1,Vc2,Vc3,Vcapa,IB,VB : double;
            res : double;

{ ********************** PROCEDURES ***************************** }

            procedure fcn (n:integer; var zpr:dim1r; z:dim1r; x:double);

            procedure rkm(n:integer; var y:dim1r;var x,h:double;
                          tol:double;ist:integer; var ier:integer);

            procedure capainit;

            procedure calstep (pval:dim1r; pari:dim1i; setflg:boolean;
                               var yy:dim1r; var xx:double);
            procedure datasave;

{ ************************************************************** }
  implementation
    procedure fcn;  (DIFFERENTIAL EQUATIONS REPRESENTING THE MODEL)
        begin
            Vcapa:= res*(Is + z[1]/R1 +z[2]/R2 + z[3]/R3)
                        /(1.0/R1 + 1.0/R2 + 1.0/R3 + 1.0/Rlea);

            zpr[1]:= res*(Vcapa - z[1])/(R1*(C0+C1*z[1]));

            zpr[2]:= res*(Vcapa - z[2])/(C2*R2);

            zpr[3]:= res*(Vcapa - z[3])/(R3*C3);

            Ic1:= (Vcapa-z[1])/R1;

            Ic2:= (Vcapa-z[2])/R2;
```

```
          Ic3:= (Vcapa-z[3])/R3;
        end;

        {$I rkm.lib }

{ ************************************************************** }
    procedure capainit; {VARIABLES INITIALIZATION}
        begin

          { ********** read integration routine var. ************ }
          h := 1.0E-5;  hmax := 1.0E-3;  hmin := 1.0E-6;
          tol := 1.0E-3;  ist := 1; con := 0;

          { ********* initialize integration routine var. ******* }
          n:= 3;
          ier:= 0; ierr:= 0;  h:= hmin;   x:= 0.0;
          for m1:= 1 to 12 do  z[m1]:= 0.0;

          Ib:= 50.0;     { base current }

          { ****** initialize spec. variables,parameters ******** }

          { no assignment of variable parameters required as the
            parameters are assigned in the SBR SAM before the first
            calculation takes place (paflg true -> setflg true)  }

          { the first plot point is set to 0.0 for all variables,
            this is fixed in SBR SAM and should not be altered to
            ensure a save start up; if the first step is kept small
            it does not matter and usually the initial step for the
            Runge Kutta Routine starts with hmin  }

        end;

{ ************************************************************** }
  procedure datasave;
        begin
                con:= con+1;
                write (ouv, x:10:6);
                write (ouv,' , ');
                writeln (ouv, vcapa:10:6);
        end;

{ ************************************************************** }
  procedure calstep;    {VARIABLES ACTUALIZATION AND CALCULATIONS}

    procedure assignpar;        {VARIABLES ACTUALIZATION}
        begin
                Is:= pval[1];
                C0:= pval[2]; C1:= pval[3];  C2:= pval[4];  C3:=pval[5];
                R1:= pval[6]; R2:= pval[7];  R3:= pval[8];
                Rlea:= pval[9];
                hmax:= pval[10]; res:= pval[11];
                z[1]:=z[1]*res;  {the input res resets the simulation}
                z[2]:=z[2]*res;
                z[3]:=z[3]*res;
        end;

    begin
        if setflg then assignpar;
        if x>=con then datasave;    {SAVE VARIABLES IN EXT FILE}
```

```
        { *******  solution mathematical problem, next step  ***** }
        rkm(n,z,x,h,tol,ist,ier);

        { ******************** error handling ******************** }
        if ier <> 0 then ierr:=ierr+1;   if h < hmin then ierr:= 5;
        if ierr > 3 then errsam := ierr;
        if h > hmax then h:= hmax/2;

        { ************** asign display variables  *************** }
        begin xx:= x;
                yy[1]:= Is/Ib; yy[2]:= Vcapa;  yy[3]:= z[1];
                yy[4]:= z[2];  yy[5]:= z[3];
                yy[6]:= Ic1/Ib; yy[7]:= Ic2/Ib; yy[8]:= Ic3/Ib;
        end;
    end;
  END.
{ ************************************************************** }
```

C.5 PROGRAM FOR ENERGY AND LOSSES SIMULATIONS

```
* SIMULATION PROGRAM FOR CAPACITOR LOSSES AND ENERGY INTERCHANGE
FACTOR, RUNS UNDER PSPICE*
* CAPACITOR CHARGE USING I=30 AMP *

Ci      7 0 ACAP 280 IC=0
Cd      8 0 100 IC=0
Cl      9 0 150 IC=0
Ri      10 7 2.5m
Rd      10 8 0.9
Rl      10 9 5
Rlea    10 0 5000
I1      0 10 PULSE (0 -30 {DELAY} 1ms 1ms {35-DELAY/100} 1100)
I2      0 10 PULSE (0 30 0 1ms 1ms 37 1100)
E1      11 0 VALUE = {LIMIT(V(10),0,3)}
R9      11 0 1000
.MODEL   ACAP CAP (C=1 VC1=0.63)
.PARAM DELAY=37
.STEP PARAM DELAY 37 1037 100
.TRAN 0.1s 1100 0 1 UIC
.PROBE
.END
```

APPENDIX D

ADDITIONAL PRACTICAL CONSIDERATIONS

At this stage the characterization of the double-layer capacitors has been completed and the objectives have been reached. However, in each specific application, additional points of interest are always present and may be studied.

In this appendix some of these additional factors will be briefly studied through a few additional experimental and simulated analyses. The studies to be presented in the following pages will not be a complete and detailed research in each aspect, but they will give a starting point if in future research it is found necessary to extend the analysis of those aspects.

D.1 CURRENT RIPPLE EFFECT

In all the previous analyses and simulations, the current applied to the capacitor or bank of capacitors was assumed to be a perfect DC current. However, in the experimental setup used and in several real applications, the current is not constant.

The DC/DC converter used in the setup has a current control which tries to keep the current close to the desired value through the switching of the devices present in the converter. However, the switching interval and the finite inductance present in the loop produce a ripple in the real current waveform at the output. The effect of the ripple present in the current applied to the capacitor is studied using the PSPICE simulation software. In the simulation, the current is considered as a triangular waveform with five amperes peak to peak plus a DC value equal to the rated current in the

circuit.

Two aspects are studied: the differences in the terminal voltage and the differences in losses under the ideal and the new condition.

Appendix C presents the program for PSPICE used in the simulations. Figure D.1 represents the terminal voltage for the constant current and for the ripple input current.

There is no appreciable difference in the values of the terminal voltage for the constant current and the ripple current. The only difference observed is the presence of a ripple in the terminal voltage. That ripple follows the ripple in the applied current, and it is due to the change in the voltage dropped across the equivalent resistance.

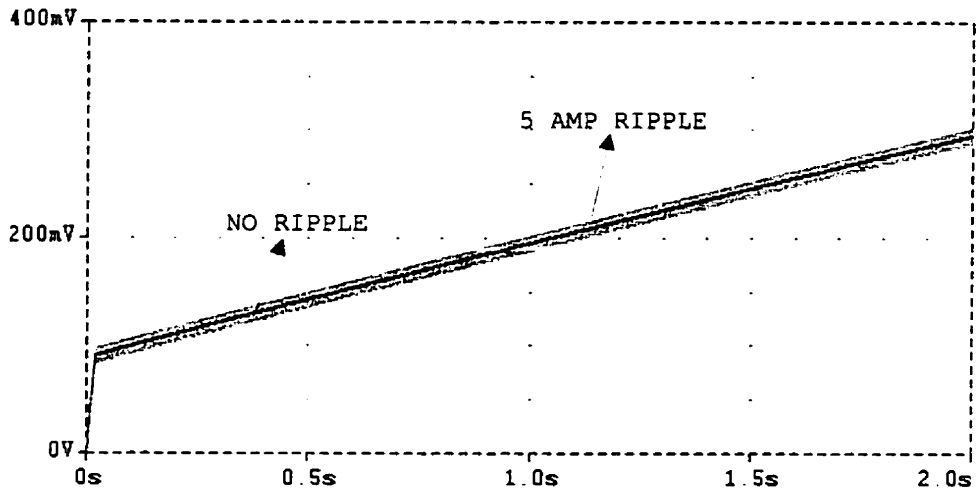
The previous result gives the conclusion that none of the experimental results of charge actions and model calculations are affected for small differences in the waveform of the input current as long as the average current value is equal to the assumed constant current.

The second factor to be studied is the change in the losses of the capacitor under test. The total energy dissipated in losses after two seconds of charge is the comparative test.

Figure D.2 represents the total energy dissipated in losses for the constant current and the ripple current.

Based on the previous figure, it can be concluded that the ripple in the current applied to the capacitor increases the total losses in the device. That effect may be explained based on the Fourier decomposition of the input current waveform which contains the average value (ideal constant current) plus some harmonics sinusoidal waveforms given by the switching frequency. Those harmonics produce

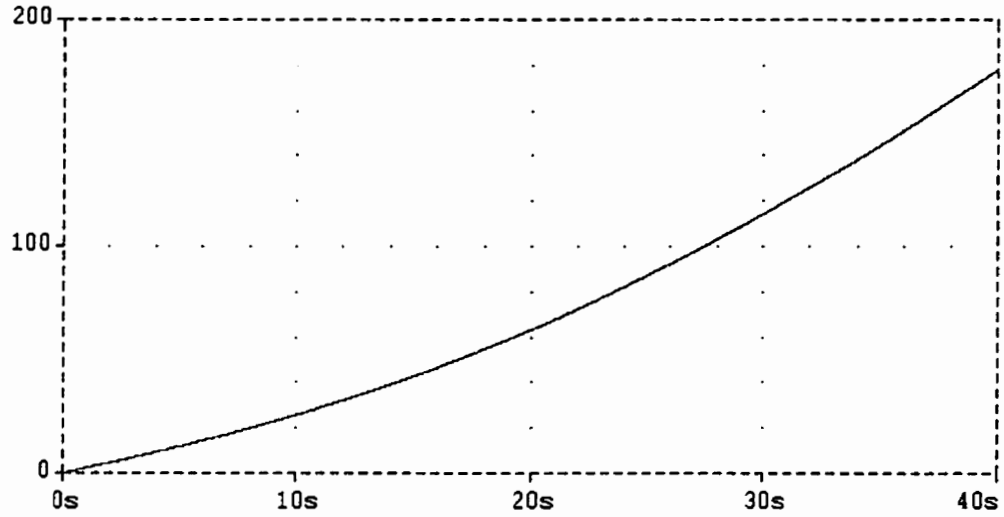
TERMINAL VOLTAGE (V)



TIME (SEC)

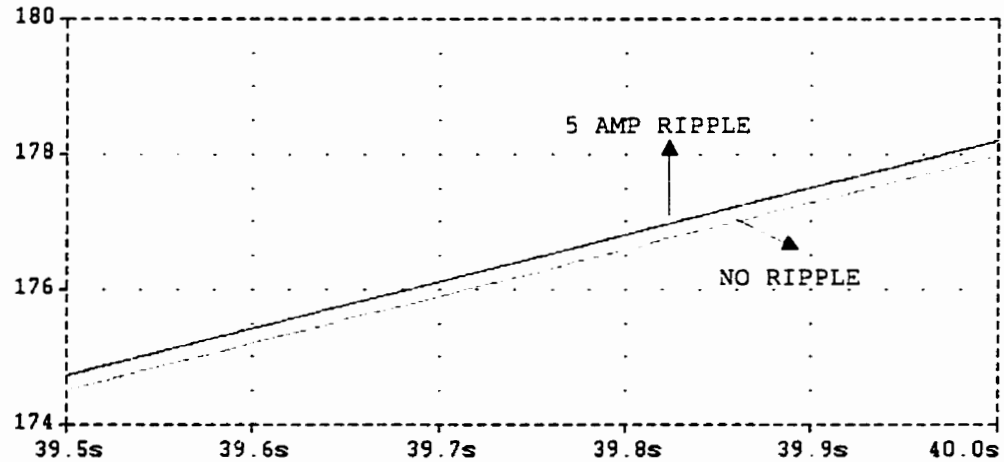
FIGURE D.1 CURRENT RIPPLE EFFECT IN THE TERMINAL VOLTAGE

ENERGY DISSIPATED IN LOSSES (W.sec)



TIME (SEC)

ENERGY DISSIPATED IN LOSSES (W.sec)



TIME (SEC)

ZOOM OF THE FINAL INSTANTS OF THE CHARGE ACTION

FIGURE D.2 CURRENT RIPPLE EFFECT IN THE CAPACITOR LOSSES

additional losses in the internal resistance of the capacitor.

In the experimental setup the increase in the total energy dissipated inside the capacitor was lower than 0.5% of the ideal value. That effect is very small and may be neglected in most of the cases. However, this value may increase if the peak to peak value of the ripple is increased.

D.2 TEMPERATURE EFFECT IN THE PARAMETERS

The calculation of the equivalent model in chapters four and five was done at an ambient temperature of approximately 20° C. In order to get a general idea about the influence that the temperature of the device has on the calculated parameters, the equivalent model was calculated again in a capacitor that was kept at a temperature of -5° C for three days.

Table D.1 indicates the results of this experiment.

PARAMETER	VALUE
Ri	3.435 mohms.
Ci0	274 F.
Ci1	195 F.
Rd	1.089 ohms.
Cd	100 F.
Rl	7.056 ohms.
Cl	234 F.

TABLE D.1

The above table indicates that the values of capacitance are not

appreciably affected by the capacitor temperature; however, the resistance of the different equivalent model branches are increased twenty per cent approximately compared to those calculated at 20º C.

D.3 CASE TEMPERATURE VARIATION

The final test was done in order to get an idea about the increase in the double-layer capacitor temperature when it is in continuous charge and discharge actions. The initial temperature of a DLC was measured and the device was charged and discharged continuously. During the charge process the case temperature and the terminal temperature was measured every thirty minutes to check the effect of the energy dissipated on the device temperature.

Figure D.3 presents the curve of the temperature as a function of the time for the experiment.

In this figure, the temperature in the capacitor case increases during the first ninety minutes of the charge test until it reaches approximately fourteen degrees celsius over the ambient temperature. After that, the temperature keeps approximately the same difference with respect to the ambient temperature.

The response of the terminal temperature is similar; that is, an important increase in the temperature for the first 90 minutes until approximately thirty degrees celsius over the ambient and then small variations with respect to the ambient temperature.

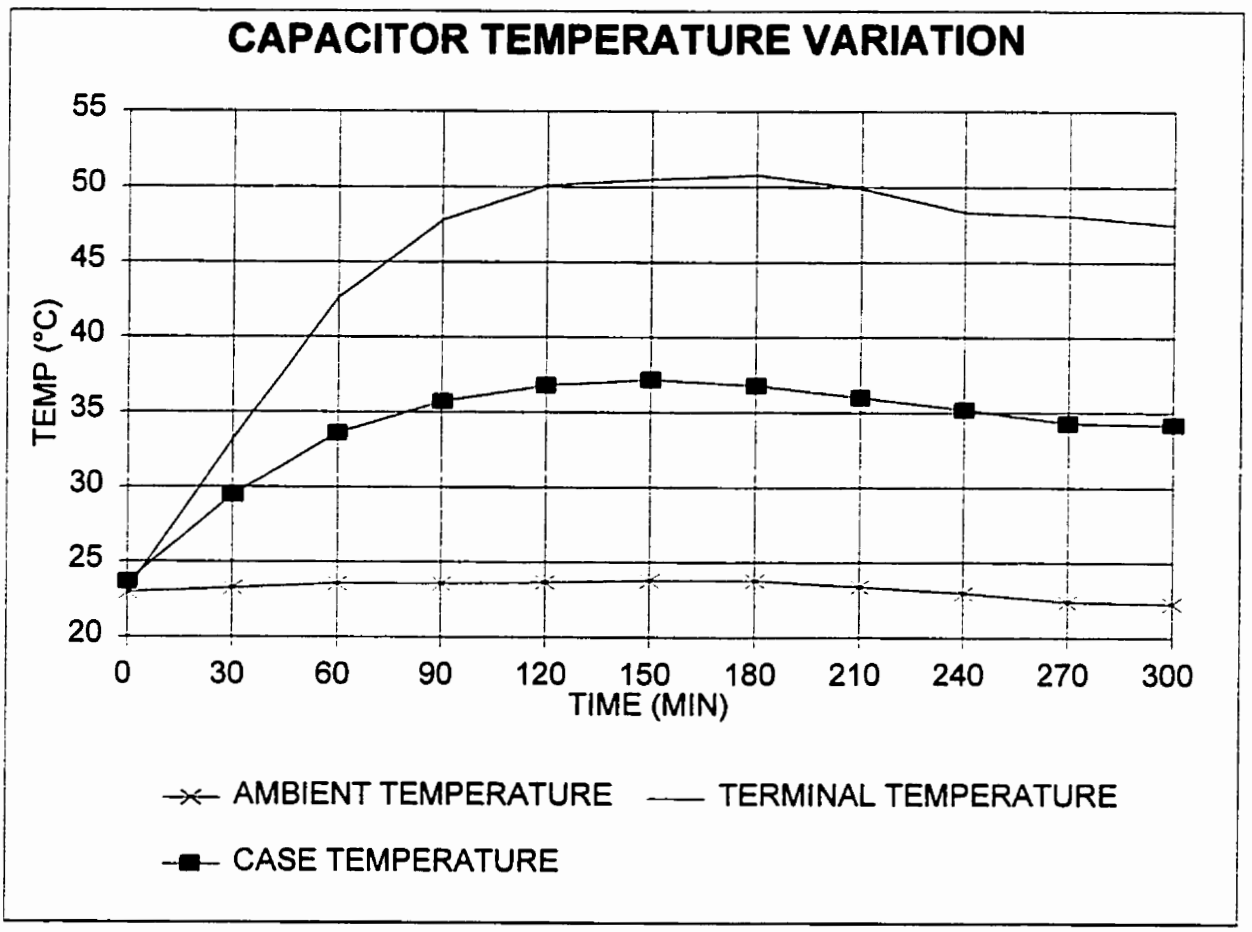
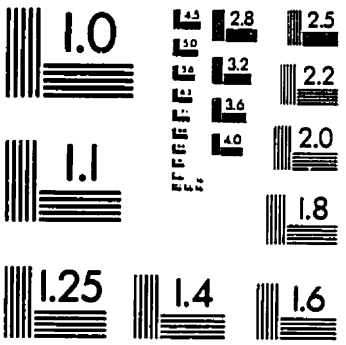
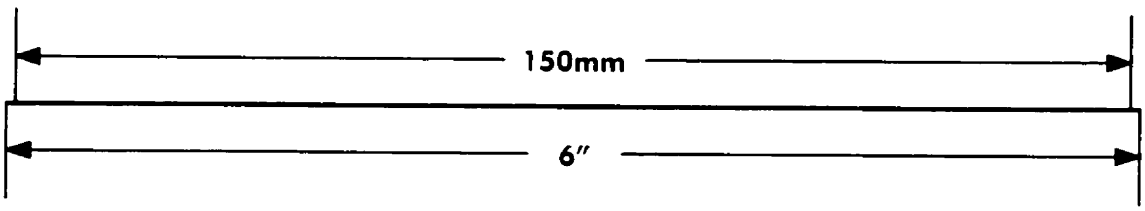


FIGURE D.3 CAPACITOR TEMPERATURE VARIATION DURING CONTINUOUS CHARGE AND DISCHARGE ACTIONS.

TEST TARGET (QA-3)





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