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Characterization of electroless nickel as a seed layer for silicon solar cell metallization

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Abstract. **Electroless nickel plating is a suitable method for seed layer deposition in Ni–Cu-based solar cell metallization. Nickel silicide formation and hence contact resistivity of the interface is largely influenced by the plating process and annealing conditions. In the present work, a thin seed layer is deposited from neutral pH and alkaline electroless nickel baths which are annealed in the range of 400–420°C for silicide morphology and contact resistivity studies. A minimum contact resistivity of 7 mΩ cm^2 is obtained for seed layer deposited from alkaline bath. Silicide formation for Pd-activated samples leads to uniform surface morphology as compared with unactivated samples due to non-homogeneous migration of nickel atoms at the interface. Formation of nickel phosphides during annealing and the presence of SiO_2 at Ni–Si interface creates isolated Ni_2Si–Si interface with limited supply of silicon. Such an interface leads to the formation of high resistivity metal-rich Ni_3Si silicide phase which limits the reduction in contact resistivity.**

Keywords. **Ni–Cu metallization; electroless nickel; contact resistivity; nickel silicide; nickel phosphides.**

1. Introduction

Silver-based front-side metallization is an established technology for silicon solar cells. However, the presence of glass-frit and voids in silver paste reduces the effective density and conductivity of silver grid lines.[1] In addition, contribution of metallization to cell processing cost is around 40% due to the expensive silver paste.[2] With a push to reduce metallization cost in c-Si technology roadmap, alternative contact scheme based on Ni–Cu stack is being considered.[3,4] The nickel seed layer prevents diffusion of copper in silicon and formation of nickel silicide at the interface reduces contact resistance with improvement in adhesion of metal stack.

Electroless nickel plating is a well-established process[5] and ideally suited to deposit the seed layer on semi-conducting surface as electroplating process requires a conducting substrate for deposition. Masking to prevent deposition on unpatterned regions would be provided by the anti-reflective coating of solar cell. One of the important aspects related to solar cell metallization is that nickel diffusion through the emitter and bulk material can lead to shunt formation and reduction in minority carrier life time.[6,7] To avoid these detrimental effects, annealing of nickel seed layer is typically done in temperature range of 300–500°C for short durations.[3,4,8–12] However, a clear relation does not exist between annealing conditions and nickel silicide formation with associated contact resistivity of the interface, though studies have been performed for higher temperature ranges.[13,14]

In the present work, a thin electroless nickel seed layer is deposited with and without Pd activation to study silicide formation and contact resistivity at the interface for annealing durations of 30–60 s in temperature range of 400–420°C. Phase identification studies for the seed layer and silicides is performed using X-ray diffraction (XRD) technique. The analysis gives a clearer understanding of influence of seed layer deposition process and the annealing conditions from solar cell metallization point of view.

2. Experimental

c-Si p-type wafer (100) of resistivity 1–3 Ω cm and thickness of 220 μm which have undergone standard solar cell fabrication of texturing, diffusion (40–60 Ω/□) and ARC deposition of 75–80 nm were used for transfer length method (TLM) sample preparation and observing silicide morphology evolution. Patterning of the ARC was done by coating self-adhesive polymer which is then patterned by CO_2 laser operating at 3–5 W with a wavelength of 10,000 nm.[15]

An optimized electroless bath with $NiCl_2$ and NaH_2PO_2 concentrations of 30 and 20 g l^{-1} are used for nickel

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deposition.[15] Bath temperature was varied in range of 70–90°C for neutral pH and acidic baths, while a temperature of 90–95°C was used an alkaline bath. Pd-based activation[16] is used for plating from acidic and neutral baths. Plating duration is in range of 60–120 s for seed layer thickness of around 140 nm. Subsequently, the samples are annealed at 400–420°C in a tube-furnace with N_2 ambient. Unreacted nickel is etched in H_2SO_4:H_2O_2 (1:1) solution for observing the surface morphology after silicidation.

Nickel seed layer growth and silicide morphology are observed using scanning electron microscopy (SEM), while Grazing Incidence XRD (GIXRD) measurements are performed with grazing angle of 0.5° and scan rate of 0.01° s^{-1} in 2θ range of 30–70° to obtain detailed phase formation information for various annealing conditions. TLM approach is used for contact resistivity (ρ_c) measurements for various annealing conditions.[15]

3. Results and discussion

3.1 *Nickel seed layer growth and contact resistivity studies*

Homogeneous deposition is obtained for neutral and alkaline baths with plating intervals up to 3 min as shown in figure 1. Seed layer thickness is approximately 140 nm for deposition of 1 min in both cases with low phosphorus content of 5% (by weight) as determined by energy dispersive X-ray spectroscopy. Acidic bath was found unsuitable due to non-homogeneous particle growth which may result in presence of voids in the seed layer. As-plated seed layers have ρ_c values of greater than 18 mΩ cm^2 which decreases to average value of 7.7 and 5.9 mΩ cm^2 for seed layer deposited from neutral and alkaline baths, respectively. Contact resistivity trend with varying annealing conditions is indicated in figure 2. Reduced contact resistivity is obtained

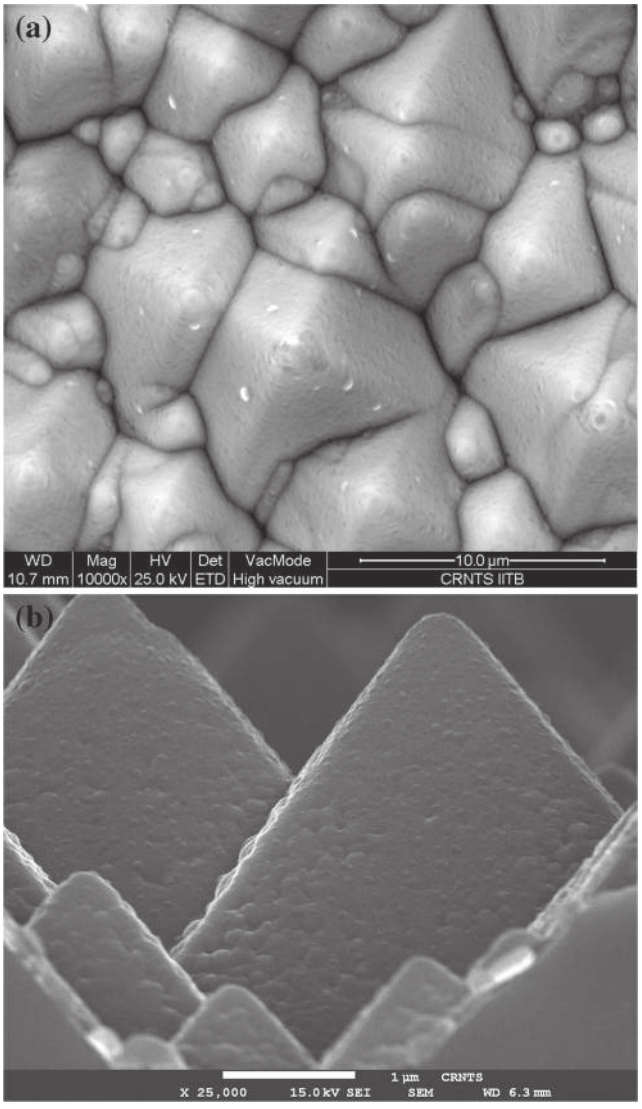

Figure 1. Electroless nickel deposition from (**a**) neutral pH bath for 3 min and (**b**) alkaline bath for 1 min.

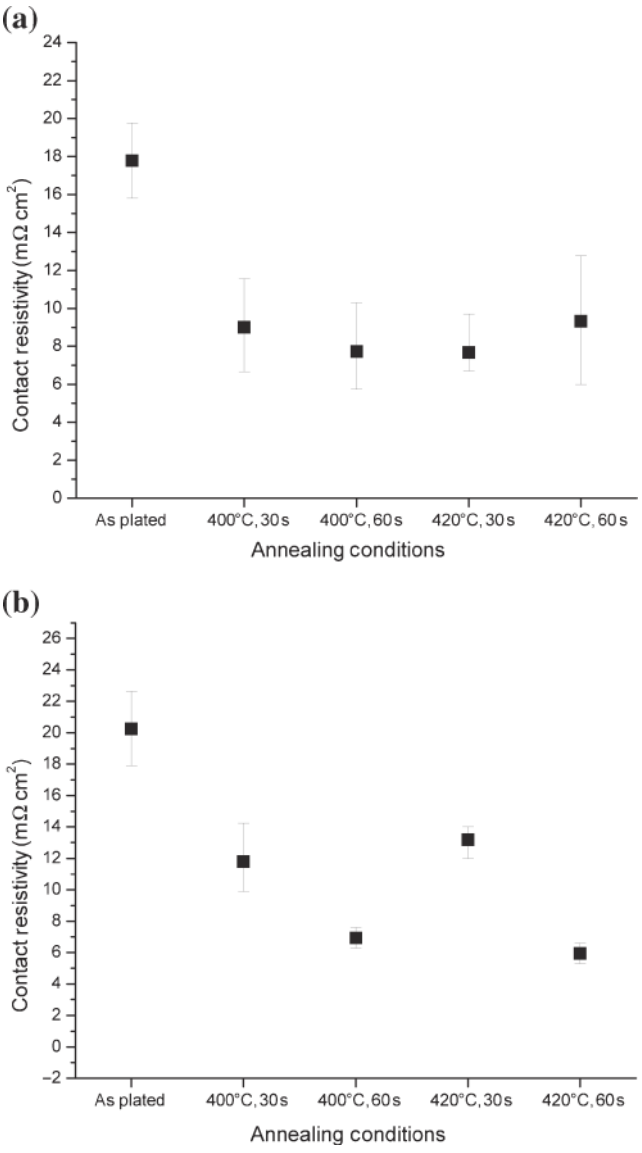

Figure 2. Contact resistivity variation for (**a**) activated samples and (**b**) non-activated samples.

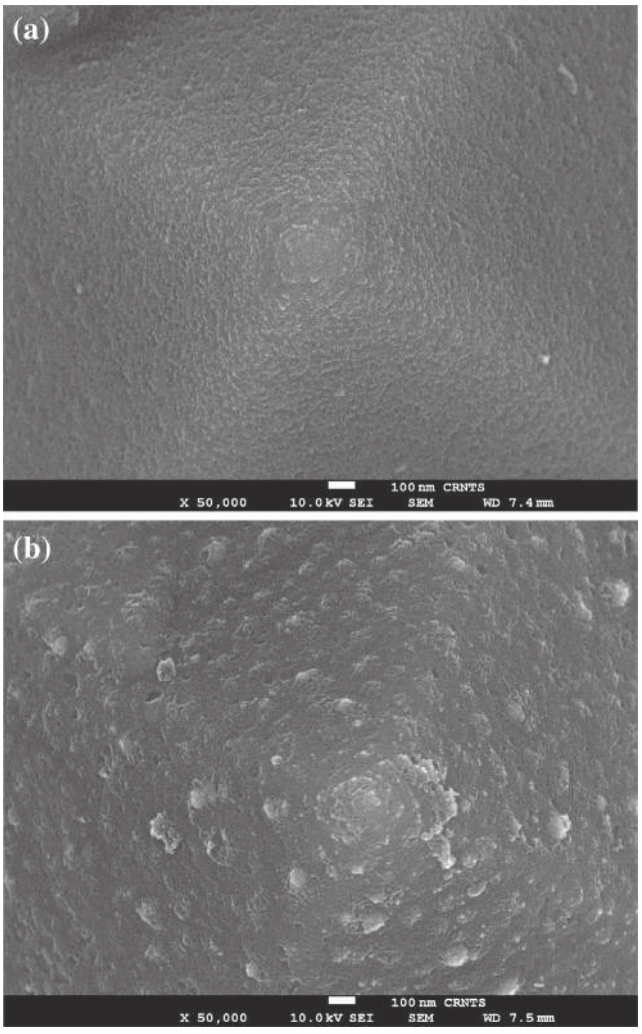

Figure 3. Silicide morphology for seed layer deposited from neutral pH bath (**a**) annealed at 400°C for 1 min and (**b**) annealed at 420°C for 1 min.

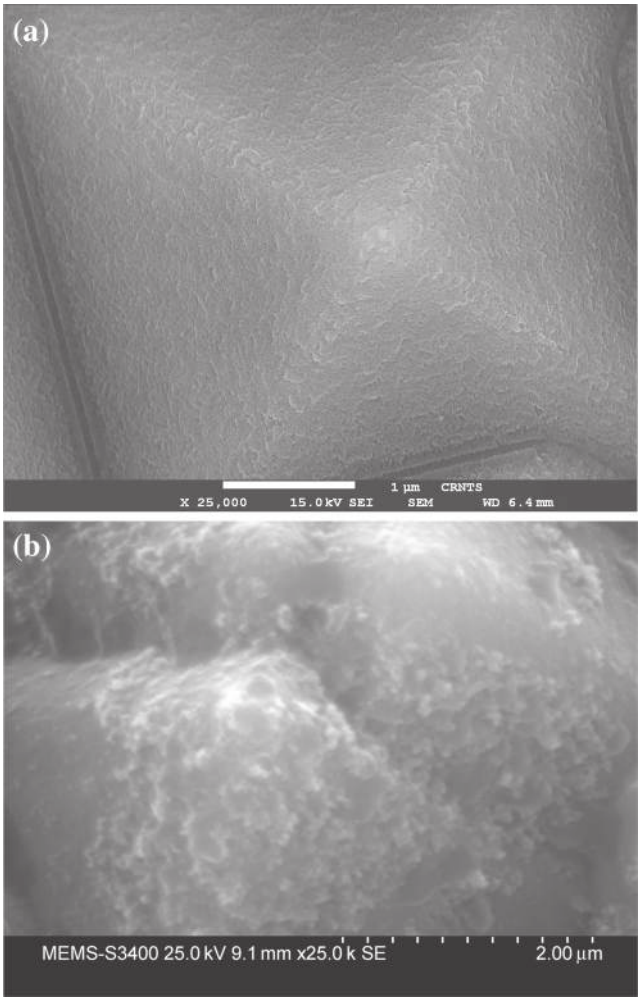

Figure 4. Silicide morphology for seed layer deposited from alkaline bath (**a**) annealed at 400°C for 30 s and (**b**) annealed at 400°C for 1 min.

for non-activated samples with increased annealing duration, while significant difference is not observed in case of activated samples.

3.2 *Silicide morphology and phase formation*

Silicide morphology for seed layer deposited from neutral bath is shown in figure 3. Silicide formation is uniform over the pyramid for annealing at 400°C, while hump-like formations are evident for higher annealing temperature. For seed layer deposition from alkaline bath, silicide formation is relatively even for a short annealing duration at 400°C with prominent roughening at many sites for increased duration as indicated in figure 4. The observations indicate that temperature in range of 350–400°C with short duration should be suitable for seed layer annealing to reduce the probability of nickel diffusion through the emitter.

Nickel deposition from an alkaline bath is initiated *via* galvanic displacement with silicon substrate, where the nickel cations receive electrons through electrochemical oxidation of silicon.[17] Subsequently, nickel deposition proceeds autocatalytically through the reducing agent. The galvanic displacement process leads to formation of a non-homogeneous SiO_2 layer at the Ni–Si interface[17] and hence non-uniform migration of nickel atoms during silicide formation. Similar observations for nickel silicide formation have also been made by Fisher.[18] As compared to deposition without activation, Pd-based activation leads to regular nucleation of nickel particles and hence relatively uniform silicide formation. Despite the advantage of uniform silicide formation, Pd-based activation can lead to significant background plating which will degrade the solar cell performance[19] and hence would require further optimization by reducing bath temperature or altering the activation process.[18]

Crystallization of the nickel seed layer occurs for increased annealing temperature, while prominent growth of nickel phosphides is observed from the XRD measurements shown in figure 5. It is known that annealing electroless nickel above 400°C leads to formation of nickel phosphide

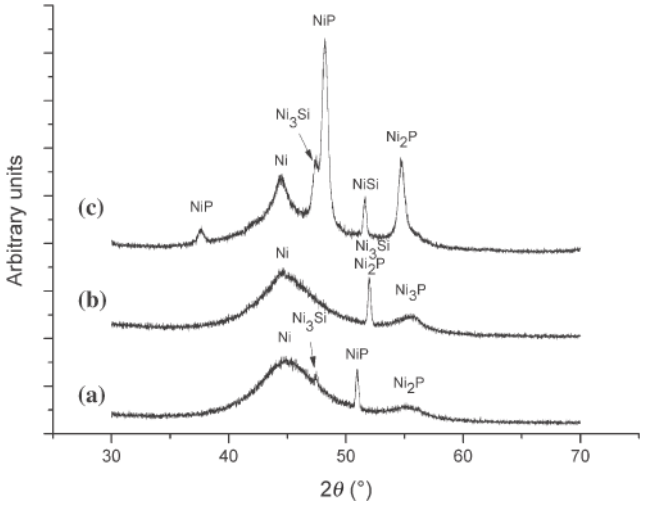

Figure 5. GIXRD data for 140 nm nickel seed layer annealed for 1 min at (**a**) 350°C, (**b**) 400°C and (**c**) 450°C.

Ni_3P with one or more intermediate phosphides,[20–22] while the equilibrium state of nickel with 0–15% (weight) P is Ni + Ni_3P.[22] Ni_2P might have also been present in the as-deposited films as has been inferred in Randin and Hintermann,[23] but might not be detected due to overlapping peak with Ni-P. The presence of nickel phosphides along with additional impurities like SiO_2 will significantly affect the silicidation process. Formation of metal-rich Ni_3Si phase is attributed to isolated Ni_2Si–Si interfaces with limited supply of silicon.[24] The desirable NiSi phase is only observed at a higher annealing temperature of 450°C. Since Ni_3Si phase has much higher resistivity compared to NiSi or Ni_2Si phases,[25] it will limit the decrease in contact resistivity at the Ni–Si interface.

4. Conclusions

A uniform and low phosphorus content thin nickel seed layer is deposited from neutral and alkaline electroless baths for solar cell metallization. The contact resistivity of as-plated seed layer is greater than 18 mΩ cm^2 which reduces to 7 mΩ cm^2 for seed layer deposited from alkaline bath and annealed at 400°C. Pd-based activation leads to uniform silicide formation, while deposition from alkaline bath leads to non-homogeneous silicide formation even for short annealing duration at 400°C. A temperature range of 350–400°C with short duration is recommended for annealing to avoid nickel diffusion through the emitter. The presence of nickel phosphides and SiO_2 in the seed layer and at Ni–Si interface play a critical role in silicide formation and leads to formation of metal-rich silicide phase Ni_3Si due to isolated Ni_2Si–Si regions with limited supply of silicon. Since Ni_3Si has higher resistivity compared with NiSi and Ni_2Si phases, it will limit the reduction in contact resistivity for Ni–Cu-based metallization.

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