Characterization of Self-Heating in Advanced VLSI Interconnect Lines Based on Thermal Finite Element Simulation

Sven Rzepka, *Member, IEEE*, Kaustav Banerjee, *Student Member, IEEE*, Ekkehard Meusel, and Chenming Hu, *Fellow, IEEE*

***Abstract*—In this paper, self-heating of interconnects has been shown to affect the lifetime of next generation integrated circuits significantly more severely than today's. The paper proves the necessity for extending the system of design rules, proposes a thermal design rule, and presents an efficient and quantitatively accurate thermal simulator as tool for the design process.**

***Index Terms*—Advanced VLSI structures, design rules, FEM, interconnects, reliability, self-heating, thermal modeling.**

I. Introduction

BEING the major limit for further performance increase, interconnect lines of integrated circuits have become the targets of massive technological improvements. The line dimensions have been downscaled aggressively (e.g., line width by factor 10, from 2 μm to 0.2 μm, in the last 5 yrs). Metallurgical and structural improvements (alloying pure Al by 0.5$\cdots$4 wt% Cu, bamboo structure) allowed the current density to rise without shortening the lifetime determined by electromigration tests. In those tests, self heating effects are mostly neglected so far. However, Fig. 1 shows how sensitively the electromigration lifetime depends on temperature. Assuming Al(Cu) lines, which have an activation energy for electromigration of about 0.7 eV, the lifetime is reduced to 50% of the room temperature level when the temperature is increased by 7.8 °C above 25 °C. It is even shrunk by 90% when the temperature increases by 27.5 °C to 52.5 °C. In cases of perfect bamboo structure or large single crystalline sections, the relative reduction in lifetime due to self heating is even more severe because the activation energy for interface and bulk diffusion is larger than 0.7 eV.

Presently, the design rules for interconnects are based on the average current density since the progress of the lifetime limiting phenomenon, which is electromigration, is proportional to it [1], [2]. Keeping the average current density constant at the design rule maximum of 0.2 MA/cm^2, Fig. 2 depicts the increase of heat generated in a line when the pulse duty factor (DF) is reduced. The reason is that heat generation is rather a function of the root-mean-square (RMS) current density than of the average current density. Today, the main power, ground, and bus lines are designed to operate at the maximum current density allowed. However, as technology moves on, even low level data lines linking individual cells of the circuit may increasingly be manufactured narrow enough to reach this level. In contrast to the main lines, these local data links tend to have a quite small DF. Due to their specific function in the circuit, they are usually switched-on less frequently than the main data distributors so that their average load remains

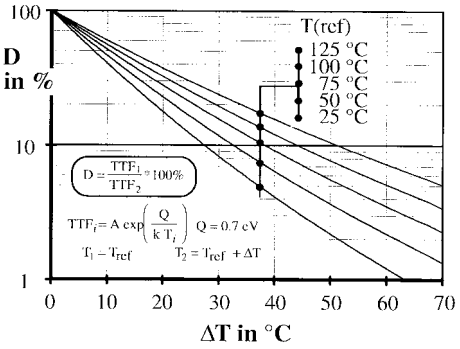

Fig. 1. Decrease D of electromigration time to failure (TTF) of an Al0.5Cu interconnection line due to self-heating temperature rise (ΔT) dependent on the reference temperature ($T_{\rm ref}$). An activation energy Q of 0.7 eV is assumed. Parameter A is dependent on current density and microstructure.

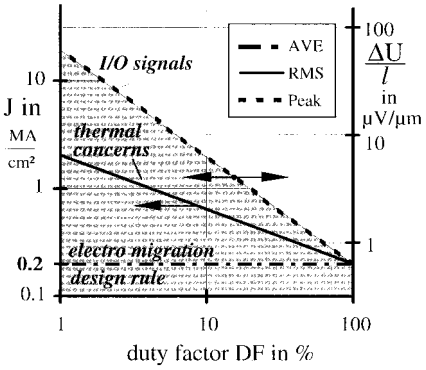

Fig. 2. Relationship between average (AVE), root-mean-square (RMS), and peak current density and voltage drop per line length for dc pulses of various duty factors.

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S. Rzepka and E. Meusel are with the Technische Universität Dresden, Dresden D-01062, Germany (email: rzepka@ehmns2.et.tu-dresden.de).

K. Banerjee and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA.

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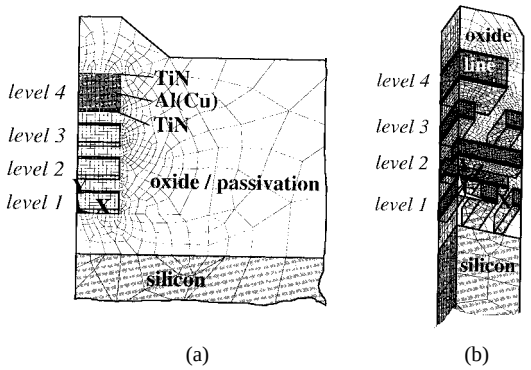

Fig. 3. Two- and three-dimensional finite element models. (a) Test structure (example for line 4) and (b) real structure.

pretty low. The RMS load, however, rises according to Fig. 2. That means, obeying all present design rules, much more heat will be generated in next generation IC's. Hence, the complex thermal situation on the chip has to be studied, tools have to be prepared to assess new structures during their design, and an extended set of design rules has be introduced.

This work has investigated the thermal situation in multilevel interconnect structures under various loads (dc and pulses) based on parametric two-dimensional (2-D) and three-dimensional (3-D) finite element models which have been calibrated by experiments to assure quantitative accuracy. The efficiency of the developed simulator allows its use during interconnect design. In this way, the number of additional experiments needed to include a thermal check-up of new structures can be limited to a large extent, which is desirable for quick turn around times of new technologies.

II. Samples, Models, and Calibration Experiments

The test samples used in the experiments were prepared in a state of the art quadruple level metallization wafer process. The test structures were isolated, i.e. there was no metal layer on top of another. In our example, all test lines were 1000 μm by 3 μm NIST recommended structures. They had TiN top and bottom barrier layers of 50 nm and 150 nm thickness, respectively. The current carrying Al0.5Cu layer was always 0.6 μm thick except for level 4 (1.2 μm). The field and dielectric silicon dioxide (SiO_2) beneath the first metallization level was 1.4 μm thick in total. Between the levels was 1.0 μm oxide. The oxide/nitride passivation on top of the structure had a total thickness of 2.0 μm.

Since the lines in the test structures were very long, both sections at the ends of the lines, in which significant thermal gradients might occur, were negligibly short. That means, most of the line is at a uniform temperature. Therefore, a 2-D finite element model is sufficient. It describes the cross section of the test structures. Due to symmetry conditions, just half of the line width has eventually been meshed as shown in Fig. 3(a) for a level 4 structure. In addition, 3-D models [Fig. 3(b)] have been set-up to describe cells of densely packed real array structures. In order to model the situation in a typical circuit correctly, different line widths and heights have been chosen for the different metallization levels. The narrowest lines have been placed in level 1 and 2 representing the local data links, while bigger lines for global data distribution and the main power supply have been considered in the upper levels. The case of lines crossing at different levels has been included as well. Analogous to the 2-D model, all metallization levels and even the single lines may individually be programmed to be active in a particular simulation or replaced by insulator. All model dimensions are represented by parameters. After editing these parameters, the finite element mesh is generated automatically in a few seconds replicating the new design. This makes the simulator very effective in analyzing various structures. In this work, the line widths has been, respectively, 0.5/0.5/1.0/3.0 μm at the metallization levels 1/2/3/4 of the 3-D models. The sandwich structure including the thicknesses of all layers has been kept unchanged to the NIST test samples.

The material data for the models were mostly taken from literature ([3], [4]). However, the most critical parameters, the resistivity of the Al(Cu) interconnect and the thermal conductivity of the SiO_2 layers, needed special attention. According to Matthiesen's rule

$$\rho_{\mathrm{line}}(T, c) = \rho_{\mathrm{pure}}(T) + \rho_{\mathrm{def}}(c) \tag{1}$$

the resistivity of the line, ρ_{line}, has been subdivided into a temperature dependent term of the perfect basis metal (Al), $\rho_{\mathrm{pure}}(T)$, and a defect term that is independent of temperature but dependent on the concentration of the alloying element and the micro structural defects, $\rho_{\mathrm{def}}(c)$. The temperature dependent data of pure aluminum is of course well documented and may be taken from literature [5] because it can by definition not be affected by any defects. The defect term, however, is very likely to vary due to effects of the numerous process steps and the stochastic variation of process parameters. Thus, first tests have already shown, the magnitude of the defect term is in the order of some 20% of the temperature dependent term. It is constant among the lines of one particular metallization level but different between the levels. Thus, quantitative accurate simulation results require the defect term to be determined experimentally. Simple four point resistance measurement at room temperature separately for each metallization level is needed. Subtracting the resistivity of the pure aluminum at RT, the defect terms of our test lines were evaluated to 0.70 $\mu\Omega$cm, 0.66 $\mu\Omega$cm, 0.63 $\mu\Omega$cm, and 0.55 $\mu\Omega$cm for the lines at level 1, 2, 3, and 4, respectively. This result may be interpreted as follows. At the SiO_2 deposition temperature of 400–450 °C, the 0.5 wt% copper is in solution within the aluminum of the line. Due to rapid cooling after the deposition, the copper remains trapped in the matrix of the grains and can not form precipitates at the boundaries. Therefore, the defect terms have relatively high magnitudes despite the low copper concentration. The trend of the measured data indicates in addition that the structural defects, which arise from thermal stress during the cool-down after a SiO_2 deposition, are just accumulated and do not relax in the subsequent deposition steps. Consequently, the defect term has the biggest magnitude in the level 1 metallization.

The thermal conductivity of SiO_2 is also likely to differ from data published in the open literature. There is an extra resistance for the heat transport at the interface between two different materials, similar to the electrical interface resistance.

It can be thought as a transient region between these materials that usually has a much lower conductivity than both materials. In the case of thin films, i.e., up to a film thickness of 2 μm, these interfaces resistors may determine the effective behavior significantly [6]. In our simulations, a downscaling factor of 0.87 has been found by the experiment described in the next paragraph that adjusts the published data of SiO_2 bulk heat conductivity to the thin film conditions.

Besides geometry and material behavior, the load and the boundary conditions (BC) have to be modeled. Using ANSYS®, a commercial code for finite element analysis, the load can easily be applied directly as an electrical current, just like in the real experiment. No pre-calculation of any energy input is needed so that current crowding and similar effects are considered correctly anytime. In our attempt to study the self-heating effects in advanced VLSI interconnect lines, direct current (dc) loads, unidirectional current pulse sequences and single pulses of different waveforms and switch-on periods, respectively, and with various current densities have been applied to the test and the real structure models. That means, the practical load cases namely, steady state, pulsed loads, as well as electrical over-stress and electrostatic discharge (EOS/ESD) have been included in the analysis. Details of the specific loads are given in the result section below.

The meaning of the BC is to replicate the experimental set-up or the conditions during service. The input of the electrical BC is rather trivial. Just a reference potential and the I/O terminals have to be set. There is no need for any experiment here. The specification of the thermal BC's, however, is more complex. There are two different paths. The main path leads from the line through the oxide layer down to the silicon of the chip and afterwards to the chuck of the probe station. Including the silicon chip in the model, the BC at the chip/chuck interface is not critical. Even one order of magnitude difference in the heat dissipation coefficient at this interface did not affect the simulation result significantly. Besides this main thermal path, convection from the top surface to the ambient air may contribute significantly, especially for the level 4 lines. The heat film coefficient at this interface, however, is dependent on many sub-parameters, which themselves vary with different probe stations and even with individual structures of the same material but different technology. Thus, it has always been a smart move to determine the heat film coefficient experimentally. This can be done in conjunction with the measurement of the thin film heat conductivity as follows. A high current density is applied to two test structures, which are identical except that one has a level 1 interconnect and the other a level 4 interconnect. Using the calibrated electrical resistivity data, the temperature increase due to self-heating can be measured. Finally, both unknowns, the heat film coefficient and the SiO_2 thin film heat conductivity can be evaluated. At our conditions, the heat film coefficient was 21.6 $Wm^{-2}K^{-1}$.

Applying the parameters that have been determined experimentally, additional simulations and experiments have been carried out varying the current densities and including all the test lines. Fig. 4 shows the excellent agreement between the experimental and the simulation data in the wide temperature range considered. The relative error never exceeds 5%. This proves that the calibration methodology is capable of generating data that leads to quantitative reliable simulation results. This effective methodology consists of two simple experiments. First, the defect term of the electrical resistivity of each metallization level has to be determined at room temperature. And second, thermal conductivity and heat film coefficient have to be determined by evaluating the actual temperature increase of two slightly different test structures due to Joule heating.

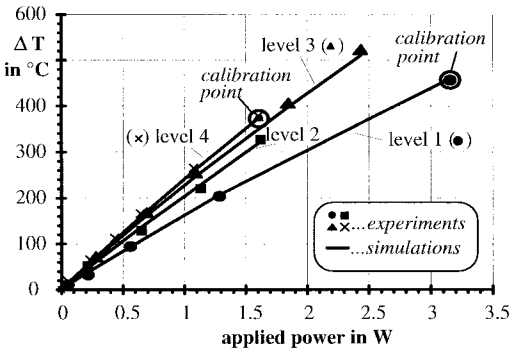

Fig. 4. DC current induced self-heating in quadruple level metallization test structures: Experimental (dots) and simulation (lines) results.

The parameters found for the test structure apply to the real structures as well because the sandwich structure, the interface conditions at the top passivation surface, and the conditions in the probe station are left unchanged.

III. Simulation Results and Discussion

In the first attempt, we studied the Joule heat generation as a result of dc loads. The selected range of current density between 0.5 MA/cm^2 and 2.5 MA/cm^2 is commonly used in accelerated electromigration tests. Because of the relationship between average and RMS current density (Fig. 2), it reflects, however, the situation under service conditions as well, even when the design rule $J_{\text{ave\_max}} = 0.2$ MA/cm^2 is obeyed. Besides the load application to each metallization level of test and real structures individually, simultaneous loading of any combination, i.e. all line of level 1 and 2, 1 and 4, or 3 and 4, and so on, have been included in the simulation program. As seen in Fig. 5, the results show distinct trends.

1) The temperature rise increases roughly proportional to the square of the current density. Actually, it rises even a bit more due to the increase of the electrical resistance with temperature.
2) The thickness of the oxide layer between the interconnect and the silicon chip has a big impact on the magnitude of the temperature increase. The thicker this layer, which has a small thermal conductivity, the larger is the temperature rise.
3) Metal lines underneath that interconnect, which is stressed by the current, increase the effective conductivity of the main thermal path. This leads to a reduction in temperature rise as long as these metal lines do not generate a significant amount of heat themselves.

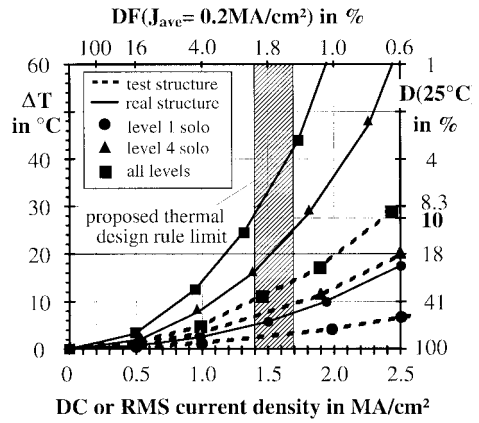

Fig. 5. Temperature rise [ΔT] beyond room temperature in test structures and real IC interconnects when stressed individually (level 1 solo and level 4 solo) or simultaneously (all levels, here temperature of level 4 interconnects is plotted). Assuming an average current density of $J_{\rm ave} = 0.2$ MA/cm^2, the RMS current densities are reached by unidirectional pulses that have the indicated duty factors [DF]. Thus, the decrease in electromigration lifetime with respect to the level at the reference temperature, here. 25 °C, [D (25 °C)] can directly be read out of the results.

4) When the current density in the lower level interconnects, however, reaches a significant level as well, the thermal situation exacerbates. The maximum temperature rise occurs when all lines are loaded simultaneously. In this case, the temperature of lines in several uppermost levels may be quite the same although the oxide thickness underneath them is different. This would be caused by the additional heat dissipation via the top passivation surface.

The most important result of this set of simulations is, however, the differences in magnitude between the temperature rise in the test structures and the real structures. Because the test structures consisted of one single line or at most of one single pile of four lines (one on top of the other[1]), more or less the entire chip can serve as heat sink for this (these) line(s). On the other hand, only the area directly underneath the line can be effective as heat sink in the densely packed real structures. The adjacent chip region has to dissipate the heat that is simultaneously generated in the adjacent lines. That means, real structures have a much higher thermal impedance than the commonly used test structures.

In our example, a current density of 1.5 MA/cm^2 leads to a temperature increase of 3 °C in a single level 1 test line. When all four test lines are stressed, the maximum temperature increase of 12 °C occurs in both, the level 3 and 4 lines. The simulated response of a typical real structure to this simultaneous load would, on the other hand, be a temperature rise of 36 °C, i.e., three times more. Because of the exponential dependency between temperature increase and electromigration damage rate (Fig. 1), 76% of the lifetime at room temperature would still be reached in the case of the single test line while it would already be reduced to 35% in the case of the four test line pile. The lifetime of the typical real structure, however, would be diminished to

[1] This case was considered in the simulation only and not in the experimental tests.

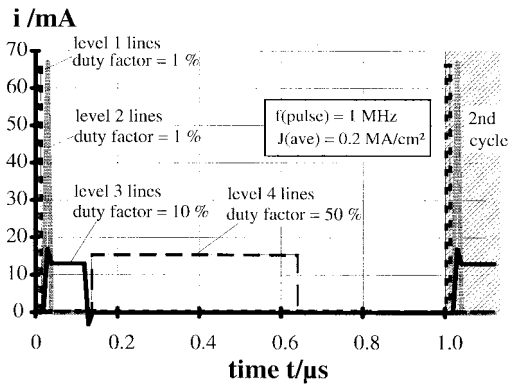

Fig. 6. Impulse loads applied to a simulated quadruple level real structure metallization with line width of 0.5/0.5/1.0/3.0 μm at level 1/2/3/4, respectively.

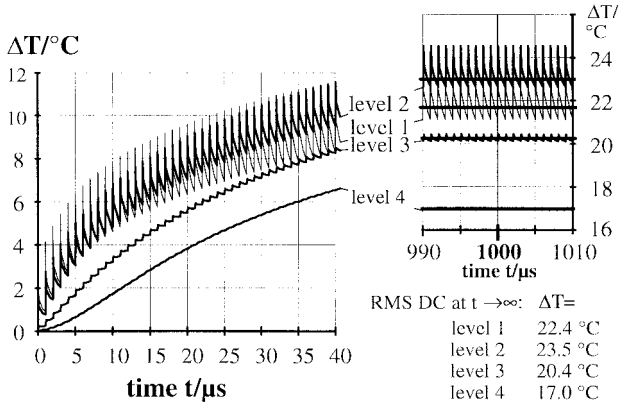

Fig. 7. Transient and the steady state thermal response of the real interconnect structure (temperature rise beyond RT) to the mixed unidirectional pulse load according to Fig. 6.

5.3%, i.e., it would be about 20 times less than at room temperature without additional Joule heating and almost seven times less than in the worst test structure case. At today's typical chip temperature under service conditions of 105 °C, those temperature increases would lead to relative lifetime reductions of 16%, 48%, and 85%, respectively.

In real circuits, the lines of multilevel interconnect systems usually handle a mixture of different pulses. Fig. 6 gives an assumed example of such a mixed signal. The pulses with the lowest DF have been assigned to the low level interconnects. The waveform has been varied to include switch-on and switch-off delays (levels 2 and 3) as well as overshoots (level 3). The average current density, however, has always been kept at the design rule limit. The frequency has intentionally been chosen rather low. At higher frequencies, any fluctuations would be leveled by the thermal moment of inertia of the structure. In the case of 1 MHz, however, the structure can still follow the pulses quite well as seen in the result plot in Fig. 7. These results demonstrate first of all the ability of the simulator to obtain thermal parameters such as characteristic time constants, temperature fluctuations per pulse, interaction between all lines, etc. precisely without further experiments. In our case, they indicate for example that the line at level 4

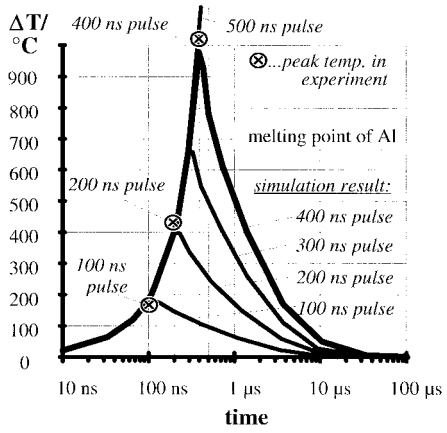

Fig. 8. Temperature rise in level 1 test structure interconnect during ESD stress (short, isolated 850 mA pulses).

is heated only indirectly, i.e. the Joule heat generated by $J_{\rm ave} = 0.2$ MA/cm^2 and $\mathrm{DF} = 50\%$ in this line itself is insignificant. That's why there is a start delay in the course of the temperature curve and the fluctuations are negligible. The results make also clear, the line at level 4, which is exposed to the highest average current load of the whole structure ($i_{\rm ave} =$ 8 mA) and could therefore be thought to fail first, actually shows the lowest temperature increase and has consequently the highest lifetime expectation. Hence, a thermal assessment is crucial for designing reliable interconnect structures. The effort needed for this assessment, however, can be limited. As seen in the results, the temperature rise reaches its maximum at the stable state, the fluctuations are rather insignificant even at the relatively low frequency (just about $\pm$ 1 °C at a level of $\Delta T \approx 23$ °C), and the transient period lasts certainly less than one millisecond. Therefore, a one-step static simulation can replace the time consuming transient analysis in most of the cases. In those static analyses, the RMS magnitudes of the current has to be applied as load. As seen in Fig. 7, the RMS load results and transient results coincide perfectly except for the small periodic fluctuations. This finally also proves the upper x axis in the dc result plot (Fig. 5) to be valid.

One of the special cases, in which a static analysis is not sufficient, is the EOS/ESD case. Here, a single, very short but huge pulse strikes the interconnects. Electromigration lifetime is therefore not the primary concern but melting that could open those lines, which are supposed to act as "lightening conductor" for the rest of the circuitry. A standard transmission line pulsing technique [7] was used in the experiments accompanied by transient thermal simulations. The constant pulse current went up to 1.5 A and the pulse widths were varied between 100 ns and 500 ns. Thus, the minimum time step size of 0.1 ns recommended by ANSYS® [8] is sufficiently small. Because melting of the aluminum line is likely, the temperature range of the included material models was extended to 1500 °C including published data for the enthalpy. Fig. 8 plots the results of a simulated test in which a level 1 test interconnect was stressed by 850 mA pulses. It can be seen, the melting point of aluminum is reached by pulses of about 300 ns width. During longer pulses, it is clearly exceeded. Passing the melting point, the temperature versus time curve does not rest, i.e., there is no delay although an extra melting energy has to be supplied. The reason is, that under constant current conditions the voltage drop at the line rises at the melting point because of the sudden increase in electrical resistivity due to the loss of the crystalline structure. In this way, the latent heat of fusion is instantaneously supplied. After melting, the temperature rises even a bit faster because the slope of electrical resistivity versus temperature is higher for the liquid metal. The most important result of this test is, however, the proof that lines can get melted under these pulses but do not necessarily fail. Both, the simulations of this work and the experiments discussed in detail by [9], have unanimously lead to a threshold temperature of about 1000 °C before the oxide layer is blasted and the circuit is opened. In the example plotted in Fig. 8, all lines did survive the 400 ns pulse but they did always fail during the 500 ns 850 mA pulse for which a peak temperature of 1700 °C was computed.

IV. Conclusion

The results have shown that real interconnects of future VLSI circuits will be affected by self-heating effects more severely than those of today's generation and much more than test structures make us believe. The reason is that while obeying all present design rules, the current density in the low level lines will reach a critical RMS level. Therefore, it seems prudent to introduce an additional self-heating design rule of about $J_{\rm RMS} \leq 1.5$ MA/cm^2 for aluminum lines. It limits the unavoidable degradation of electromigration lifetime due to temperature increase in the current carrying or in any nearby interconnect. It makes sure that all structures have a real lifetime of at least 10% of the theoretical level without self-heating (Fig. 5). According to Fig. 1, the exact magnitude of the thermal design rule limit may vary dependent on the reference temperature between $J_{\rm RMS\_max} = 1.4$ MA/cm^2 ($T_{\rm ref} = 25$ °C) and $J_{\rm RMS\_max} = 1.7$ MA/cm^2 ($T_{\rm ref} = 125$ °C) and as a function of the specific thermal situation in the particular structure.

A methodology has been introduced for an effective assessment of the thermal situation in interconnect structures right during their design process. The perfect agreement with experimental results proves the applied simulator to be a trustworthy tool when it is sufficiently calibrated by the described few simple experiments. Quantitatively accurate results can be obtained for both, static and transient thermal situations.

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Sven Rzepka (M'95) received the M.S. and Ph.D. degrees from the Dresden University of Technology, Dresden, Germany, in 1988 and 1991, respectively.

Since 1992, he has been a Research Associate at Semiconductor Technology and Microsystems Lab, Dresden University of Technology. In 1995 and 1996, he was a Postdoc at the University of California at Berkeley. Before returning to Dresden University, he was a Research Associate at Cornell University, Ithaca, NY, for another year. His scientific interests are in advanced packaging technologies and reliability issues of interconnect systems and packaging structures. After developing soldering and welding processes for large area array flip-chip assemblies during his graduate and doctoral periods, he has focused on finite element simulations of failure mechanisms in flip-chip modules and interconnect lines afterwards. He has published more than 25 technical papers on those subjects.

Kaustav Banerjee (S'97) received the B.S. degree from the University of Bombay, India, in 1990, the M.S. degree from Marquette University, Milwaukee, WI, in 1993, and is currently pursuing the Ph.D. degree in the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley.

He has been engaged in a number of joint projects with Texas Instruments, Dallas, TX, on high current effects in VLSI interconnects, contacts, and silicides. He has also worked on contact resistance modeling and electromigration. He has authored or co-authored over 15 technical publications on these subjects, and has made a number of presentations at leading international meetings and conferences on electron devices and reliability physics, including an invited tutorial at the 1998 International Reliability Physics Symposium.

Mr. Banerjee is a member of the IEEE Electron Devices Society.

Ekkehard Meusel received the M.S. degree in electrical engineering and and the Ph.D. and Habilitation degrees from the Dresden University of Technology, Dresden, Germany, in 1961, 1971, and 1982, respectively.

During the subsequent years, he has responsibly participated in various projects on die bonding, wire bonding, flip-chip, and chip-on-board technologies. In 1991, he became Full Professor for micropackaging at Dresden University. He has supervised numerous research projects supported by industry or government. He is the head of the Semiconductor and Microsystems Technology Laboratory, Dresden University. He has published and presented more than 40 technical papers.

Chenming Hu (F'90) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., and the Ph.D. degree in electrical engineering from the University of California at Berkeley.

He was an Assistant Professor at the Massachusetts Institute of Technology, Cambridge, for three years. Since 1976, he has been a Professor of electrical engineering and computer sciences at the University of California at Berkeley. He was the Board Chairman of the East San Francisco Bay Chinese School and is a frequent advisor to industry and educational institutions. His research areas include microelectronic devices, thin dielectrics, circuit reliability simulation, and nonvolatile memories. He has authored or co-authored four books and over 600 research papers and supervised 60 doctoral students.

Dr. Hu received the Excellence in Design Award, Design News, and the first semiconductor Research Corporation Technical Excellence Award for leading the development of IC reliability simulator, BERT, in 1991. He also received the SRC Outstanding Inventor Award in 1993 and 1994. He leads the development of the MOSFET and model BSIM3v3 that was chosen as the first industry standard model for IC simulation in 1995 and given an R&D 100 award as one of the 100 most technologically significant new products of the year in 1996. IEEE awarded him the 1997 Jack A. Morton award for his contributions to MOSFET reliability physics and modeling. Also in 1997, he received the Berkeley Distinguished Teaching award. In 1998, he was given the Moni Ferst award by the Georgia Institute of Technology, Atlanta, for inspiring graduate student research. He is a member of the U.S. National Academy of Engineering and an Honorary Professor at Beijing University, Beijing, China, and of the Chinese Academy of Science.