Open access • Journal Article • DOI:10.1109/TEMC.2009.2033577

Characterization of the Evolution of IC Emissions After Accelerated Aging

Alexandre Boyer, A.C. Ndoye, S. Ben Dhia, L. Guillot ...+1 more authors

Institutions: Freescale Semiconductor

Published on: 17 Nov 2009 - IEEE Transactions on Electromagnetic Compatibility (IEEE)

Topics: Electromagnetic compatibility and Electronic component

Characterization of the Evolution of IC Emissions after Accelerated Aging

Alexandre Boyer, Amadou Ndoye Cisse, Sonia Ben Dhia, Laurent Guillot, Bertrand Vrignon

Characterization of the Evolution of Integrated Circuit Emissions after Accelerated Aging

Alexandre Boyer, Amadou Cisse Ndoye, Sonia Ben Dhia, *Member, IEEE*, Laurent Guillot, Bertrand Vrignon

***Abstract*—With the evolving technological development of integrated circuits, ensuring electromagnetic compatibility (EMC) is becoming a serious challenge for electronic circuit and system manufacturers. Although electronic components must pass a set of EMC tests to ensure safe operations, the evolution over time of EMC is not characterized and cannot be accurately forecast. This paper presents an original study about the consequences of the aging of circuits on electromagnetic emissions. Different types of standard applicative and accelerated-life tests are applied on a mixed power circuit dedicated to automotive applications. Its conducted emissions are measured before and after these tests, showing variations in EMC performance. Comparisons between each type of aging procedure show that the emission level of the circuit under test is affected differently.**

***Index Terms*— aging effects, conducted emissions, electromagnetic compatibility, integrated circuit testing**

I. Introduction

EMC requirements for electronic system manufacturers are becoming increasingly severe, because of more stringent demands on safety and technology scaledown. Integrated circuits (ICs) therefore have to comply with many different specifications in terms of quality to ensure system functional safety. Components dedicated to safety-critical applications operating in harsh environments, such as automotive, aeronautics, or electrical supplier applications, must ensure nominal functionality throughout the minimum exploitation duration (ten to thirty years) [1]-[2]. Hence qualification tests are required to check the compliance of components to customer specifications, such as electromagnetic compatibility (EMC) tests. In this context, emission and susceptibility of integrated circuits are both critical issues for reducing interference risks at system level [3].

However, EMC qualifications are often carried out on only one burn-in component. Moreover, EMC tests are rarely coupled with reliability tests to check EMC in harsh environments. EMC research projects mainly focus on low emission and susceptibility design techniques, while little attention is given to the real-life environment of electronic devices (e.g., effects of temperature or electromagnetic environment [4] [5]) including the impact of natural aging [6], which can degrade both functionality and the electromagnetic behaviour of an integrated circuit. The evolution over time of emission and susceptibility levels and the relevance of the aging margin used to compensate for the drift of EMC levels are not evaluated during qualification phases. Although these topics are crucial for ensuring sufficient long term safety, EMC standards give no guidance. Different expert groups have identified gaps in usual EMC qualification procedures and pointed out several issues such as the life profile conditions, process dispersion, or aging. In [7], many guidelines are given to improve EMC test plans and choices of EMC mitigation techniques to guarantee the functional safety of electronic systems, e.g., by taking into account actual environmental and physical conditions of devices during EMC tests and their whole lifecycle.

In this context, a new request from electronic equipment suppliers aimed at ensuring the electromagnetic robustness (EMR) of embedded systems appeared recently with the emphasis on going further in electromagnetic behaviour improvement at the IC level, by taking aging factors into account [8]. This concept is an extension of EMC for the full lifetime of a product in order to improve safety and long term reliability. This paper presents an original study of the impact of circuit aging on electromagnetic emissions, in order to provide better insight into the impact of intrinsic circuit degradation due to natural aging on electromagnetic emissions, which can justify the usefulness of further EMC level margins or EMC mitigation techniques. One case study based on a commercial off-the-shelf IC dedicated to automotive applications is proposed. Its emission spectrum is compared prior to and after applicative and accelerated-life tests according to reliability standards. Statistical analyses are performed to identify and clarify the effects of aging on the evolution of parasitic electromagnetic emission.

In the first section of the paper, common IC intrinsic failures are reviewed and the links between circuit reliability and EMC issues are analyzed to highlight the need to characterize EMC on aged components. We then describe the proposed

Manuscript received October 9, 2001.

A. Boyer, A. Cisse Ndoye and S. Ben Dhia with the National Institute of Applied Sciences, 135 Avenue de Rangueil, 31077 Toulouse, France (e-mail: alexandre.boyer@insa-toulouse.fr, amadou.ndoye@insa-toulouse.fr, sonia.bendhia@insa-toulouse.fr).

L. Guillot and B. Vrignon are with Freescale Semiconductors, Avenue du general Eisenhower, 31100 Toulouse, France. (e-mail: Laurent.guillot@freescale.com, Bertrand.vrignon@freescale.com).

methodology for characterizing the evolution of emissions, the component under test, the emission measurement set-up, and the aging tests. In the fourth section, emission measurement results obtained before and after the different aging tests are compared. Resulting emission drifts are analyzed. In the final section, some hypotheses are proposed to explain the drifts of emission level.

II. Consequences of Integrated Circuit Aging on Electromagnetic Compatibility

A. Reliability Issues in CMOS Circuits

During their lifetime, components are affected by intrinsic failure mechanisms such as electro-migration, gate oxide breakdown, or hot carrier injection [9] [10], mainly activated by harsh environmental conditions such as high or low temperature and electrical overstress. Table I sums up the main failure mechanisms which may affect MOSFET transistors and their characteristics. The most common intrinsic failures of CMOS circuits induce charge trapping and breakdown in gate oxide, and migration in the metal levels, as illustrated in the cross section of a CMOS device presented in Fig. 1. The degree of degradation of a device and, hence, its lifetime depends on the stress level and duration.

TABLE I
Common CMOS integrated circuit intrinsic failure mechanisms and failure mode [11]

Failure mechanism	Cause of failure	Failure mode	Acceleration factor
Gate oxide defect	Crack, holes in oxide	Open circuit	High temp. Electrical field
Hot carrier injection	Trapped carrier in gate oxide	Threshold voltage and saturation current drift	Low temp.
Electro - migration	Atom movement in metal layers	Open circuit	High temp. High current density
Negative Bias Temperature Instability (NBTI)	Trapped carrier in gate oxide	Threshold voltage and saturation current drift	High temp. High negative voltage
Mobile ion contamination	Polarisable molecule	Threshold voltage drift	High temp. Electrical field

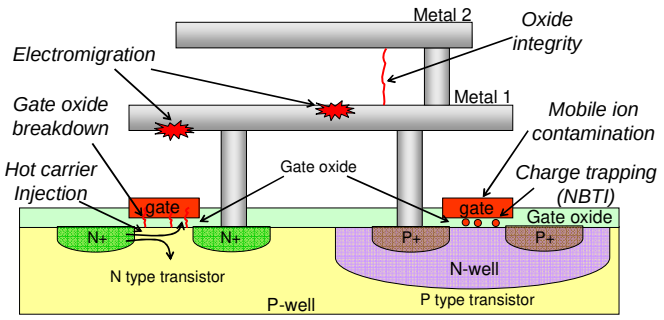


Fig. 1. Common failure mechanisms in CMOS circuits [12]

B. Accelerated Life Tests

Accelerated life tests consist in applying a high level stress condition (e.g., high temperature or high voltage) for a short period in order to accelerate the damage rate for relevant wear-out failure mechanisms [13]. If the acceleration factor (AF) related to a degradation mechanism and an environmental condition is known, then the lifetime of the device under test can be extrapolated, e.g., by using the Arrhenius Law for thermal acceleration (1), as explained in Fig. 2:

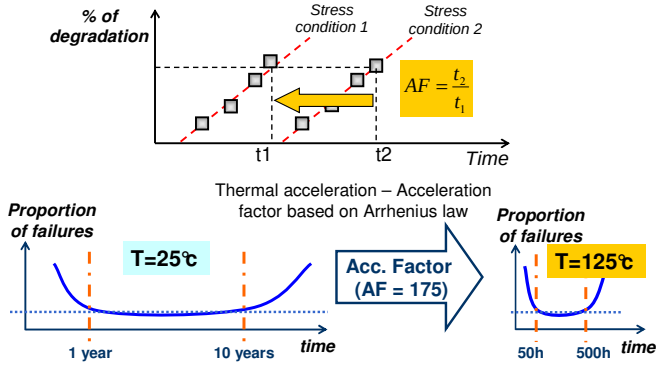
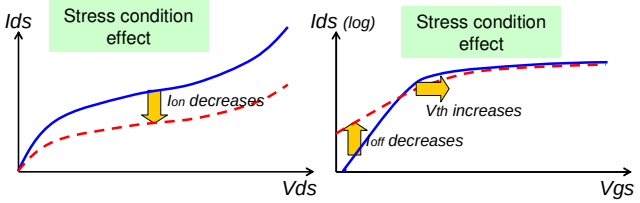


Fig. 2. Principles of accelerated life test

$$AF = \exp\left(\frac{E_A}{K} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \quad (1)$$

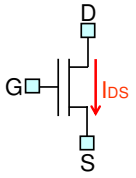
C. Effect of Intrinsic Failures on CMOS Device Characteristics

Various studies have shown that the first failures affecting a component appear sooner for nanometric technologies than for older technologies [14]. Even if functionality is often preserved especially in digital circuits [15], many circuit characteristics such as operating frequencies, current consumption, leakage current [15], noise [16], gate capacitance, or gate oxide resistance [17] can be noticeably modified. Fig. 3 presents the typical MOSFET transistor parameters affected by degradation mechanisms which induce performance losses in circuits and (2) a simplified equation for the drain current of a MOS transistor in the saturation region based on the BSIM3 model [18]:



Parameters	Drift sense
Threshold voltage Vth	Increasing
Mobility Ueff	Decreasing
Saturation current Ion	Decreasing
Leakage current Ioff	Increasing

Fig. 3. Effect of transistor degradations on characteristics of MOS transistor



$$I_{ds} = U_{eff} \frac{\varepsilon_0 \varepsilon_r}{T_{ox}} \frac{W}{L} \left(V_{gs} - V_{th}\right)^2 \quad (2)$$

D. *Effects of Circuit Intrinsic Failures on EMC*

EMC can also be affected by the intrinsic failures of CMOS circuits. For example, the modification of MOS transistor parameters (Fig. 3) such as threshold voltage or mobility can directly influence IC transient current and thus the IC conducted emissions [19]. It can also modify delay propagations within the digital cores of ICs which make them more sensitive to delays induced by electromagnetic interference [20].

In practice, the effects of component aging, dispersion, or measurement uncertainties are compensated for by additional compatibility margins, which are typically about 6 - 20 dB in many applications [21]-[22], as explained in Fig. 4.

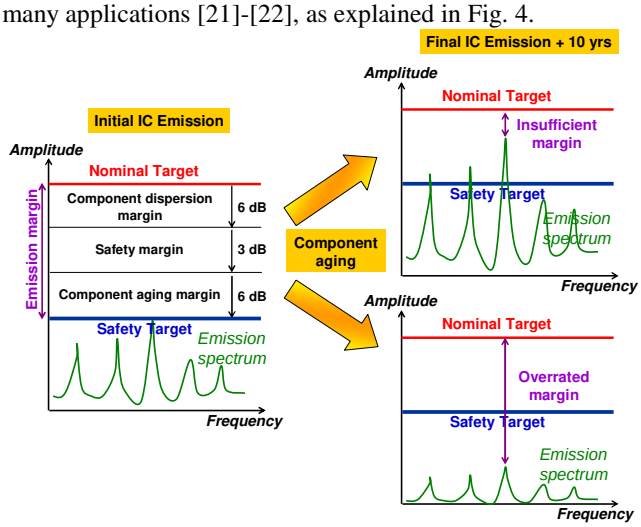


Fig. 4. Impact of component aging on emission level

However, the effects of IC aging on EMC performance are not clearly identified. This lack of knowledge could have dramatic consequences on system safety. If the emission levels increase, the aged circuit would cease to comply with EMC requirements. The risk that the emission level exceeds the emission limit and causes interference between neighbouring electronic devices increases (Fig. 5). Conversely, if the emission levels decrease, although interference risks are reduced, the initial EMC requirements become too severe and could lead to over-design and unnecessarily high costs.

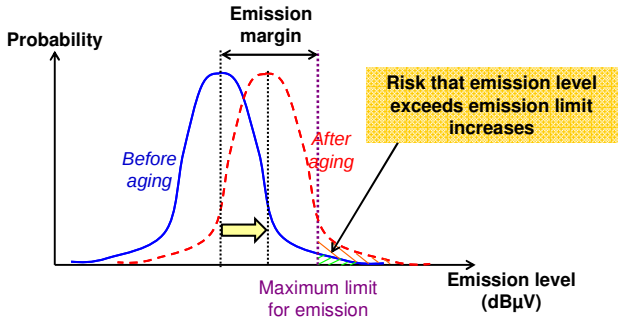


Fig. 5. Emission level increase due to circuit aging has an impact on the risk that the emission level exceeds the emission limit

Although commercial ICs have to be qualified for both EMC and reliability to ensure customer requirements, these two areas remain totally disjoined and are tested independently. EMC tests are always performed on "fresh" components, so the effects of aging on EMC performance cannot be accurately evaluated and additional margin and mitigation EMC techniques may be justified. In the following sections, the conducted emission level of a circuit is characterized before and after aging tests to ensure accurate measurements of the drift of emission spectrum induced by IC degradation mechanisms.

III. Experiment Description

A. *EMR Qualification Methodology*

In order to exhibit aging effects on emission, emission spectrums were compared before and after an accelerated-life test (Fig. 6).

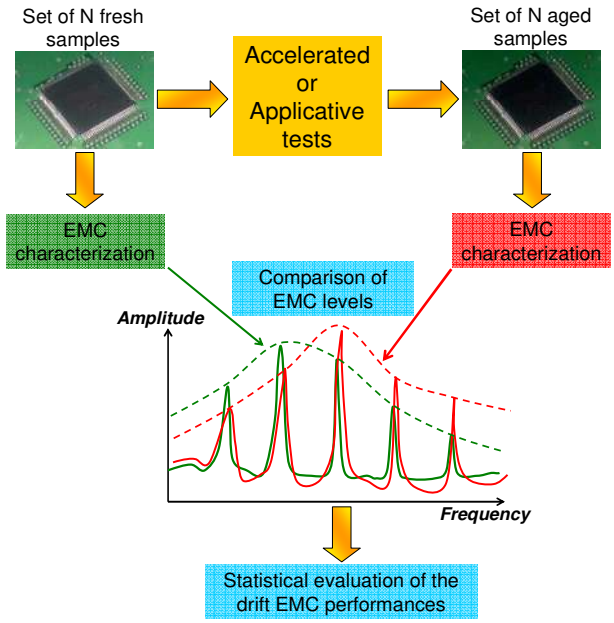


Fig. 6. EMR qualification methodology

The EMR procedure must be applied to a sufficiently large number of samples to obtain an accurate estimation of EMC variation due to aging, because measurements done on only one sample cannot be representative of the characteristics of a whole device family. The measured drifts between samples can have several origins:

- Measurement repeatability for a given sample;
- EMC-level dispersion due to differences or process variations between tested samples;
- EMC-level global drift due to technological intrinsic degradation effects.

Measured drifts are consistent only if they are greater than measurement repeatability and are independent of time. Like the global EMC-level drift due to aging, process variations can also be affected by aging and degrade EMC performance. In order to isolate the drift caused by the accelerated aging from the process variations and measurement repeatability, the experimental procedure described in Fig. 7 is used. A

reference part allows measurement repeatability to be quantified with regard to variations in measurement devices or test benches. EMC characterization is repeated several times on this reference part. All the others parts are then tested once to evaluate the EMC differences due to the component process variations before aging. The different parts are divided into separate batches, dedicated to one or several specific applicative or accelerated-life tests. Finally, all the samples from each batch are tested again and two values linked to the aging effects are extracted. First, comparison of EMC levels of each sample of a given batch obtained before and after aging gives the global EMC drift due to a particular aging test. Second, dispersion of EMC levels of all parts of a given batch is computed to highlight the effect of aging on the process variations. Statistical analyses such as mean drift σ_M (3) or standard deviation σ (4) are required to assess EMC level modification induced by aging.

$$\sigma_M = \frac{1}{N_{sample}} \sum_{i=1}^{N} X_i - \overline{X} \quad (3)$$

$$\sigma_M = \sqrt{\frac{\sum_{i=1}^{N} \left(X_i - \overline{X}\right)^2}{N_{sample} - 1}} \quad (4)$$

X_i is the emission level of one sample,

$\overline{X}$ is the mean emission level of all samples,

N_{sample} is the number of samples.

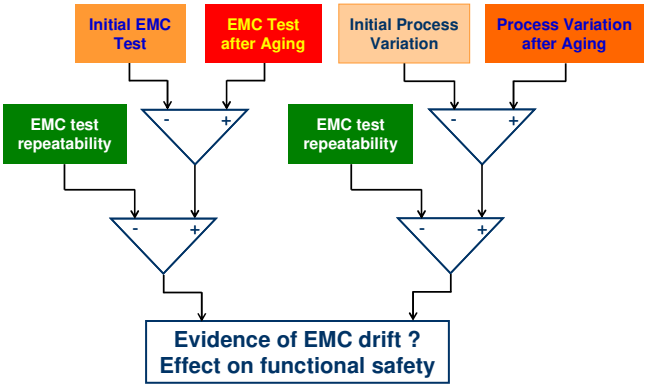


Fig. 7. Analysis methodology of electromagnetic robustness test

B. Description of the Component Under Test

The circuit tested was an “eXtreme Switch” (E-Switch), a mixed power circuit designed to replace electrical relays, fuses and discrete components within automotive embedded power applications. Like all electronic devices for automotive applications, the E-Switch must comply with severe reliability and EMC requirements. Maintaining EMC compliance during the vehicle’s lifetime is critical to ensure passenger safety.

The E-Switch includes a power circuit with four integrated self-protected 15 mΩ TMOS switches and a 0.25µm BiCMOS control circuit for an extended diagnosis system for vehicle front lighting management. The combination of power and digital parts in a low thermal impedance package requires two separate chips within the same Plastic Quad Flat No lead (PQFN) package. The digital part is clocked by an internal 9 MHz oscillator. An internal charge pump is used to produce the high voltage required on the gate of N-channel TMOS. Fig. 8 gives an overview of the internal architecture of the component.

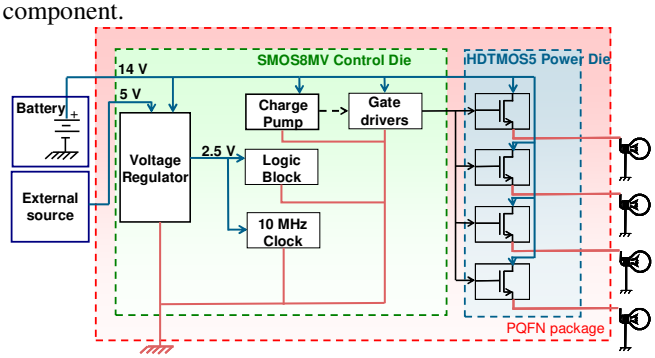


Fig. 8. Internal architecture of the E-Switch

C. Applicative and Accelerated-life Tests

Applicative and accelerated-life tests used for this experiment are typical of those used in the automotive industry and are described by the AEC-Q100 standard published by the Automotive Electronics Council [23]. They are required to qualify integrated circuits and guarantee the quality and the robustness of automotive applications. Samples of the studied component underwent the different applicative and accelerated-life tests described in Table II. These different tests do not affect all of the circuit under test in the same way. While HTOL usually has a major impact on intrinsic degradations in the silicon die, TC induces mechanical constraints on the package. Both tests are performed in a climatic chamber to control temperature accurately. HTOL and TC test set-ups are described in Fig. 9. ESD and LD tests reproduce the electrical overstress used for the burn-in of the component that can affect ESD and I/O pad structures.

The different circuits are placed on specific boards during reliability tests. They are then mounted on the EMC test board by a socket for the conducted emission characterization, so that only the circuit is degraded during the reliability tests. Therefore, if a deviation of the emission spectrum is detected, only the aged component will be responsible. For reasons of cost and component availability, a batch of 16 samples was studied. Once the measurement repeatability and the process variations had been characterized, the components were separated into four sub-batches to pass the four different reliability tests described in Table II.

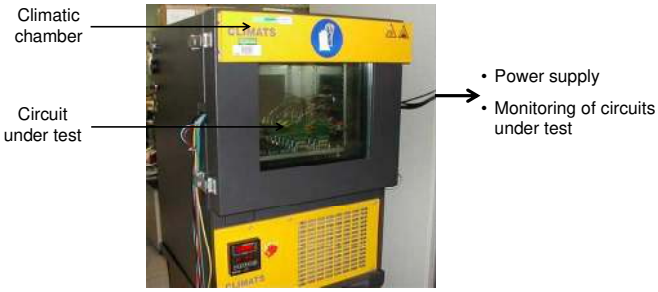


Fig. 9. Climatic chamber for accelerated-life tests

TABLE II
APPLICATIVE AND ACCELERATED-LIFE TEST CONDITIONS [23]

Test type	Test name	Conditions	Number of samples
Applicative tests (overstress)	**Electrostatic Discharge** (ESD)	+/-8kV HBM on Power I/Os +/-2kV HBM on Digital I/Os	4
	Load Dump (LD)	+41V during 400msec Sub-tests: Outputs "on" Outputs "off"	4
Accelerated-life tests (time dependent)	**Temperature Cycling** (TC)	Ambient temperature cycling from -65°C to +150°C,1000 cycles	4
	High Temperature Operating Life (HTOL)	Ambient temperature +150°C 408 hours Typical device operation	4

D. Conducted Emission Measurement Setups

Fig. 10 describes the E-Switch conducted emission measurement test bench and the nominal operating conditions of the device under test. The measurement is carried out in accordance with the international standard CISPR25 [24]. The noise conducted on the VPWR power supply line is characterized in the 150 kHz – 80 MHz band. The measured noise corresponds to interference produced by the circuit activity and conducted along the battery cables. A line impedance stabilizer network (LISN) is used to set the line impedance and isolate the power supply source from the device under test.

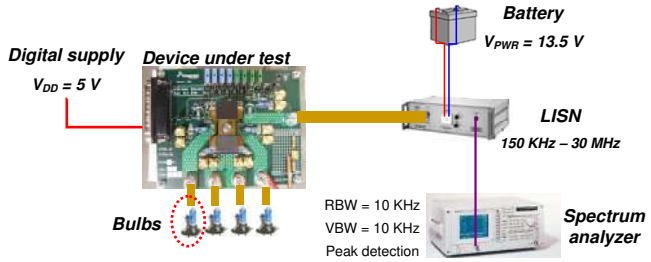


Fig. 10. Power supply conducted emission measurement test-bench

IV. RESULT ANALYSIS

A. Characterization of Conducted Emissions

Fig. 11 presents the conducted emission spectrum measured on the VPWR supply of a non-aging component between 150 kHz and 80 MHz. This measurement is representative of a component without external decoupling capacitors. Only components dedicated to HTOL aging are correctly decoupled so that the emission spectrum level is lower. However, this procedure can affect the accuracy of the characterization of aging effects. High amplitude peaks appear at each harmonic of 9 and 18 MHz related to the activity of the digital part, and also at 26 MHz because of the charge pump activity. Only the higher harmonics of these frequencies are taken into account for this study. The harmonic which appears at 3 MHz is due to a parasitic activity of the component so it is not considered.

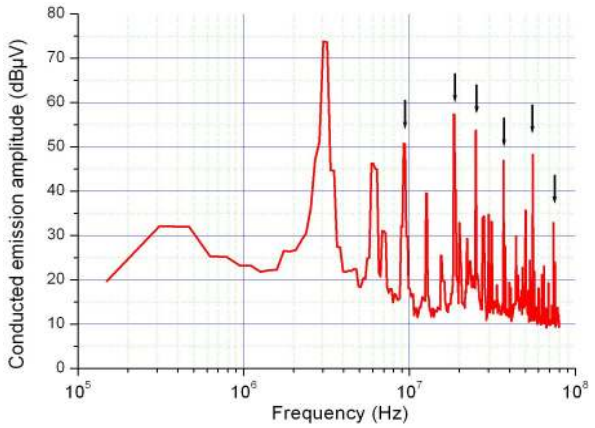


Fig. 11. Conducted emission spectrum measured on VPWR supply of a non-burned component

B. Characterization of Measurement Repeatability and Process Variations

Table III sums up the results for the characterization of measurement repeatability for the six higher harmonics of the emission spectrum and gives an indication of the resulting dispersion due to the repeatability errors of the measurement system. Conducted emission measurements on the VPWR supply were repeated five times on the reference sample 0. Amplitude measurement errors remain negligible up to 26 MHz and increase from 36 MHz. The mean repeatability for the different harmonics is about 0.45 dB. Frequency measurement errors are null whatever the frequency.

Effects of process variations on emission dispersion before aging were also characterized on all 16 available samples. Table IV sums up the effects of the process variations on the amplitude and frequency dispersions of the six higher harmonics. The frequency dispersion is given in terms of the ratio between the frequency drift and the frequency of the harmonics. Dispersions due to process variations on amplitude are higher than measurement errors, but remain within an acceptable margin, proving that the technological process is controlled.

TABLE III
REPEATABILITY CHARACTERIZATION (10 MEASUREMENTS)

Frequency (MHz)	9	18	26	36	54	72	Repeatability
Amplitude mean drift (dB)	0.16	0.18	0.17	0.57	0.59	1.05	0.45
Frequency mean drift (Hz)	0	0	0	0	0	0	0

TABLE IV
PROCESS VARIATION CHARACTERIZATION BEFORE AGING (FOR 16 SAMPLES)

Frequency (MHz)	9	18	26	36	54	72	Process dispersion
Amplitude mean drift (dB)	0.26	0.53	0.41	0.56	0.83	0.86	0.58
Frequency mean drift (%)	1.34	1.2	1.21	1.17	1.25	1.25	1.24

C. *Emission Spectrum Drift After Different Reliability Tests*

Fig. 12 presents an example of emission spectrum drift on a sample stressed by a set of load dumps. The comparison between the spectrum envelopes of the fresh and aged samples indicates that emission levels increase (up to 2.3 dB at 72 MHz) after a load dump test. Fig. 13 presents other results concerning the samples stressed by HTOL. The peaks of the charge pump harmonic at 26 MHz measured for the fresh and the aged components were compared; the mean values of this peak for the fresh and aged batches also appear on the graph. The amplitude and frequency of the 26 MHz harmonics of each sample have drifted as a result of HTOL stress effects. Both emission level and performance of the charge pump have been affected by HTOL stress.

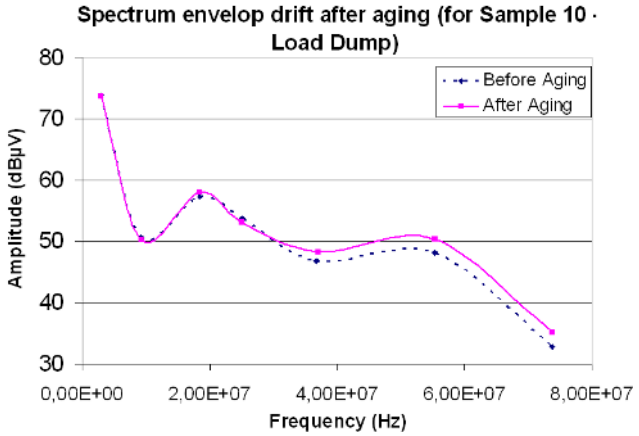


Fig. 12. Emission level increase after load dump test for sample 10

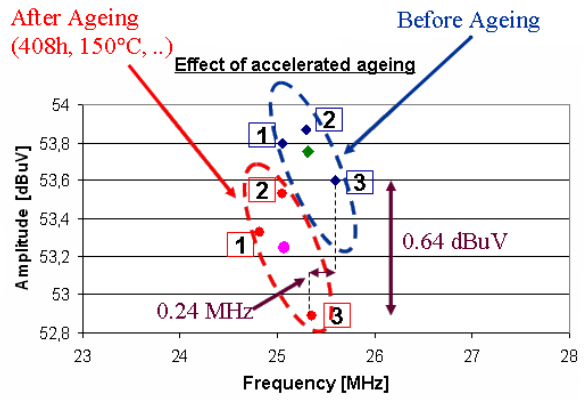


Fig. 13. Measurement of amplitudes and frequencies of 26 MHz harmonic before and after HTOL test

Fig. 14 summarizes the effects of the four aging tests on the amplitude drift of the emission level. Histograms describe the mean amplitude drift measured on each sample of the different batches for the six higher harmonics of the emission spectrum. Arrows superimposed on the histograms give the repeatability dispersions in order to evaluate the consistency of measured drifts. For HTOL tests, only the amplitude drifts of three harmonics were characterized because of different experimental conditions compared to other tests.

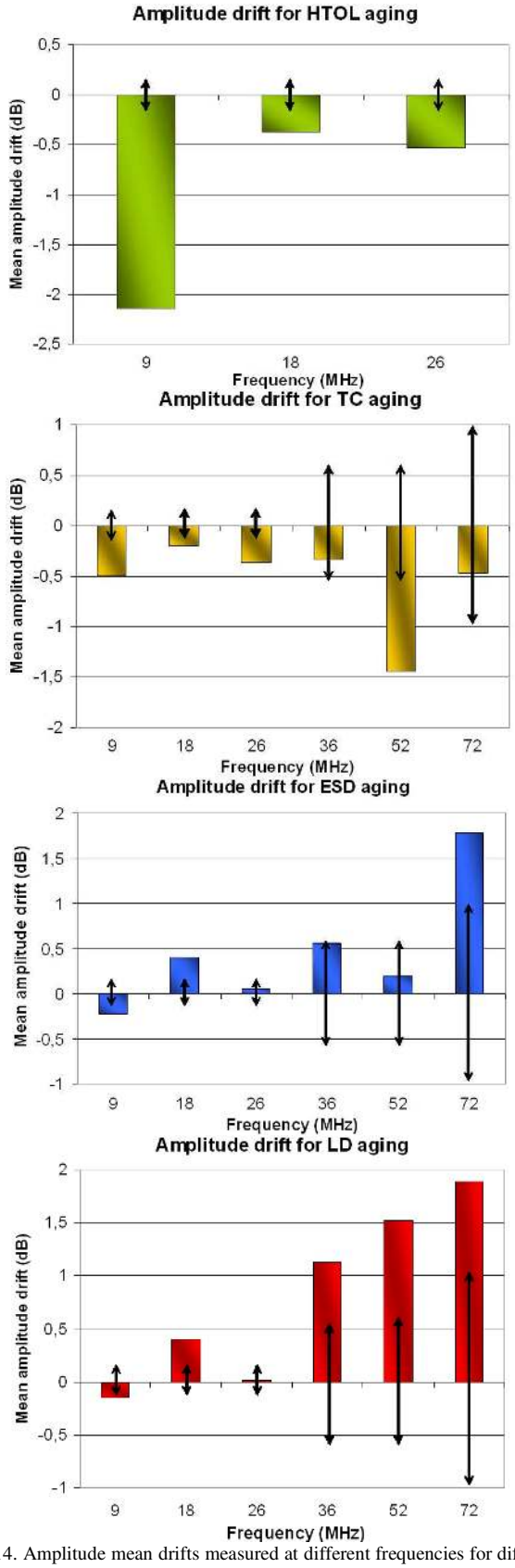


Fig. 14. Amplitude mean drifts measured at different frequencies for different aging tests

The four aging tests have contrasting consequences on parasitic emissions. While HTOL and TC contribute to reducing the emission level, ESD and LD induce an increase of parasitic emissions which can reach 2 dB for some frequencies. Amplitude measurements done before and after aging tests indicate that dispersions between components remain fairly stable, showing that aging has a negligible effect on process dispersion.

The mean emission amplitude drift for each aging test was also computed to evaluate the global impact on the evolution of conducted emissions, and these are presented in Fig. 15. They are compared with measurement repeatability and process dispersion. Amplitude drifts after TC and ESD tests are of the same order of magnitude as measurement error dispersions, so their effects on the emission spectrum are not consistent. However, amplitude drifts after HTOL and LD tests are not only higher than variations in measurement repeatability but also higher than process dispersion so that the impact of these tests on the emission spectrum is significant.

Conducted emission measurements taken after aging tests show that the harmonic frequencies also drifted. Fig. 16 presents the mean drift for the 6 main harmonics of the spectrum after the four aging tests. As the operating frequencies of the digital core and the charge pump are set by internal oscillators, this measurement gives an indirect indication of the degradation of the E-Switch silicon die and the internal blocks. Unlike HTOL, which induces a systematic reduction of the harmonic frequencies, TC, ESD and LD tests have only a negligible impact on harmonic frequency variations and, hence, on IC functional and physical degradations.

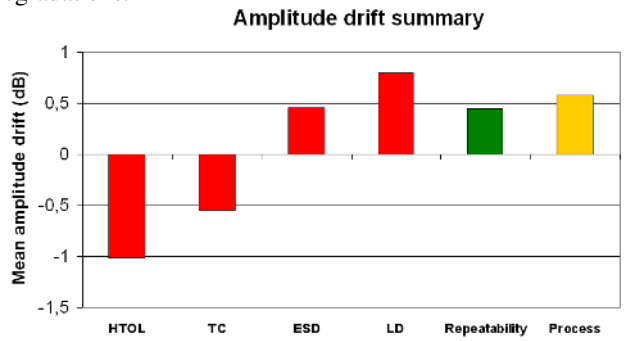


Fig. 15. Emission spectrum mean amplitude drifts after various reliability tests

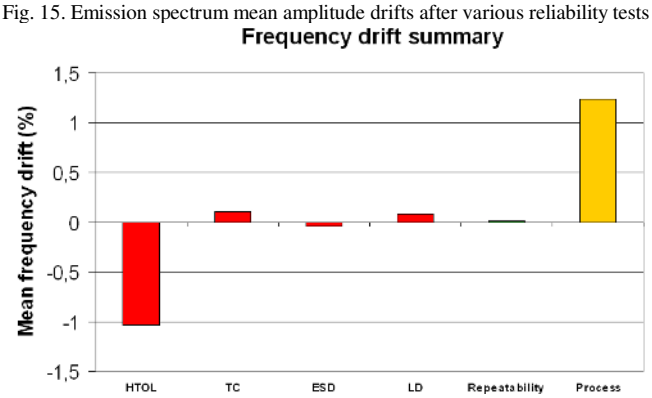


Fig. 16. Spectrum harmonic frequency drifts after various reliability tests

The load dump test had the greatest impact on the IC emission drift. Although the emission level rises, the 0.8 dB emission level increase observed after the load dump test could not have serious consequences on the safety of neighbouring components. However, it reduces the emission margin and thus increases the risk that IC emissions may exceed the emission limit (Fig. 5). For critical applications such as in the automotive sector, it can have more serious consequences since the margin is set to ensure that the failure probability is less than 1 ppm. We can illustrate this issue with the emission measurements taken on the E-Switch. If process variations and measurement repeatability errors are considered as Gaussian distribution functions, the necessary emission margin between the measured emission level and an emission limit can be numerically computed. From the measurements taken before load dump burn-in tests, it was found that a 6.2 dB margin reduces the risk that the emission level exceeds the limit to a probability of less than 1 ppm. As the emission limit remains constant over time, a 0.8 dB increase of the emission level leads to a 152 ppm risk, which is no longer acceptable for critical applications. However, other sources of variations have to be considered, such as environmental and EMC test equipment uncertainties which can be larger than 0.8 dB. In practice, larger margins are required to compensate all these effects and reduce the EMI risk at system level.

V. Discussion of the Origins of Emission Drift

Investigations about circuit intrinsic failures are necessary to determine clearly how the conducted emissions are affected by applicative and accelerated-life tests. Unfortunately, we could not undertake failure analysis procedures on the circuits. However, amplitude and frequency drift of the harmonics of the emission spectrum given by EMC measurements provides some elements on component degradations that allow us to put forward a hypothesis about the origins of emission drift.

The HTOL test accelerates several CMOS intrinsic degradation mechanisms, such as dielectric breakdown or negative bias temperature instability [11]. These mechanisms induce degradations at the transistor level that affect carrier mobility and transistor threshold voltage and thus tend to decrease transistor saturation current [18]. This effect has a direct consequence on the transient current due to switching activity and on the conducted emissions, since the noise source amplitude is reduced.

Although TC induces mainly mechanical strains on the package and has a minor effect on CMOS degradation mechanisms, it contributes to a small reduction in the level of parasitic emissions. IC emissions are not only dependent on the IC switching activity and generated transient current but also on the noise propagation through the power supply decoupling network. The reduction in emission amplitude measured after the TC test can be explained by the degradation of the power decoupling network and the resulting increase of parasitic serial resistance of power supply package pins.

ESD and LD tests produce the strongest effects on parasitic

emissions since they tend to increase the emission level. They can induce severe degradation on ESD protections and I/O pads but do not accelerate degradation mechanisms in the IC core, as shown by the frequency drift measurements. The electrical overstress applied on power supply pins could affect the circuit power decoupling network. All the ESD protection structures placed between power and ground rails act as an equivalent capacitive load and thus as an internal decoupling capacitance. ESD and load dump could degrade this capacitance, creating a resistive path between power supply and ground and hence increasing the emission level. Table V summarizes the consequences of aging tests on parasitic emissions and the hypothesis about the origins of emission drift. A quantitative prediction of emission level variations will require physics-of-failure based modeling [8], which is able to predict accurately degradation impact at transistor level and the effects on circuit performances.

TABLE V
EFFECTS OF VARIOUS AGING TESTS ON PARASITIC EMISSION AND HYPOTHESIS ABOUT THE ORIGINS OF EMISSION DRIFT

Aging test	Effect on emission level	Origin hypothesis
HTOL	Decrease	Acceleration of CMOS degradation mechanisms → reduction of IC transient current
TC	Small decrease, same order of magnitude as repeatability	Mechanical strains on package → increase of power supply pin parasitic resistance
ESD	Small increase, same order of magnitude as repeatability	Degradation of I/O pads and ESD protections → increase of parasitic resistance between power and ground pins
LD	Increase	Degradation of I/O pads and ESD protections → increase of parasitic resistance between power and ground pins

VI. CONCLUSION

IC aging has serious consequences on electrical characteristics, which could lead to electromagnetic emission modifications. Therefore, aged circuits embedded within critical electronic systems could increase the electromagnetic interferences level and thus increase the risk to disturb nearby sensitive ICs. Despite the possible dramatic consequences on system functional safety, the impact of the evolution of IC electromagnetic emissions due to aging has rarely been clearly evaluated. This study proposed a characterization of the impact of aging induced by different types of standard applicative and accelerated-life tests on the emission spectrum of a 0.25 µm mixed power device dedicated to automotive applications. After a first round of exposures, some changes concerning the conducted emission level were identified. Although some of these tests induced an increase in the emission level, the measured drifts are not critical for applications if a sufficient emission margin is planned.

On the basis of emission measurements, several hypotheses are proposed to explain the observed drifts. Degradation mechanisms related to aging tests affect transient current related to IC switching activity and power supply decoupling networks. These degradations could also affect the noise and delay margins of circuits [25] and thus the susceptibility to radiofrequency interferences [26].

In spite of this qualitative analysis made on one component, a quantitative estimation of EMC level drift and an extrapolation to other circuits in different technologies are difficult without a complete physics-of-failure modelling. This type of modelling can take into account integrated circuit technological parameters and has already been applied to predict performances of functional blocks after stress [27] [28]. However, these approaches are limited for EMC simulation due to the size and the complexity of models. Original prediction methods have to be developed to address this issue.

ACKNOWLEDGMENT

The authors would like to thank Professor Etienne Sicard for his valuable comments and suggestions.

REFERENCES

[1] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, M Christopher, "The changing automotive environment: high-temperature electronics", IEEE Transactions on Electronics Packaging Manufacturing, vol. 27, no 3, pp. 164 – 176, July 2004.

[2] T. Furnell, M. Harris, "Management of EMC in aging aircraft in the australian defence force", SETE 2004 (Systems Engineering / Test and Evaluation) Conference Adelaide, Australia, Nov. 2004.

[3] S. Ben Dhia, M. Ramdani, E. Sicard, Electromagnetic Compatibility of Integrated Circuits, Springer, ISBN 0-387-26600-3, 2005

[4] K. Armstrong, "Specifying lifecycle electromagnetic and physical environments – to help design and test for EMC for functional safety", 2005 International Symposium on Electromagnetic Compatibility, pp. 495-500, vol. 2, 8-12 Aug. 2005.

[5] S. Ben Dhia, E. Sicard, Y. Mequignon, A. Boyer, J.M. Dienot, "Thermal influence on 16-bits microcontroller emission", IEEE Symposium on EMC, Hawaii, 6 – 13 July 2007.

[6] W. H. Parker, W. Tustin, "The case for combining EMC and environmental testing", ITEM 2002, pp 54-60, 2002.

[7] "The IET 2008 Guide on Electromagnetic Compatibility for Functional Safety", The Institution of Engineering and Technology, 2008, available on www.theiet.org/factfiles/emc/index.cfm

[8] W. Pfaff, "Industrial use of EMC: trends in system development", Invited Paper, EMC Compo 2005, Munich, Nov. 2005.

[9] M. White, J. B. Bernstein, "Microelectronics Reliability: Physics-of-Failure Based Modeling and Lifetime Evaluation", NASA WBS 939904.01.11.10, 2008, nepp.nasa.gov

[10] J. B. Bernstein, "Physics based reliability qualification", IEEE International Reliability Physics Symposium 2007.

[11] J.C. Gourdon et al., ASTE, "La fiabilité des composants électroniques", in French, 1991.

[12] J. Segura, C. F. Hawkins, *CMOS Electronics: How it works, how it fails ?*, Wiley-IEEE Press, 2004, ISBN 978-0471476696

[13] F. Jensen, *Electronic Component Reliability*, Wiley&Sons, 1995, ISBN 0-471-95296-6

[14] J. Srinivasan, S. V. Adve, P Bose, "The impact of technology scaling on lifetime reliability", International Conference on Dependable Systems and Networks (2004)

[15] B. Kaczer et al., "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability", IEEE Transactions on Electron Devices, vol. 49, no 3, March 2002.

[16] B. E. Weir et al., "Ultra-thin gate dielectrics: they break down, but do they fail?", International Electron Devices Meeting, 1997.

[17] A. Sadat et al., "Analysis and modeling of LC oscillator reliability", IEEE Transactions on Device and Materials Reliability, vol. 5, no 1, March 2005.

[18] W. Liu, *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*, Wiley Interscience, 2001, ISBN 0-471-39697-4.

[19] R. Senthinathan, J. L. Prince, "Simultaneous switching ground noise calculation for packaged CMOS devices", IEEE Journal of Solid-State Circuits, vol. 26, no. 11, Nov. 1991.

[20] J. F. Chappel, S. G. Zaky, "EMI effects and timing design for increased reliability in digital systems", IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications, vol. 44, no. 2, Feb. 1997.

[21] S. Bendhia, F. Lafon, "Impact du vieillissement des composants sur la CEM : du composant au système", in French, Printemps de la Recherche d'EDF R&D, 29 - 30 May 2007.

[22] R. M. Lawton, "Systems guidelines for EMC safety-critical circuits: design, selection and margin demonstrations", NASA Contractor Report 4759, October 1996, http://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/19970005154_19970005074.pdf

[23] *Automotive Electronics Council, Component Technical Committee, Stress test qualification for integrated circuits*, AEC-Q100-Rev-F, 2003.

[24] International Electrotechnical Commission, *Radio disturbance characteristics for the protection of receivers used on board vehicles, boats and on devices. Limits and methods of measurement*, CISPR25 Second Edition, 2002.

[25] R. Fernandez, R. Rodrıguez, M. Nafrıa, X. Aymerich, "Effect of oxide breakdown on RS latches", Microelectronics Reliability, vol. 47, pp 581 – 584, Feb. 2007.

[26] A. Boyer, S. Ben Dhia, "Fiabilité des circuits intégrés face aux agressions électromagnétiques", in French, ANADEF Atenier 2008, Port d'Albret, France, 9 – 13 June 2008, www.anadef.org/

[27] X. Li, J. Qin, B. Huang, X. Zhang, J.B. Bernstein, "A New SPICE Reliability Simulation for Deep Submicrometer CMOS VLSI Circuits", IEEE Transactions on Device and Materials Reliability, vol. 6, no 2, June 2006.

[28] V. Huard, C.R. Parthasarathy, A. Bravaix, C. Guerin, E. Pion, "CMOS Device Design-in Reliability Approach in Advanced Nodes", 47th Annual International Reliability Physics Symposium, Montreal, 2009.

Alexandre Boyer was born in Annemasse, France, in 1981. He received his engineering diploma, Masters and PhD degrees in electronics from the National Institute of Applied Sciences (INSA) in Toulouse, France, in 2004 and in 2007 respectively.
He is currently an Assistant Professor in the Department of Electrical and Computer Engineering at INSA, Toulouse. His current research interests include IC susceptibility modeling, reliability of ICs and computer aided design (CAD) tool development for electromagnetic compatibility (EMC).

Amadou Cisse Ndoye was born in Dakar, Senegal, in 1979. He received his Master degree in Electronics and Microelectronics System Design from the University Paul Sabatier of Toulouse in 2007.
He is currently a PhD student at National Institute of applied Science (INSA) in Toulouse since 2007. His research interests include IC susceptibility measurement and modeling and the impact of circuit degradation on electromagnetic compatibility.

Sonia Ben Dhia received her engineering diploma in 1995, and a Ph.D. in Electronic Design from the National Institute of Applied Sciences (INSA), Toulouse, France, in 1998. She currently holds the rank of associate professor at INSA-Toulouse, Department of Electrical and Computer Engineering, where she teaches digital electronics, IC testability and reliability, and analog and RF CMOS design. She is a member of the INSA Studies Directorate board, organizes transversal educational courses and has responsibility for internal organization. Her research interests include signal integrity in deep sub-micron CMOS ICs and electromagnetic compatibility and reliability of ICs. She has authored technical papers on signal integrity and EMC. She has also contributed to the publication of 3 books.

Laurent Guillot received the Graduate Engineer Degree in Electronics and Information Processing from ICPI Lyon in 1996 and a Master in microelectronics (Diplôme d'etudes Approfondies) from the University of Lyon in 1996.
He joined Dolphin Delegation, a microelectronic fabless company, in 1997 where he was primarily in the design of PLLs for Private Communication Terminals.
In 1999, he joined Freescale Semiconductor (formerly Motorola Semiconductor Products Sector) as Analog IC designer and developed ICs for Automotive Applications such as Airbags and Multiplexing. He is presently System and Application Engineer in charge of the Smart Power Switches family. He has co-authored 15 papers and holds 10 patents.

Bertrand Vrignon was born in Tours, France, in 1979. He received an engineering diploma from ESEO, Angers, France in 2002, and a Ph.D in Electronic Design from the National Institute of Applied Sciences, Toulouse, France, in 2005.
His doctoral research was in cooperation with STMicroelectronics, Crolles, France, where he characterized low electromagnetic emission guidelines for integrated circuits. In 2005, he joined Freescale Semiconductor, Toulouse, France, as research engineer on EMC at IC level. His current research interests include several aspects of design methodology to reduce emission, and improve noise susceptibility of deep-submicron ICs.