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Charge-based continuous model for long-channel Symmetric Double-Gate Junctionless Transistors

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ABSTRACT

A new charge-based continuous model for long-channel Symmetric Double-Gate Junctionless Transistors (SDGJLTM) is proposed and validated with simulations for doping concentrations of 5×10^{18} and 1×10^{19} cm^{-3}, as well as for layer thicknesses of 10, 15 and 20 nm. The model is physically-based, considering both the depletion and accumulation operating conditions. Most model parameters are related to physical magnitudes, and the extraction procedure for each of them is well established. The model provides an accurate description of the transistor behavior in all operating conditions. Among important advantages with respect to previous models are the inclusion of the effect of the series resistance and the fulfilment of the requirement of being symmetrical with respect to $V_d = 0$ V.

1. Introduction

Scaling of MOS transistor conduces to the reduction of the electrostatic control of the charges in the channel. For transistors with channel length in the order of tens of nanometers, with less technology requirements, the junctionless transistors (JLTs) with a constant doping concentration from source to drain and surrounded by the gate stack, represent a promising solution [1]. These transistors present performance similar to FinFETs with inversion channel, but with reduced short-channel effects, practically ideal subthreshold slope and high I_{on}/I_{off} ratio. The development of specific models to describe the behavior of these devices is an important task. Some work on physical, numerical and compact models can be found. For nanowire JLT, in [2], an interesting analysis of operation is done using numerical calculation and a piecewise model with a division in three regions: subthreshold, depletion and approximation in the accumulation. In [3], a model for the trigate JLT was proposed, but the expressions used are not continuous in the different operation regions. The solution was obtained separately in two operation regimes: bulk conduction and accumulation. Regarding Double-Gate JLT, among published work, a bulk current model was obtained using two expressions, one in the region of depletion and another in subthreshold [4]. Even with this approximation, the coincidence with simulated data is not good enough. Paper [5] presents another approximation for JLT model, where some non-physical elements, as equivalent thickness and the definition of threshold voltage are introduced. The numerical solution is obtained in two regions: depletion and accumulation. The agreement with simulation is only acceptable.

At present, much work is still needed to obtain higher precision and to cover a wider range of operating conditions in a continuous way, as well as to represent different possible device structures. In this work we propose a new charge-based model for Symmetric Double-Gate Junctionless Transistors (SDGJLTM). The model is based on physical parameters and is continuous in all operating regions; it also considers the series resistance. The expressions derived can be a basis to develop analytical solutions, including the variable mobility and short-channel effects.

Validation was made using ATLAS simulator with constant mobility μ_0, channel length and width of 1 μm, with channel doping concentration N_D of 5×10^{18} and 1×10^{19} cm^{-3} and different silicon layer thickness t_s of 10, 15 and 20 nm.

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2. Model description

2.1. Potentials and charges

The analyzed JLT structure is shown in Fig. 1. Charge density in the N-type silicon layer with doping concentration N_D, and electron mobile charge, is equal to:

$$\rho = qN_D\left(-e^{\frac{\varphi_S - V}{\varphi_t}} + 1\right) \tag{1}$$

where $\varphi_t = kT/q$ is the thermal potential at temperature T; φ_s is the surface potential and V is the potential drop across the silicon layer, from source $V_s = 0$ to drain V_d. In JLT majority carriers, electrons are present in the whole silicon layer that is considered the transistor channel.

Applying the Poisson to the silicon layer from the surface interface to the center of the Si layer of thickness equal to t_s, the surface electric field is equal to:

$$E_S = \varphi_t \frac{C_{ox}}{\varepsilon_s}\sqrt{\frac{q_b^2 C_S}{C_{ox}}}\,sign(\alpha)\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}} - e^{\frac{\varphi_0 - V}{\varphi_t}} - \left(\frac{\varphi_S - \varphi_0}{\varphi_t}\right)} \tag{2}$$

where ε_s – silicon dielectric constant; $C_s = \varepsilon_s/t_s$; $C_{ox} = \varepsilon_{ox}/t_{ox}$; ε_{ox} is the SiO_2 dielectric constant; t_{ox} is the equivalent dielectric thickness; φ_o is the potential at the center of the layer and q_b is the total fixed charge, Q_b, in the silicon layer, normalized to $C_{ox}\varphi_t$:

$$q_b = \frac{qN_D t_S}{C_{ox}\varphi_t} = \frac{Q_b}{C_{ox}\varphi_t} \tag{3}$$

The normalized difference of potential surface-center is defined as:

$$\alpha = \frac{\varphi_S - \varphi_0}{\varphi_t} \tag{4}$$

It is important to define the difference of potential at deep subthreshold regime, when full depletion is considered, leading to:

$$\alpha_{st} = -\frac{Q_b}{8C_s\varphi_t} = -\frac{q_b C_{ox}}{8C_s} \tag{5}$$

JLT can operate in depletion mode when the applied gate voltage, V_g, is lower than flat band voltage plus the applied drain voltage, $V_{fb} + V_d$, or in accumulation mode if $V_g > V_{fb} + V_d$. In depletion mode surface potential is lower that potential at center, that is, $\alpha < 0$, and the surface electric field is negative. In accumulation mode α and E_s are positive. For this reason the symbol of the sign is included in (2).

Considering that our model is for a symmetric double-gate device, the total charge in one half of the channel, calculated from the surface interface to the center, is equal to:

$$Q_{sem} = -sign(\alpha)C_{ox}\varphi_t\sqrt{\frac{q_b^2 C_s}{C_{ox}}}\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}}(1 - e^{-\alpha}) - \alpha} \tag{6}$$

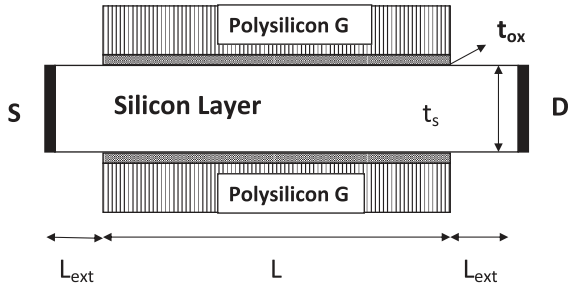

Fig. 1. JLT structure.

2.2. Difference of potential between surface and center

The surface potential as function of the potential at the center [5] can be calculated as:

$$\varphi_S = \varphi_0 + \frac{Q_b}{8C_s}\left(e^{\frac{\varphi_0 - V}{\varphi_t}} - 1\right) \tag{7}$$

After some mathematical manipulation the difference of potential can be calculated by the following expression:

$$\alpha = \alpha_{st} + LW\left[-\alpha_{st}e^{-\alpha_{st}}e^{\frac{\varphi_S - V}{\varphi_t}}\right] \tag{8}$$

where LW is the Lambert function.

From (5) and (7) the following relation is obtained:

$$e^{\frac{\varphi_0 - V}{\varphi_t}} + \alpha = -1 - \alpha\left(1 - \frac{1}{\alpha_{st}}\right) \tag{9}$$

Eq. (6) can be rewritten considering (9) and normalizing the charge in the semiconductor to $C_{ox}\varphi_t$. The following expression is obtained:

$$q_{sem} = -sign(\alpha)\sqrt{\frac{q_b^2 C_s}{C_{ox}}}\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}} - \left(1 - \frac{1}{\alpha_{st}}\right)\alpha - 1} \tag{10}$$

The normalized electron charge is equal to:

$$q_n = q_{sem} - \frac{q_b}{2} \tag{11}$$

Expressions (10) and (11) consider all the charges inside the silicon layer, from the surface to the center, meaning that both surface and bulk charges are included.

Considering (8) and (10), the electron charge is only function of the surface potential and drain voltage.

From the voltage drop across the MOS structure, the relation between the applied gate voltage and the surface potential is given by:

$$V_g - V_{fb} = \varphi_s + sign(\alpha)\,\varphi_t\sqrt{\frac{q_b^2 C_s}{C_{ox}}}\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}} - \left(1 - \frac{1}{\alpha_{st}}\right)\alpha - 1} \tag{12}$$

This transcendental equation can be solved only numerically.

2.3. Current calculation

Drain current is calculated including all electron charge inside the silicon layer using (11) by:

$$I_d = K\varphi_t\int_{V_s}^{V_d} q_n\,dV \tag{13}$$

where the current factor K, without the consideration of series resistance, is defined as,

$$K = 2\frac{W}{L}C_{ox}\mu_0 \tag{14}$$

2.4. Threshold voltage

A precise definition of threshold voltage, V_T, is necessary for each MOSFET model. For JLT, V_T has been defined in different ways, as for example, in [4] where it is obtained from the approximated I–V expression. In [5,6], V_T is calculated under the consideration of electron charge equal to zero. This consideration is not physically correct for a continuous model, because when $Q_n = 0$, the transistor is in deep depletion with practically no current through it, while at V_T, it is well known that the drain current is already important. In [7], the threshold voltage is extracted from the voltage at which

(g_m/I_d) is equal to one half of its maximum value. The extraction is done using measured or simulated characteristics. For DG transistors with inversion channel, the use of the physically based double derivative method for the extraction of threshold voltage provides very good results [8]. In this work, the same method will be used for DG JLT. The maximum of the second derivative of the current corresponds to the condition where the third derivative of the current is equal to zero. The same result is obtained if the third derivative of the surface potential is used.

From the analysis of different JLT structures and silicon layer doping concentrations, the behavior of the third derivative of the surface potential around V_T is always the same, showing a very abrupt transition around zero, as shown in Fig. 2. At the same time, the electron charge, q_n, begins to increase abruptly at gate voltage values close to $V_g = V_T + V_d$, see Fig. 3, where the value of electron charge becomes equal to value −0.25, see inset in Fig. 3. From this figure it is clear the physical meaning of the extracted value of V_T.

The behavior just described, was observed for all analyzed structures, for which the silicon thickness and doping concentration were varied, confirming that this condition can be used for the determination of V_T. From Eqs. (7), (11), and (12) the difference of potentials α at V_T and the extracted V_T are calculated, respectively, as:

$$\alpha_T = \frac{\alpha_{st}}{1-\alpha_{st}}\left[1-\alpha_{st}\left(1-\frac{1}{2q_b}\right)^2\right] \tag{15}$$

$$V_T = V_{fb} - \varphi_t\left[\frac{q_b}{2} - \frac{1}{4} - \alpha_T - \ln\left(1-\frac{\alpha_T}{\alpha_{st}}\right)\right] \tag{16}$$

As shown in Table 1, the threshold voltage values calculated from (16) and extracted from the second derivative method V_{Td} agree very well.

2.5. Series resistance

Extensions in source and drain are inherent to the JLT, with length indicated as L_{ext} in Fig. 1. These extensions introduce an important series resistance that had to be taken into account even for long channel transistors. Using the typical expression used in MOSFETs the series resistance R is considered in the factor, [9]:

$$F = KR\left(V_g - V_T - nV_d\right) \tag{17}$$

In order to avoid the unnecessary effect of this factor in the subthreshold regime, in this region, it is made equal to zero. In saturation, the effect of the saturation voltage is considered through an effective drain voltage, V_{deff}, as usual.

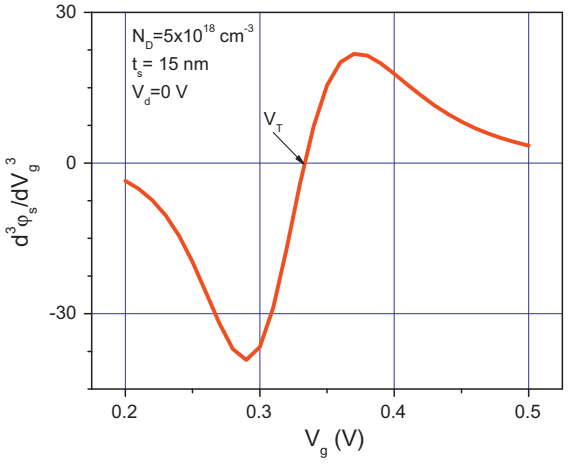

Fig. 2. Third derivative of surface potential around V_T.

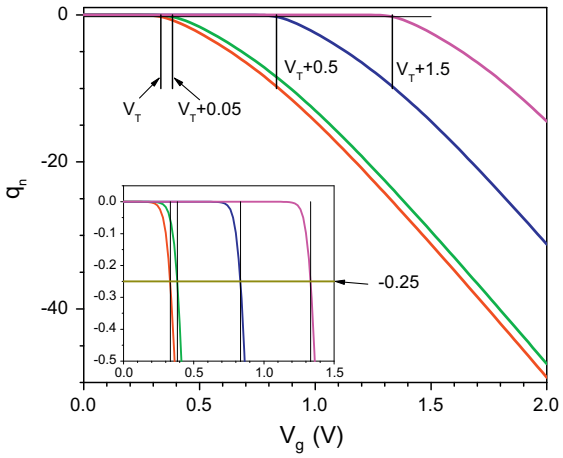

Fig. 3. Variation of the electron concentration with gate voltage for three values of drain voltage equal to 0.05, 0.5 and 1.5 V. The value of q_n reaches the level −0.25 at $V_g = V_T + V_d$, marked with a vertical line for each value of $V_T + V_d$. Inset figure shows a zoom around $q_n = -0.25$ for the three values of V_d.

Table 1
Extracted parameters for different transistors. V_T is calculated by (16) and V_{Td} is extracted from de second derivative method.

Parameter	Transistor				
	1	2	3	4	5
N_D (cm^{-3})	5e18	5e18	5e18	1e19	1e19
t_s (nm)	10	15	20	10	15
V_{fb} (V)	0.989	0.989	0.989	1	1
V_T (V)	0.589	0.333	0.033	0.244	−0.253
V_{Td} (V)	0.578	0.332	0.04	0.236	−0.252
R (Ω)	738	454	369	409	264
n	0.499	0.526	0.551	0.527	0.558

Taking the saturation voltage equal to $V_g - V_T$, as in long channel MOSFET, the effective drain voltage value, V_{deff}, is calculated by:

$$V_{deff} = V_{sat} + \frac{1}{2}\left[V_d - V_{sat} + \frac{\varphi_t}{3} - \sqrt{\left(V_d - V_{sat} + \frac{\varphi_t}{3}\right)^2 + 4V_{sat}\frac{\varphi_t}{3}}\right] \tag{18}$$

Eq. (17) can be rewritten as:

$$F = KR\left(V_g - V_T - nV_{deff}\right)\frac{1}{2}\left[1 + \tan h\left(V_g - V_T - nV_{deff}\right)\right] \tag{19}$$

After the inclusion of limits in subthreshold and in saturation, considering R and n as adjusting parameters, the drain current can be written as:

$$I_d = \frac{K\varphi_t}{1+F}\int_{V_s}^{V_d} q_n\, dV \tag{20}$$

In (18) and (20) the source voltage V_s is considered as an external source voltage equal to zero, and V_d is the external drain voltage.

3. Model validation

Validation of the proposed model was done using ATLAS simulations of N-type JLT structures with fixed channel length of $L = 1$ μm; channel width of $W = 1$ μm; P-type polysilicon doped to 10^{20} cm^{-3}; the charge at interface $N_{ss} = 5 \times 10^{10}$ cm^{-2}; EOT $t_{ox} = 2$ nm; mobility $\mu_0 = 100$ cm^2/Vs and extension length $L_{ext} = 50$ nm. Two magnitudes were varied in these structures: the silicon layer width and the doping concentration. All combinations of silicon layer widths of $t_s = 10$, 15 and 20 nm and doping

concentrations of 5×10^{18}, 1×10^{19} and 2×10^{19} cm^{-3} were analyzed. The simulated currents and device parameters are compared with those obtained from the model, using (20). Calculations were done in Mathcad.

After a detailed analysis, results for JLT with $N_D = 10^{19}$ cm^{-3} and $t_s = 20$ nm, as well as all corresponding to $N_D = 2 \times 10^{19}$ cm^{-3}, are not presented in this work since these JLT present high negative V_T and a normally-on operation condition. The other five JLT are analyzed and the extracted parameters corresponding to each case are shown in Table 1.

The extracted parameters are the threshold voltage, V_T, the series resistance, R and the adjusting parameter n. V_T is obtained from the analytical expression (16), R is extracted from the linear transfer characteristic at the maximum gate voltage and n was extracted from the saturation transfer characteristic at maximum gate voltage. It is important to remark that these three parameters are used for considering the series resistance effect. The polydepletion effect was calculated and considered by increasing the dielectric thickness in 0.1 nm.

Comparison of the simulated I–V characteristics and the modeled I–V characteristics calculated from (20) are shown in Figs. 4 and 5, corresponding to the linear and saturation transfer characteristics at $V_d = 50$ mV and 1.5 V respectively. An important shift in the characteristics and V_T, is observed, indicating that V_T reduces when the silicon layer concentration increases for the same silicon layer thickness. It also reduces when t_s increases for the same doping concentration. The subthreshold slope S, calculated from simulations and from the model is the same and equal to 61 mV/dec, which was the value to be expected. Fig. 6 shows the transconductance in the linear region where the complex variation of the current is clearly reproduced. Fig. 7 shows the transconductance in saturation. Fig. 8 shows the output characteristics for the five transistors at $V_g = 1.5$ V. As expected, an important increase of current in saturation is observed in these JLT when t_s increases or when the doping concentration increases, due to the contribution of the bulk conduction.

The good agreement between simulated and modeled conductance curves is shown in Fig. 9. The complex transition from different regions of operation in the transconductance and in the g_m/I_d characteristics are very well reproduced by the modeled curves, for which the derivatives of the current must be calculated, see Fig. 10.

An important feature for any model is the proof of model symmetry around $V_d = 0$ V, for both the current and the derivative of the current characteristics. In Fig. 11 it is seen that the proposed model meets very well this requirement.

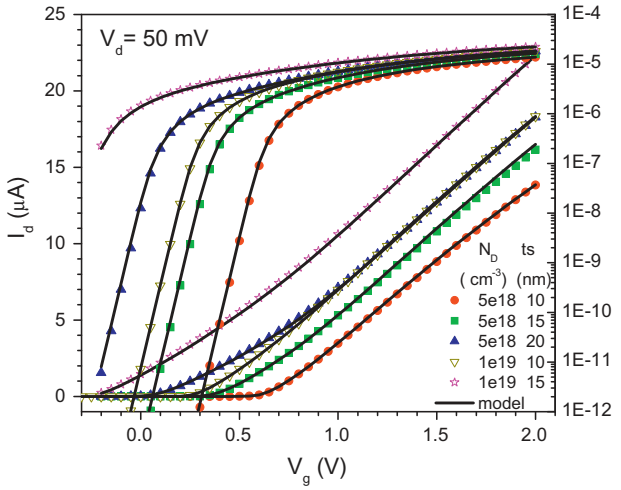

Fig. 4. Comparison of the simulated and modeled transfer characteristics at $V_d = 50$ mV.

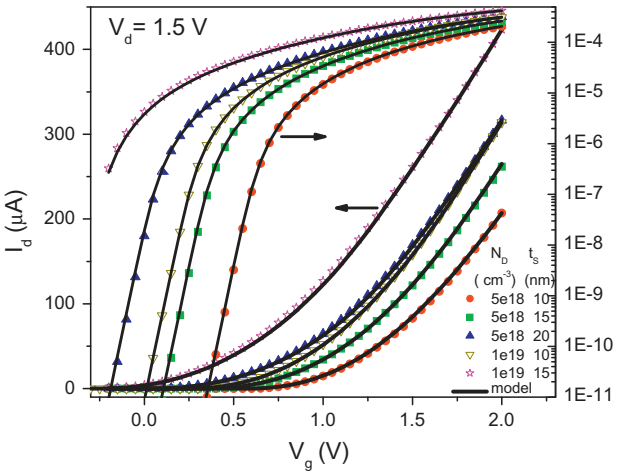

Fig. 5. Comparison of the simulated and modeled transfer characteristics at $V_d = 1.5$ V.

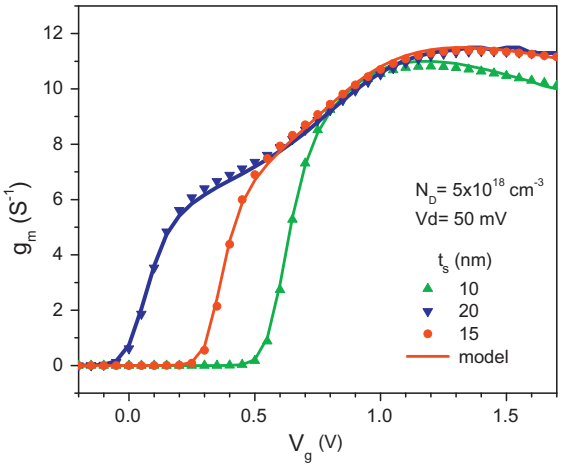

Fig. 6. Comparison of the simulated and modeled transconductance at $Vd = 50$ mV.

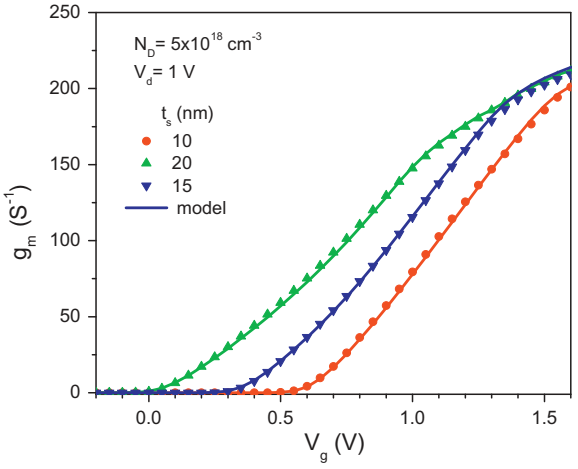

Fig. 7. Comparison of simulated and modeled transconductance at $V_d = 1$ V.

4. Conclusions

A new charge-based continuous model for long-channel Symmetric Double-Gate Junctionless Transistors (SDGJLTM) has been

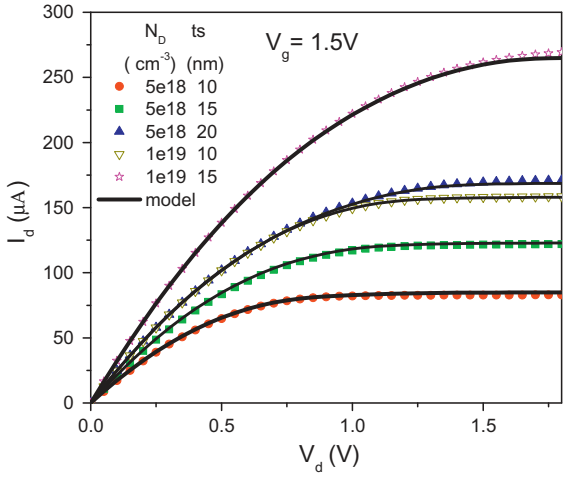

Fig. 8. Comparison of simulated and modeled output characteristics at V_g = 1.5 V.

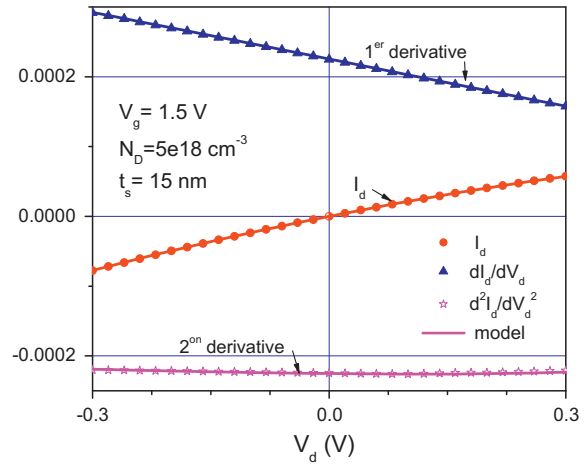

Fig. 11. Current continuity and symmetry around V_d = 0 V for the current, as well as its first and second derivative.

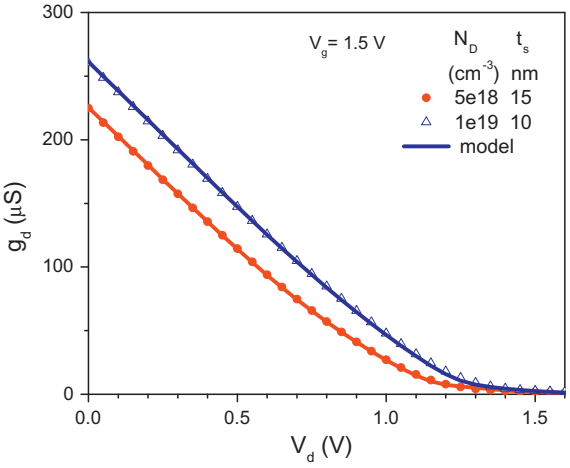

Fig. 9. Comparison of simulated and modeled output conductance at V_g = 1.5 V.

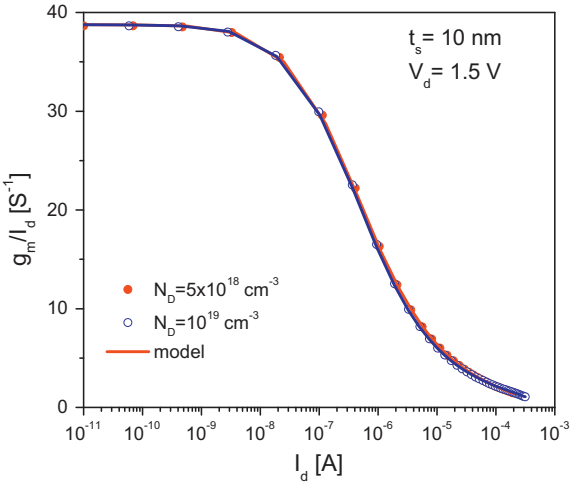

Fig. 10. Comparison of simulated and modeled g_m/I_d vs. log(I_{DS}) at V_d = 1.5 V.

proposed and validated with simulations for doping concentrations of 5×10^{18} and 1×10^{19} cm^{-3}, as well as for layer thickness of 10, 15 and 20 nm. It is shown that the model represents transfer, output, transconductance and conductance curves, as well as g_m/I_d characteristic with an excellent agreement with respect to the simulated curves in all operating conditions. The model is based on the device physics, considering both the depletion and accumulation operating conditions. Most model parameters are related to physical magnitudes, and the extraction procedure for each of them is well established. An analytical expression to calculate the threshold voltage developed by the second derivative method was obtained. Some of the main advantages with respect to previous models are the inclusion of the effect of the series resistance and the fulfilment of the requirement of being symmetrical with respect to V_d = 0 V.

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