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Charge Injection Transistor Based on Real-Space Hot-Electron Transfer

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***Abstract*—We describe a new transistor based on hot-electron transfer between two conducting layers separated by a potential barrier. The mechanism of its operation consists of controlling charge injection over the barrier by modulating the electron temperature in one of the layers. This physical principle is different from those employed in all previous three-terminal amplifying devices—which are based either on the modulation of a potential barrier (vacuum triode, bipolar transistor, various analog transistors) or on the modulation of charge in a resistive channel (field effect transistors). In contrast to this, the present device can be compared to a hypothetical vacuum diode whose cathode has an effective electron temperature which is controlled without inertia by an input electrode ("cathode heater").**

The device has been implemented in an AlGaAs/GaAs heterojunction structure. One of the conducting layers is realized as an FET channel, the other as a heavily doped GaAs substrate. The layers are separated by an $Al_xGa_{1-x}As$ graded barrier. Application of a source-to-drain field leads to a heating of channel electrons and charge injection into the substrate. The substrate thus serves as an anode and the FET channel represents a hot-electron cathode, whose effective temperature is controlled by the source-to-drain field.

Operation of the charge injection transistor is studied at 300, 77, and 4.2 K. At 77 K the existence of power gain is demonstrated experimentally with the measured value of the mutual conductance g_m reaching 280 mS/mm (at 300 K, $g_m \approx 88$ mS/mm). The fundamental limit on the device speed of operation is analyzed and shown to be determined by the time of flight of electrons across a high-field region of spatial extent ~10^{-5} cm. Practical ways of approaching this limit are discussed. The process of hot-electron injection from the channel is studied experimentally at 77 and 4.2 K with the purpose of measuring the electron temperature in the channel at different bias conditions. For not too high substrate bias the electron temperature in the channel is found to be proportional to the square of the heating voltage.

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I. Introduction

In a recent paper [1] we proposed several new device concepts based on hot-electron transfer between two conducting layers in a unipolar semiconductor structure. One of these layers is an FET channel. The other—independently contacted—layer is separated from the channel by a potential barrier. Application of a source-to-drain field causes heating of channel electrons and charge injection into the subsidiary layer. One of the consequences of this phenomenon is a strong negative differential resistance (NDR) in the drain circuit, experimentally studied in [2]. The NDR device received the name NERFET, which stands for **ne**gative **r**esistance **f**ield-**e**ffect **t**ransistor.

The present paper deals with another device based on the same physical process of charge injection of hot electrons—the **ch**arge **in**jection **t**ransistor or CHINT. The idea of CHINT is best illustrated by the analogy with a vacuum diode, Fig. 1. The device channel plays the role of a cathode, the second conducting layer that of an anode, and the source-to-drain field serves as a cathode heater. The height of the potential barrier corresponds to the cathode's work function. Like in the vacuum diode, the anode current, as a function of the anode voltage, must saturate at a level determined by the temperature and the barrier height. In contrast to the vacuum diode, however, the thermionic emission from the channel of CHINT is governed by the *temperature of electrons T_e* rather than that of the cathode material, which means that it can be modulated very rapidly by the source-to-drain field. The equilibration time for T_e—the energy relaxation time—is in the picosecond range [3].

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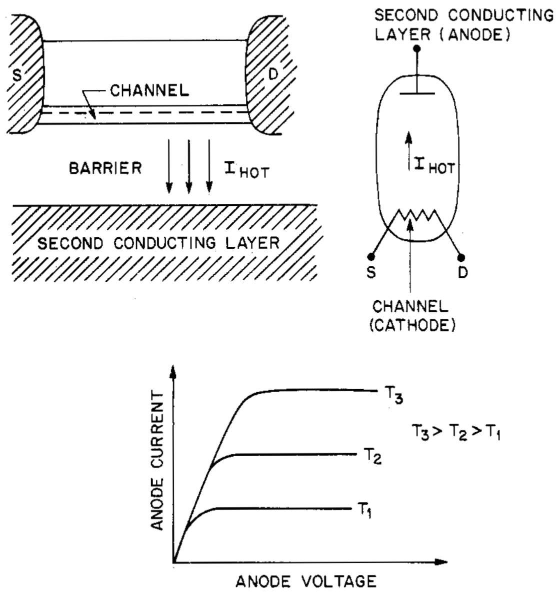


Fig. 1. Illustration of the CHINT principle. The channel serves as a cathode whose effective electron temperature is controlled by the source-to-drain field. The second conducting layer, separated by a potential barrier, serves as an anode and is biased positively. The anode current as a function of the anode voltage saturates at a value determined by the cathode temperature.

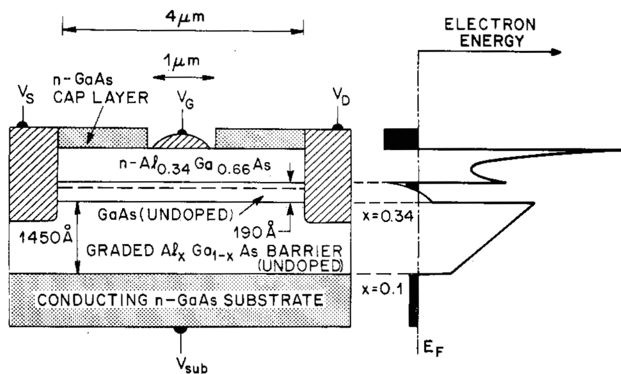
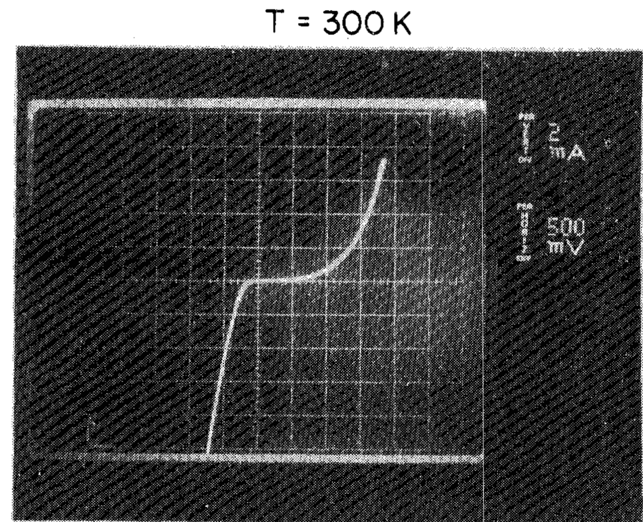


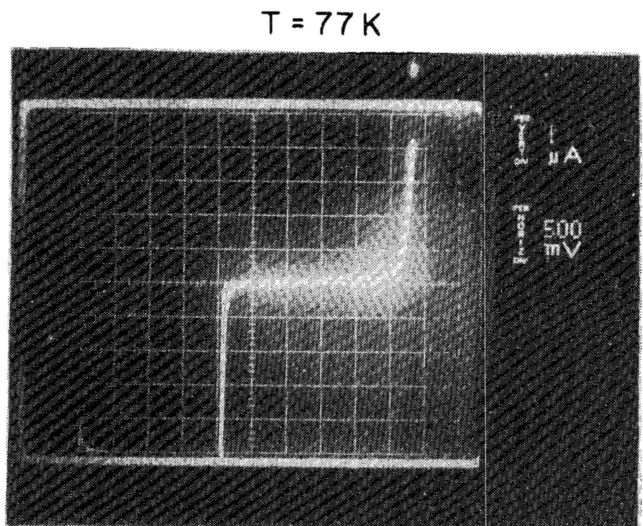
Fig. 2. Device structure and energy diagram. Regions, where the electron gas is degenerate are indicated in black on the band diagram.

Experimental realization of the CHINT concept was carried out with the same multilayered AlGaAs/GaAs heterostructure which was used previously [2] in our study of the NERFET. This structure and the device processing will be described in the next section (Section II). In Section III we present the observed device characteristics and discuss the fundamental limits for the speed of operation of CHINT. Physics of the hot-electron injection will be discussed in Section IV, where we present the results of our measurements at 77 and 4.2 K. Our conclusions will be summarized in Section V.

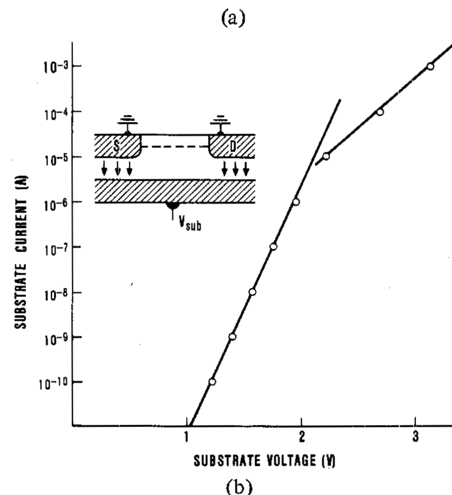
II. Device Structure and Processing

Fig. 2 shows the device structure and its band diagram. It has been grown by molecular-beam epitaxy (MBE) on Si-doped (10^{18} cm^{-3}) GaAs substrate, which plays the role of the second conducting layer. We used a {100} substrate orientation and a 640°C growth temperature with arsenic-rich growth conditions and conversion of the arsenic beam from As_4 to As_2. The growth sequence commenced with a 1-μm homoepitaxial layer of Si-doped (~10^{18} cm^{-3}) GaAs. The content of aluminum in the 1450-Å undoped $Al_xGa_{1-x}As$ barrier layer was graded from $x = 0.11$ to $x = 0.34$ by progressively increasing the aluminum molecular-beam cell temperature during growth of the layer. The upper GaAs conducting channel layer was undoped and 190 Å thick. The $Al_{0.34}Ga_{0.66}As$ layer which pro-





(a)



(b)

Fig. 3. Current–voltage characteristics in the substrate circuit. Source and drain are grounded; the total area of alloyed contacts is 3×10^{-5} cm^2. (a) Curve-tracer characteristics at 300 and 77 K. (b) Reverse-bias characteristic ($V_{SUB} > 0$) at 77 K.

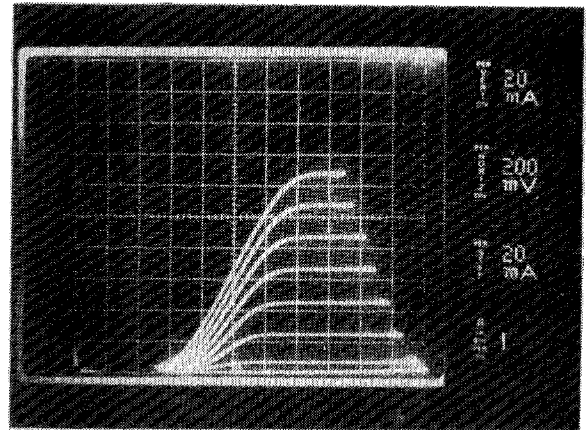
vided the conduction electrons to the channel contained $\sim 2 \times 10^{18}$ cm^{-3} silicon atoms, was 390 Å thick, and was separated from the channel by an 80-Å-thick undoped $Al_{0.34}Ga_{0.66}As$ spacer layer.

For device operation it is vitally important that source and drain contacts to the channel were insulated from the second conducting layer. The choice of a contact alloy is thus very important. Even though Ni based contacts show consistently lower contact resistance to GaAs/AlGaAs two-dimensional electron systems, they penetrate deeply into the semiconductor material—and were therefore rejected. We used Au/Ge-Ag-Au alloy which is known to give shallow (~2000 Å) and abrupt ohmic contacts. We sought to have the bottom edge of contact penetration stop near the top of the graded barrier. To this end we used a thick (1400-Å silicon-doped) GaAs cap layer (making the total thickness of the structure above the graded barrier about 2100 Å), and experimented with different alloying cycles and temperatures. Best results were obtained by alloying at 420°C for 20 s. Fig. 3(a) shows the resultant current-voltage (I_{SUB}-V_{SUB}) curves in the substrate circuit (source and drain grounded) at 300 and 77 K. These are typical rectifying characteristics of a one-sided triangular barrier of approximate height 0.4 eV [4]. The absence of any ohmic leakage down to $I_{SUB} \sim 10^{-10}$ A is demonstrated in Fig. 3(b) which shows a semilog plot of the reverse substrate characteristic at 77 K. Linear dependence of $\log I_{SUB}$ versus V_{SUB}, which persists over five orders of magnitude in current, corresponds to a diode ideality factor of about 13. This ideality factor is large enough that the barrier can be regarded as blocking for $V_{SUB} \lesssim 3$ V.

Devices were isolated from one another by selectively removing the conducting material between individual transistors and covering the resultant mesa pattern by silicon nitride. The Si_3N_4 layer was required in order to avoid electrical shorts between the off mesa bonding pads and the doped substrate. Active device area was cut into the nitride by a CF_4/O_2 plasma etch. Gates were deposited after a self-aligned chemical etch through the cap layer. The gate was notched into the AlGaAs layer enough to produce a slight channel depletion and ensure concentration of the source-to-drain field in the normally-on device. The gate (notch) length was 1 μm, while the total separation between source and drain was 4 μm; we used 250-μm-wide gates.

III. Charge Injection Transistor

As discussed in the Introduction, the physical mechanism of CHINT is analogous to that in a vacuum diode with an effective cathode temperature controlled by the source-to-drain electric field. Electrically, however, its operation is similar to that of a bipolar transistor with *source* $\equiv$ *emitter*, *drain* $\equiv$ *base*, and the second conducting layer (*substrate*) $\equiv$ *collector*. In what follows, speaking of the terminals in CHINT we shall be using the bipolar and FET nomenclatures interchangeably with the above correspondence. As we shall see now, most of electrons leaving the source are collected in the second conducting layer, because of the efficient hot-electron injection and the strong NDR in the drain circuit.



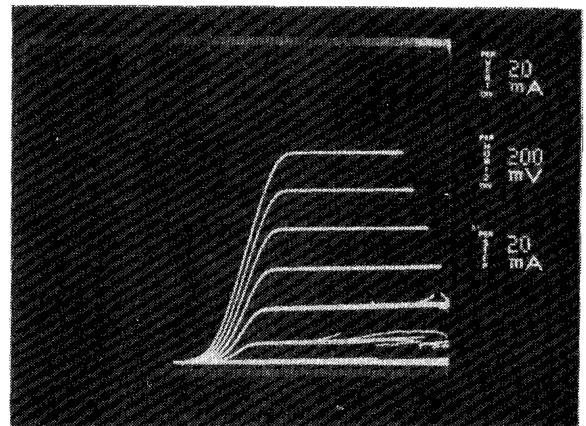


Fig. 4. Collector (substrate) characteristics in the common base (drain) configuration at 300 and 77 K with the emitter current as a parameter. Note that steps in the emitter current result in larger steps in the saturated collector current, which means $\alpha > 1$.

Fig. 4 shows the typical collector characteristics of CHINT in the common base (drain) configuration. These characteristics are seen to resemble those of a bipolar transistor. If we define α_0 as the ratio of the collector and the emitter currents, $\alpha_0 = I_c/I_e$, we find $\alpha_0 \gtrsim 0.9$. On the other hand, there is a range of currents where the differential $\alpha \equiv \partial I_c/\partial I_e$ is greater than unity. This effect, which can be seen both at 300 K where $\alpha \approx 1.1$ and at 77 K ($\alpha \approx 1.3$), is a peculiar feature of our device which has a negative differential resistance in the emitter-base circuit. Indeed, the emitter, collector, and base currents in CHINT are related by the Kirchhoff law $I_e = I_c + I_b$. Fig. 5 shows a simultaneous plot of the base and collector current characteristics as functions of the source-to-drain voltage. We note that rise in the collector current is accompanied by a drop in the base (drain) current, so that the total emitter current varies little in the NDR region. Thus the presence of a strong NDR in the emitter-base circuit implies the possibility

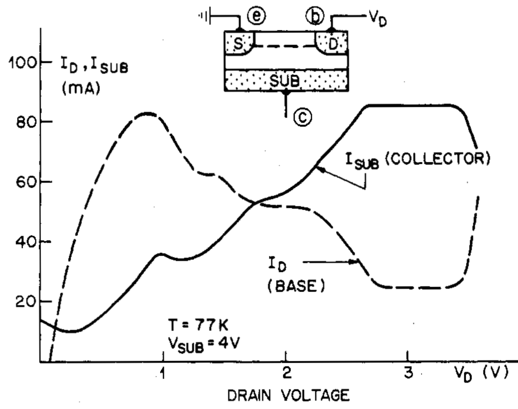


Fig. 5. Simultaneous plots of the base (I_D) and collector (I_{SUB}) currents at a fixed collector voltage: $V_{SUB} = 4$ V; $T = 77$ K; $V_G = 0$.

of obtaining $\alpha \gg 1$. It is interesting to note that the early bipolar transistors also had an alpha greater than unity, cf., [5, p. 110]. At the same time their static emitter-base characteristics exhibited an NDR. This effect resulted from parasitic positive feedback mechanisms (e.g., the so-called p-n hook effect) and was not an intrinsic property of the ideal transistor. In CHINT, on the other hand, both the NDR and the $\alpha > 1$ effect are inherent properties of the device. They are highly reproducible and do not impede the speed of operation.

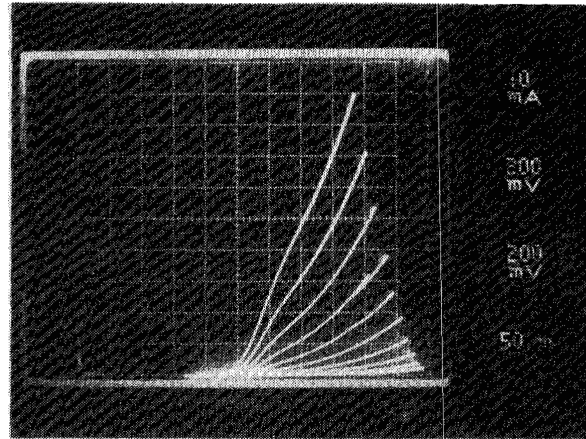
Fig. 6 shows the dependence of collector characteristics I_c versus V_c with the heating voltage V_{SD} as a parameter. These curves exhibit no saturation because of the parasitic effect of a direct injection of electrons from the source contact into the second conducting layer. In order to obtain the true characteristics of CHINT, determined entirely by the hot-electron injection, we must subtract the parasitic leakage. This is done in Fig. 7, where we plot the substrate current versus source-drain voltage at different substrate biases. Dashed lines indicate the source–substrate leakage measured with the drain floating. We see that although the hot-electron current dominates, the parasitic component is not negligible. The net curves representing the hot-electron injection into the second conducting layer as a function of the applied voltages in the common-base configuration at 77 K are shown in Fig. 8 (collector current as a function of (a) collector voltage and (b) emitter voltage). These characteristics permit us to determine the intrinsic transconductance, $g_m = (\partial I_c/\partial V_e)|_{V_c}$, and the collector impedance, $r_c = (\partial V_c/\partial I_c)|_{V_c}$, in a chosen bias range. It should be realized that the dependences $I_c(V_e, V_c)$ in CHINT are more complicated than the analogous characteristics in a bipolar transistor, mainly because of the strong influence of the collector voltage on the physical process of electron heating. This point will be further discussed in Section IV.

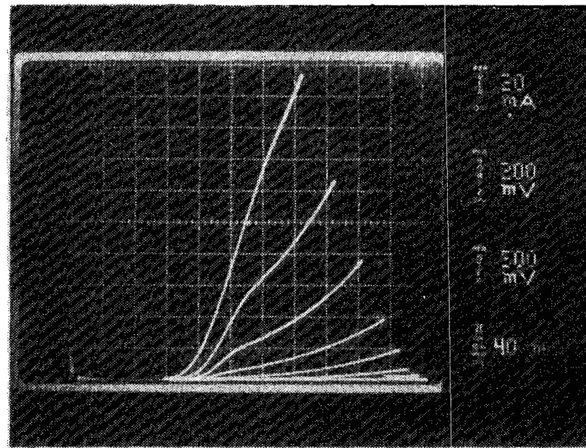
The maximum available power gain G (see, for example, [5, pp. 37-50]) can be approximately expressed in the form

$$G = \alpha r_c g_m/4. \tag{1}$$

Taking $\alpha = 1.3$ (from Fig. 4), and $r_c = 36\ \Omega \cdot$ mm, and g_m = 240 mS/mm (from Fig. 8(a) and (b), respectively, at $V_e = 2.5$ V and $V_c = 2$ V), we find $G \approx 2.8$ in the chosen bias regime. The highest transconductance observed at 77 K was about 280

300 K





77 K

Fig. 6. Collector (substrate) characteristics in the common base (drain) configuration at 300 and 77 K with the emitter–base voltages as a parameter.

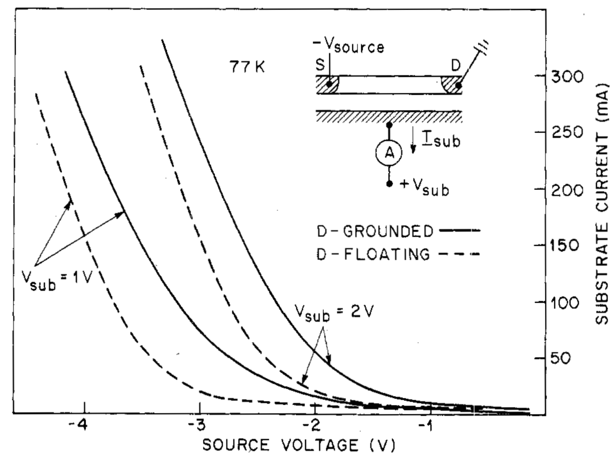


Fig. 7. Subtraction of the parasitic source–substrate leakage. Substrate is kept at a fixed positive voltage with negative voltage applied to the source; the drain terminal is either grounded (solid lines) or left floating (dashed lines). Difference between these curves represents the net hot-electron injection characteristics.

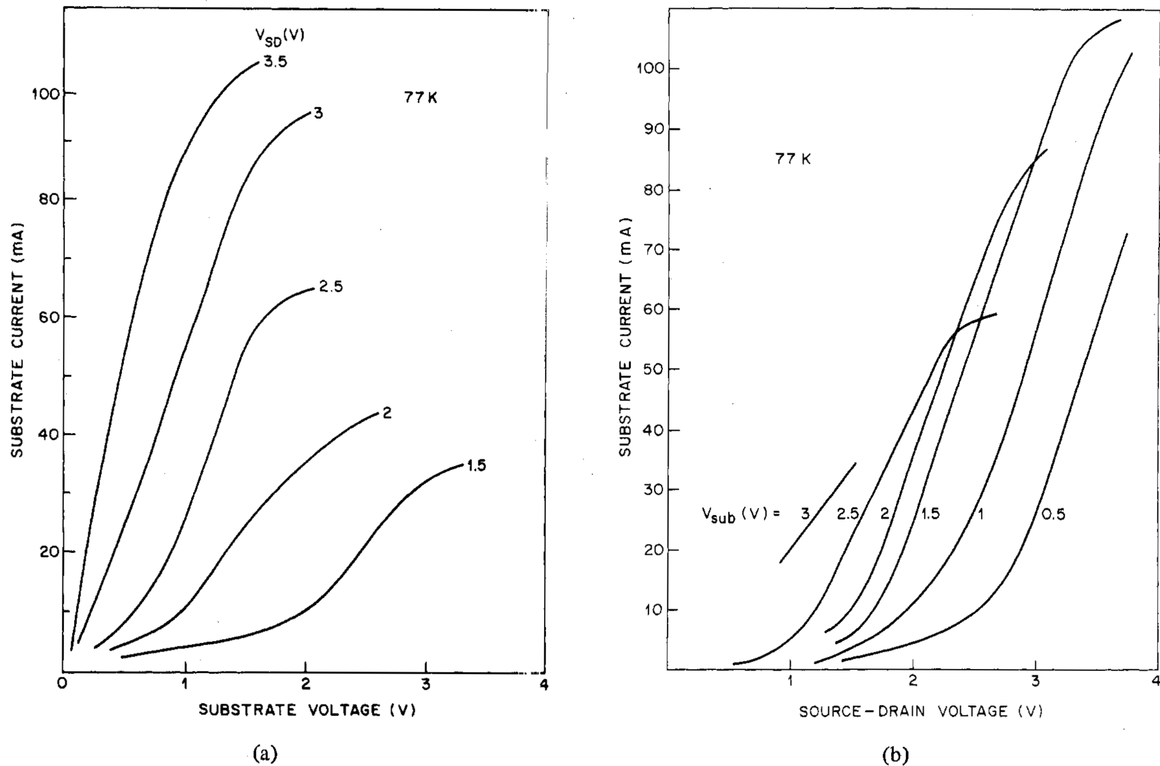


Fig. 8. The net transistor curves at 77 K, derived from the data of Fig. 7. (a) Collector current versus collector voltage in the common-base configuration with the emitter voltage as a parameter. (b) Collector current versus emitter voltage V_{SD} with the collector voltage as a parameter. The slope of these characteristics is the transconductance g_m.

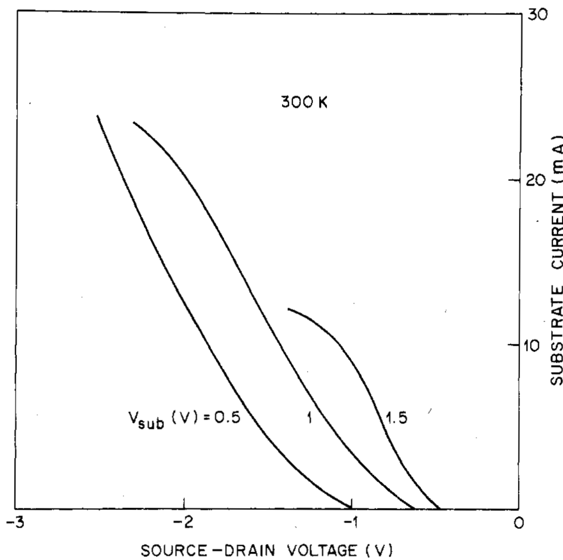


Fig. 9. The net injection characteristics at 300 K.

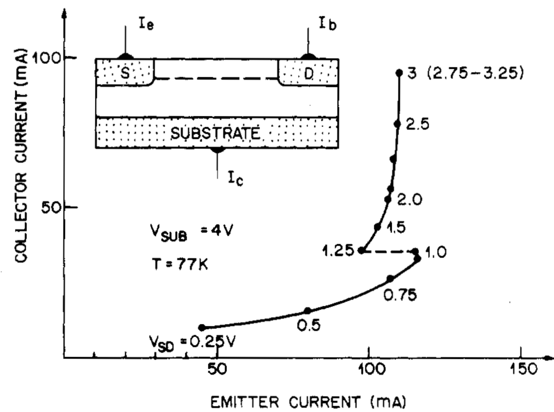


Fig. 10. Collector current versus emitter current at a fixed collector voltage V_{SUB} = 4 V. The curve is derived from the parametric dependences $I_D(V_{SD})$ and $I_{SUB}(V_{SD})$ in Fig. 5 by eliminating V_{SD}.

mS/mm. Similar analysis at room temperature (see the net curves in Fig. 9) gave the highest g_m = 88 mS/mm at a gain $G \approx 0.5$. It should be noted, however, that we have underestimated the current gain α. The values of α used in our estimates at both temperatures were taken from the curve-tracer characteristics in Fig. 4 containing the parasitic emitter-collector leakage discussed above. True values of α unmasked by the parasitic effect should be much higher.

Indeed, consider the dependence of the collector current on the emitter current at a fixed collector voltage V_{SUB}. This characteristic, which can be easily obtained from the curves in Fig. 5, is shown in Fig. 10 (for 77 K). We see a multivalued "S-shape" curve, which results from the existence of an NDR in the corresponding range of voltages, $V_{SD} \sim (1 \div 3)$ V and V_{SUB} = 4 V. Note that in a rather large interval of heating voltages, $V_{SD} \gtrsim 1.25$ V, the net values of α can be extremely high.

To improve the performance of CHINT it is, of course, imperative to reduce the parasitic leakage. This can be done in

two ways: one is to shrink the contact pads, so as to reduce the area of the parasitic injection, and the other—to shorten the gate length, which would allow us to obtain the same heating fields by applying a lower voltage. As will be discussed next, both of these improvements are also important for the *frequency* performance of the device—in order to achieve its ultimate speed.

Like in any other transistor, the gate delay τ in CHINT is determined by the time of charging its input capacitance by the output current, $\tau = C/g_m$. The total capacitance C can be split into two terms $C = C_g + C_m$, where C_g is the geometric capacitance between electrodes (including stray fields) and C_m is the capacitance associated with the moving injected charge. For this separation it is essential that C_g is independent of the current, while C_m is proportional to the space-charge limited current in the device. Analysis of the space-charge capacitance C_m shows that the ratio C_m/g_m is independent of the injected current [6]. Quite generally, the delay associated with C_m reduces to the time of flight of the injected carriers over high-field regions of the device—where the current is space-charge limited. In the CHINT these regions are: i) the high-field domain in the channel [2], and ii) the downhill slope of the graded barrier. Both times of flight are of the order of a picosecond and represent the fundamental limitation on the device speed. (Another speed limitation, mentioned in the Introduction, is due to the energy relaxation time.)

It should be emphasized that our time-of-flight limitation is different from the time-of-flight-under-the-gate delay, characteristic of an FET. The latter result from charging the channel by the gate voltage through the output resistance of the previous (identical) stage—which necessarily gives $\tau = L/v$ with L being the gate length. In the CHINT the controlling electrode is the drain and L is the total length of space-charge-limited-current regions, which can be considerably shorter than the gate length.

The fixed capacitance C_g is determined by the contact geometry and the associated delay time decreases with increasing g_m. In our device the main contribution to C_g results from the capacitance between the controlling electrode (either source or drain) and the second conducting layer (substrate). This capacitance equals 2 pF (i.e., 8 pF/mm) which approximately corresponds to the designed contact area 10 μm $\times$ 250 μm and the capacitor thickness 1500 Å. For g_m = 240 mS/mm (at 77 K) the resultant delay is ~30 ps, i.e., it is an order of magnitude higher than the fundamental limit. In order to approach this limit we should shrink the contact pad length to about 1 μm. Another way of approaching the fundamental limit is by increasing the g_m—which is essentially controlled by the efficiency of electron heating. In the next section we shall describe some of our experiments aimed at understanding the physics of hot-electron injection in the CHINT structure.

IV. Hot-Electron Injection at 77 and 4.2 K

In the present section we describe an experiment which we carried out in order to 1) verify unambiguously the hot-electron nature of charge injection in our structure, and 2) obtain information on the dependence of the electron heating

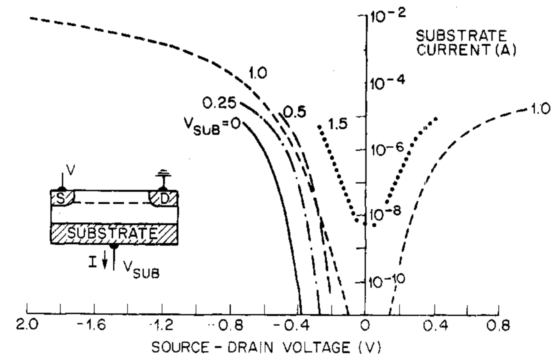


Fig. 11. Hot-electron injection at 77 K.

on the applied voltages. To this end we measured the current collected in the second conducting layer (substrate) at different substrate biases $V_{SUB} \geq 0$ and varying source-drain voltages V_{SD}.

Fig. 11 shows on a semilog plot the charge injection curves at 77 K. One of the surface electrodes, labeled D ("drain") was grounded. Voltage V_{SD} of both polarities was applied to the other electrode S. Consider the curve corresponding to V_{SUB} = 1.0 (dashed line). We see that the substrate current I_{SUB} exhibits a sharp minimum when $V_{SD} \to 0$. For $|V_{SD}| \geq$ 0.15 V the current rises by more than eight orders of magnitude. The fact that the current polarity is the same for *both* polarities of V_{SD} and corresponds to electrons injected into the substrate, is a direct evidence of its hot-electron nature. Similar results were obtained with V_{SUB} = 1.5 V (dotted line) and V_{SUB} = 2 V (not shown).

At low substrate biases ($V_{SUB} < 0.5$ V) the hot-electron injection is observed only when $V_{SD} < 0$. At positive V_{SD} this effect is masked by a "cold" electron current of opposite polarity thermionically emitted from the substrate. In this case the thermionic emission in the forward-biased triangular barrier diode (substrate–S) occurs before the onset of an efficient hot-electron injection. We had actually observed the competition between these two currents (on the level of ~10^{-10} A, not shown) at $V_{SD} > 0$ and V_{SUB} = 0.5 V. We shall return to this effect again in connection with our data at liquid helium temperatures.

As seen from Fig. 11, an increase in V_{SUB} shifts the threshold for hot-electron injection toward lower $|V_{SD}|$. When $V_{SUB} \geq 1$ V, the heating efficiency drops markedly. In what follows, we shall make an attempt to extract from our data some information about the electron temperature T_e and its dependence on the heating voltage V_{SD}.

This analysis employs a simple thermionic formula for the hot-electron current over a potential barrier of height ψ

$$I_{SUB} = I_0 e^{-e\psi/kT_e}. \tag{2}$$

We neglect a weak ($\sim\sqrt{T_e}$) dependence of I_0 on the source-drain voltage [1], [2] and assume that $\psi = \psi(V_{SUB})$ is independent of V_{SD}. The dependence $T_e(V_{SD})$ will be assumed to be of the form

$$T_e = T(1 + \gamma V_{SD}^m). \tag{3}$$

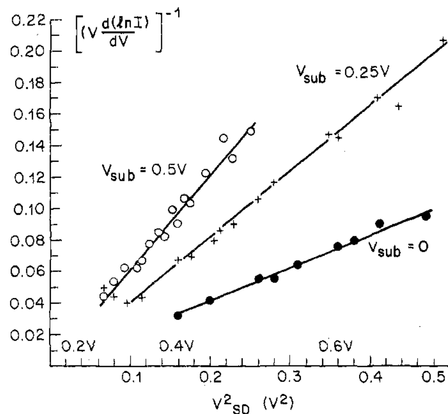


Fig. 12. Function f defined by (4) versus the square of the heating voltage V_{SD}^2 for three different substrate biases $V_{SUB} \leqslant 0.5$ V.

Under these assumptions one has

$$f \equiv \left(V_{SD} \frac{d \ln I_{SUB}}{dV_{SD}}\right)^{-1} = \frac{kT_e}{m\psi} \frac{T_e}{T_e - T}. \tag{4}$$

In most of our low-temperature experiments, a detectable hot-electron current I_{SUB} was observed only when the source-drain field exceeded ~1000 V/cm in which case one can expect $T_e \gg T$ and hence $f \approx kT_e/m\psi$. This allows us to determine the functional dependence of the electron temperature on V_{SD}. Fig. 12 plots f versus V_{SD}^2 for three different values of V_{SUB}. The obtained linear dependences suggest that we have $m = 2$. If the value of $\psi(V_{SUB})$ is known, then the plots in Fig. 12 directly give T_e. We note a strong dependence of the function $f = kT_e/2\psi$ on V_{SUB}: the slope df/dV_{SD}^2 increases by almost a factor of 3 when V_{SUB} is changed from 0 to 0.5 V. Such a dramatic dependence can hardly be attributed to a decreased barrier height ψ—even assuming a "thermally" assisted tunneling mechanism (tunneling of hot electrons under the barrier). The observed effect must therefore be related to changed conditions for electron heating, i.e., $\gamma = \gamma(V_{SUB})$. Our data suggest that in the range $0 < V_{SUB} < 0.5$ V γ increases. However, this is no longer true when $V_{SUB} \gtrsim 1$ V. It is already seen from Fig. 11 that at $V_{SUB} = 1$ V and $V_{SUB} = 1.5$ V the electron heating is less efficient. In these cases our analysis similar to that in Fig. 12 did not reveal any consistent value of m. Fig. 13 shows f versus V_{SD} at $V_{SUB} = 1$ V. The observed minimum is consistent with (4), which gives $f_{min} = 4kT/m\psi$ at $T_e = 2T$. Thus interpreting the data and taking $m = 1$, we find $\psi(V_{SUB} = 1 \text{ V}) \approx 0.3$ eV, which shows again that most of the substrate-bias dependence is due to changed conditions for electron heating rather than to barrier-height lowering. Application of V_{SUB} can affect the electron temperature in several ways.

In our view, the possible mechanisms are:

1) Gate action. Higher V_{SUB} leads to higher electron concentration and enhanced mobility. On the other hand, V_{SUB} may affect the length of the high-field domain in the channel [2]. Increasing V_{SUB} may lead to a disappearance of the pinch-off region and a rapid drop in T_e.

2) Charge redistribution in the potential well. At higher V_{SUB} electrons begin to accumulate near the opposite wall confining the channel (at the graded barrier). This hetero-

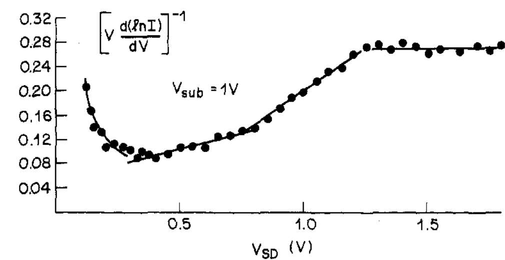


Fig. 13. Function f defined by (4) versus the heating voltage V_{SD} for $V_{SUB} = 1.0$ V.

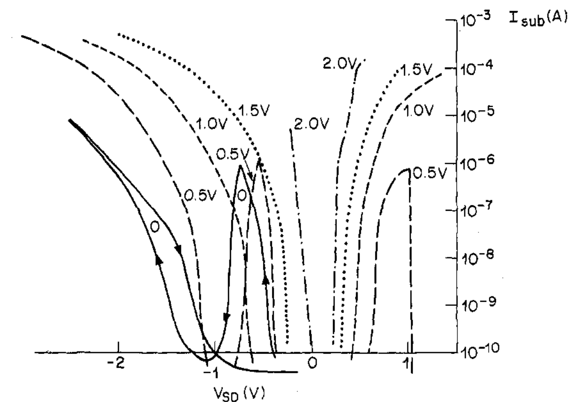


Fig. 14. Hot-electron injection at 4.2 K.

junction is known to have a high trap concentration and give lower electron mobility.

3) Momentum-space charge transfer in the channel. At high T_e electrons begin to occupy the subsidiary minima in the GaAs conduction band, which may adversely affect the efficiency of electron heating (see, e.g., [3]). This effect should be sensitive to the relation between the barrier height ψ and the energy separation between the Γ and the subsidiary minima. It should be interesting to implement CHINT with InGaAs/InAlAs heterostructures. In this material one can expect a higher heating efficiency because the subsidiary minimum in InGaAs lies substantially above the barrier height for real-space transfer [7]. (Another advantage of this material is, of course, the lower electron effective mass.)

On the basis of our present knowledge, we are unable to distinguish between these and possibly other mechanisms. The electron heating in the channel is a complicated physical process which obviously requires further study. The complex nature of the real-space hot-electron injection is dramatically illustrated by our results at 4.2 K, shown in Fig. 14. The charge injection curves shown in this figure are analogous to those obtained at 77 K (Fig. 11). The new features should be noted, however.

Firstly, the curve corresponding to $V_{SUB} = 0.5$ V exhibits a sharp drop at $V_{SD} \approx +1$ V, and at higher V_{SD} the current changes polarity. This is an evidence of the above-mentioned competition between the positive hot-electron current and the negative current corresponding to the substrate-to-drain thermionic injection.

An entirely novel feature is seen at $V_{SD} < 0$ and $V_{SUB} \leqslant 0.5$ V. A sharp rise in the hot-electron current is followed by its abrupt drop over almost five orders of magnitude. Further

increase in the negative V_{SD} leads to another rise in the hot-electron current. This fine structure in the I_{SUB}-V_{SD} characteristic is hysteretic, i.e., it is not seen on the way back—when $|V_{SD}|$ is reduced. It is restored only after the application of a sufficiently large positive V_{SD}. No fine structure is observed at higher V_{SUB}.

V. Discussion

We have described the principle and the operation of a new transistor based on hot-electron injection. Quite generally, by the physical principle involved, *all* previous *transistors* could be classified in one of the *two groups*: potential-effect and field-effect devices. The first group contains the bipolar transistor and all *analog* devices [8], such as the static induction transistor [9], the permeable base transistor [10], and the thermionic emission transistor [11]. In these devices the transistor action results from modulating the height of a potential barrier by a controlling electrode. The second group, containing a great variety of FET's [12], employs the field effect, i.e., the *screening* of the gate electric field by an accumulation or depletion of the mobile charge in the channel.

Neither of these mechanisms is essential for the operation of CHINT, where control of the output current is effected by a modulation of the electron temperature in the channel, resulting in charge injection over a potential barrier of fixed height. Electrically, CHINT is similar to the bipolar transistor, although the device is entirely unipolar. An essential feature of CHINT is the fact that its common-base current gain α exceeds unity. This feature, which is intimately related to the negative differential resistance in the source-drain (emitter-base) circuit, is an intrinsic property of the device structure and it does not impede its speed of operation. As discussed in Section III, the intrinsic speed of the CHINT is limited by the time of flight of electrons over high-field regions of the device (distances of order 10^{-5} cm).

The transistor performance of CHINT is governed by the efficiency of the electron heating and the subsequent charge injection over the barrier into the second conducting layer. Physics of this process is quite involved and its study has only begun. In Section IV we obtained (within the framework of a simple model for electron heating) the dependence of electron temperature on the applied voltages. On the basis of this rather preliminary investigation we were able to suggest two main directions for device improvement. One is to reduce the gate length and thus obtain higher heating fields at the same source-to-drain voltage. Also, shrinking the contact pads should reduce the parasitic emitter-to-collector leakage, discussed in Section III and permit us to approach the fundamental transit-time limit on the device speed. The other direction is to use different materials. The InGaAs/InAlAs heterojunction structure appears to be a promising candidate because of the lower effective mass of electrons in InGaAs and the higher energy separation of the satellite valleys.

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