CHARGE PUMPING IN SILICON ON INSULATOR STRUCTURES USING GATED P-I-N DIODES

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Résumé - Nous présentons une extension de la technique de pompage de charge sur des diodes P^+IN^+ à grille de contrôle, fabriquées sur silicium sur isolant. Cette méthode nous permet d'accéder aux propriétés des interfaces des structures SOS et SIMOX, tout en évitant l'utilisation de transistors MOS à 5 contacts. Les mesures effectuées sur SIMOX en pulsant la grille et/ou le substrat révèlent l'existence d'une forte densité d'états d'interface rapides et de pièges volumiques au voisinage de l'oxyde enterré.

Abstract - The extension of the charge pumping technique to gated P^+IN^+ diodes fabricated on silicon on insulator is analysed. This method allows us to evaluate the interface properties in SOS and SIMOX structures, without the need for 5-terminal MOS transistors. The experiment, performed on SIMOX films by pulsing both the gate and substrate, reveal the existence of a high density of fast interface states and bulk traps near the buried oxide.

1 - INTRODUCTION

The great interest in Silicon On Insulator (SOI) structures has generated an effort in the research of appropriate and reliable interface characterization techniques. Indeed, conventional MOS capacitance measurements suffer from the inherent existence of high series resistances and interface coupling in very thin films /1/. Current based techniques (dynamic transconductance /2/, low frequency noise /3/) are much more suitable for SOI.

It has been recently demonstrated that the charge pumping can be successfully applied to short-channel MOSFET's fabricated in SOI /4,5/. This technique is able to resolve the contributions of front and back interfaces while avoiding the influence of parasitic capacitances and series resistances. A major practical limitation is, however, due to the necessity of a film contact to measure the charge pumping current ; this requires the fabrication of special 5-terminal MOSFET's. In this paper we make use of the presence of the charge pumping phenomenon in standard gate-controlled diodes /6/ in order to demonstrate that charge pumping measurements can be used to characterize not only the two interfaces but also the bulk traps in SOI films.

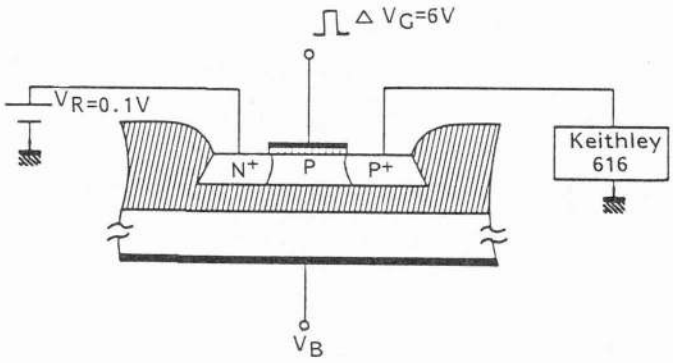

Fig.1. Experimental set-up of charge pumping technique

2 - EXPERIMENT

The schematic set-up of the experiment is shown in Fig. 1. The P^+PN^+ diode is reverse biased while the gate is continuously pulsed from strong inversion to accumulation. In strong inversion, minority carriers are rapidly supplied by the N^+ contact to form the inversion layer and fill the interface traps. As the device is pulsed into accumulation, the inversion layer electrons return almost instantaneously to the N^+ contact whereas trapped electrons recombine with majority carriers supplied by the P^+ contact.

This recombination and the underlying net flow of holes give rise to a charge pumping current I_{cp} in the film which is proportional to both the pulse frequency (Fig. 2) and the amount of interface traps /4-6/. It follows that the P^+ contact plays here the role of the film contact in the 5-terminal MOSFET. The method was validated by comparison with conventional charge pumping in 5-terminal MOSFET's and dynamic transconductance measurements.

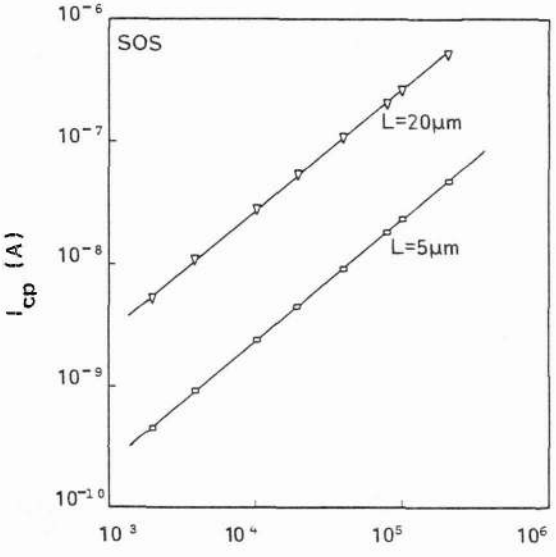

Fig.2. Charge pumping current versus frequency for SOS diodes

The influence of gate length, reverse bias and substrate bias are also investigated. A further development consists of taking into consideration the contributions of two emission processes. Firstly, some of the interface states can be directly filled by the emission of holes to the valence band. Secondly, a portion of the trapped minority carriers are emitted from the interface states in the silicon conduction band instead of recombining with substrate majority carriers. The model shows that by changing the 4 parameters of the gate pulse (top and bottom levels, rise and fall times) it becomes possible to determine the energy profile of interface states /7/.

The experiment was carried out in silicon on sapphire (SOS) films 0.5 µm thick and in SIMOX structures formed by deep oxygen implantation (200 keV, 1.7×10^{18} O/cm^2) and high temperature annealing. The thicknesses of the Si film and buried oxide were about 0.2 µm and 0.4 µm, respectively. The silicon overlayer forming the diode base was either P-type doped or natural with an unintentional residual doping of about 10^{15} cm^{-3} still subsisting as a consequence of the annealing process and oxygen activity.

3 - DISCUSSION

Figure 2 shows the variation of I_{cp} with the pulse frequency for two SOS diodes of different lengths (L = 5 µm, L = 20 µm). The linear behaviour of I_{cp} with the frequency is in agreement with the theoretical predictions [7], however the ratio between the two currents is greater than that between the two gate areas. This is attributed to a geometric component present in the longer device. Indeed, some of the inversion electrons may recombine with holes supplied by the P^+ contact and contribute to the total measured current (Fig. 3 for L = 20 µm). This effect is observed for transistors with relatively long channels : L ≥ 20 µm. Bearing in mind that the inversion layer formation delay in a P-I-N diode is twice as large as in a transistor, one should expect the geometric component to exist in diodes of gate lengths of the order of 10 µm.

Figure 3 shows I_{cp} versus the pulse base level for the two diodes. For L = 20 µm, I_{cp} does not go to zero when the whole pulse lies in strong inversion ; according to Elliot /8/, this confirms the presence of a geometric component. In contrast, for the shorter diode, I_{cp} decays rapidly as the pulse excursion is shifted towards accumulation or strong inversion.

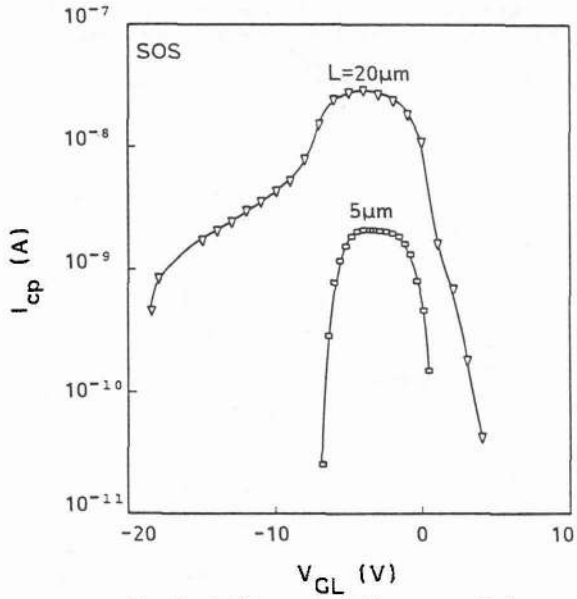

Fig.3. Influence of the geometric component on the charge pumping current measured as a function of the gate pulse base level

More information about bulk traps is obtained by pulsing simultaneously both gates. According to the new principle of *volume inversion* /8/, not only the two interfaces but also the whole film volume are now driven from accumulation into strong inversion. In our case (Fig. 4), the total value of I_{cp} is almost the same as that of the back interface. This implies that bulk traps are localized mainly near the buried oxide.

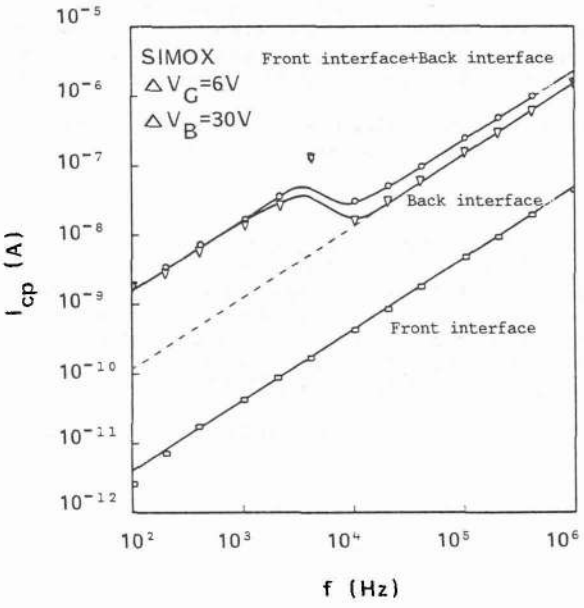

Fig.4. Charge pumping current versus frequency

Furthermore, Fig. 5 shows a maximum in I_{cp} at the front interface as the substrate voltage is varied. The behaviour of this curve can be explained by the fact that when the back interface is in strong inversion or in accumulation, the influence of the front gate bias on the back interface potential is negligible. On the other hand, when the back gate is biased in depletion or weak inversion a larger portion of the energy gap can be scanned near the buried oxide as a consequence of the front gate pulse. This leads to a partial pumping of those charges which are trapped near the back interface. The maximum in I_{cp} (Fig. 5) corresponds, therefore, to an additional contribution of the more defective region situated close to the buried interface.

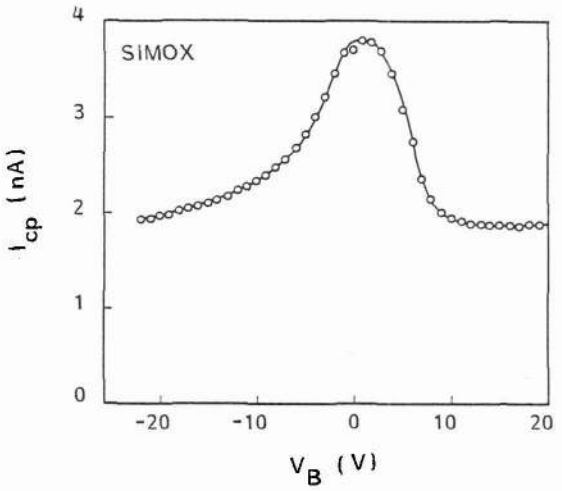

Fig.5. Front interface charge pumping current versus back gate bias

4 - CONCLUSION

In conclusion, the extension of the charge pumping method to gated diodes offers an elegant alternative to 5-terminal transistors for the assessment of bulk traps in the Si film and fast states at the interfaces of SOI structures. The density of fast states was found to be reasonably low (10^{11} $cm^{-2}eV^{-1}$) at the front interface in both SOS and SIMOX. A higher density of traps was determined for the buried interface and results probably from the oxygen implantation induced damage. The charge pumping in P-I-N diodes is a simple and accurate method and does not require any ad-hoc test device to be specially processed.

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