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Charge Sheet Super Junction in 4H-Silicon Carbide: Practicability, Modeling and Design

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ABSTRACT We discuss details of the Charge Sheet SuperJunction (CSSJ) in 4H-Silicon Carbide (SiC). This device was earlier proposed in Si material. A CSSJ is obtained by replacing the p-pillar of a SJ by a bilayer insulator, e.g., Al_2O_3/SiO_2; the inter-layer interface of this insulator has a negative charge-sheet, whose magnitude is easily controlled via the insulator deposition temperature. This charge-sheet depletes the n-pillar. Two potential advantages of this structural modification are brought out. First, it can avoid the problems related to SiC SJ's p-pillar fabrication. Second, it can lower the specific-on resistance, R_{ONSP}, below that of SJ by 5–45 %, since SiC technology allows the insulator to be thinner than the p-pillar. The critical field, E_C, in SiC is $>$ 10 times higher than that in Si. We give an analytical breakdown voltage, V_{BR}, model, which shows that the V_{BR} sensitivity to charge imbalance due to inevitable process variations is inversely proportional to E_C; hence, this sensitivity of CSSJ in SiC is $>$ 10 times lower than that in Si. On the other hand, we give numerical simulations to establish that, in spite of E_C differences, the SiC CSSJ inherits the advantage of upto 15% higher V_{BR} compared to SiC SJ, from its Si counterparts. We show how our prior analytical procedure of designing a SJ can be adapted to design a CSSJ having a lower R_{ONSP} than the SJ, at a specified V_{BR} in 1-10 kV range and charge imbalance $\leq$ 20 %. Our work should strengthen the motivation for fabricating the CSSJ in SiC.

INDEX TERMS 4H-SiC, breakdown voltage, specific on-resistance, TCAD simulation, analytical model, charge imbalance.

I. INTRODUCTION

The performance of a conventional silicon (Si) unipolar device based on the 1-Dimensional (1-D) p-n junction is limited by the so called *Si limit*, which is the minimum specific on-resistance, R_{ONSP}, achievable for a given breakdown voltage, V_{BR} [1]. The superjunction (SJ) structure (see Fig. 1(a)) was proposed [2] to lower the R_{ONSP} below this limit. In this structure, p-pillars are introduced into the n-type drift layer of the 1-D junction to realize a stack of alternating p- and n-pillars. This configuration transforms the field distribution from 1-D to 2-D, reducing the peak field for a given reverse bias, and hence yielding the V_{BR} at a much higher doping, N_d, than the 1-D junction. About a decade ago [3], we presented a variation of the SJ called the Charge Sheet SJ (CSSJ) (see Fig. 1(b)). Here the p-pillar of the SJ is replaced by a thin Al_2O_3 layer deposited on a thermally grown SiO_2 liner. The Al_2O_3/SiO_2 interface has a negative fixed charge whose magnitude can be controlled via the Al_2O_3 deposition temperature [4]. Based on qualitative physics and numerical simulation, we showed that the R_{ONSP} of the C_{SSJ} is even lower than that of a SJ by upto 50 %, for a given V_{BR}. Our subsequent work [5] explained the evolution of the CSSJ and SJ structures from a simple Γ-shaped p^+-n junction, and also, the practicability of the CSSJ concept.

The above devices were discussed in Si material. However, 4H-Silicon Carbide (SiC) has emerged as an alternative to Si for power semiconductor applications due to its superior material properties. Compared to Si devices, 4H-SiC devices provide $\sim$ 2000 times lower R_{ONSP}, for the same V_{BR}, [6]. Devices with V_{BR}, R_{ONSP} = 700 V, 1.01 mΩ-cm^2 [7] and 1726 V, 3.6 mΩ-cm^2 [8], which are close to the 1-D theoretical limit of unipolar 4H-SiC devices, have been reported.

Recently [9], we presented a preliminary account of a CSSJ in SiC using TCAD simulation. We showed that, apart from inheriting a lower R_{ONSP} for a given V_{BR} as compared to a SJ from its Si counterparts, the CSSJ in SiC has two additional advantages: a potentially much simpler fabrication process than a SJ in SiC, and 10 times lower V_{BR} sensitivity to charge imbalance (due to inevitable process variations) than a CSSJ in Si. In the present paper, we discuss these features further to build a strong motivation for actual device fabrication. We derive an analytical model for V_{BR} sensitivity to charge imbalance, and point out that the fall in V_{BR} with pillar doping is much less in SiC than in Si. Further, we show how the V_{BR} model and design procedure developed for SJ can be adapted for CSSJ in spite of some differences in the physics of SJ and CSSJ. Finally we establish how the CSSJ has the potential to solve the fabrication problems of the SJ.

The operation, practicability, V_{BR} model and design of CSSJ having $V_{BR} = 1 - 10$ kV are discussed in Sections II, III, IV and V respectively.

II. DEVICE OPERATION

To provide a background for later sections, we summarize the key features of the CSSJ theory and illustrate them with numerical simulations. The CSSJ theory is presented in comparison to that of SJ to highlight the advantages of the former. Most qualitative aspects presented here follow those reported in [3], [5] considering a Si device. However, the quantitative results are significantly different since the impact ionization and mobility parameters of SiC differ vastly from those of Si. Moreover, the R_{ONSP} formulae given below include the n-pillar depletion width, W_d, under zero-bias, denoted W_{d0}, which was ignored in prior works [3], [5].

The simulations use the Silvaco TCAD tool [10], Selberherr's impact ionization model for SiC with

$$a_n, a_p = 7.26, 6.86 \times 10^6 \text{ cm}^{-1}$$
$$b_n, b_p = 23.4, 14.1 \text{ MV cm}^{-1} \quad (1)$$

calibrated against the data in [11], and a mobility, μ_n, dependent on the doping, N_d, of the n-pillar as per

$$\mu_n = 40 + \frac{950 - 40}{1 + \left(\frac{N_d}{2\times 10^{17}}\right)^{0.76}} \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \quad (2)$$

which fits into the measured data at $T = 300$ K [12]. The details of the device structures simulated appear in the relevant figures. The structures are compatible with the state of the art as per which the negative fixed charge N_I at the insulator/semiconductor interface can be varied in the range of 2.5–7.9 $\times 10^{12}$ cm^{-2} [4] and the aspect ratio of the insulator (which fills trenches) and pillars can be as high as 18 [13].

A. SPECIFIC ON-RESISTANCE

In an SJ (see Fig. 1(a)), the p-pillar does not conduct in the ON-state and so, assuming $W_p = W_n$ without any loss of generality

$$R_{ONSP} = \frac{2L}{qN_d\mu_n\left[1 - (W_{d0}/W_n)\right]}. \quad (3)$$

Here, q is the electron charge and μ_n is electron mobility. Further, W_{d0} supports half of the built-in voltage V_{bi} of the junction between p and n pillars, and is given by

$$W_{d0} \approx \sqrt{\varepsilon_s V_{bi}/qN_d}, \quad V_{bi} \approx 2V_t \ln(N_d/n_i), \quad (4)$$

where ε_s is the dielectric constant, V_t is the thermal voltage and n_i is the intrinsic concentration. If the R_{ONSP} is sought to be reduced by reducing W_n and increasing N_d to maintain the charge balance, the V_{BR} degrades due to the increased peak field at the horizontal n$^+$/p-pillar interface. Instead, the CSSJ replaces the p-pillar of the SJ by an insulator film of thickness $W_I \leq W_n$ (see Fig. 1(b)). The negative interface charge, N_I, inverts the n-pillar inducing a vertical p$^+$n junction over L. The zero bias depletion width of this induced junction is $\sqrt{2}W_{d0}$ since it drops a potential $\approx V_{bi}$. The R_{ONSP} of CSSJ is given by

$$R_{ONSP} = \frac{L\left[1 + (W_I/W_n)\right]}{qN_d\mu_n\left[1 - \left(\sqrt{2}W_{d0}/W_n\right)\right]}. \quad (5)$$

Using the approximation $W_n >> \sqrt{2}W_{d0}$ for simplicity, (3) and (5) show that, for a given N_d, the R_{ONSP} of the CSSJ is lower than that of SJ by the factor

$$\frac{R_{ONSP,CSSJ}}{R_{ONSP,SJ}} \approx 0.5\left(1 + \frac{W_I}{W_n}\right). \quad (6)$$

Fig. 2 compares the N_d dependencies of the simulated R_{ONSP} of typical SJ and CSSJ. The devices simulated are balanced, but R_{ONSP} does not depend on the p-pillar doping, N_a. The CSSJ is seen to have 40% lower R_{ONSP} in accordance with (6). The difference in the N_d dependence of the V_{BR} of CSSJ and SJ, shown in this figure, is explained below.

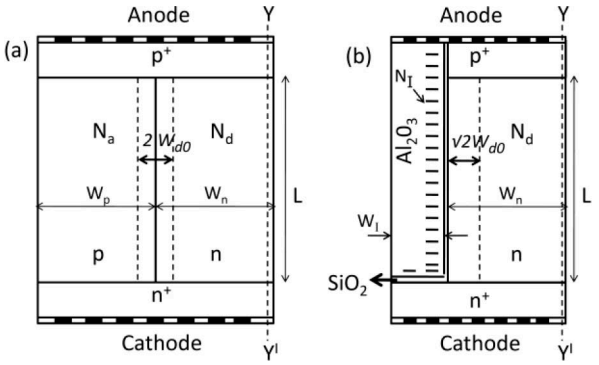

FIGURE 1. Cross section of a *linear* cell of a SuperJunction (SJ) (a) and Charge Sheet SuperJunction (CSSJ) (b). The device consists of lateral repetition of this cell.

B. BREAKDOWN VOLTAGE

We show that breakdown occurs in SiC, i.e., in the n-pillar, because in this condition, the field in SiO_2 or Al_2O_3 is below

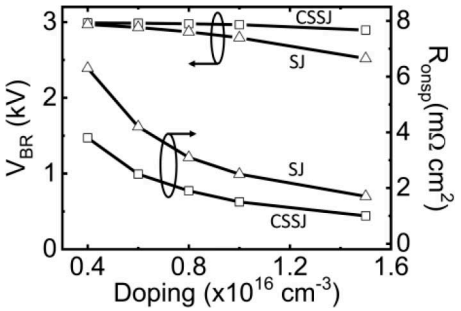

FIGURE 2. Simulated dependence of the breakdown voltage and specific on-resistance on the n-pillar doping, N_d, of balanced SJ and CSSJ realized in 4H-SiC; $W_n = W_p = 5$ μm, $W_I = 1$ μm and $L = 18$ μm.

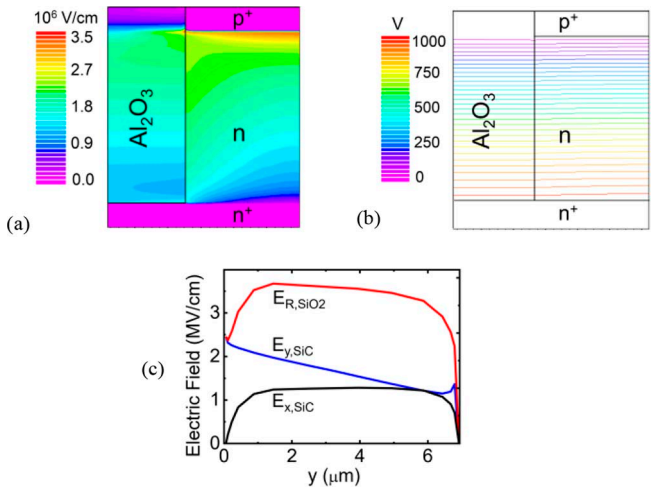

FIGURE 3. Simulations at breakdown in a 4H-SiC CSSJ with $W_n = 0.7$ μm, $W_I = 0.5$ μm, $L = 7$ μm, $N_d = 1 \times 10^{17}$ cm^{-3}, $N_I = N_d W_n = 7 \times 10^{12}$ cm^{-2} and $V_{BR} = 1$ kV. (a) Field contours; (b) potential lines; (c) vertical and lateral components of the n-pillar field ($E_{y,SiC}$ and $E_{x,SiC}$), and the resultant field in SiO_2 liner ($E_{R,SiO2}$) along the Al_2O_3/SiC interface over the pillar length, L.

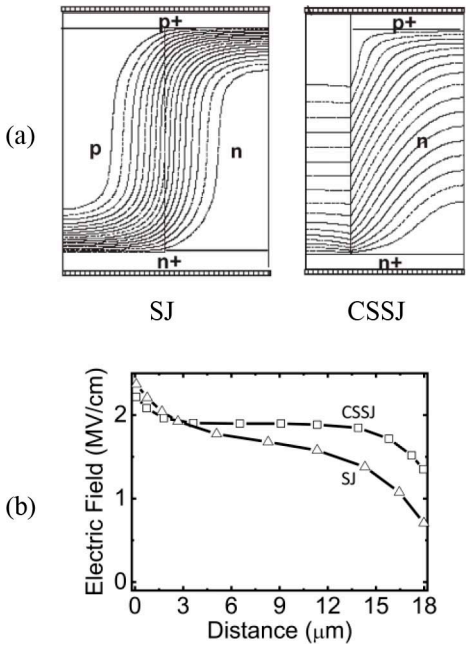

FIGURE 4. (a) Simulated potential lines at 300 V illustrating early lateral depletion in CSSJ than SJ. (b) Simulated field distribution over the pillar length, L, at breakdown, along the cut-line YY$^{\prime}$ of Fig. 1. The devices are realized in 4H-SiC; $W_p = W_n = 5$ μm, $W_I = 1$ μm, $L = 18$ μm, $N_d = 1.5 \times 10^{16}$ cm^{-3} and $N_I = N_d W_n = 7.5 \times 10^{12}$ cm^{-2}.

the critical breakdown field of these insulators which is ≥ 5 MV/cm as against ∼ 3 MV/cm of SiC [14]. For this purpose, we use the simulated field and potential distributions at breakdown in a device with 20 % charge imbalance and $V_{BR} = 1$ kV, given in Fig. 3. This is the worst case scenario since the field is lower in devices with higher V_{BR} and lower charge imbalance. The Silvaco simulator [10] allows the definition of an interface charge at a semiconductor/insulator interface but not at an insulator/insulator interface. We overcome this limitation and derive the accurate field distribution in all regions of the device by exploiting the fact that the SiO_2 liner thickness (∼ 7 nm) is << Al_2O_3(500 nm) or n-pillar thickness (700 nm). We ignore the SiO_2 liner and place N_I at the Al_2O_3/SiC interface. The field and potential distributions in the SiC and Al_2O_3 regions of such a structure closely simulate those with SiO_2 included and N_I placed at the Al_2O_3/SiO_2 interface. We then obtain the field distribution in SiO_2 using Gauss law, as per which the field E_y *parallel* to the interface is continuous across the SiO_2/SiC interface while the field E_x *normal* to the interface in SiO_2 is $\varepsilon_{SiC}/\varepsilon_{SiO2} \approx 2.5$ times that in SiC; the resultant field in SiO_2 is therefore $E_{R,SiO2} = \sqrt{E_{y,SiC}^2 + (2.5E_{x,SiC})^2}$, where $E_{y,SiC}$ and $E_{x,SiC}$ are the simulated fields at the Al_2O_3/SiC interface.

Fig. 3(a) confirms the following: the resultant field is maximum at the top right corner of the n-pillar, and hence maximum impact ionization or breakdown occurs at this point; the field reduces as one moves downward; the field in Al_2O_3 is less than that in SiC over the pillar length, and is everywhere < 1 MV/cm so that Al_2O_3 does not breakdown. The almost flat potential lines of Fig. 3(b) confirm that $E_y >> E_x$ in SiC and Al_2O_3. Fig. 3(c) shows the distributions of $E_{y,SiC}$, $E_{x,SiC}$ and $E_{R,SiO2} = \sqrt{E_{y,SiC}^2 + (2.5E_{x,SiC})^2}$ over the pillar length. It is seen that $E_{R,SiO2}$ remains well below 5 MV/cm and so breakdown does not occur in SiO_2. The validity of our simulations is confirmed by the fact that the simulated $E_{x,SiC} \approx qN_I/\varepsilon_{SiC}\varepsilon_0$ where $N_I = 7 \times 10^{12}$ cm^{-2}, over most of the pillar length.

B.1. BREAKDOWN VOLTAGE OF BALANCED DEVICES

Fig. 2 shows that the V_{BR} of a balanced CSSJ is same as that of a comparable SJ at low N_d. However, CSSJ's V_{BR} does not degrade as N_d is raised unlike the SJ's V_{BR} for the following reason. The reverse bias applied across the CSSJ terminals transfers to the induced inversion layer/n-pillar p^+n junction, expanding its lateral depletion width, W_d. However, the body effect shrinks the inversion layer; the shrinkage is more at the n^+ end than the p^+ end due to 2-D effects. The formation and non-uniform shrinkage of the inversion

layer as a function of reverse bias were discussed, illustrated pictorially and validated with TCAD in Section IV-A of our prior work on Si CSSJ [5]. The qualitative features of this work apply to SiC CSSJ as well.

As in zero bias, at other reverse biases too, W_d of CSSJ is $\sqrt{2}$ times that of SJ near the p^+ end where inversion layer is present. This is illustrated in Fig. 4(a) with the help of simulated potential lines in comparable SJ and CSSJ compatible with the state of the art [4], [13]. The nearly flat potential lines over W_I point to negligible voltage drop across the insulator thickness. Consequently, in CSSJ, the n-pillar gets fully depleted laterally at nearly half of the reverse bias required in an SJ; so this bias in CSSJ remains $<< V_{BR}$ even when N_d is raised. Once the n-pillar is fully depleted laterally, the field lines due to any more reverse bias emanating from the bottom n^+ directly terminate on the top p^+ as they find no charge left in the pillar to terminate on. Lower the bias for such lateral depletion, more the vertical field lines terminating directly or more uniform the vertical field distribution, E_y, over L, at breakdown. In corollary, even as N_d is increased, the breakdown field distribution in a CSSJ remains uniform unlike in a SJ (see Fig. 4(b)), and the area under this distribution, i.e., V_{BR}, remains constant.

It is of interest to compare the V_{BR} versus N_d behavior of SiC CSSJ (see Fig. 2) with that of its Si counterpart with comparable geometry and same N_d range of $0.4 - 1.6 \times 10^{16}$ cm^{-3} (see Fig. 4 of [3]). It is found that the V_{BR} of CSSJ in Si falls from 325 V to 150 V. The CSSJ's V_{BR} in both Si and SiC falls by $\sim$ 175 V. However, the absolute value of V_{BR} in SiC is $\sim$ 10 times higher than in Si due to the much higher E_C of the former. Hence, while the Si CSSJ's V_{BR} falls by a factor > 2, the relative fall in SiC CSSJ's V_{BR} is very small.

Since, at any N_d, CSSJ has a significantly lower R_{ONSP} and the same or slightly higher V_{BR} than an SJ, the CSSJ's R_{ONSP} is $\sim$ 40% lower for a given V_{BR} (see Fig. 5).

B.2. BREAKDOWN VOLTAGE OF IMBALANCED DEVICES

The *VBR* falls if the charge N_dW_n in the n-pillar differs from the p-pillar charge N_aW_p in an SJ or the interface charge, N_I, in a CSSJ. Such charge imbalance is inevitable due to process variations. For CSSJ, we define a charge imbalance factor as

$$k_{eff} = 1 - (N_I/N_dW_n) \quad N_I \leq N_dW_n. \tag{7}$$

Here, we have considered the case $N_I \leq N_dW_n$ rather than $N_I > N_dW_n$ since the V_{BR} is less for more n-pillar charge N_dW_n.

We can define the sensitivity of V_{BR} to k_{eff} as

$$S = \left[1 - \frac{V_{BR}(k_{eff})}{V_{BR}(k_{eff} = 0)}\right] \times 100. \tag{8}$$

Simulations have shown that the S of SJ and CSSJ realized in the same material differ by $< 5\%$ [3]. However, it is significant that S of SJ or CSSJ realized in SiC is $\sim$ 10 times lower than those realized in Si. This is illustrated for the CSSJ in Fig. 6, where the simulated percentage degradation in V_{BR} is plotted against k_{eff}. Charge imbalance of significant degree may be present in a practical device, even with state of the art technology. Hence, apart from achieving a higher V_{BR} that has long been the motivation for replacing Si with 4H-SiC, the above reduced sensitivity is an added motivation to realize the CSSJ in 4H-SiC.

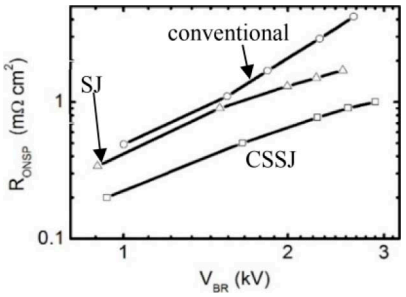

FIGURE 5. Simulated specific on-resistance versus breakdown voltage for theSJ and CSSJ realized in 4H-SiC; $W_n = W_p = 5$ μm, $W_I = 1$ μm and $N_d = 1.5 \times 10^{16}$ cm^{-3}; L is varied to vary the V_{BR}. Conventional 4H-SiC junction data is shown for reference.

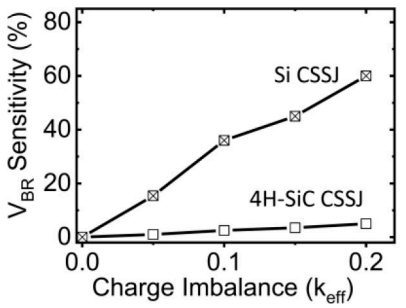

FIGURE 6. Simulated V_{BR} Sensitivity versus charge imbalance of a Si and 4H-SiC CSSJ with $N_d = 7 \times 10^{15}$ cm^{-3}, $W_n = W_p = 2.5$ μm and $W_I = 1$ μm. For Si CSSJ, data is reproduced from [3].

Considering the above advantages of CSSJ from physics point of view, we are motivated to examine the practicability of CSSJ fabrication in the next section. Subsequent sections describe an analytical model for the V_{BR} degradation with k_{eff}, the above material dependence of S and the design of an optimum CSSJ in the presence of charge imbalance.

III. DEVICE PRACTICABILITY

In [9], we gave the following possible sequence of key steps for fabricating a CSSJ and briefly discussed the practicability of the device.

1) Starting n^+ substrate
2) Epitaxial growth of the n-type drift layer
3) Aluminum implantation of the top p+ region
4) High aspect ratio trench formation using Inductively Coupled Plasma (ICP) etching
5) SiO_2 liner growth by dry oxidation
6) Al_2O_3 deposition by Atomic Layer Deposition (ALD) at a temperature, T_{dep}, in the range of 150–350°C

7) Filling of the any unfilled trench by Chemical Vapor Deposited (CVD) Al_2O_3.
8) Contact formation

In the present work, we explain in detail the advantages of CSSJ from fabrication point of view by contrasting the above steps 4) – 7) used to realize the insulator with those used to realize the p-pillar of a SJ in 4H-SiC material.

The fabrication of SJ in 4H-SiC has been problematic. The first two reported works could not make a functional SJ device [16], [17]. The first functional 4H-SiC SJ was reported by Zhong *et al.* [18], [19] using trench etching and sidewall implantation of p-dopant. However, the fabrication of this 1.35 kV SJ device required six implantations of 40-360 keV energy followed by a high temperature anneal at 200 – 1400°C for 30 minutes, for creating a p^+ liner along the sidewalls of a 6 μm deep trench. Also, the p-dopant activation efficiency varied between 20–65 % in the annealing temperature range, and required a trial and error approach to locate the temperature corresponding to the "optimum charge balance" that yields the maximum V_{BR}. This temperature was found to be 1350°C and applies only to the device fabricated in [18]. A similar trial and error approach is required for fabricating devices with any other V_{BR}. Considering that the charge imbalance level in Si SJ can go up to 20 % [20], such imbalance levels could be even higher in 4H-SiC SJ due to this added difficulty in controlling the p-dopant activation efficiency [21]. In addition, the above steps of fabricating p-pillars in a 4H-SiC SJ are tedious, expensive and prone to causing severe wafer damage. We shall now assess the CSSJ steps 4) – 6) in the above backdrop.

Consider the trench width in the trench formation step 4). An SJ requires wider and hence lower aspect ratio trench to uniformly implant the trench side walls. The CSSJ could have a narrower trench than SJ, enabling reduction in R_{ONSP} as per (6). This is because, the CSSJ fabrication involves formation of trenches and subsequent insulator deposition on an SiO_2 liner, which is very well practiced in the case of trench dielectric isolation in CMOS and DRAM cells. These steps are also employed for creating isolation and edge termination in high voltage devices including super junctions [15], [22]. In addition, highly conformal Al_2O_3 deposition by ALD could be achieved in trench with very high aspect ratio up to 50 [23].

Consider the trench depth in the trench formation step 4). Trenches of depth varying from few microns to > 100 μm may be required for making devices in the range of 1-10 kV or higher [24]. In SiC, high aspect ratio trenches with depth up to 53 μm have been fabricated using ICP etching [13] and up to 200 μm using laser ablation method [25]. However, for SJ devices, the number of high energy implantations, required to create a p^+ layer with uniform charge along the walls, may significantly increase for deeper trenches [19]. This limits the voltage range of SJ devices realizable in 4-H SiC. However, the fabrication complexity of CSSJ does not increase with V_{BR} as multiple implantation steps are avoided, Thus, CSSJ is suitable for applications with a wider range of V_{BR}.

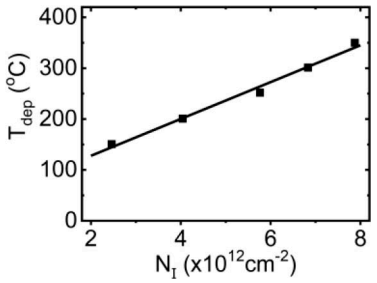

FIGURE 7. The Al_2O_3 deposition temperature versus the negative charge concentration at the Al_2O_3/SiO_2 interface. Line is our model (17); points are experimental data from [4].

Consider the step 5) involving SiO_2 liner growth. The liner thickness is ∼ 7 nm [4] but not critical for three reasons. First, it makes negligible contribution to W_I(see Fig. 1(b)) which happens to be > 100 nm due to the limitations of the trench realization process. Second, it does not affect N_I formed at the liner's interface with Al_2O_3 [4]. Third, there is negligible potential drop over this thickness even at high reverse bias as illustrated by the potential lines of the CSSJ in Fig. 4(a).

Consider the step 6) involving Al_2O_3 deposition by ALD to realize N_I at Al_2O_3/SiO_2 interface. The magnitude of N_I can be controllably varied in the range

$$2.5 \times 10^{12} \leq N_I \leq 7.9 \times 10^{12}\text{cm}^{-2} \tag{9}$$

by varying the deposition temperature, T_{dep}, in the range 150–350°C (see Fig. 7) [4]. The controllability of the charge at the SiO_2/4H-SiC interface does not affect the CSSJ operation. This is because, decades of research has reduced this charge from 5×10^{12} cm^{-2} [26] to 3×10^{11} cm^{-2} [27], i.e., to < 10 % of N_I of (9). Efforts are on to further reduce this charge which degrades inversion layer mobility of SiC MOSFETs.

We recognize that the data of (9) and Fig. 6 correspond to a Al_2O_3/SiO_2 bilayer realized on a Si substrate [4]. We are justified in using this data for the SiC substrate of our case because of the following reason. Theories of N_I at the Al_2O_3/SiO_2 interface attribute N_I to either the uncompensated negative $(AlO_{4/2})^-$ units at the interface [28], or the OH groups trapped in the volume of the Al_2O_3 [29]. In either theories, the nature and magnitude of N_I depend primarily on the Al_2O_3 and SiO_2 layers and their interface, and the role of the substrate on which these layers are deposited is secondary. Thus, [30], [31] report a negative charge of the same order as in (9) at the Al_2O_3/SiO_2 interface formed on 4H-SiC substrate and explain its origin using the theory of [4] based on Si substrates. This is analogous to the situation for the 2-Dimensional Electron Gas (2-DEG) at the AlGaN/GaN interface. The guidelines for the 2-DEG

in AlGaN/GaN layers on sapphire substrate [32] are widely used for such bilayers on Si or SiC substrates as well.

Thermal cycles at 500–850°C occur after the ALD of Al_2O_3 during possible trench filling by CVD deposited insulator [33] in step 7) or silicidation during contact formation [18], [34] in step 8). These cycles can be designed to affect the N_I minimally. For example, [4] showed that annealing at 700°C for 60 minute causes only $< 5\%$ increase in N_I from the as-deposited value. Even if N_I turns out to be different than [4] for any reason or during further studies, our models and design procedure can still be used with suitable modification of the numbers in (9) and (17).

The CSSJ fabrication involves only a single high energy implantation process given in step 3), thereby saving cost and time, and reduces crystal damage and defects. Unlike this, for an SJ, multiple implantations of appropriately designed energy, dose and tilt angle are crucial in realizing a thin p^+ region with uniform charge along the walls of the trench. The large number of parameters involved makes this a tedious design problem. Process variations in all these parameters contribute to charge imbalance. In contrast, design of the p-pillar equivalent charge, N_I, in CSSJ is simpler as it involves choosing a single parameters, T_{dep}. Also, the easier control over the T_{dep} than the p-dopant implantation and activation parameters in SiC, enables fabrication of CSSJ with a lower charge imbalance than SJ.

Reference [22] has given evidence for the lateral depletion of a SJ pillar by fixed charge of the insulator employed between p- and n-pillars to prevent dopant inter-diffusion. Reference [5] has argued that insulator charges do not always pose reliability problems. For instance, in AlGaN/GaN HEMTs, a high interface charge (due to polarization) has been exploited to improve the device performance. Moreover, reliability problems posed by the trapped charge in the gate insulator of small-signal MOSFETs do not apply to the insulator charge providing the charge sheet essential for CSSJ operation. This is because the field in the insulator of a CSSJ is negligible (see Fig. 3(a)), unlike in the gate of a small-signal MOSFET.

Thus, CSSJ has the potential to solve the fabrication problems of SJ. We now discuss how the V_{BR} model and design procedure developed for SJ can be extended to CSSJ.

IV. ANALYTICAL MODEL OF THE BREAKDOWN VOLTAGE

We derive a model for the V_{BR} in balanced and imbalanced CSSJ by considering the vertical breakdown field distribution, E_y, over L in a CSSJ along the cut-line Y-Y' in the n-pillar (see Fig. 1(b)). Fig. 8 shows this distribution for various $k_{eff} \leq 1$ as obtained from a TCAD simulator. We can regard this distribution as reducing linearly from an extrapolated peak value, E_C (the slope is zero for the balanced case $k_{eff} = 0$). This situation is analogous to that in an SJ analyzed in [24], [35], where the linear segment of the E_y versus y distribution has been shown to have the slope $= qk_{eff}N_d/2\varepsilon_S$. Based on this approximation, we write

$$V_{BR} \approx E_C L - 0.25\left(qk_{eff}N_d/\varepsilon_S\right)L^2. \tag{10}$$

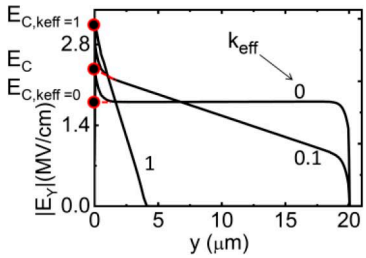

FIGURE 8. Simulated vertical field distribution in a CSSJ at breakdown over pillar length along the cut-line YY' of Fig. 1 for different charge imbalance factors, k_{eff}. Pillar parameters are $L = 20$ μm, $W_n = 0.56$ μm, and $N_d = 8 \times 10^{16}$ cm^{-3}.

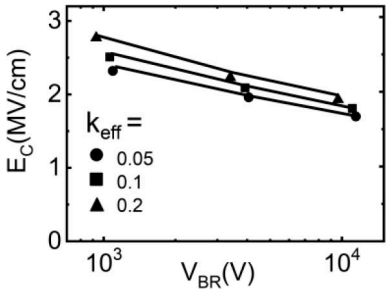

FIGURE 9. Critical electric field as a function of V_{BR} for several values of charge imbalance factor, k_{eff}, and $r_n = 11$; values remain unaffected for $r_n > 11$. Lines are model results using (12)-(14) and (10) which apply to SJ [24]; solid circles are TCAD simulation results of CSSJ.

A simple formula for S defined in (8) can be derived using (10) and approximating E_C to be independent of k_{eff} as

$$S \approx 25qk_{eff}N_dL/\varepsilon_s E_C. \tag{11}$$

It is seen that $S \propto 1/E_C$ for a given value of N_d and L; as E_C of 4H-SiC is $\sim$ 10 time higher than Si, the V_{BR} sensitivity of 4H-SiC CSSJ to charge imbalance is lower than that of Si CSSJ by the same factor.

For accurate estimation of V_{BR}, the dependence of E_C on L, N_d and k_{eff} should be taken into account. For this purpose, we adopt the following interpolating function given for an SJ [24]

$$E_C = \left(1 - k_{eff}\right)^{\beta} E_{C,k_{eff}=0} + k_{eff}^{\beta} E_{C,k_{eff}=1} \tag{12}$$

where $E_{C,k_{eff}=0}$ is the value at low N_d and so a function of L alone, and $E_{C,k_{eff}=1}$ is the breakdown field in a 1-D p-n junction and so a function of N_d alone, as given below

$$\begin{aligned} E_{C,k_{eff}=0} &= (\gamma L)^{-1/8}, \quad E_{C,k_{eff}=1} = \alpha N_d^{1/8} \\ \gamma &= 4 \times 10^{-48}\ \text{cm}^7 \cdot \text{V}^{-8}\ \ \alpha = 2.56 \times 10^4 \text{V} \cdot \text{cm}^{-5/8} \\ \beta &\approx 0.8 + 1.85e^{-0.35r_n} \text{ for } r_n \geq 5. \end{aligned} \tag{13}$$

Here, r_n denotes the aspect ratio of the n-pillar as per

$$r_n = L/2W_n. \tag{14}$$

The α and γ are based on the impact ionization coefficients of (1). The β expression has been verified upto $k_{eff} = 0.2$, and reduces to $\beta \approx 0.8$ for $r_n > 11$. Fig. 9 plots the E_C

calculations using (12)-(14) versus V_{BR} calculated using this E_C in (10), and compares this plot with TCAD simulations, for $r_n \geq 11$ or $\beta = 0.8$. The agreement between the compared results validates the adoption of SJ's E_C formula for estimating CSSJ's V_{BR} using (10).

It is seen that the difference in the breakdown field distributions in the CSSJ and SJ at high N_d do not matter here. This difference is ultimately traced to the presence of inversion layer along the vertical interface of the n-pillar with the Al_2O_3/SiO_2in a CSSJ that is absent in the SJ. It is significant that the E_C and V_{BR} formulae developed for SJ apply to the CSSJ in spite of this difference in the physics of the two devices.

V. DEVICE DESIGN

Recently [24], we gave an analytical procedure for designing a SJ having the minimum R_{ONSP} for a specified $V_{BR,target}$ and a k_{eff} governed by technology. We can adapt this procedure to design a CSSJ as follows. We set L and N_d of the CSSJ equal to the optimum n-pillar parameters – L_{opt} and N_{dopt} of the SJ. However, W_n of the CSSJ can differ from that of the SJ. Moreover, as pointed out in Section III, the present SiC technology allows W_I of the CSSJ to be much thinner than the p-pillar of the SJ. We choose the maximum possible W_n and minimum possible W_I to minimize R_{ONSP} given by (5), i.e.,

$$W_I = L_{opt}/2r_{I,\max},\ \ W_n = L_{opt}/2r_{n,\min},\ N_I = N_{dopt}W_{nopt}. \tag{15}$$

Here, $r_{I,max}$ is the maximum aspect ratio of the insulator permissible in the technology. Further, $r_{n,min}$ is the minimum aspect ratio of the n-pillar limited by the condition $N_I \leq N_{Imax}$ which is the maximum value in (9)

$$r_{n,\min} \geq \left(N_{dopt}L_{opt}/2N_{I\max}\right). \tag{16}$$

Both r_I and r_n differ from aspect ratio r of the pillars of a SJ. Finally, we estimate R_{ONSP} from (5), and the insulator deposition temperature by the following empirical fit to the measured data (see Fig. 7)

$$T_{dep} = 3.62 \times 10^{-11}N_I + 55.4, \tag{17}$$

where T_{dep} is in °C and N_I is in cm^{-2}.

Reference [24] gave the formulae for L_{opt} and N_{dopt} of an SJ as

$$L_{opt} \approx 2.08 \times 10^{-7}V_{BR\text{target}}^{8/7} \text{ for } r_n = 5, k_{eff} \geq 0.1, \tag{18}$$

whose values deviate from those of TCAD by ≤ 5 % in the validity range, and

$$N_{dopt} = \frac{2\varepsilon_s V_{BR\text{target}}}{qk_{eff}L_{opt}^2}\left[\frac{1-\left(\sqrt{2}W_{d0}/2W_{nopt}\right)}{1-\left(3\sqrt{2}W_{d0}/4W_{nopt}\right)}\right] \text{ for } k_{eff} >> 1/2r_n^2, \tag{19}$$

where we have used the zero bias depletion width $\sqrt{2}W_{d0}$ of CSSJ instead of W_{d0} of SJ used in [24] and given by (4).

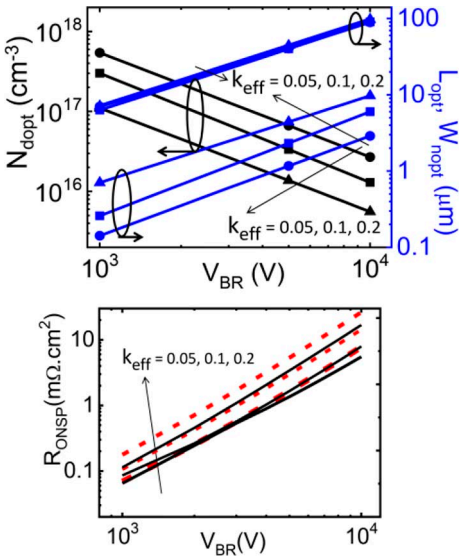

FIGURE 10. (Top) The n-pillar parameters of the CSSJ versus V_{BR} for different charge imbalance factors; the insulator thickness W_I is given by (15) using the L_{opt} data and $r_{I,max} = 18$ [13], [23]; $r_{n,min}$ is varied to yield the optimum results. Lines are our design results and points are TCAD simulations. (Bottom) R_{ONSP} versus V_{BR} plots for the CSSJ (solid lines) and for a SJ with $r = 5$ (dashed lines).

We can get a quick approximate estimate of the various parameters in closed-form using (15)-(19) in the following sequence: L_{opt} from (18), W_{nopt} and W_{Iopt} from (15), N_{dopt} from (19) where W_{d0} is calculated from (4) using the value of N_{dopt} with $W_{d0} = 0$, N_I from (15) and T_{dep} from (17).

For accurate results with a general k_{eff} and r_n, an iterative calculation is done as follows by including (10) and using L_{opt} from (18) as initial condition. A numerical calculator does this in < 1 s, while our MATLAB code [36] takes $\approx$ 70 ms.

a) $r_{n,min} = 1$, which is an initial guess.
b) $W_{nopt} = L_{opt}/2r_{n,min}$.
c) N_{dopt} from (19), where W_{d0} is estimated using N_{dopt} for $W_{d0} = 0$ for the first time, and using the previous N_{dopt} thereafter.
d) E_C from (12)-(14) and L_{opt} as the root of the quadratic (10). Iterate a)−c) until successive values of L_{opt} differ by < 1 %.
e) If $W_{nopt}N_{dopt} > N_{Imax} = 7.9$ x 10^{12} cm^{-2} increment $r_{n,min}$ by 0.2 and repeat a) – d).
f) $W_{Iopt} = L_{opt}/2r_{I,max}$

Fig. 10 (Top) shows that the above calculations of the CSSJ parameters for $V_{BR,target} = 1 - 10$ kV and $k_{eff} = 0.05 - 0.2$ agree with TCAD simulations. Fig. 10 (Bottom) compares the R_{ONSP} of the CSSJ so designed with that of a SiC SJ having the same $V_{BR,target}$ and k_{eff}. It can be seen that for $V_{BR,target}$ in the range of 1–10 kV, the R_{ONSP} of CSSJ is lower than that of SJ by 5–30%, 19–45%, and 36% for $k_{eff} = 0.05, 0.1$ and 0.2 respectively. Thus, CSSJ is a viable alternative to SJ in 4H-SiC material with superior electrical performance for high voltage applications in the range 1-10 kV.

VI. CONCLUSION

It was shown that the Charge Sheet SuperJunction (CSSJ) proposed earlier in Silicon (Si) has significant advantages over SJ in 4-H Silicon Carbide (SiC) material. These include, as compared to SJ in SiC, potentially simpler fabrication process, lower charge imbalance and 5–45 % lower specific ON-resistance for a given breakdown voltage. Further, a CSSJ in SiC is $>$ 10 times less sensitive to charge imbalance than that in Si. The theory, modeling and design of SJ can be easily extended to CSSJ over 1-10 kV in spite of some differences in the physics of these two devices. Our work provides a strong motivation for fabricating the 4H-SiC CSSJ proposed.

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