Charge Steering: A Low-Power Design Paradigm

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Abstract

Discrete-time charge-steering circuits consume less power than their continuous-time current-steering counterparts even at high speeds. This advantage can be exploited in the design of semi-analog circuits such as latches, demultiplexers, and CDR circuits as well as mixed-mode systems such as ADCs. Employing charge steering in 65-nm CMOS technology, a 25-Gb/s CDR/deserializer consumes 5 mW and a 10-bit 800-MHz pipelined ADC draws 19 mW.

I. Introduction

The thrust for low-power circuit design continues unabated, presenting especially tough challenges as high speeds are sought. The power-speed trade-off associated with any circuit function becomes nonlinear as the frequency of operation exceeds a certain limit, motivating efforts toward developing new techniques.

This paper presents the concept of "charge steering" as a candidate for low-power, high-speed design. Applicable to both digital and analog circuits, the concept offers a factor of 2 to 4 power saving for a given set of design constraints, and it has been demonstrated in the context of a 25-Gb/s clock and data recovery (CDR)/deserializer circuit [1] and a 10-bit 800-MHz analog-to-digital converter (ADC) [2].

Section II introduces the basic idea and Section III deals with charge-steering logic. Section IV applies the concept to CDR and deserializer design, describing how charge steering issues can be resolved at the architecture level. Section V presents charge-steering op amps and their use in pipelined ADCs.

II. Basic Idea

A continuous-time current-steering circuit can be transformed to a discrete-time charge-steering topology as depicted in Fig. 1: the tail current source is replaced with a charge source, and the load resistors with capacitors. Discrete-time operation requires two switches in the tail path and two at the output nodes. Shown here for a simple differential pair, the transformation can be applied to other circuit topologies as well.

Figure 2 illustrates the operation of the charge-steering stage. The circuit begins in the reset mode, with C_T discharged to ground and the output nodes precharged to V_{DD}. When CK goes high, the circuit enters the amplification mode,

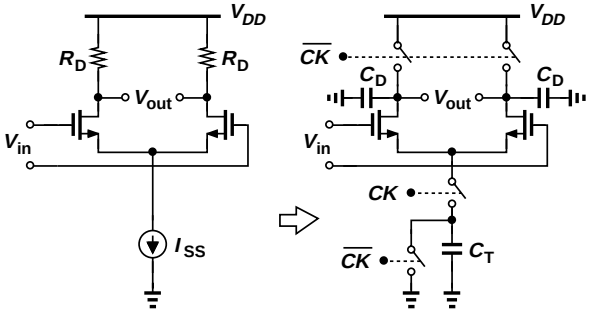

Fig. 1. Transformation from current steering to charge steering.

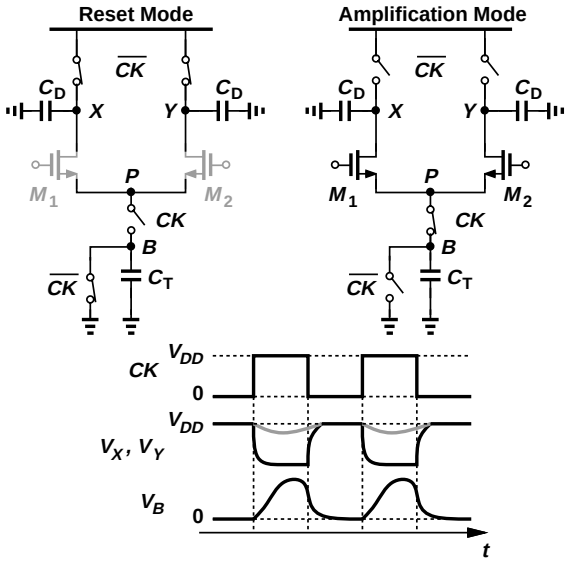

Fig. 2. Operation of charge-steering stage.

C_T pulls current from M_1 and M_2, and nodes X and Y are released. The two transistors continue to draw differential and common-mode (CM) currents from the load capacitors until C_T charges to approximately one threshold below the higher input level. As explained below, with proper choice of device parameters, the charge-steering stage can provide voltage gain.

The discrete-time nature of this topology offers three advantages over its continuous-time counterparts. First, the circuit can serve as a latch with moderate, controlled output swings, potentially running faster than rail-to-rail (CMOS) logic. Second, the stage steers current for a fraction of the clock period, thereby consuming less power than continuous-time topologies such as current-mode logic (CML) circuits. Third, since the average power consumption of the stage scales with fre-

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quency, the same design can be reused at different clock rates with no modification. For example, the ADC described in Section V has been tested with clock frequencies ranging from 100 MHz to 800 MHz, with its power consumption varying from 2.4 mW to 19 mW. This attribute is particularly attractive for applications that require a wide range of clock frequencies and typically dictate extensive programmability in the design.

Charge steering faces two issues. First, in contrast to conventional CML circuits, the switches in Fig. 2 must be driven by rail-to-rail clock swings. Nonetheless, the power savings afforded by this technique typically outweigh the clock power consumed in a CML environment. Second, as with any precharged circuit, charge-steering topologies produce a return-to-zero (RZ) output. This issue manifests itself in data communication systems, e.g., CDR circuits, but not in inherently discrete-time applications such as ADCs.

The charge-steering stage of Fig. 2 forms the foundation for the digital and analog circuits described in this paper. We will employ this building block to develop phase detectors (PDs), CDRs, and demultiplexers (DMUXes) for wireline design as well as op amps for ADC design.

It is important to distinguish this topology from other differential dynamic logic styles. In the differential precharged stage of Fig. 3(a), the absence of a tail capacitor allows the

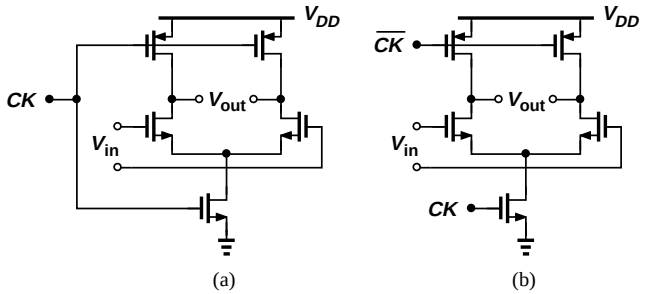


Fig. 3. Examples of differential dynamic circuits: (a) precharged, (b) dynamic amplifier.

outputs to collapse to zero, leading to a slow response. Also, in the logic style of Fig. 3(b) [3], the circuit draws current from V_{DD} for half a clock cycle and, more importantly, suffers from a lower speed because its tail current must flow from both the PMOS loads and the load capacitances.[1]

III. Charge-Steering Logic

A. Gain and Power Consumption

For use in high-speed digital design, the charge-steering circuit of Fig. 2 must operate with moderate input and output voltage swings while providing some voltage gain so as to restore the logical levels. It can be shown that, for a small differential input, V_{in}, the voltage gain is relatively independent of the input CM level, V_{CM}, and is given by [1]

$$A_v \approx \frac{2C_T}{C_D}. \tag{1}$$

[1]But one advantage of this style is that it produces an NRZ output.

For moderate to large inputs, on the other hand, the differential output voltage depends on V_{CM} and is equal to

$$V_{out} = \frac{C_T}{C_D} \frac{(V_{CM} - V_{TH})^2 + \frac{3V_{in}^2}{4}}{V_{CM} - V_{TH} + \frac{V_{in}}{2}}, \tag{2}$$

where V_{TH} denotes the threshold voltage of M_1 and M_2 [1]. Derived using simple, rough approximations, these expressions are plotted in Fig. 4 against simulation results, exhibiting modest accuracy. In this example, the circuit provides a small-signal gain of about 2 and an output swing of about 350 mV.

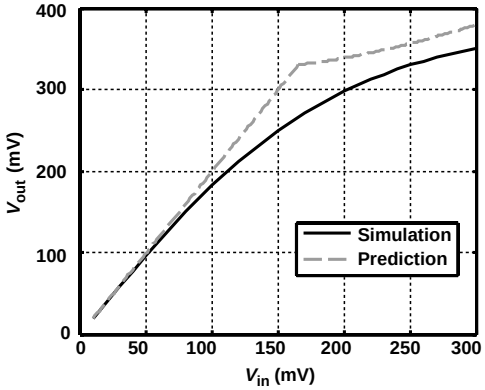


Fig. 4. Simulated and calculated characteristics of charge-steering stage.

In order to appreciate the power swings, we perform a comparison with a continuous-time CML stage. Suppose the two topologies in Fig. 1 operate at the same rate, r_b, and deliver equal voltage swings to equal load capacitances, C_D. Note that C_D is not an explicit capacitor and simply models the parasitics at each node and the input capacitance of the following stage. The CML circuit must provide a bandwidth of about $0.7r_b$, i.e., $(2\pi R_D C_D)^{-1} = 0.7r_b$, while producing a single-ended output swing of $\Delta V = I_{SS}R_D$. In the charge-steering configuration, only one load capacitor charges to V_{DD} and discharges to $V_{DD} - \Delta V$ in each bit period, yielding an average supply current equal to

$$I_{DD} = C_D r_b \Delta V. \tag{3}$$

Eliminating r_b and R_D from the foregoing expressions, we obtain

$$\frac{I_{DD}}{I_{SS}} = \frac{1}{1.4\pi}, \tag{4}$$

predicting a factor of 4.4 reduction in power.

B. Regenerative Latch

The concept of charge steering can be applied to regenerative latches as well. Let us contemplate a discrete-time version of a standard CML latch [Fig. 5(a)], assuming that M_1-M_2 and M_3-M_4 are enabled by complementary clocks. Unfortunately, this circuit requires three phases for precharge, amplification, and regeneration. We instead consider only the cross-coupled

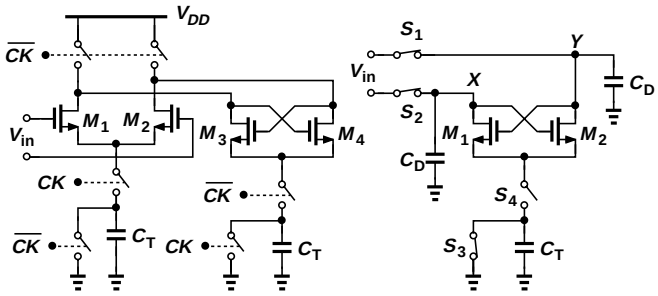


Fig. 5. (a) Charge-steering implementation of a CML latch, (b) single regenerative latch.

pair and convert its precharge mode to a *sampling* mode [Fig. 5(b)]. The circuit now tracks the input for half a clock cycle and regenerates for the other half, thus producing a non-return-to-zero (NRZ) output.

The NRZ latch of Fig. 5(b) can provide voltage gain. If the transistors operate in weak to moderate inversion, the gain can be approximated as [1]

$$\frac{V_{XY\infty}}{V_{XY0}} = \exp\left(\frac{C_T}{C_D}\frac{V_{CM}-V_{GS}}{2\zeta V_T}\right), \qquad (5)$$

where the left-hand side represents the ratio of the final and initial voltages, V_{GS} is assumed relatively constant, and ζ denotes the subthreshold nonideality factor and is given by $1 + C_d/C_{ox}$, where C_d is the depletion capacitance under the channel. Figure 6 plots Eq. (5) with $V_{GS} = 450$ mV along with simulation results, indicating good agreement.

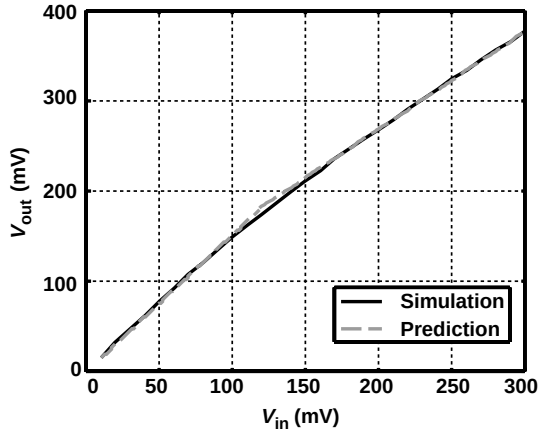


Fig. 6. Simulated and calculated characteristics of NRZ latch.

C. Cascading Issues

In order to implement flipflops and more complex functions, charge-steering latches must be cascaded. We consider the topologies in Figs. 2 and 5(b) for this purpose, noting that one permutation, Fig. 5(a), has not proved practical. Figure 7(a) shows another permutation consisting of two cascaded RZ latches driven by CK_1 and CK_2. This arrangement faces an issue if the two clocks are simply complementary: when the slave begins to sense, the master enters the precharge mode

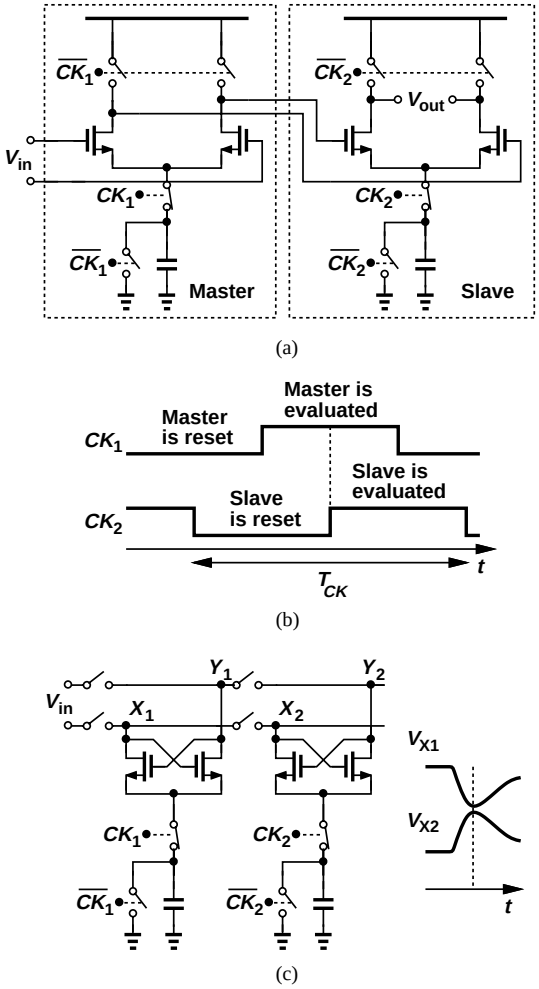


Fig. 7. (a) Cascade of two RZ latches, (b) use of quadrature clocks, (c) cascade of two NRZ latches.

and its differential output begins to collapse. The slave may therefore generate a small output swing in some corners of the process. To avoid this race condition, one can employ quadrature phases for CK_1 and CK_2 so that the master output is held constant when the slave enters the evaluation mode [Fig. 7(b)] - but at the cost of power and complexity in clock generation.

Figure 7(c) shows another cascading permutation using two NRZ latches. In this case, the circuit contains no internal path from V_{DD} and hence provides no charge amplification. That is, only the charge deposited by V_{in} must produce the voltage swings as the signal propagates down the chain, leading to substantial corruption of random data. As illustrated in Fig. 7(c), if the states on X_2 and Y_2 are opposite of those on X_1 and Y_1, when S_3 and S_4 turn on, the master and slave capacitances experience severe charge sharing, heavily attenuating the data swings. Even if the master devices are scaled up by a factor of 5, this memory effect still produces significant intersymbol interference (ISI).

The last permutation of the RZ and NRZ latches is shown in Fig. 8. Here, the master consists of the passive sampling

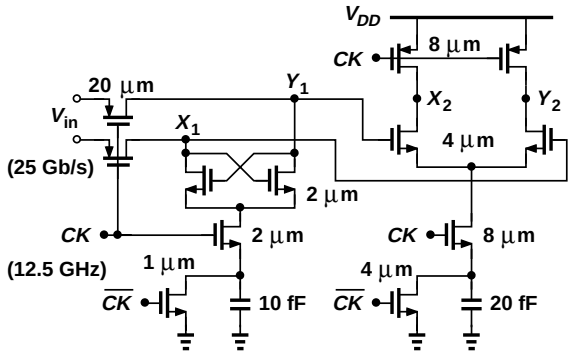


Fig. 8. Cascade of NRZ and RZ latches.

network, S_1 and S_2, while the slave is formed by M_1-M_2 and M_3-M_4. The charge amplification provided by the latter pair avoids corruption of the state stored by the former. Clocked simultaneously, the two stages amplify the sampled signal at X_1 and Y_1, generating a single-ended swing of about 400 mV at X_2 and Y_2 with a power consumption of 158 μW at a data rate of 25 Gb/x and a clock rate of 12.5 GHz. However, the output is still in RZ form

IV. CDR AND DMUX DESIGN

The concepts developed above can be applied to the design of high-speed CDRs and (de)multiplexers. In this section, we present some examples for 25-Gb/s operation, assuming a half-rate architecture but without quadrature clock phases.

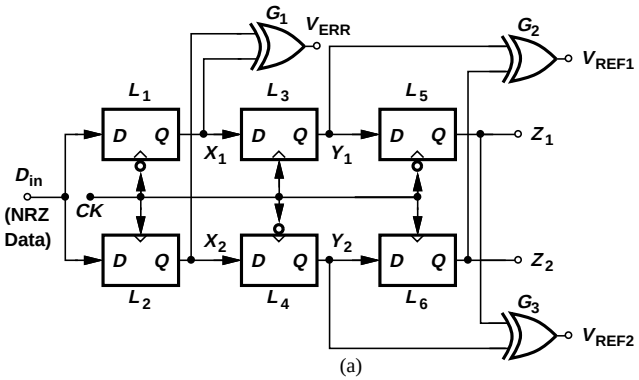
A. Half-Rate Phase Detector

A half-rate PD that does not require quadrature clocks can be realized as four latches and two exclusive-OR (XOR) gates [4]. Unfortunately, this topology does not lend itself to charge steering circuits with RZ outputs [1]. Fortunately, it is possible to modify the PD so as to operate with RZ data [Fig. 9(a)]. Here, latches L_5 and L_6 are added to insert half a cycle delay, and XOR gates G_2 and G_3 are respectively used to compare Y_1 with a delayed version of Y_2 and Y_2 with a delayed version of Y_1. The average difference between V_{ERR} and $V_{REF} = V_{REF1} + V_{REF2}$ represents the phase difference between the random data and the clock [Fig. 9(b)].

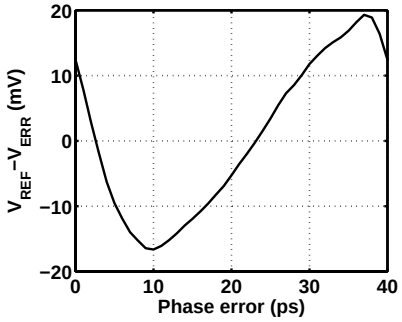
In the circuit of Fig. 9(a), the latch pairs L_1-L_3 and L_2-L_4 are constructed as shown in Fig. 8. Latches L_5 and L_6 employ the RZ topology of Fig. 2. The retimed half-rate data is available at Y_1 and Y_2 but still in RZ form.

B. Demultiplexer

In order to further demultiplex the data, we cascade RZ latches but ensure that when one is being reset, the next does not begin to sense. This is possible because the half-rate (12.5-GHz) clock can be divided by 2 so as to produce quadrature phases at 6.25 GHz. Figure 10 depicts such an arrangement and its timing diagram, where $CK_{1/2,I}$ and $CK_{1/2,Q}$ represent the quadrature phases of the 6.25-GHz clock. We note that at $t = t_1$, L_3 (one of the latches within the PD) enters the evaluation mode and, after one divider delay, so does L_7. Next,

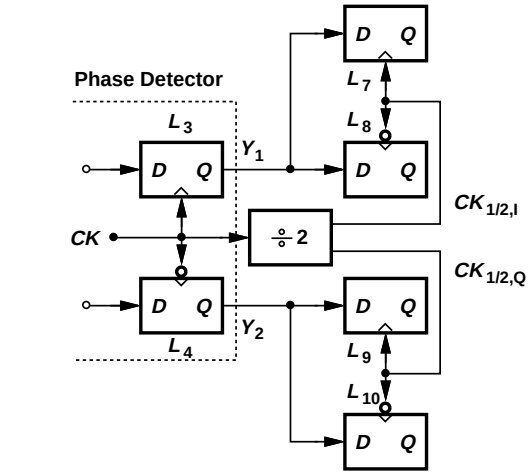


(a)

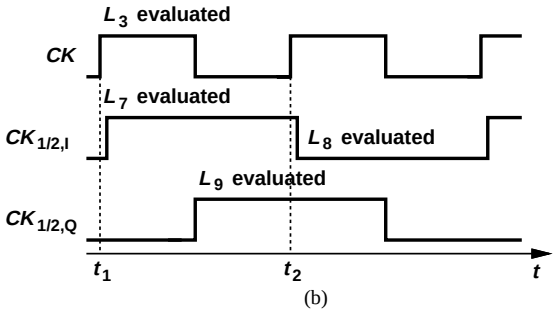


(b)

Fig. 9. PD using charge-steering latches, (b) simulated input-output characteristic.



(a)



(b)

Fig. 10. DMUX realization.

at $t = t_2$, L_3 enters the evaluation mode again and so does L_8.

The bottom DMUX path consisting of L_9 and L_{10} operates in a similar manner but with $CK_{1/2,Q}$. The four latches consume 183 μW at 6.25 GHz. According to simulations, for a given power consumption, charge-steering latches running at 6.25 GHz still outperform rail-to-rail logic in terms of the output ISI.

C. RZ-NRZ Conversion

The low-swing RZ waveforms produced by charge-steering circuits can be converted to NRZ data by means of a rail-to-rail RS latch. However, the amplification of the RZ waveform to achieve rail-to-rail swings demands substantial power. A more efficient approach incorporates a clocked dynamic comparator for amplification [1]. Exemplified by the StrongArm topology, such a comparator too produces RZ outputs when it is reset and hence resembles the dynamic circuit in Fig. 3(a). If cascaded with a charge-steering latch, the comparator thus suffers from the race condition described for the flipflop in Fig. 7(a). Since the demultiplexed data is now available at the quarter rate, we may reconsider the scenario in Fig. 7(b) and utilize the quadrature phases of the quarter-rate (6.25-GHz) clock.

Figure 11 depicts the DMUX/RZ-NRZ conversion chain.

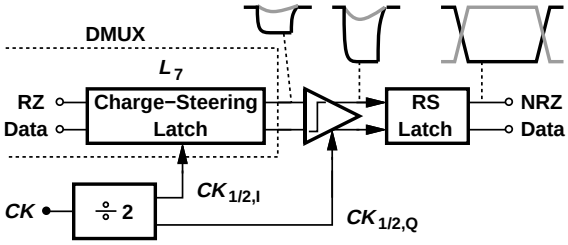


Fig. 11. RZ-to-NRZ conversion.

As mentioned earlier, L_7 is driven by $CK_{1/2,I}$. We choose $CK_{1/2,Q}$ to clock the comparator, applying the result to a CMOS RS latch. The comparator and the RS latch draw 130 μW at 6.25 GHz, far less than typical CML-CMOS converters do.

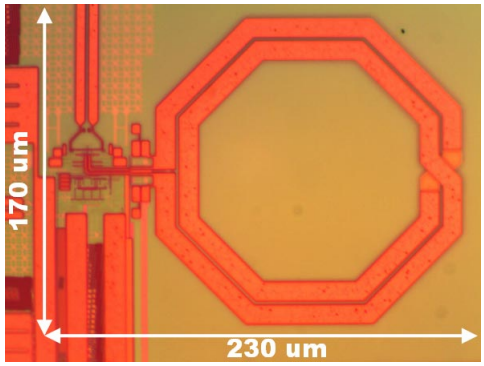
D. Clock Generation and Distribution

As pointed out in Section II, charge-steering circuits dictate rail-to-rail clock swings, a condition afforded by LC oscillators. However, the important question is whether the VCO should drive the latches, the frequency divider(s), and the wiring capacitance directly or through a buffer. The total load capacitance presented by this network is about 270 fF in our work, demanding a power of $2 \times fCV_{DD}^2 \approx 8$ mW if two inverters follow the differential VCO outputs. It is therefore beneficial to omit the buffers and absorb this capacitance in the VCO tank even at the cost of a lower tank inductance and hence a greater bias current. In this case, the higher VCO power dissipation also translates to a lower phase noise.

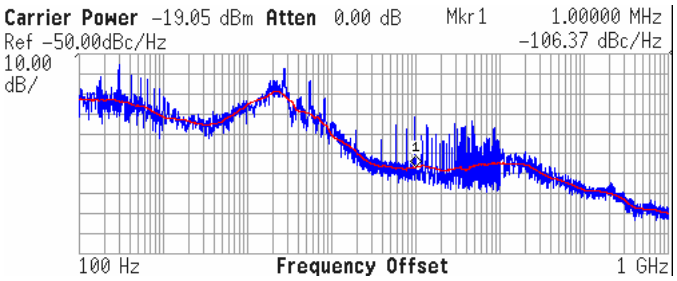
The critical point here is that a given power budget is more efficiently utilized in a VCO than in buffers, suggesting that buffers are generally redundant [1]! One exception is a case where the loss associated with the interconnects significantly lowers the VCO tank Q.

E. Experimental Results

A 5-mW 25-Gb/s CDR/deserializer using an LC VCO has been fabricated in 65-nm CMOS technology. The die photograph is shown in Fig. 12(a), the recovered clock phase noise in Fig. 12(b), and the jitter tolerance for two different supply voltages in Fig. 12(c) [1]. Exhibiting an rms jitter of 1.52 ps with a $2^{15} - 1$ PRBS, the prototype consumes about a factor of 20 less power than the prior art [5, 6] and demonstrates the advantages of charge steering.



(a)



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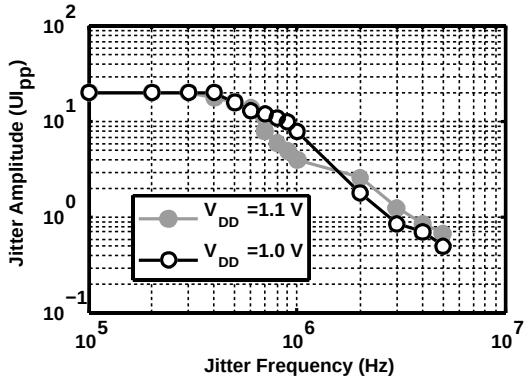

(c)

Fig. 12. CDR/deserializer's (a) die photo, (b) recovered clock phase noise, and (c) jitter tolerance.

V. Charge-Steering ADCs

A. Charge-Steering Op Amps

A practical one-stage charge-steering amplifier can achieve a gain of 2 to 4, pointing to a two-stage configuration if a gain commensurate with pipelined ADC design is desired. Figure

13(a) shows a basic topology, where the tail capacitors are

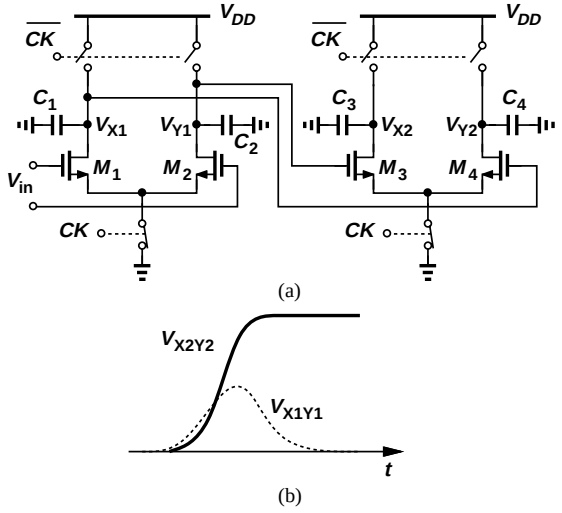

Fig. 13. (a) Charge-steering op amp, and (b) its waveforms.

removed to allow a large amount of charge to flow.[2] Here, the two stages simultaneously amplify until the outputs of the first stage collapse and the second stage turns off. During this transient, V_{X1Y1} rises to a peak and falls back to zero whereas V_{X2Y2} monotonically increases to an amplified copy of the input [Fig. 13(b)]. This two-stage design can provide an open-loop gain of about 10. The values of C_1-C_4 are dictated by kT/C noise requirements.

The charge-steering op amp exhibits a unique behavior in a closed-loop configuration [2] such as the multiplying digital-to-analog converter (MDAC) of Fig. 14(a). Owing to the large load capacitors and the absence of load resistors, each stage behaves as an integrator, incurring loss only due to the output resistance of the transistors. Simplified as shown in Fig. 14(b), the two-integrator feedback loop thus produces an underdamped output that is frozen when the second stage turns off at $t = t_1$ [Fig. 14(c)]. As a result of this overshoot, the closed-loop gain can be *greater* than C_{in}/C_F.

It is possible to design the first stage such that its CM level falls to one threshold above ground by the time V_{out} reaches its peak value at t_p. Freezing the output in its zero-slope regime, such a choice minimizes PVT-induced variations in the final value of V_{out}.

The gain, noise, speed, power dissipation, and linearity of the above op amp can be compared with those of continuous-time topologies. In a pipelined ADC environment, the MDAC stage depicted in Fig. 14(a) exercises all of these properties. We design the op amp of Fig. 13(a) as well as the two configurations shown in Fig. 15 for C_{in} = 480 fF, C_F = 240 fF, C_L = 250 fF, V_{DD} = 1 V, a differential output swing of 0.6 V_{pp}, an open-loop gain of 10, a power dissipation of 2.5 mW, and a clock rate of 1 GHz. The simulated settling time, distortion, and input-referred noise of the MDAC are

[2]Although not identified as a charge-steering op amp, a similar topology without explicit load capacitors has been used in [7] for 6-bit resolution.

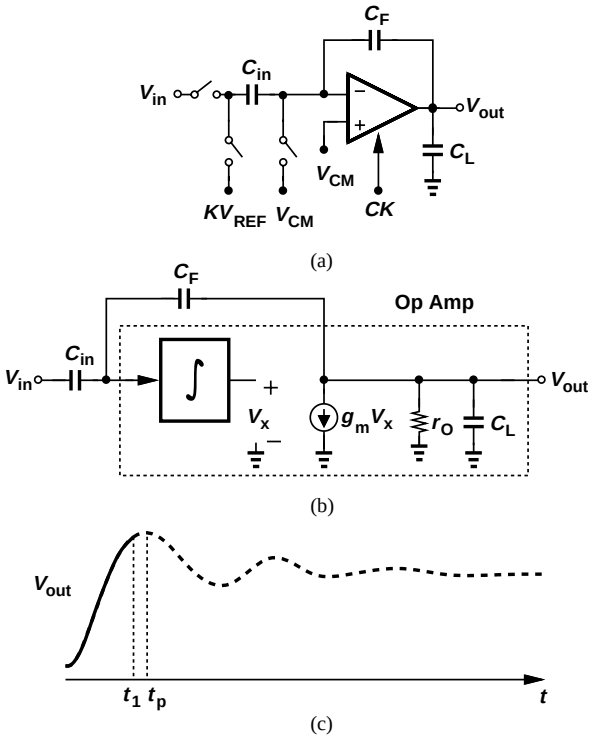

Fig. 14. (a) MDAC environment for charge-steering op amp, (b) simplified closed-loop model, (b) self-timed underdamped behavior.

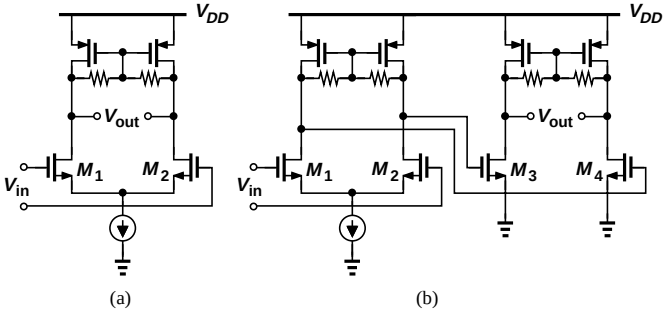

Fig. 15. One-stage and two-stage op amps studied for quantitative comparisons.

listed in Table 1, revealing the "best of all worlds" for the charge-steering topology.

	One−Stage Op Amp	Two−Stage Op Amp	Charge−St. Op Amp
Settling Time	560 ps	370 ps	80 ps
SDR	48 dB	53 dB	54 dB
Input−Ref. Noise	67 nV^2	138 nV^2	65 nV^2

Table 1. Simulated performance of MDAC using each op amp topology.

The results depicted in Table 1 imply that, due to their low open-loop gain, charge-steering op amps do not provide adequate linearity for a 10-bit ADC, dictating nonlinearity

(and gain error) calibration. For example, an accurate on-chip ladder can be utilized to calibrate the ADC in the digital domain by means of an LMS machine [8]. However, the characteristics of these op amps are somewhat sensitive to the input and output CM levels. In particular, if the output CM level, $V_{out,CM}$, shifts from its optimum value by more than 100 mV, the open-loop linearity degrades, making calibration difficult.

It is difficult to apply CM feedback to charge-steering op amps in the analog domain because the output CM level reaches its final value *after* the stages have turned off. Alternatively, the optimum value of $V_{out,CM}$ can be viewed as that which maximizes the MDAC linearity. That is, during calibration, the LMS machine can adjust $V_{out,CM}$ along with the digital coefficients so as to minimize the nonlinearity [2]. Illustrated in Fig. 16, this approach tunes $V_{out,CM}$ in discrete

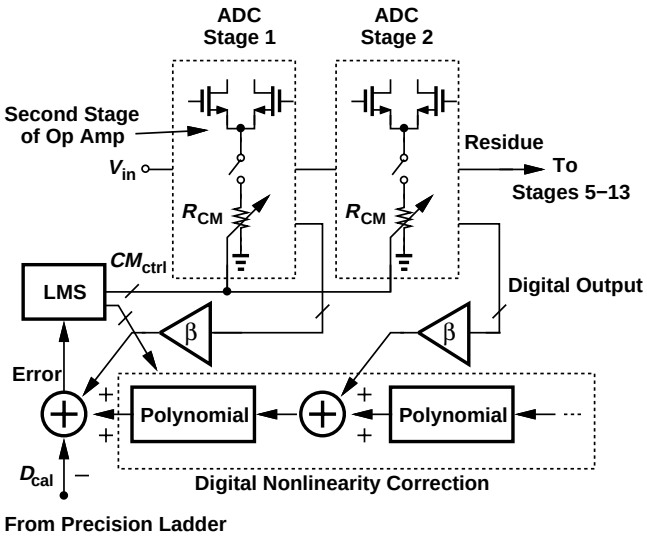

Fig. 16. Common-mode control by LMS machine.

steps by controlling the tail resistance, R_{CM}, in the second stage of each op amp.

B. Three-Stage Op Amps

The "self-timed" nature of charge-steering op amps suggests that more than two stages can be cascaded so as to increase the open-loop gain. Consider the arrangement shown in Fig. 17(a), where the outputs of the first and second stages collapse to zero at about the same time, allowing the third stage to maintain an amplified output. According to simulations, this circuit can achieve a gain of 20.

To study the circuit's behavior in a closed-loop configuration, we approximate the transfer function of each lossy integrator by $A_0/(1+s/\omega_0)$, where $A_0 = g_m r_O$ and $\omega_0 = g_m/C_D$. [The load capacitors, C_D's, are not shown in Fig. 17(a) for simplicity.] With unity-gain negative feedback, the

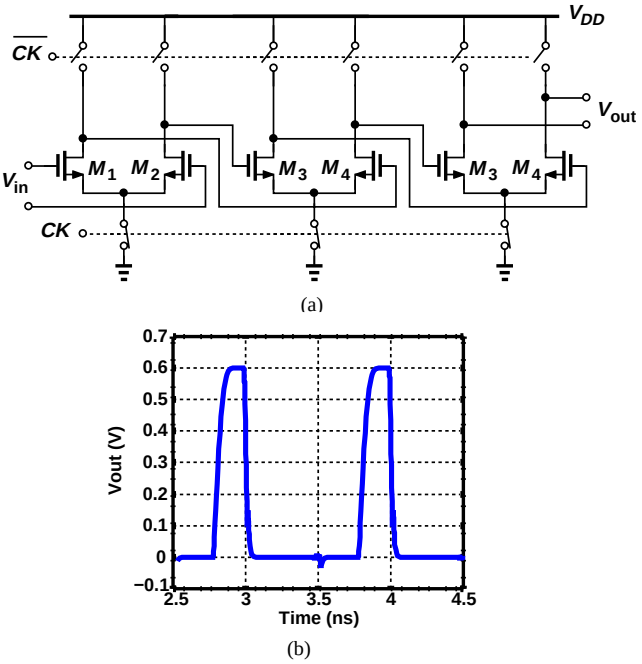

Fig. 17. (a) Three-stage charge-steering op amp, and (b) its response in an MDAC environment.

closed-loop transfer function is given by

$$H(s) = \frac{\frac{A_0^3}{(1+\frac{s}{\omega_0})^3}}{1+\frac{A_0^3}{(1+\frac{s}{\omega_0})^3}}, \tag{6}$$

and the poles are computed from

$$(1+\frac{s}{\omega_0})^3 + A_0^3 = 0. \tag{7}$$

The loop contains one real pole located at $-(A_0+1)\omega_0$ and two complex poles at $(A_0/2-1)\omega_0 \pm j(\sqrt{3}/2)A_0\omega_0$, which for $A_0 > 2$, fall in the right half plane and yield a growing sinusoid - just as in a three-stage ring oscillator. However, the last two stages turn off after a brief period of time, stopping the growth and producing an amplified output. Figure 17(b) plots the simulated step response of the three-stage op amp in the MDAC environment of Fig. 14(a), revealing a settling time of about 70 ps.

The foregoing study indicates that the design of charge-steering op amps markedly departs from the conventional wisdom. The closed-loop circuit is allowed to be unstable so long as the stages turn off before or at the (first) peak value of the output. It is conceivable that a larger number of stages can also be used to further increase the gain.

C. Experimental Results

A 10-bit 800-MHz pipelined ADC using two-stage charge-steering op amps has been designed and fabricated in 65-nm CMOS technology [2]. Figure 18(a) shows the die photograph

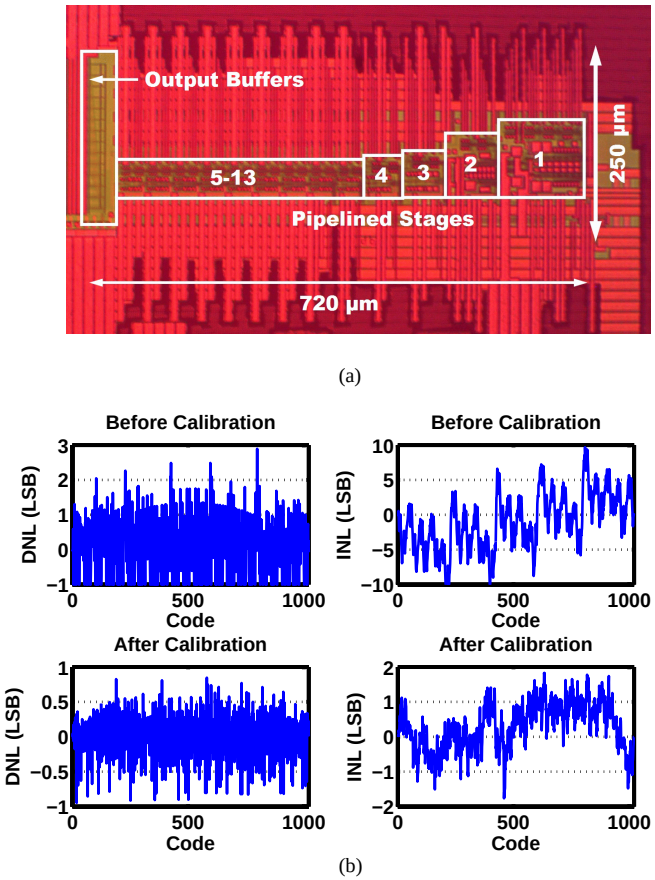

Fig. 18. (a) ADC die photograph, (b) measured DNL and INL before and after calibration.

and Fig. 18(b) the DNL and INL before and after calibration. Figure 19 plots the SNDR as a function of the input frequency,

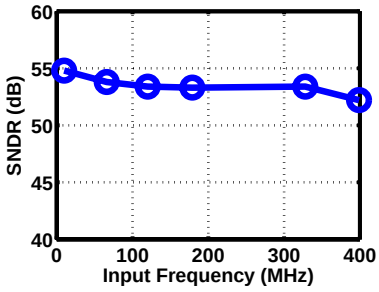

Fig. 19. Measured SNDR of the ADC at a sampling rate of 800 MHz.

exhibiting a value of 52.2 dB at Nyquist rate. The ADC draws 19 mW from a 1-V supply and provides an FOM of 53 fJ per conversion step.

VI. Conclusion

Charge steering holds promise for high-speed analog and mixed-signal circuits with low power consumption. The discrete-time nature of this design technique enables digital latching as well as muti-stage, nominally unstable op amps to perform in complex circuits. Issues associated with this design paradigm have been discussed and solutions have been proposed. Providing a fourfold power advantage over CML circuits, charge steering has been exploited in a 25-Gb/s CDR/deserializer dissipating 5 mW and a 10-bit 800-MHz ADC consuming 19 mW.

Acknowledgments

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