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R. C. Jeff, Minseong Yun, Balavinayagam Ramalingam, Bongmook Lee ...+3 more authors

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Reginald Jeff
University of Missouri

M Yun
University of Missouri

B Ramalingam
North Carolina State University

See next page for additional authors

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Charge storage characteristics of ultra-small Pt nanoparticle embedded GaAs based non-volatile memory

R. C. Jeff, Jr.,[1] M. Yun,[1] B. Ramalingam,[1] B. Lee,[2] V. Misra,[2] G. Triplett,[1,a)] and S. Gangopadhyay[1,b)]
[1]*Department of Electrical and Computer Engineering, University of Missouri, Columbia, Missouri 65211, USA*
[2]*Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695, USA*

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Charge storage characteristics of ultra-small Pt nanoparticle embedded devices were characterized by capacitance-voltage measurements. A unique tilt target sputtering configuration was employed to produce highly homogenous nanoparticle arrays. Pt nanoparticle devices with sizes ranging from ~0.7 to 1.34 nm and particle densities of $\sim 3.3–5.9 \times 10^{12}$ cm^{-2} were embedded between atomic layer deposited and e-beam evaporated tunneling and blocking Al_2O_3 layers. These GaAs-based non-volatile memory devices demonstrate maximum memory windows equivalent to 6.5 V. Retention characteristics show that over 80% charged electrons were retained after 10^5 s, which is promising for device applications. © *2011 American Institute of Physics*. [doi:10.1063/1.3625426]

Si-based floating gate non-volatile memories[1] have experienced significant growth in mobile data storage applications. Even more, discrete nanocrystal/nanoparticle (metal) embedded devices are also attractive because of the lateral isolation of each storage site. Sub-2 nm platinum (Pt) nanoparticle embedded non-volatile memory devices with controllable (1–4.3 V) memory windows under low programming/erasing (P/E) voltages[2] were recently reported where nanoparticles smaller than 2 nm demonstrate Coulomb blockade effect.[3] In this study, we explore ultra-small Pt nanoparticle embedded GaAs metal-oxide-semiconductor (MOS) structures for operation at room temperature.

Replacing Si with GaAs offers unique performance capabilities, particularly for memory devices.[4] The charging effect, however, influences carrier leakage through the Al_2O_3 and is sensitive to temperature (due to thermal excitation).[5] For GaAs memory devices, several issues include: (i) deposition of dielectric layers onto the GaAs surface and Fermi level pinning from high density surface states[6] and (ii) difficulty with producing high quality oxide/GaAs interfaces to allow controlled charge transfer, which is associated with native/deposited oxides at the GaAs surface.[7–9] Appropriately, efforts have included surface passivation and interfacial cleaning techniques to perfect the interface.[10–13] Atomic layer deposition (ALD) has also been employed to synthesize high-quality gate dielectrics onto GaAs and has shown suppressed interface trap densities with proper post-deposition annealing.[14] Here, we report charge storage characteristics of GaAs MOS structures with high-density ultra-small Pt nanoparticles between ALD tunneling and e-beam evaporated blocking Al_2O_3 layers. The nanoparticle formation utilizes a unique tilted-target sputter (TTS) configuration producing low density and low energy metal atoms, from which highly homogenous Pt nanoparticles in the sub-2 nm range are observed. In TTS configuration, dimensions of Pt nanoparticles can be controlled by varying deposition time and power. Room temperature capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) measurements show memory effects due to electron charging via Pt nanoparticles, which is in contrast to observations attributed to trapped sites between Al_2O_3 and GaAs.

In this study, memory devices were fabricated using p-type GaAs (100) substrates. Fabrication steps include: wafer degreasing, wafer cleaning in HCl:H_2O (1:5), sulfur passivation in NH_4S_2 (40%–48% by weight in H_2O) at room temperature, 3 nm thick ALD deposited Al_2O_3 tunnel dielectric at 200 °C, post-deposition annealing using rapid thermal annealing in N_2 at 400 °C, and Pt nanoparticle deposition using TTS configuration. With TTS configured at 23.8° angle, deposition time and power were varied producing nanoparticle arrays with sizes ~0.7-1.34 nm and densities $3.3–5.9 \times 10^{12}$ cm^{-2}. Twenty nanometer thickAl_2O_3 blocking layers were then deposited by e-beam evaporation, and H_2 annealed at 260 °C. Ti electrodes were then patterned using a shadow mask.

Pt nanoparticles were also deposited on Al_2O_3 (5 nm) coated carbon grids for transmission electron microscopic (TEM) imaging (Figure 1). Nearly homogeneous particle arrays were obtained unlike that observed in other dewetting techniques.[15,16] Particle size homogeneity can be attributed to shadowing effect caused by the angular flux and low energy metal atoms in the deposition regime for particle formation.

C-V measurements were executed under dark conditions with a voltage step of 0.1 V and a 30 mV ac signal at frequencies varying from 10 kHz to 1 MHz. Figure 2 shows the frequency dependent C-V curves of the control sample and the Pt nanoparticle embedded memory devices. This data are evident that the memory window was independent of frequency from 10 kHz to 1 MHz, indicating that the obtained charging effect originates from Pt nanoparticles, not the trapped states in Al_2O_3 or Al_2O_3/GaAs interfaces. Figure 3 shows *C-V* curves of the control sample and the Pt

a)Electronic mail: triplettg@missouri.edu.
b)Electronic mail: gangopadhyays@missouri.edu.

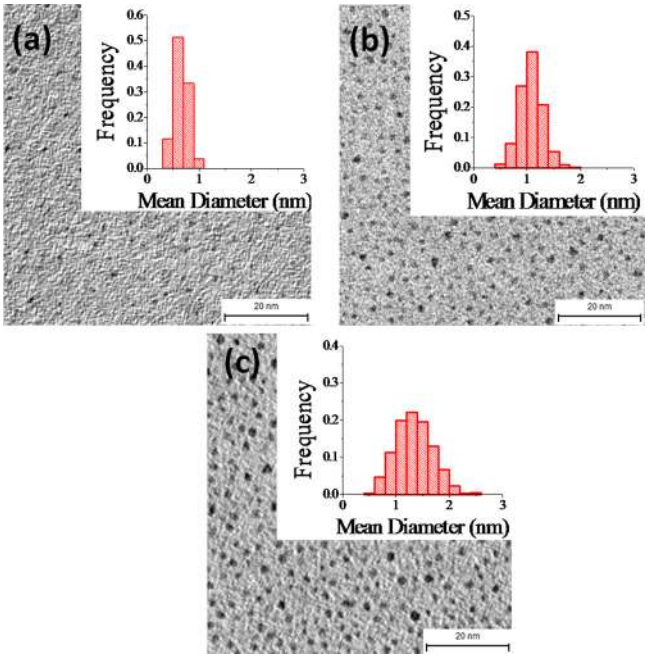

FIG. 1. (Color online) TEM images and particle size distribution (inset) (a) ~0.696 nm nanoparticles, (b) ~1.08 nm nanoparticles, (c) ~1.34 nm nanoparticles.

nanoparticle embedded memory device under various sweeping gate voltages. Samples did not reach saturation in the accumulation region because of quantum mechanical tunneling from the ultra-thin tunneling layer.[17] The control sample shows an approximate initial flatband voltage, $V_{FB} = -4$ V (and ~0.5 V negligible hysteresis), which is attributed to traps developed during fabrication of the two Al_2O_3 layers. V_{FB} for the smallest nanoparticles varied with voltage sweep (Figure 3(b)), but for the purpose of measuring flatband shifting (ΔV_{FB}), V_{FB} was assumed to be -1.8 V at ± 2 V. Counterclockwise hysteresis loops shown to indicate electron injection under positive voltage for P-modes and hole injection under negative voltage for E-modes. Unlike 3–4 nm AuPd nanoparticle embedded metal-insulator-semiconductor field-effect transistors (MISFETs),[10] charge storage was demonstrated at room temperature due to high quality Al_2O_3 tunneling layer and ultra-small particles.

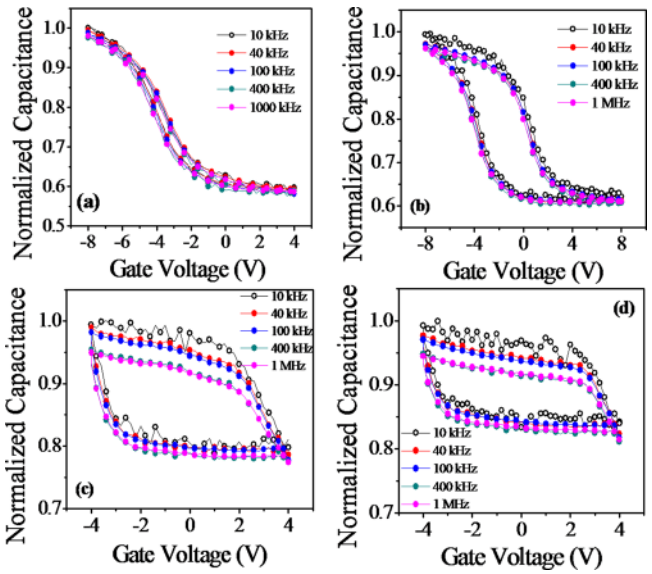

FIG. 2. (Color online) Normalized frequency dependent C-V curves of (a) control, (b) ~0.696 nm nanoparticles, (c) ~1.08 nmnanoparticles, (d) ~1.34 nm at frequencies 10 kHz to 1 MHz.

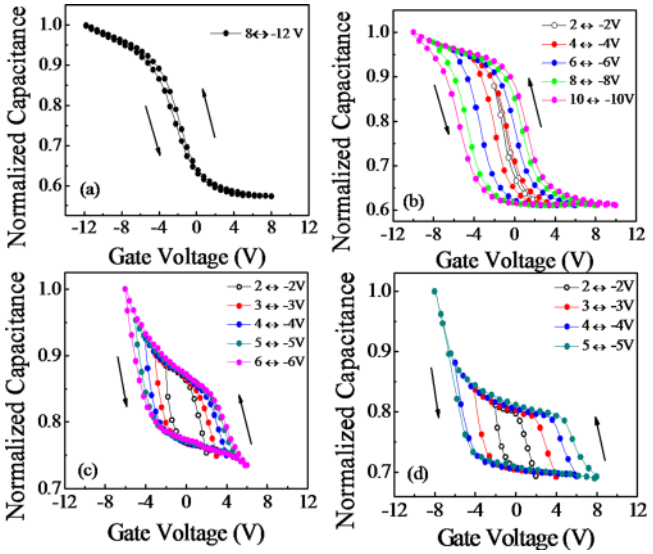

FIG. 3. (Color online) Normalized C-V curves of (a) control, (b) ~0.696 nm nanoparticles, (c) ~1.08 nmnanoparticles, (d) ~1.34 nm nanoparticles samples under different sweeping gate voltages.

Memory devices (~1.08 nm and ~1.34 nm particle arrays) exhibited adverse initial charging effects, as shown in Figures 3(c) and 3(d). This demonstrates that larger particles produce initial charging due to weaker Coulomb blockade effect. Using an approximation for the self-capacitance (C) of a single nanoparticle, Coulomb charging energies, $q^2/2C$ (where C is the self-capacitance[18]), were calculated and ranged from ~170-320 meV.

Although the Coulomb charging energies for all samples are above kT (25 meV), very thin tunnel layers increase leakage, thus requiring larger Coulomb blockade effect to confine charges. Figure 4 illustrates C-V and G-V curves for smaller nanoparticles at ± 10 V voltage sweep. Here, the conductance peaks are positioned close to V_{FB} in both forward/reverse directions. The hysteresis characteristics observed can be attributed to electrons trapped in or at the interface of the embedded Pt-nanoparticle.[19]

The change in ΔV_{FB} was also calculated, where ΔV_{FB} increased under both the P/E directions due to an increase in

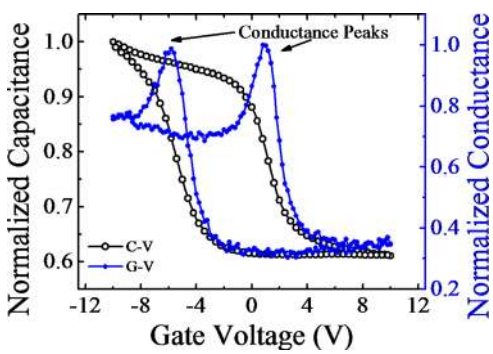

FIG. 4. (Color online) C-V versus G-V curves for ~0.696 size nanoparticles (±10 V bi-direction sweep).

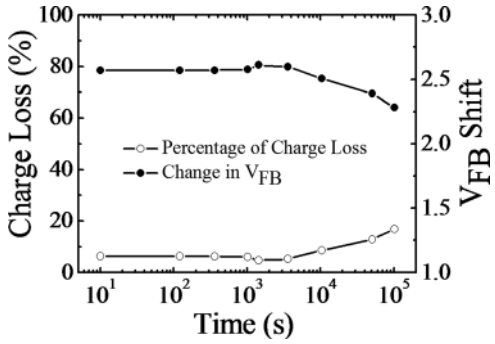

FIG. 5. Retention characteristics of the Pt nanoparticle embedded GaAs memory device.

Pt nanoparticle stored charges. The forward/reverse *C-V* sweeps also revealed that the maximum magnitude of charge storage effect was 6.5 V. Using the relationship, $N = \frac{C_{ox}\Delta V_{FB}}{qA}$, where N is the trapped charge density, C_{ox} is the accumulation capacitance, and A is device area, the maximum electron charge density ($\sim 6.75 \times 10^{12}$ cm^{-2}) and particle density ($\sim 3.294 \times 10^{12}$ cm^{-2}) was determined revealing that approximately two electrons are stored in or at the interface of a single Pt nanoparticle. The initial stressing for retention measurements confirms that electrons have been trapped in Pt nanoparticles. An initial loss of 6.3% was demonstrated after 10 s (due to back electron tunneling), and as illustrated in Figure 5, charge losses up to 16.8% of the initial charge values were observed after 10^5 s, which demonstrates the feasibility of these structures in non-volatile memory.

In summary, near homogenous ultra-small Pt nanoparticles between ALD and e-beam deposited Al_2O_3 layers in GaAs MOS structures revealed a charge storage effect with a maximum flatband voltage shift of 6.5 V. Test structures demonstrated ~83% retention after 10^5 s. These dielectric layers together with the use of ultra-small Pt nanoparticle could lead to room temperature operation of GaAs non-volatile memory applications.

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