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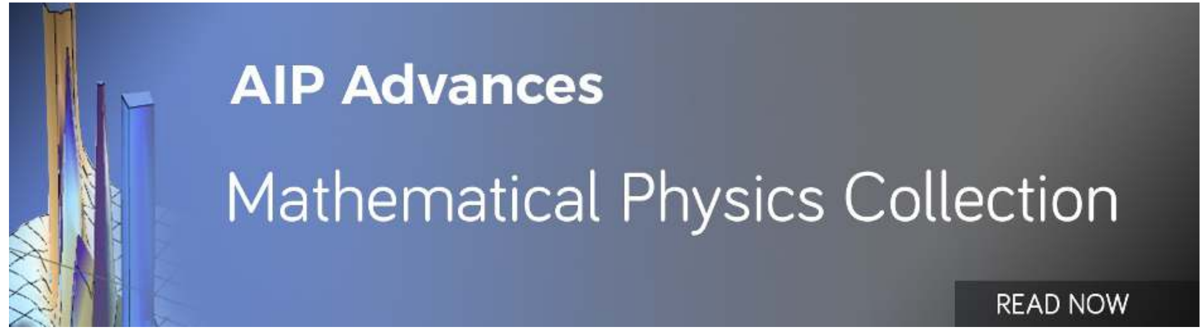

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Hassan Ul Huzaibi,[1,2,3,a)] Xuewen Shi,[1,2,3,a)] Di Geng,[1,2,3] Nianduan Lu,[1,2,3,b)] Ling Li,[1,2,3,c)] and Ming Liu[1,2,3]

AFFILIATIONS

[1] Key Laboratory of Microelectronics Device & Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China
[2] University of Chinese Academy of Sciences, Beijing 100049, China
[3] Jiangsu National Synergetic Innovation Center for Advanced Materials (SICAM), Nanjing 210009, China

[a)] Hassan Ul Huzaibi and Xuewen Shi contributed equally to this work.
[b)] **Electronic mail address:** lunianduan@ime.ac.cn
[c)] **Electronic mail address:** lingli@ime.ac.cn

ABSTRACT

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) are recently used in many display applications due to its high mobility and high stability. However, its processing at low temperature causes defects which affect charge carrier mobility. So, it is essential to completely understand the effects of defects on charge transport mechanism. In this paper, experimental results are presented to investigate the charge carrier mobility of LTPS device. Furthermore, based on the theoretical model, the charge transport characteristic for LTPS has been interpreted. Our results show that, at low gate voltage, the charge transport of LTPS TFT displays multiple trapping and release mechanism, while free charge carrier transport mechanism at high gate voltage.

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I. INTRODUCTION

In last decade, thin-film transistors (TFTs) have grown into a huge industry due to their broad applications such as large area electronics, active-matrix display industry, radio frequency identification tags (RFID) and logical applications.[1] High-resolution displays constructed using the TFT technology are particularly useful in combination with other display technologies such as organic light-emitting diodes, electronic papers, liquid crystal displays and other flat panel displays.[2–5] In recent years, active matrix organic light-emitting diode (AMOLED) has attracted much attention because of its fast response time, low driving voltage, no requirement of backlight and large possible angle to view display.[6] Low-temperature polycrystalline silicon (LTPS) is preferred for AMOLED as compared to amorphous Si TFTs because LTPS is more stable and have higher mobility as compared to amorphous Si.[7,8] As compared with amorphous Si TFTs, LTPS TFTs have practical advantages of higher speed images, brightness and resolution over Si TFTs due to advantage of increased charge carrier mobility.

To optimize the performance of polycrystalline silicon, a complete understanding of the transport properties for poly crystalline silicon films is indispensable. Based on the transport properties, effect of trap states on field effect mobility for large grain poly silicon films has also been explained.[9,10] Later on, charge transport in poly-Si thin-film was investigated in more depth with respect to deposition temperature, the amorphous material and the used substrate.[11] Charge transport mechanism of the polycrystalline silicon has been discussed at low deposition temperature previously. However, the influence on mobility of LPTS is still ambiguous at low deposition temperature under various temperatures after construction of device.

In case of LTPS, several investigations have been reported to improve the mobility on the basis of developments in processing techniques of TFTs.[12–14] Variations in performance of bias stressed LTPS fabricated on metal foil substrate has been studied.[15] Bridged-grain (BG) technique was also introduced to improve the charge transport and also render the cost in LTPS.[16] Although these current processing techniques have been presented on developing LTPS, the

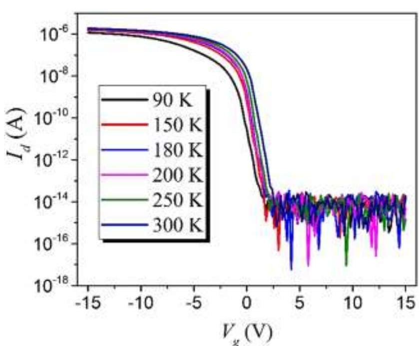

FIG. 1. Vg dependent Id at Vd=-0.1V.

dependency of mobility on gate voltage and temperature for LTPS TFTs is still unavailable. Since the change in temperature and gate voltage in LTPS would remarkably affect the electrical properties of device, the understanding of the charge transport mechanisms for different applied gate voltages and temperatures is crucial not only for the fundamental understanding of the device working but also for improvement in device performance.

In this paper, experiments are observed to study the charge transport mechanism for LTPS TFT. Furthermore, some theoretical models have been proposed to explain the experimental results. Based on the experimental and simulated results, the charge transport mechanism of LTPS TFT has been determined.

II. EXPERIMENTAL METHOD

The sample is from BOE Technology Group Co. And top gate coplanar structure was used in this study. The fabricated process is following. Firstly, 200nm buffer layer consisted of SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) followed by 50nm a-Si:H also deposited by PECVD and crystallized by excimer laser annealing. After defining active island, 120nm SiO_2 gate insulator and 200nm Mo gate metal was deposited by PECVD process and sputtering respectively. Then gate electrode was patterned and low resistance source and drain region was formed by doping. After interlayer dielectric was deposited and contact holes were opened. Finally 200nm Al source and drain metal was sputtered and patterned. Current-voltage (I-V) characteristics of LTPS sample were measured with a Keithley 4200-SCS analyzer. Temperature range for I-V measurement is selected from 90 K to 300 K. Both channel width (W) and channel length (L) are kept at 3 μm. Thickness of oxide layer (t_{ox}) is 120 nm.

The voltage drop from end to end is not equal in the insulator at drain and source of TFT because the voltage distribution in transistor is controlled by two autonomous biases. At each temperature, drain current (I_d) is measured as a function of gate bias (V_g) at fixed drain voltage (V_d) of -0.1 V with the help of equation given below to keep the transfer characteristics in liner region.

$$g_m = \left|\frac{\partial I_d}{\partial V_g}\right|_{V_d=-0.1V} = \frac{W}{L}\mu C_{ox} V_d, \tag{1}$$

here, g_m is the trans-conductance and μ is the mobility of charge carriers. At each temperature, measured transfer characteristics of the LTPS are shown in Fig. 1.

III. RESULTS AND DISCUSSION

The V_g dependent I_d at $V_{d=}$-0.1V for different temperatures has firstly measured, as shown in Fig. 1. One can see that the V_g-I_d keep the transfer characteristics, which is consistent with the reported results in linear region.[17] At each temperature, drain current is measured as a function of voltage bias at fixed drain voltage of -0.1 V to keep the transfer characteristics in linear region. Capacitance at oxide-substrate interface is C_{ox}=2.86×10^{-8} F-cm^{-2}. C_{ox} is measured from equation

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}}, \tag{2}$$

where, ε_{ox} is silicon dioxide permittivity and ε_o is absolute permittivity. By using the value of C_{ox} in equation 1, we can obtain mobility of charge carriers in linear region. To understand the transport mechanism of LPTS device, we then measure the V_g dependence of mobility for different temperatures, as shown in Fig. 2(a). Solid lines in graphs are representing the fitting values while the symbols are representing the experimental values.

In Fig. 2(b), one can see that charge carrier mobility increases with temperature at low gate bias. However, for high gate bias, the charge carrier mobility shows the different trend, that is decreases with temperature. Therefore, the charge transport of LTPS should be various for the low and large gate voltage. Defects can create during processing of LTPS.[18] Several localized states can originate due to

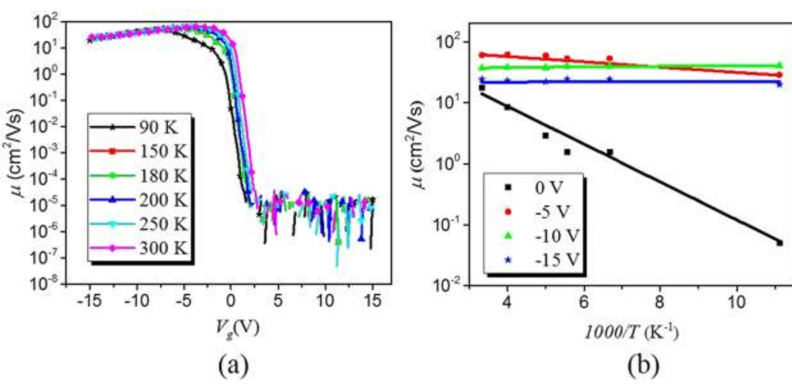

FIG. 2. (a) Vg dependence of mobility for different temperatures. (b) Temperature dependence of mobility for different Vg.

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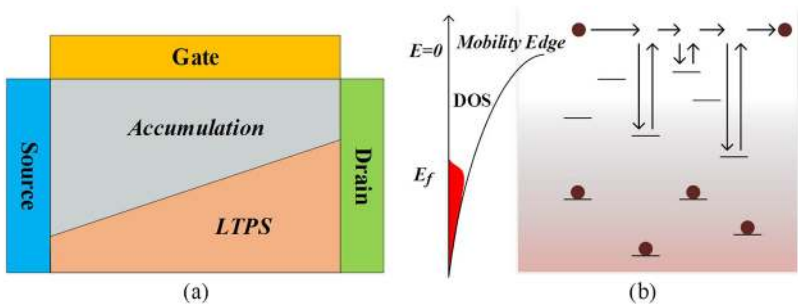

FIG. 3. (a) Geometric definition for LTPS. (b) Schematic view for multiple trapping and release and free carrier transport mechanisms.

these defects. Energy of these localized states is far below the Fermi energy level (E_f). These localized states play a vital role in carrier transport in LTPS TFTs.

Site energy plays an important role and it is affected by the electric field applied that involves the importance of Fermi energy level (E_f) in the charge transport. The charge carrier transport occurs only if a starting site i have a charge carrier while the destination site j is empty. If the sites i and j are far above the Fermi energy level (E_f), both sites will be empty and there is no possibility of charge transfer from one site to another. Contrarily, if the sites i and j are far below the E_f both sites will be occupied so a charge will have no destination site to transfer. Hence, the possibility of charge transport deep below the E_f is also not possible. The frequency at which charge carriers transfer from an occupied site i to an unoccupied site j, is parted by distance r_{ij}, with reference to Fermi energy level, and is expressed by Miller-Abrahams expression[19]

$$\nu_{ij} = \nu_o \exp\left(-\frac{2r_{ij}}{\alpha} - \frac{|E_i - E_j| + |E_i - E_F| + |E_j - E_F|}{2kT}\right), \quad (3)$$

here, α is the localization length, E_i and E_j are the carrier energies on the sites i and j respectively. T is temperature, and k is Boltzmann constant. ν_o is prefactor, termed as attempt to escape frequency, which depends on transport mechanism. According to multiple trapping and release theory (MTR), the carrier transport occurs in extended states while most of the carriers are trapped in localized traps at low gate voltage. An energy difference separates localized state from mobility edge. If the localized state is at less energy difference from mobility edge, it acts as a shallow traps. Merely thermal activation can release the carrier from shallow trap to extended state. However, if the carrier is trapped in deep trap state below the mobility edge, then mere thermal activation cannot release the carrier into the extended state. In such situation, increase in potential can decrease the energy difference between the extended state and localized state. Moreover, at much higher potential, Fermi level can reach beyond the extended state which can keep the carriers in free states. Therefore, for the low gate voltage, the charge transport can be interpreted by multiple trapping and release (MTR). For the high gate voltage, the charge transport can be interpreted by free charge carrier transport mechanism. Fig. 3 illustrates the geometric definition of device structure, basic definition of channel configuration, and schematic of multiple-trapping and release mechanism for LTPS TFT, respectively.

Based on the MTR theory, the mobility can be simply expressed as

$$\mu(T) = \mu_o \exp(-E_a/kT), \quad (4)$$

here, μ_o is prefactor, E_a is activation energy for mobility, k is Boltzmann constant.

According to the free charge carrier transport mechanism, the mobility can be simply expressed as

$$\mu = \mu_o T^{-\gamma}, \quad (5)$$

here, γ is the parameter that indicates the deviation from standard field-effect transistor theory.

To better interpret the charge transport properties of LTPS, we have plotted the simulation results based on MTR and free charge transport theories, as shown in Fig. 2(b). The input fitting parameters are, E_a=0.015 meV and 0.0021 meV, μ_o=150 cm^2/Vs and 85 cm^2/Vs for V_g=0 V and -5 V, respectively. Similarly, input

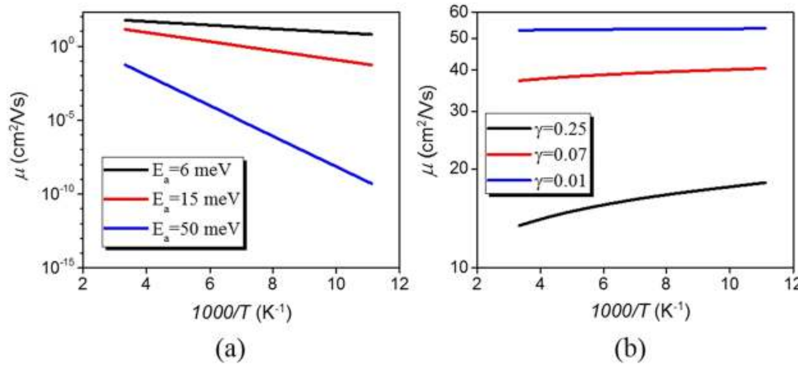

FIG. 4. (a) Mobility dependence on temperature at different deviation prefactor values. (b) Mobility dependence on temperature at different activation energies.

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fitting parameters for V_g=-10 V and -15 V are, γ=0.072 and γ=0.018, μ_o=56 cm^2/Vs and μ_o=24 cm^2/Vs, respectively.

To further understand the effects of variable deviation factor (γ) and activation energy (E_a), dependence of mobility on various temperatures is demonstrated, as shown in Fig. 4. In Fig. 4(a), with increasing the activation energy, the temperature dependence of mobility will be stronger. Increase in activation energy which apparently defines the energy required for the charge carrier to move to extended state, is also increasing. Increase in temperature dependence of mobility required for charge carrier to reach above the mobility edge depending on the activation energy also explains the MTR mechanism at low V_g. On the other hand, with increasing γ, the temperature dependence of mobility will be weak. At high V_g, the charge carriers are in extended state where increase in temperature decreases the mobility.

IV. CONCLUSION

In this paper, the properties of LTPS TFTs from the commercial corporation have been measured. The measured results show that I_d-V_g of LPTS TFTs keeps the transfer characteristics in linear region at each temperature. Otherwise, experimental results are presented to investigate the charge carrier mobility of LTPS device. The results show that for the low gate voltage, the charge transport is attributed to the multiple trapping and release (MTR) mechanism, while free charge carrier transport mechanism for the high gate voltage. Based on MTR and free charge transport mechanism, the charge transport characteristic for LTPS has been interpreted.

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