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Charge transport studies on Si nanopillars for photodetectors fabricated using vapor phase metal-assisted chemical etching

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Abstract Si nanopillars (SiNPLs) were fabricated using a novel vapor phase metal-assisted chemical etching (V-Mace) and nanosphere lithography. The temperature dependent current–voltage (*I*–*V*) characteristics have been studied over a broad temperature range 170–360 K. The SiNPLs show a Schottky diode-like behavior at a temperature below 300 K and the rectification (about two orders of magnitude) is more prominent at temperature < 210 K. The electrical properties are discussed in detail using Cheung's and Norde methods, and the Schottky diode parameters, such as barrier height, ideality factor, series resistance, are carefully figured out and compared with different methods. Moreover, the light sensitivity of the SiNPLs has been studied using *I*–*V* characteristics in dark and under the illumination of white light and UV light. The SiNPLs show fast response to the white light and UV light (response time of 0.18 and 0.26 s) under reverse bias condition and the mechanism explained using band diagram. The ratio of photo-to-dark current shows a peak value of 9.8 and 6.9 for white light and UV light, respectively. The Si nanopillars exhibit reflectance < 4% over the wavelength region 250–800 nm with a minimum reflectance of 2.13% for the optimized sample. The superior light absorption of the SiNPLs induced fast response in the *I*–*V* characteristics under UV light and white light. The work function of the SiNPLs in dark and under illumination has been also studied using Kelvin probe to confirm the light sensitivity.

1 Introduction

One dimensional semiconductor nanostructures including nanopillars, nanowires, nanotubes, nanorods have emerged as one of the most promising materials for the applications in various fields such as optoelectronics, nanoelectronics, energy storage, chemical and biosensors [1–4]. Specifically, the nanopillar- or nanowire-based devices are precisely adapted for electronic and photonic applications due to their enhanced subwavelength optical coupling, ability to integrate with electronic devices, very high surface-to-volume ratio, etc. [5–7]. Various substrates, such as single crystalline semiconductor wafers, glass, metal foils, quartz, have been used for nanowire-based devices in variety of ways. Chueh et al. have reported Ge nanoneedles grown on low temperature substrates such as plastic and rubber [8–10]. An UV–visible photodetector with high responsivity using GaN nanowires on Si substrates was demonstrated by Bugallo et al. GaInAs/InP nanopillar arrays have been utilized by Gin et al. for the infrared photodetectors along with theoretical investigation [11]. Among the semiconductor nanowire devices, the electronic and photonic applications of Si nanowires/pillars are particularly important due to their properties such as the ability of miniaturization in microelectronics, compatibility with currently existing semiconductor technology and enhanced light matter interaction [12–14].

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Recently, Grego et al. have reported waveguide integrated photodetectors based on Si nanowires. These types of structures can act as a building block for the CMOS compatible chip because of their waveguiding and light detection properties [15]. The Si nanowires/pillars play a dominant role in developing Si based technology due to their enhanced light absorption and emission characteristics, which arise from the manipulation of Si into nanostructures [16]. These Si nanopillars-based devices outperform the other compound semiconductors because of the evolution of Si technology in device processing, packaging, quality control, etc. [13, 14, 17]. These subwavelength structures on the Si substrate can reduce the very high reflectance of bulk Si in the visible region. Other materials such as II–VI and III–V compound semiconductors also have applications in the optoelectronic industry [3, 18–20]. However, these materials are still under research since they are not established for practical applications. Further, one of the disadvantages of these materials is the low absorption coefficient in the visible region, which hinders the application in solar cell. Studies about electrical properties of Si nanopillars have gained a lot of research attention since the Si nanostructure-based heterojunctions such as Si/graphene and Si/MoS_2 are reported for photodetectors and photovoltaic applications [21–24].

The fabrication of Si nanopillars (SiNPLs) includes different methods such as chemical vapor deposition, electrochemical etching, vapor–liquid–solid growth, dry etching and metal-assisted chemical etching [25–28]. Out of various fabrication methods, metal-assisted chemical etching is the most commonly used, simple and low cost technique for the fabrication of SiNPLs [29–31]. However, H_2 gas bubbles generated during liquid phase metal-assisted chemical etching process (L-Mace) can produce local differences in the etching rate, which leads to non-uniformly etched surfaces [32]. Another difficulty is the fluid flow, which alters the catalyst morphology during the metal-assisted chemical etching. Recently, Hildreth and Schmidt [32] have reported vapor phase metal-assisted chemical etching (V-Mace) that overcomes all the above mentioned difficulties. The V-Mace provides many advantages over the L-Mace to control the nanostructure effectively during the growth process [32–34]. The process parameters such as substrate temperature, temperature of the etchant, distance between the etchant and substrate can be varied to get the nanostructure in a controlled manner. The substrate temperature is used to adjust the adsorption/desorption rate of the etchant vapors on the substrate. Since the V-Mace is completely a dry process, the gaseous by-products formed during the etching diffuse out from the substrate [32]. This ensures uniform etching throughout the Si surfaces. Moreover, catalyst morphology remains unaltered in V-Mace as there is no direct contact between the substrate and etchant. Nanosphere lithography is one of the most effective tools that can be used with the V-Mace to produce the Si nanostructures with controlled size and periodicity [35, 36].

Herein, for the first time, we report the fabrication of SiNPLs utilizing V-Mace and nanosphere lithography. The temperature-dependent current–voltage (*I–V*) characteristics have been discussed over a wide range of temperature 170–360 K. The SiNPLs exhibit Schottky diode-like behavior especially at temperature < 210 K. The temperature-dependent Schottky diode parameters such as barrier height, ideality factor and series resistance were calculated using Cheung's and Norde methods. Moreover, the SiNPLs exhibit ultra-low reflectance in the visible region with a minimum reflectance of 2.2%. This superior light absorption leads to the very good sensitivity of light and the sensitivity is more prominent under reverse bias. The mechanism behind the optical sensing properties is explained using the energy band diagram.

2 Experimental details

Si wafer with (100) orientation was ultrasonicated with isopropyl alcohol (IPA) followed by acetone for 15 min each to remove the contamination. The wafers were treated with boiling piranha (4:1 (v/v) H_2SO_4:H_2O_2) and RCA solution (1:1:5(v/v/v) NH_4OH:H_2O_2:H_2O) at 80 °C for 1 h. Polystyrene nanosphere lithography was used to get a nanoporous gold template on the Si wafers. PS spheres of diameter 90 nm, as 10% by weight in solution, were used in this fabrication process. The PS nanospheres were diluted in ethanol by volume ratio 1:1 and a volume of 20 µL was dropped on the Si substrates placed on a spin coater. Spin coating of PS nanosphere has been conducted in three steps: (1) 200 rpm for 20 s, (2) 1000 rpm for 20 s and (3) 8000 rpm for 60 s. To reduce the size and increase the separation between the PS spheres, O_2 plasma etching was performed using magnetron sputtering system. The gold film is deposited with an optimum chamber pressure of 5.1×10^{-3} mbar and target power density of 0.58 W/cm^2 for 10 s. The PS spheres were then removed by sonication in dichloromethane. Si substrate with porous Au film was loaded in an etching set up for vapor phase metal-assisted chemical etching (V-Mace), as shown in Supplementary Fig. S1. An optimum temperature of 45 °C was used to control the adsorption and desorption rate of the etchant vapors on the substrate.

The etching solution contains HF (40%), H_2O_2 (30%) and ethanol with volume ratio 3:1:1. The etchant vapors from the etching solution were transferred to the substrate and it got adsorbed on the substrate surface in a condensed form. The schematic diagram showing the mechanism of vapor phase etching is illustrated in Fig. 1. The etching mechanism of V-Mace can be written as:

At the cathode (on the metal surface),

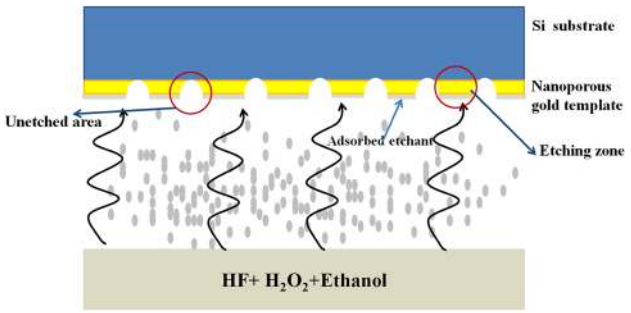

Fig. 1 Schematic diagram for the mechanism of V-Mace

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+.$$

At the anode (on the Si substrate),

$$Si^{0+} + 4h^+ \rightarrow Si^{4+}$$
$$Si^{4+} + 4HF \rightarrow SiF_4 + 4H^+.$$

It should be noted that unlike L-Mace, the end product in V-Mace is SiF_4. Finally, the samples were rinsed with DI water several times and the Au film was removed in aqua regia (3:1 (v/v) HCl:HNO_3). Subsequently, the samples were cleaned in DI water and IPA.

The surface roughness of the SiNPLs, fabricated by V-Mace, is very less in comparison to the L-Mace. The RMS roughness values of the V-Mace-etched samples are 4–12 nm for the samples etched for 10–25 min as shown in Supplementary Fig. S2. Moreover, the RMS roughness of the liquid phase etched samples is in micron range (0.5–2 µm). The reduced RMS roughness in V-Mace etching helps to make uniform electrical contact to the substrate. To achieve good electrical contact In balls of diameter 1 mm were used. The electrical contacts were made in top–bottom geometry and the schematic is also shown in Supplementary Fig. S3. The temperature-dependant *I–V* measurements were carried out by keeping the sample in a temperature-controlled stage (Linkam; THMS600) with the help of a source measurement unit (Agilent B2911A). The work function of SiNPLs and In were measured by Kelvin probe technique (SKP 5050, KP Technology Ltd. UK) with gold tip having diameter 2 mm (2 meV resolution). The reflectance properties of etched Si were observed by UV–Vis–NIR spectroscopy (PerkinElmer, Lambda 950).

3 Results and discussion

The FESEM images corresponding to the sequential steps for the fabrication of SiNPLs are shown in Fig. 2. The morphology of the monolayer of polystyrene (PS) nanospheres on Si wafer is presented in Fig. 2a. Figure 2b represents the separated PS nanospheres by oxygen plasma etching. The top view and cross-sectional FESEM images of the SiNPLs fabricated by V-MACE are shown in Fig. 2c, d, respectively. The cross-sectional FESEM images of the SiNPLs with different etching durations and the etching time versus pillar height plot are given in Supplementary Fig. S4. The Raman spectra of the SiNPLs in comparison with the bare Si are shown in Fig. 3. For the Raman experiment, the laser beam is illuminated parallel to the axis of the SiNPLs, and then the laser is pointed to the tip of the SiNPLs. The intensity of the Raman spectrum of the SiNPLs is found to be increased with respect to the bare Si due to the increased light tapping. The Raman peak for the crystalline Si is located at 521 cm^{-1}. At the same time, the Raman peak for the SiNPLs is shifted to 518 cm^{-1} with an asymmetric broadening in comparison to the bare Si, which is clearly visible in the inset of Fig. 3. The peak shift and broadening in the SiNPLs are attributed to the phonon confinement in the porous Si nanocrystallites on the top of the SiNPLs, which arises from the metal-assisted chemical etching as a by-product [37].

The semi-logarithmic plot for temperature-dependent *I–V* characteristics of an array of SiNPLs fabricated by V-MACE is shown in Fig. 4a. The *I–V* characteristics exhibit Ohmic behavior at temperatures greater than 300 K. At room temperature 300 K, the *I–V* characteristics starts showing rectifying behavior and the Schottky behavior is more prominent at temperatures less than 210 K. The room temperature Schottky barrier height can be calculated directly from the work function of SiNPLs and In, measured using Kelvin probe. The work function of the sample can be calculated from the contact potential difference (V_{CPD}) between the tip and the sample, and is given by [29]

$$V_{CPD} = \frac{\Delta\Phi}{e}, \quad \Delta\Phi = \Phi_{tip} - \Phi_{sample}, \tag{1}$$

Φ_{tip} and Φ_{sample} are the work functions of tip and the sample, respectively. The work functions of the SiNPLs and In, calculated using Eq. (1) are 4.52 and 4.07, respectively as shown in Fig. 4b. The barrier height at room temperature is ~0.45 eV, according to Kelvin probe measurement. The origin of the measured barrier height and low temperature characteristics of the SiNPLs can be analyzed in detail using thermionic emission (TE) model. The current–voltage relation in TE model is given by [38]

$$I = I_o \exp\left(\frac{qV}{nk_BT}\right)\left[1 - \exp\left(\frac{-qV}{k_BT}\right)\right], \tag{2}$$

where $I_o = AA^*T^2 \exp\left(\frac{-q\Phi_b}{k_BT}\right)$ is the saturation current. V is the applied voltage, q is charge of electron, T is absolute temperature, k_B is Boltzmann's constant, A^* Richardson's constant (32 A cm^{-2} K^{-2} for *p*-type Si), A is the contact area, n is the ideality factor and Φ_b is the Schottky barrier height.

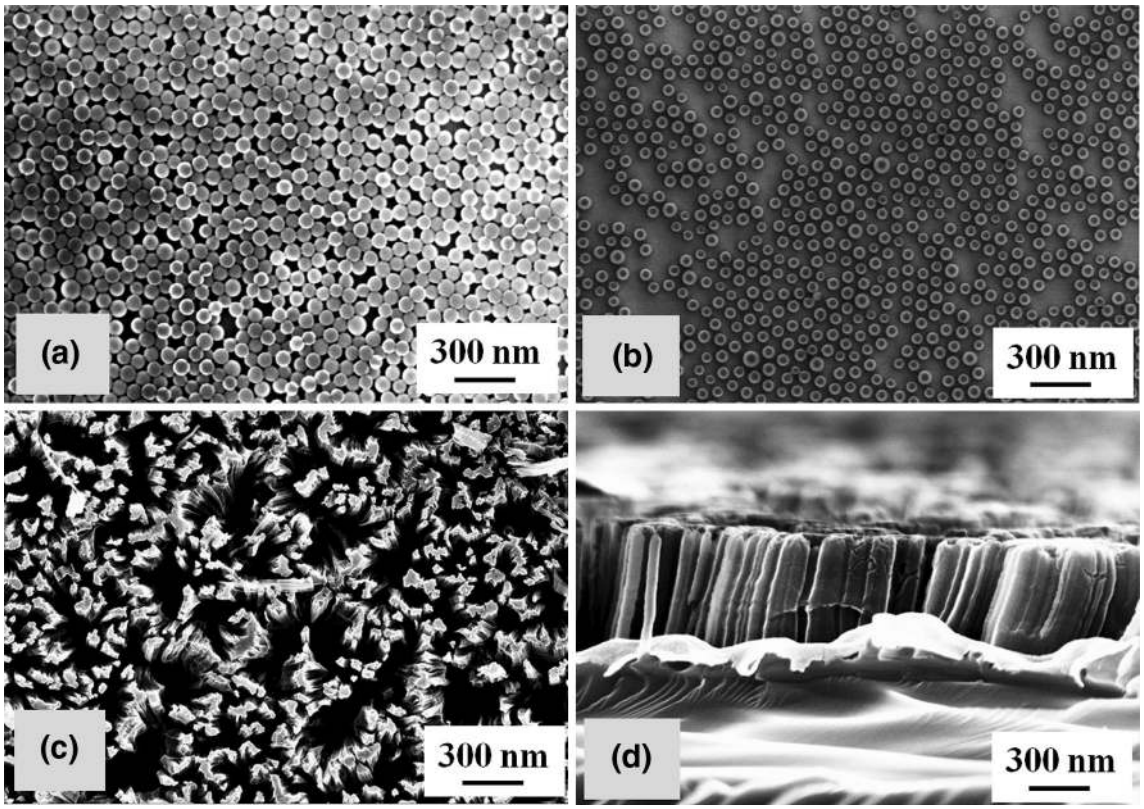

Fig. 2 FESEM images for: **a** monolayer of PS nanospheres on the Si substrate, **b** PS nanosphere separated by oxygen plasma etching, **c** top view of the SiNPLs fabricated by V-Mace, **d** cross-sectional image of SiNPLs

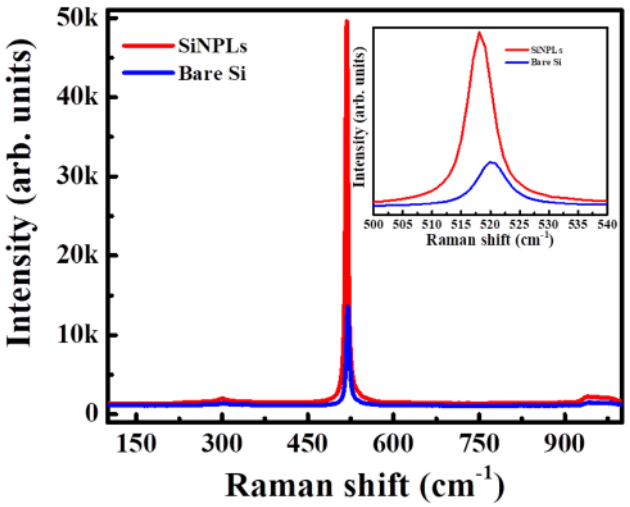

Fig. 3 Raman spectra of SiNPLs and bare Si

The saturation current I_o can be determined from the $I/(\exp(qV/k_BT) - 1)$ versus V plot as shown in Fig. 5a. The intercept of the straight line at $V = 0$ gives the saturation current and the Schottky barrier height is defined as [39]

$$\Phi_b = \frac{k_B T}{q} \ln\left(\frac{AA^*T^2}{I_o}\right). \quad (3)$$

The ideality factor can also be calculated from the slope of the linear forward bias region of ln I versus V plot using TE theory using the following equation [40]:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right). \quad (4)$$

The ideality factor and the Schottky barrier height at temperature ranging from 300 to 170 K calculated by Eqs. (3) and (4) are given in Table 1. The room temperature barrier height calculated by Eq. (3) is 0.48 eV, which is in good agreement with the barrier height measured using Kelvin probe. The barrier height is found to be raised from 0.299 to 0.482 eV and the ideality factor decreases from 7.74 to 2.93 with temperature varying from 170 to 300 K. In general, the barrier height decreases with increase in temperature for most of the II–IV semiconductors [41]. But the increase in barrier height with temperature is also reported for GaAs [42, 43] and Si Schottky contacts [44]. Werner and Guttler have reported that the temperature dependence on barrier height arises from the Schottky

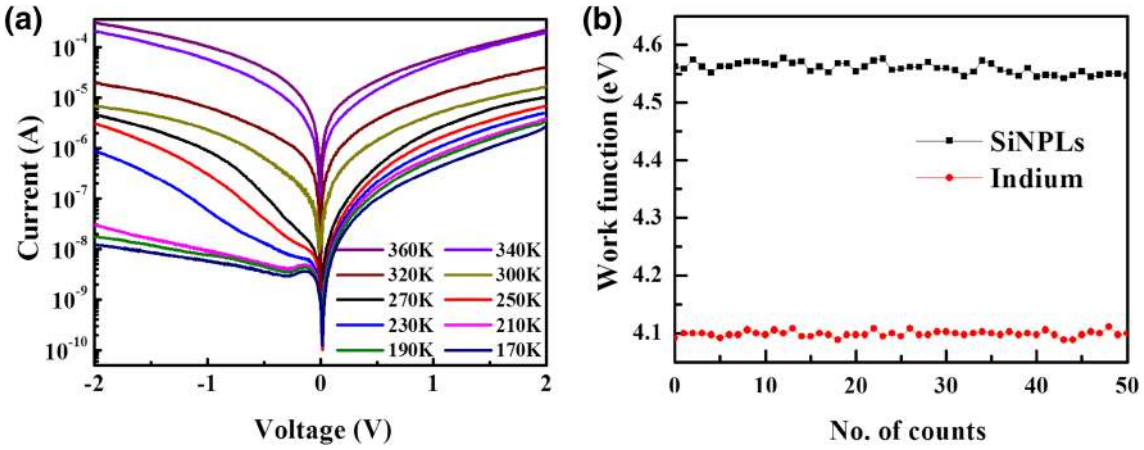

Fig. 4 **a** Current–voltage characteristics of the SiNPLs over a temperature range 170–360 K. **b** Work function of the SiNPLs and indium measured by Kelvin probe

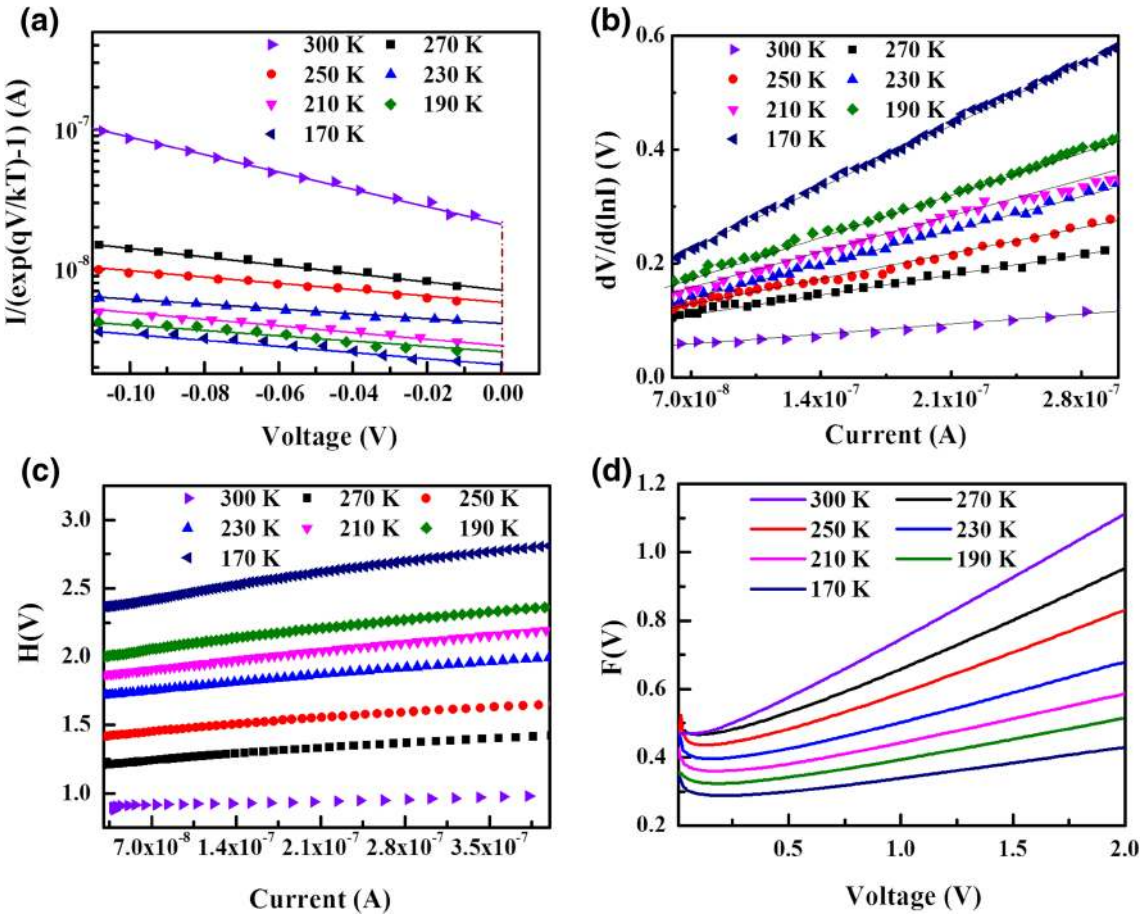

Fig. 5 **a** $I/(\exp(qV/kT) - 1)$ versus voltage plot for the SiNPLs in the temperature range 170–300 K. **b** $dV/d(\ln I)$ versus current plot in the temperature range 170–300 K. **c** $H(V)$ versus current plot using Cheung's function. **d** $F(V)$ versus voltage plot in the temperature range 170–300 K using Norde function

Table 1 Schottky diode parameters of the SiNPLs obtained using different methods

Temperature (K)	Schottky barrier height From *I–V* (eV)	Ideality factor From *I–V* *n*	Cheung's function				Norde	
			d*V*/d(ln *I*) vs *I*		*H*(*I*) vs *I*			
			R_S (MΩ)	*N*	Φ_b (eV)	R_S (MΩ)	Φ_b (eV)	R_s (MΩ)
170	0.299	7.74	1.50	7.91	0.297	1.26	0.295	1.23
190	0.334	6.80	1.07	6.10	0.326	0.94	0.332	1.17
210	0.370	6.16	0.92	5.20	0.350	0.91	0.372	0.76
230	0.400	5.47	0.86	4.20	0.405	0.81	0.409	0.67
250	0.430	4.84	0.71	3.10	0.452	0.68	0.452	0.63
270	0.460	3.81	0.58	2.52	0.462	0.56	0.478	0.55
300	0.482	2.93	0.38	1.86	0.479	0.34	0.482	0.45

barrier inhomogeinity [44]. In our case, also the possible reason for the increase in barrier height with temperature could be ascribed to Schottky barrier inhomogeinity. The poor quality of the interface, which mainly depends on the surface defects, surface treatments such as cleaning and etching, deposition process, is known to affect the Schottky barrier height [45–50]. In the present case, this inhomogeinity may arise as the Si wafer was treated with boiling Piranha and RCA solution for the cleaning of Si wafer. The formation of a thin surface oxide layer on Si nanopillars also affects the quality of interface. In addition, for the present work, ideality factor is $n > 1$, which is again the indicative of the presence of barrier inhomogeinity at the interface [44]. It could be inferred from Fig. 2a that the Schottky diode behavior of the *I–V* characteristics disappears at temperature greater than 300 K and becomes purely Ohmic at high temperature. We deduce the existence of series resistance R_S, which is another important parameter as it can affect the ideality factor and barrier height at low temperatures. Therefore, at present, the task is to determine the series resistance by making use of Cheung's and Norde functions. The series resistance, barrier height and ideality factor can be calculated by Cheung's method using the following equations [51]:

$$\frac{dV}{d(\ln I)} = IR_S + n\frac{k_B T}{q}, \tag{5}$$

$$H(I) = V - n\frac{k_B T}{q}\ln\left(\frac{I}{AA^* T^2}\right), \tag{6}$$

and

$$H(I) = IR_S + n\Phi_b. \tag{7}$$

The d*V*/d(ln *I*) versus *I* derived from the downward curvature in forward bias *I–V* characteristics of the SiNPLs is plotted in Fig. 5b. According to Eq. (5), the slope of the straight line from the d*V*/d(ln *I*) versus *I* plot corresponds to series resistance R_S and the ideality factor can be calculated from the intercept. The series resistance and the ideality factor of the SiNPLs are 1.50 MΩ, 7.91 at 170 K and 0.38 MΩ, 1.86 at 300 K. The consistency of the Cheung's method has been checked through the second determination of series resistance using *H*(*I*) versus *I* plot by giving the value of ideality factor obtained from the d*V*/d(ln *I*) versus *I*, as shown in Fig. 5c. The slope of the straight line directly gives the series resistance R_S and the intercept points out the barrier height of the SiNPLs. The series resistance and the barrier height are 1.26 MΩ, 0.297 at 170 K and 0.34 MΩ, 0.479 at 300 K. The calculated R_S from d*V*/d(ln *I*) versus I and *H*(*I*) versus *I* are in good agreement with each other, implying the validity of Cheung's function.

The high series resistance associated with the Schottky diode causes a voltage drop across the junction. Thus, for a diode with high series resistance, Norde proposed empirical function for the determination of series resistance R_S and barrier height $\Phi_{b,}$ and the modified Norde function is given by [52]

$$F(V) = \frac{V}{\gamma} - \frac{1}{\beta}\ln\left[\frac{I(V)}{AA^* T^2}\right), \tag{8}$$

where γ is the dimensionless integer greater than ideality factor. $\beta = \frac{q}{k_B T}$, and $I(V)$ is the current estimated from the *I–V* curve. The effective barrier height and the series resistance can be defined as [52]

$$\Phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{k_B T}{q}, \tag{9}$$

$$R_S = k_B T\frac{\gamma - n}{qI_{min}}, \tag{10}$$

where $F(V_0)$ is the minimum value of $F(V)$ and V_0 is the voltage corresponds to $F(V_0)$. I_{min} is the current corresponding to the voltage minimum in $F(V)$ versus V plot. The Norde function $F(V)$ plotted against voltage V for the SiNPLs Schottky diode is shown in Fig. 5d. The barrier height

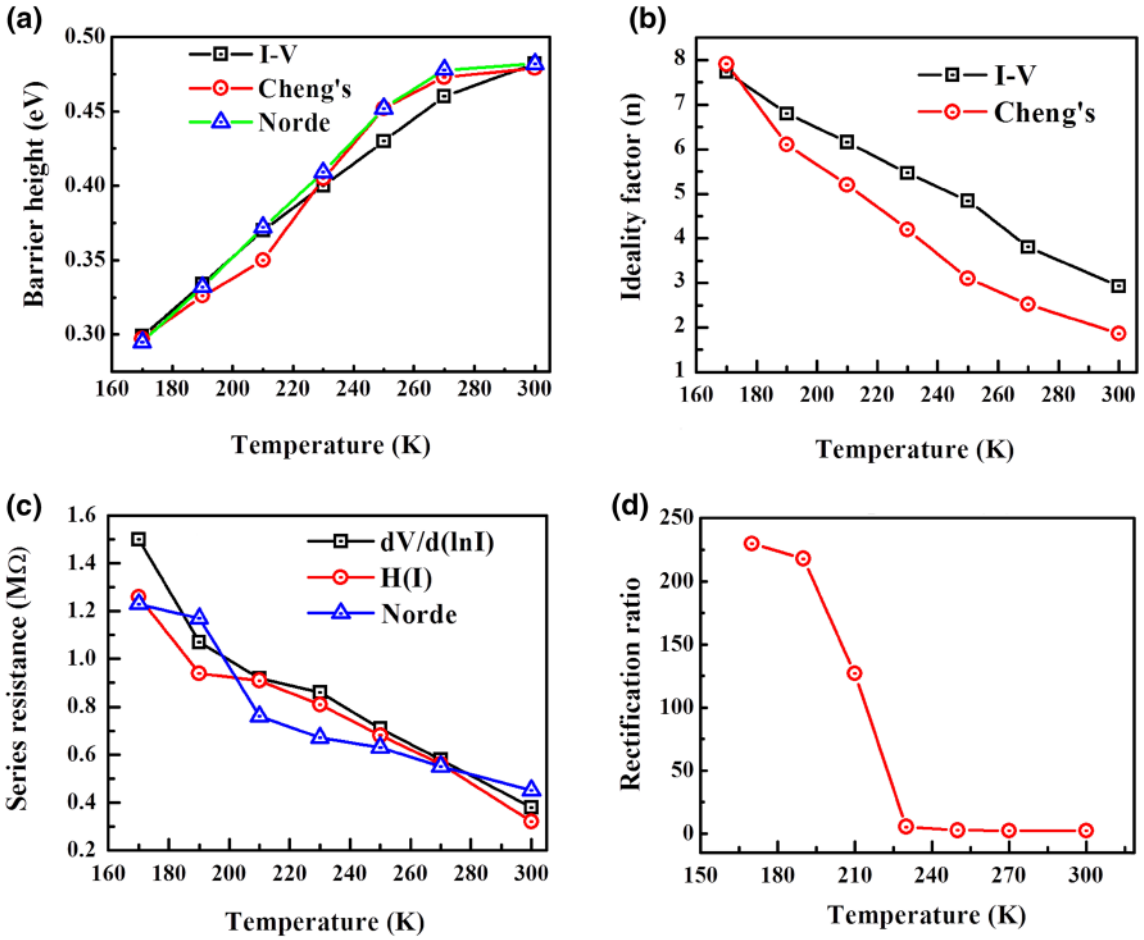

Fig. 6 **a** Variation of barrier height with temperature obtained by different methods. **b** Ideality factor variation with temperature in different methods. **c** Plot for the variation of series resistance with temperature using different methods. **d** Rectification ratio versus temperature plot

and the series resistance values by Norde analysis are 0.295, 1.23 MΩ at 170 K and 0.482 and 0.45 at 300 K. The variations of barrier height, rectification ratio, and ideality factor and series resistance and with temperature in all the models are shown in Fig. 6a–d.

To study the physics underlying the charge transport mechanism, we have recorded the *I–V* characteristics in dark and with illumination of UV and white LEDs of power density 2 mW/cm^2 as shown in Fig. 7a. It could be seen from Fig. 7a that the photocurrent under reverse bias increases drastically in comparison to the dark current. On the contrary, the change in the current with and without illumination is lesser in scope at forward bias. The ratio of photo-to-dark current is ~9.8 and 6.9 for white light and UV light, respectively, in reverse bias at −2 V. At the same time, the ratio is only 1.6 and 1.9 in forward bias at 2 V. The responsivity at reverse bias is defined as $R = \frac{I_{ph}}{P_{opt}}$, [53] shows maximum of 1.3 mA/W and 0.82 mA/W for white light and UV light, respectively. The responsivity is less in comparison to the heterojunction photodetectors but higher than the recently reported Si nanowire based metal–semiconductor–metal photodetectors [54]. The high response of light at reverse bias than the forward bias can be explained using the band diagram. The work functions of indium and SiNPLs (Φ_{In} and Φ_{SiNPLs}) measured using Kelvin probe are already shown in Fig. 4b. The band diagrams of indium and SiNPLs before making contact are shown in Fig. 7b. Since $\Phi_{in} < \Phi_{SiNPLs}$, the electrons flow from indium to SiNPLs to equalize the Fermi level and the corresponding band bending is shown in Fig. 7c. The majority carrier faces high potential barrier, which results in less current under reverse bias condition. Now, with illumination, the electron–hole pairs are produced due to the absorption of photons. The photo-generated electrons in the valence band of SiNPLs are excited to the conduction band and collected by the positive electrode immediately [55]. In the same way, the holes in the valence band are collected by the negative electrode, which reduces the probability of recombination. Thus, the barrier height between the metal and semiconductor decreases, which

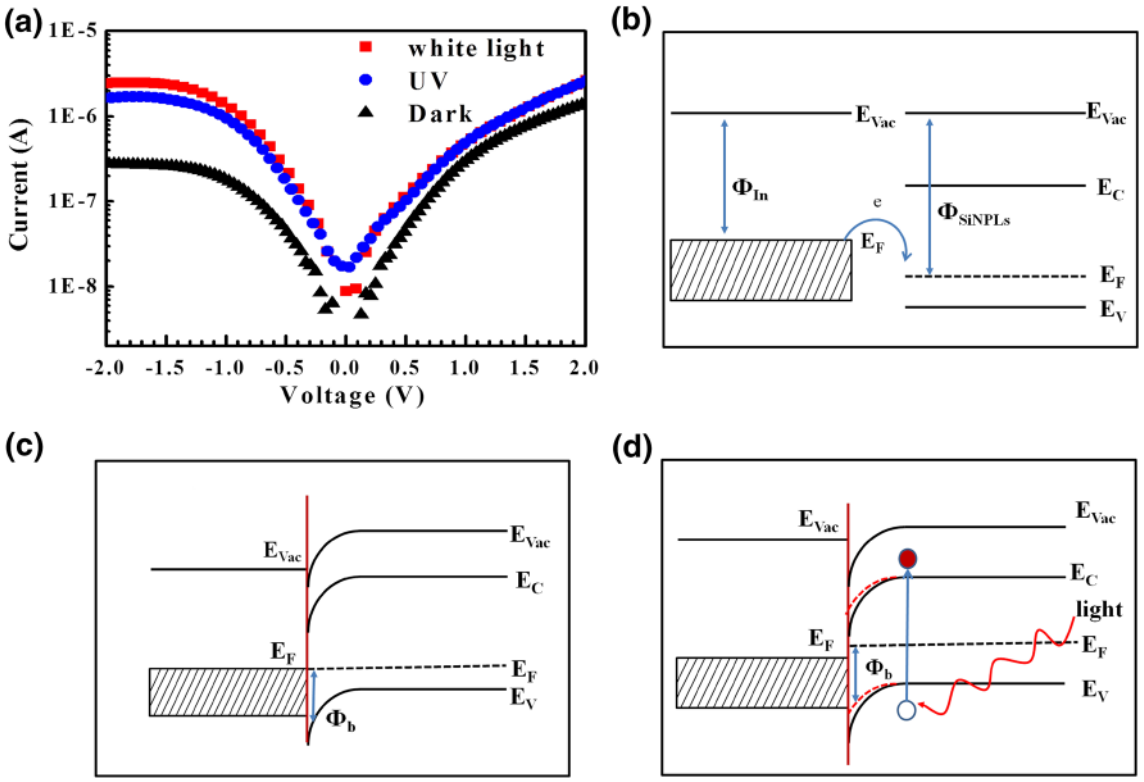

Fig. 7 **a** *I–V* characteristics of SiNPLs in dark and under UV, white light illuminations, **b** band diagram of the SiNPLs and indium before making contact, **c** band bending after making contact, **d** band diagram after illumination of light

results a huge increase in the free carrier density. As a result, upon the illumination of light, the current remains much higher than the dark current in reverse bias mode. The band diagram after illumination is presented in Fig. 7d. At the same time, for the forward bias, the additional charge carriers generated by the photons are only contributing to increase the current. Therefore, the photo-to-dark current ratio is found to be less in forward bias.

The light sensing properties of the SiNPLs were further investigated by taking the time-dependent photo-response of UV light and white light at room temperature under reverse bias of −2 V. The increase in photocurrent is clearly observed with four cycles as presented in Fig. 8a. The SiNPLs shows very fast response to the light with response time 0.18 and 0.26 s for white light and UV light, respectively. The enhanced photo–dark current ratio in the SiNPLs is ascribed to the reduction in the reflectance, which arises from the antireflecting property of the SiNPLs. The generation of electron–hole pair in the SiNPLs is directly related to the absorption of light through the relation [56]:

$$g_{\text{opt}} = \frac{\alpha P_{\text{in}}}{AE}, \tag{11}$$

where g_{opt} is the optical generation rate, A is the illuminated area of photodiode, P_{in} is the incident optical power, α is the absorption coefficient and $E = h\nu$ is the photon energy. The photocurrent is related to the optical generation rate by the equation [56]

$$I_{\text{ph}} = -qA \int_{-X_p}^{X_n+d} g_{\text{opt}}\, \mathrm{d}x, \tag{12}$$

where d is the thickness of undoped region. For the p-type semiconductor, the integral can be reduced to [56]

$$I_{\text{ph}} = \frac{-q(1-R)P_{\text{in}}}{h\nu}(1 - \mathrm{e}^{-\alpha d}), \tag{13}$$

where R is the reflection at the SiNPLs surface and P_{in} is the incident power. Since the SiNPLs are grown on 500 µm substrate, the transmittance of the sample is zero. Therefore, $(1 - R)$ gives absorption of the sample. According to Eq. (13), the increase in absorption of light increases the photocurrent. The reflectance of the SiNPLs is compared with the bare Si in Fig. 8b. The reflectance of the SiNPLs stays less than 4% in the visible region with a minimum reflectance of 2.13% for a sample etched for 25 min. The effective absorption of light > 95% ensures the photocurrent enhancement and fast photo-response to the light. The effect of illumination on the SiNPLs is further

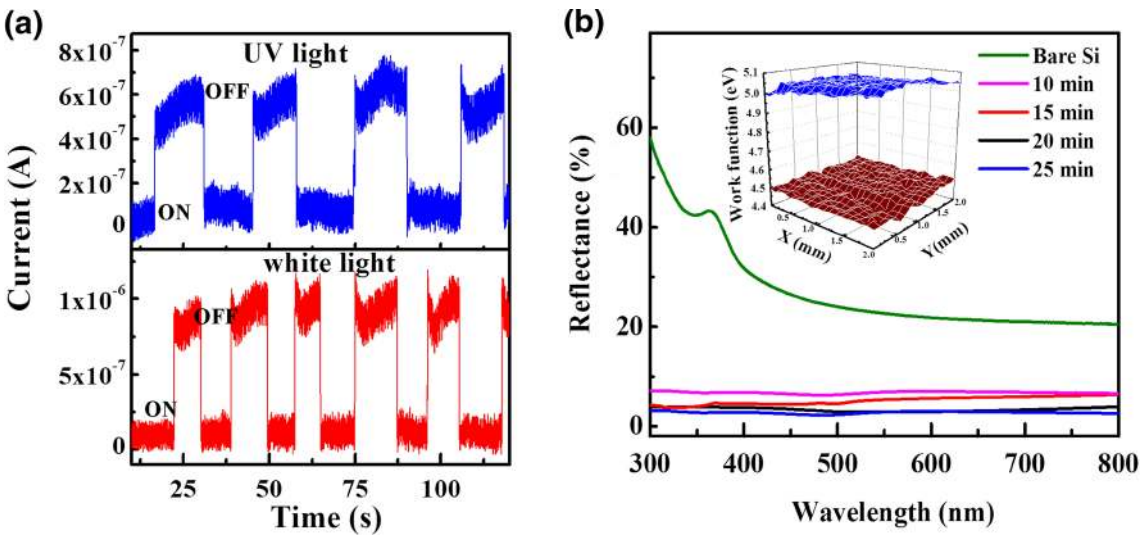

Fig. 8 **a** Time-dependent photo-response for UV and white light. **b** The reflectance of the SiNPLs in comparison with the base Si. The work function variation before and after illumination is shown in the inset

verified by measuring the work function in dark and under illumination using Kelvin probe. The changes in the work function observed in dark and under light are shown in the inset of Fig. 8b.

4 Conclusion

Vapor phase metal-assisted chemical etching (V-Mace) was employed along with nanosphere lithography to fabricate uniform arrays of Si nanopillars (SiNPLs) in a controlled manner, and the mechanism of V-Mace has been discussed in detail. The current–voltage characteristics were studied over a wide temperature range of 170–360 K. The SiNPLs exhibit Schottky diode behavior for a temperature < 300 K and the Schottky diode parameters, such as barrier height, ideality factor, series resistance, were extracted using Cheung's and Norde method. The Schottky diode parameters calculated directly from *I–V* characteristics match with Cheung's as well as Norde methods. Moreover, the light sensing properties of the SiNPLs have been studied by measuring the *I–V* characteristics in dark and under illumination of UV light and white light. The SiNPLs exhibited good and fast response to the white and UV light, especially in reverse bias region. In reverse bias region, along with the photo-generated charge carriers, the carriers transferred to the conduction band due to the reduction in barrier width also contribute for the conduction. Moreover, in forward bias, the photo-generated carriers only contribute to the increase in current under illumination. Further, the SiNPLs showed superior light trapping properties with a reflectance less than 4% over a wavelength region 300–800 nm. This ultra-high absorption of light in UV–visible region has led to light sensing properties of the SiNPLs. The light sensing properties are further confirmed by work function measurement in dark and under illumination.

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