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2013 J. Phys. D: Appl. Phys. 46 095306

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J. Phys. D: Appl. Phys. **46** (2013) 095306 (5pp) doi:10.1088/0022-3727/46/9/095306

Charge trapping properties and retention time in amorphous SiGe/SiO_2 nanolayers

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Received 3 November 2012, in final form 5 January 2012
Published 7 February 2013
Online at stacks.iop.org/JPhysD/46/095306

Abstract
In this paper, we report on the electrical properties of metal–oxide–semiconductor (MOS) capacitors containing a well-confined 8 nm-thick SiGe amorphous layer (a-SiGe) embedded in a SiO_2 matrix grown by RF magnetron sputtering at a low temperature (350 °C). Capacitance–voltage measurements show that the introduction of the SiGe layer leads to a significant enhancement of the charge trapping capabilities, with the memory effect and charge retention time larger for hole carriers. The presented results demonstrate that amorphous floating-gate SiGe layers embedded in SiO_2 may constitute a suitable alternative for memory applications.

(Some figures may appear in colour only in the online journal)

1. Introduction

An important research effort is currently being devoted to the investigation of high-mobility semiconductors and their potential applications in future high-performance metal–oxide–semiconductor field-effect transistors (MOSFETs). In particular, there is great interest in the development of memory devices with nanometre-thick charge trapping layers as required by the downscaling of non-volatile memories. Metal–oxide–semiconductor structures (MOS) based on Si, Ge and SiGe nanocrystals (NCs) have been studied actively in recent years. Investigations on their charge trapping properties and retention time have shown that these systems are promising for electronics, optoelectronics and solar cell applications [1–6]. In the case of flash-memory device applications, they ensure long-term charge storage, fast response and low power requirement [7, 8]. However, the main charge storage mechanism is still not completely clear. In these devices, charge trapping may occur at the oxide–substrate interface (presence of dangling bonds [9]), inside the oxide matrix, into NCs' quantum confined states and/or at their interface with the oxide matrix. However, the application of new characterization methods has shown the possibility of gaining useful insights into their properties. The charge pumping method recently applied to silicon NCs embedded in ultra-thin SiO_2 oxide has allowed extracting most of their structural and electrical characteristics [10]. In general, the electrical properties of most of these devices depend on the nanostructure surface state density whose modifications may alter the device performance. The trap density can be increased by increasing the NCs' density. However, obtaining both high trap density ($>10^{13}$ cm^{-2}) and long retention time from non-volatile floating gate memory has remained challenging owing to the difficulty of maintaining sufficient isolation between NCs as their density is increased.

On the other hand, amorphous nanoparticles (NPs) present interesting advantages in comparison with crystalline NPs. Specifically, they can be produced following a low-temperature production process and a lower strain is expected in the NPs embedded in the matrix due to their more flexible amorphous structure [10]. Charging effects and good retention properties have been observed in amorphous silicon NPs (a-Si NPs) [7, 11, 12], amorphous hydrogenated silicon (a-Si : H) thin films [13] and silicon germanium nitride layers [14]. The

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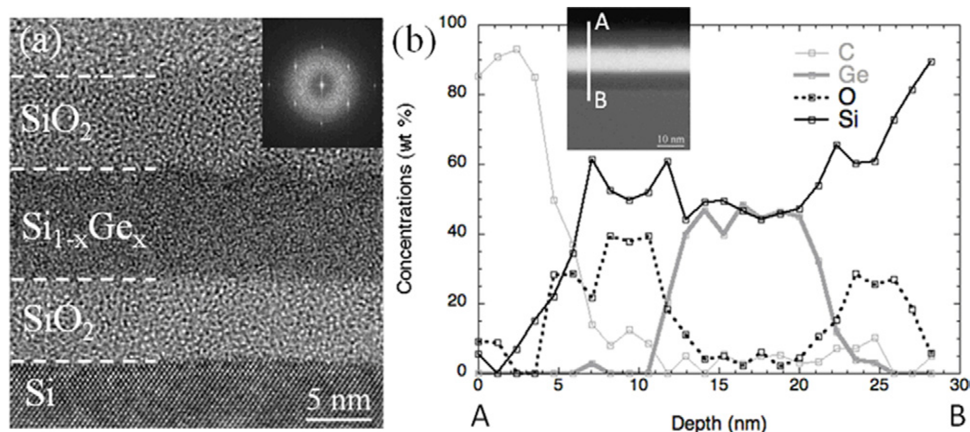

Figure 1. Structural and compositional analysis of the SiGe/SiO_2 sample: (*a*) HRTEM cross-sectional micrograph and the corresponding diffractogram (inset); (*b*) wt% concentration profiles of the constituting elements of the cross-sectional sample. The EDS profiles were obtained along the A–B line marked in the STEM image shown in the inset.

disordered structure of these amorphous materials is at the origin of the observed high density of localized defect states that can capture electrons and/or holes [15]. Furthermore, for thin MOS structures the role of interface layers should be included in the realistic model of memory devices that can present both deeper trap energy and longer retention time.

In this work, we demonstrate high charge trapping and good retention time obtained on an amorphous tri-layered SiO_2/SiGe/SiO_2 nanostructure. The charge trapping capabilities of this simple structure for both electrons and holes are investigated by capacitance–voltage (C–V) measurements. The functionality of this structure for memory applications is discussed in terms of charge carrier storage in the layer and retention time measurements.

2. Experimental

p-Type Si (1 0 0) substrates (1–5 Ω cm), high-purity SiO_2 target (99.999%) and a composite target of Si (99.999%) plate covered with Ge (99.999%) polycrystalline pieces were used in this work. The ratio between the Ge pieces and the Si target was 1 : 4. The native oxide was removed by dipping the substrates in a dilute HF (10%) solution for 1 min. Afterwards, the substrates were transferred to the deposition chamber of an Alcatel 650 RF magnetron sputtering machine with a multi-target system. A tri-layered SiO_2 (7 nm)/SiGe (8 nm)/SiO_2 (6 nm) nanostructure was grown in Ar^+ ambient (10^{-3} mbar) at a substrate temperature $T_s = 350\,^\circ$C using a RF power of 80 W. The growth rates were approximately 4.6 nm min^{-1} and 6.7 nm min^{-1} for SiO_2 and SiGe layers, respectively. A reference sample made exclusively of a 28 nm-thick SiO_2 layer (without any SiGe layer embedded in the oxide layer) deposited on the p-type Si substrate was also prepared. MOS capacitors were fabricated by depositing 1 mm-diameter Al square contacts by thermal evaporation on the top surface at room temperature under vacuum conditions (10^{-6} mbar). The back ohmic contacts to the substrate were burned from the Al foil by electric sparks. Structural and compositional characterizations of the as-grown SiGe/SiO_2 sample were carried out by cross-sectional high-resolution transmission electron microscopy (HRTEM) and energy dispersive x-ray spectroscopy (EDXS) using a FEI Tecnai F20 transmission electron microscope operating at 200 kV. Capacitance–voltage (C–V) measurements were carried out using a Keithley 4200SCS dc characterization system equipped with a Model 4210-CVU 1 kHz–10 MHz capacitance–voltage measurement unit. C–V sweep measurements were first performed at various frequencies to discriminate between slow traps (inside the matrix) and fast traps (interface with the substrate). The retention characteristics were measured by monitoring the flat-band voltage shift (ΔV_{FB}) of the C–V curves after application of a ±14 V gate voltage stress for 1 s. All measurements were performed at room temperature under dark conditions.

3. Results and discussion

In figure 1(*a*), a typical cross-sectional HRTEM micrograph of the SiO_2/SiGe/SiO_2 tri-layered structure is reported. The darkest layer above the crystalline Si substrate corresponds to the SiGe layer with an average thickness of 8.2 ± 0.4 nm whose amorphous nature is revealed by the complete absence of crystalline features. This finding is also confirmed by the diffraction pattern reported in the inset to this figure, uniquely showing crystalline Si substrate reflections. In figure 1(*b*), the concentration profiles of the constituting elements were measured along the A–B line marked in the Z-contrast STEM image reported in the inset to this figure. In this analysis, the precision of element concentrations is rather poor (±10%) owing to the rather low signal obtained from these thin layers. However, the tri-layered elemental composition is clearly revealed; a $Si_{1-x}Ge_x$ layer is embedded between two SiO_2 layers (∼45 wt% obtained for Ge should be considered a lower limit in SiGe as, with the intention to show all the elements present in the cross-sectional sample, it is the sum of all the element concentrations shown in the figure that has been normalized to 100%).

Figure 2 compares normalized C–V characteristics between the SiO_2 control sample (*a*) and the SiGe/SiO_2 sample (*b*). The flat-band voltage (V_{FB}) values measured under low-voltage conditions are about −4.1 V and −2.5 V

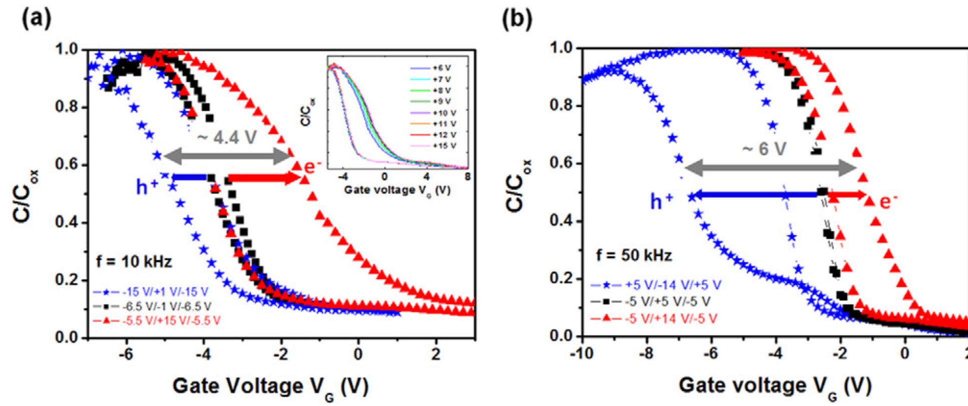

Figure 2. *C–V* hysteresis curves of (*a*) SiO_2 (reference sample) and (*b*) SiGe/SiO_2 capacitors as a function of voltage sweep range for 10 kHz and 50 kHz, respectively. The *C–V* hysteresis loop as a function of voltage sweep for the SiO_2 sample is presented in the inset to (*a*).

for control SiO_2 and SiGe/SiO_2 samples, respectively. Once these reference values of V_{FB} under low stress were obtained, the V_{FB} shift (ΔV_{FB}, memory window width) was obtained as a function of electrical stress and frequency. At a given voltage stress, the frequency response of traps gives information about their location into the volume, the traps' distance from the interface with the substrate increasing with decreasing frequency. The largest memory window is obtained at low frequencies, precisely at 10 kHz for the SiO_2 sample and at 50 kHz for the SiGe/SiO_2 sample, using the same voltage sweep conditions. This result demonstrates a low defect density at the interface with the substrate, most of the trap centres being located in the oxide volume (SiO_2 defects and/or traps related to the SiGe layer). In the case of the SiO_2 sample, the shift of the *C–V* curve is clearly larger for a voltage sweep from −5.5 to +15 V and back to −5.5 V (−5.5 V/+15 V/−5.5 V) that corresponds to electron charging than that obtained for a voltage sweep −15 V/+1 V/−15 V (hole charging). These shift values are measured considering the reference *C–V* curve obtained for −6.5 V/−1 V/−6.5 V and indicate that holes can escape more easily than electrons. A systematic hysteresis is observed when positive voltages are applied with a nearly constant flat-band voltage shift value $\Delta V_{FB} = 2.4$ V, independently of the maximum voltage sweep value (positive), as shown in the inset of figure 2(*a*). This indicates that electron trapping is limited, where the shift hardly increases for high voltages (not more than +0.5 V in the ΔV_{FB} value between injections with +6 and +15 V). Under the same conditions, the hysteresis measured at 1 MHz was about 0.1 V (not shown here), indicating that the SiO_2 sample contains a low density of interfacial traps (at the interface with the substrate) but mostly volume traps storing negative charges. The same difficulty in injecting positive charges was observed while applying high negative voltages.

In the case of the SiGe/SiO_2 sample, no significant hysteresis is detected at low voltages, as shown in figure 2(*b*). Higher positive or negative gate voltages cause the *C–V* characteristics to shift, respectively, in the direction of negative (electrons) or positive (holes) charges. However, the *C–V* curve shift is more pronounced for holes than for electron charging, suggesting an easier mechanism for hole trapping that are stored by slow traps into the volume of the SiGe/SiO_2 structure (low-frequency conditions). Figure 2(*b*) also shows changes in the slope of the *C–V* curve in the depletion/inversion regime when the voltage is swept back from accumulation (−14 V) to inversion (+5 V), whereas no slope modification was detected for lower voltages (parallel shifts). However, we note that no relevant modification is observed in the case of the SiO_2 sample, even for a +15/−5.5 V sweep range (figure 2(*a*)). Maximum magnitudes of electric fields applied to the SiO_2 and SiGe/SiO_2 capacitors are, respectively, 5.3 MV cm^{-1} and 5.8 MV cm^{-1}. These values correspond to a high electric field, close to the breakdown field for SiO_2 layers (in the 5–10 MV cm^{-1} range, depending on the oxide quality). Thus, capacitance modifications in the depletion/inversion regime may be caused by a degradation of the oxide subjected to a high electric field or to the diffusion of mobile charges (ions). The magnitude of the hysteresis reaches ∼4.4 V for $V_G = +15/-15$ V and ∼6.0 V for $V_G = +14/-14$ V, respectively, for SiO_2 and SiGe/SiO_2 samples. Thus, a gain of about +1.6 V in the memory window width is obtained by introducing the thin SiGe layer embedded in the SiO_2 matrix, under a sufficiently strong electric field necessary for charge injection into the SiGe layer (5–6 MV cm^{-1}). Under lower electric field conditions, this gain is negative (about −0.3 V), indicating that the SiGe layer contains fewer trapped charges than the SiO_2 control sample. These traps could be associated with defects present in the SiO_2 matrix volume and located close to the substrate.

The amorphous SiGe layer can be seen as a layer of high density of 'nanoclusters', charge trapping being attributed to the presence of defects in the SiGe layer due to the disordered structure of the amorphous material and the band-gap off-set between the amorphous SiGe and SiO_2 barrier layer. The magnitude of trapped charge density can be roughly estimated using the following relation assuming single charge storage per nanocluster [16]:

$$N_{\text{charge}} = \frac{\Delta V_{FB}}{\frac{q}{\varepsilon_0}\left(\frac{t_{\text{control}}}{\varepsilon_{OX}} + \frac{t_{\text{SiGe}}}{\varepsilon_{\text{SiGe}}}\right)} \quad (1)$$

where q is the magnitude of the electronic charge, ε_0 is the permittivity of the free space, ε_{ox} is the relative permittivity of the control SiO_2 layer, ε_{SiGe} is the relative permittivity of

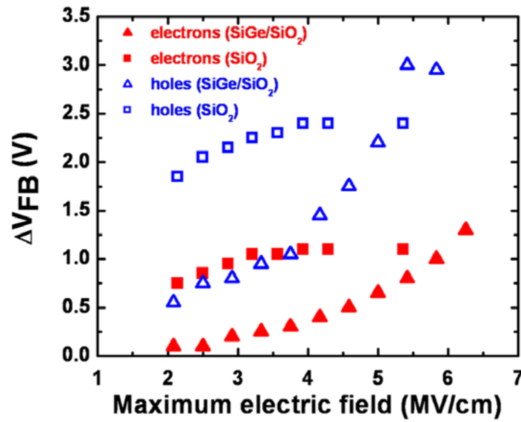

Figure 3. Memory window (ΔV_{FB}) given by electron and hole trapping as a function of the electric field magnitude for $SiGe/SiO_2$ and SiO_2 samples.

$Si_{1-x}Ge_x$ ($x = 0.3$), $t_{control}$ is the control oxide thickness and t_{SiGe} is the thickness of the amorphous SiGe layer. A value $\varepsilon_{SiGe} = 4.9 \pm 0.3$ was obtained from the C–V experimental data and a trapped charge density of $N_{charge}(SiGe) = 9.7 \times 10^{12}$ cm^{-2} was calculated for a sweeping voltage of ±15/14 V. The SiO_2 control sample can be seen as a sample where the 8 nm-thick SiGe layer is substituted by a 15 nm-thick SiO_2 layer. In this case, using the same relation, the trapped charge density in the SiO_2 reference sample is calculated to be $N_{charge}(SiO_2) = 4.3 \times 10^{12}$ cm^{-2} for the same sweeping voltage (±15/14 V). Interestingly, although the equivalent SiO_2 layer thickness (15 nm) is double of that corresponding to the SiGe layer (8 nm), the charge trapping capabilities of the film can be increased by a factor of about 2.3 when the SiGe layer is introduced. This layer can provide additional traps due to its amorphous disordered structure and/or their interfaces with SiO_2 that promote the appearance of effective charge trapping centres for electrons and holes.

In order to compare charge carrier trapping for both structures independently of the total oxide thickness, the memory window is plotted in figure 3 as a function of the electric field applied to the $SiGe/SiO_2$ and SiO_2 structures from 2 to 6.5 MV cm^{-1}. We limited the measurements to 6.5 MV cm^{-1} to prevent oxide breakdown. First, figure 3 shows a significant charging effect for the SiO_2 sample compared with the $SiGe/SiO_2$ sample for low electric field conditions. For example, for 2 MV cm^{-1}, the electron charging values are around 0.1 V and 0.75 V respectively, for $SiGe/SiO_2$ and SiO_2 samples, whereas these values are, respectively, around 0.55 V and 1.85 V for hole charging. A stronger charging effect under a low electric field for SiO_2 samples could be explained by a higher oxide defect density and a trap-assisted direct tunnelling current between the substrate and oxide. While increasing the electric field, the memory window quickly saturates for SiO_2 samples for an electric field around 4 MV cm^{-1}, whereas it increases exponentially for $SiGe/SiO_2$ samples, becoming larger than charging in SiO_2 samples for electric fields higher than 5 MV cm^{-1}. Finally, between 2 and 6 MV cm^{-1}, ΔV_{FB} increases for $SiGe/SiO_2$ samples by a factor of 15 and 5, respectively, for electron and hole charging, whereas it hardly increases by a factor of 1.5 and 3 for SiO_2 samples. The charging effect is then larger for $SiGe/SiO_2$ samples under an electric field stronger than 5 MV cm^{-1} for both kinds of carriers (electrons and holes), this enhancement being better for holes. These results suggest a better oxide quality in the $SiGe/SiO_2$ sample. It is inferred that a direct tunnelling injection occurs in the SiGe layer for sufficiently strong electric field conditions.

Figure 4 presents a comparison of the charge retention characteristics for SiO_2 and $SiGe/SiO_2$ samples by stressing the samples for 1 s with voltage pulses of ±14 V (positive for electron charging and negative for hole charging). The time evolution of ΔV_{FB} is presented for both samples in figures 4(*a*) and (*b*), while the time evolution of the retained charge is presented in figures 4(*c*) and (*d*). The initial stored charge is not the same when charging with electrons with respect to holes for both samples. In particular, retention times for holes and electrons of about 2 s and 10 s are measured to keep at least 80% of the injected charge for SiO_2 and SiGe samples, respectively. However, a different loss process is found for longer delays. Specifically, although the retention times for electrons decrease to zero for 10^2 s for both samples, the introduction of the SiGe layer remarkably improves the hole retention. The hole retention decreases to zero for 4×10^3 s and 5×10^4 s, respectively, for SiO_2 and $SiGe/SiO_2$ samples, the remaining stored charges being about 32% for the $SiGe/SiO_2$ sample (10% for the SiO_2 sample) for a waiting time of 10^3 s.

Compared with the SiO_2 sample, the good hole retention time observed in the $SiGe/SiO_2$ structure (with a more than 10 times slower charge loss process) is clearly due to the introduction of the SiGe layer. This result indicates that the two oxide layers sandwiching the SiGe layer have a good capability to prevent the release of the trapped holes. However, it should be noted that the presented results could be improved further by increasing the SiGe layer and/or SiO_2 gate and tunnel layer thicknesses. In this regard, further investigations are in progress to distinguish the contribution of the interfaces and the volume of the SiGe layer to the charge trapping process more accurately.

4. Conclusions

In summary, electron and hole charging/discharging was studied on MOS capacitor structures based on amorphous $SiGe/SiO_2$ layers produced at a low temperature (350 °C) by RF magnetron sputtering. Interestingly, the introduction of a thin SiGe layer into the SiO_2 matrix induces a charge trap density $>10^{12}$ cm^{-2} with better memory characteristics and long-term charge retention for holes. In view of the presented results, the promising potentialities of amorphous SiGe thin layers when used as a floating gate for charge trapping applications in memory devices are demonstrated.

Acknowledgments

This study was partially funded by: (i) European COST Actions MP0901-NanoTP and MP0903-NanoAlloy; (ii) FEDER through the COMPETE Program and by the Portuguese

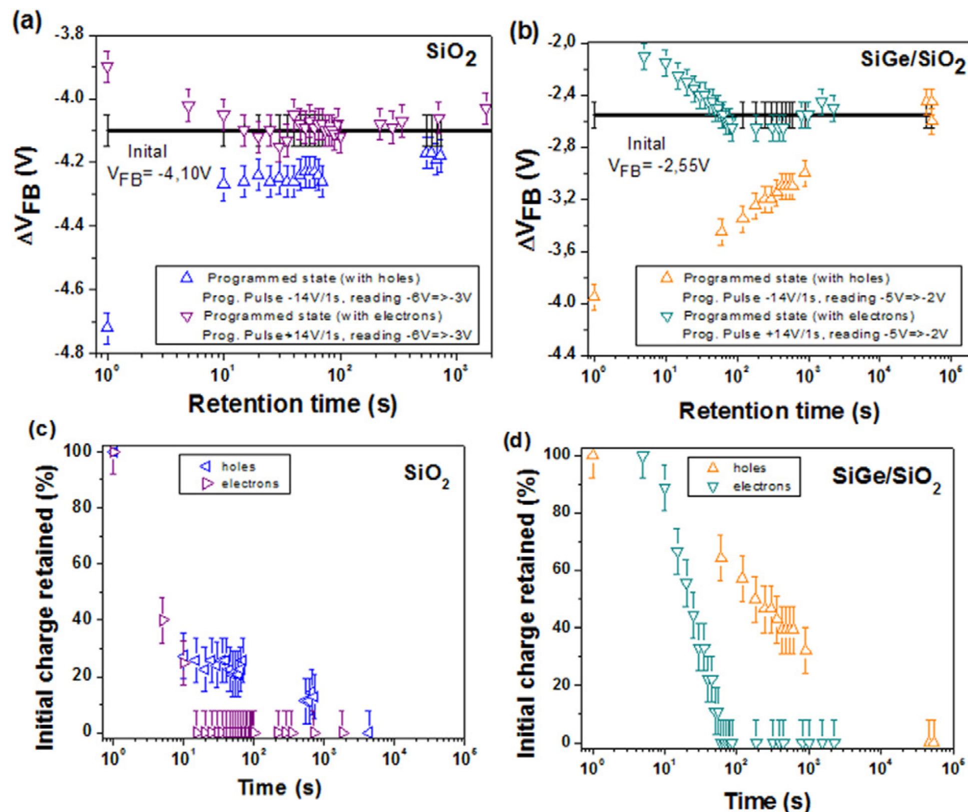

Figure 4. Retention characteristics for SiO_2 (*a*) and $SiGe/SiO_2$ (*b*) samples. Pulses of (+14/+15 V, 1 s) and (−14/−15 V, 1 s) were applied for SiO_2 and $SiGe/SiO_2$ samples for electron and hole charging, respectively. Time evolutions of retained charge for both samples are shown in (*c*) and (*d*).

Foundation for Science and Technology in the framework of the Strategic Project PEST-C/FIS/UI607/2011; (iii) the transnational access framework of the ANNA Eu Project (Contract No 026134-RII3) through the funding of the ANNA_TA_UC9_RP006 proposal. EMFV is grateful for financial support through the FCT and POPH of the grant SFRH/BD/45410/2008. JMS is grateful for financial support through the Spanish CSIC JAE-DOC-070/01 program co-funded by FSE. The authors would also like to thank Engineer José Santos for technical support at the Thin Film Laboratory.

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