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Charging dynamics of a floating gate transistor with site-controlled quantum dots

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A quantum dot memory based on a GaAs/AlGaAs quantum wire with site-controlled InAs quantum dots was realized by means of molecular beam epitaxy and etching techniques. By sampling of different gate voltage sweeps for the determination of charging and discharging thresholds, it was found that discharging takes place at short time scales of μs, whereas several seconds of waiting times within a distinct negative gate voltage range were needed to charge the quantum dots. Such quantum dot structures have thus the potential to implement logic functions comprising charge and time dependent ingredients such as counting of signals or learning rules. © *2014 AIP Publishing LLC*.
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Quantum dots (QDs) located in close vicinity of transistor channels can induce significant threshold voltage shifts, which depend on the number of QD localized charges, the capacitive coupling, and the electrochemical properties.[1–3] The floating gate function of QDs has been demonstrated in different material systems such as lithography defined[1] and self-assembled QDs[4–7] and down to the quantum limit of one electron.[1,8,9] Since self-assembled QDs are randomly distributed, charges on several QDs contribute to the threshold voltage shift. Thus, ensembles of QDs are typically not practical for the study of single electron properties. Therefore, an accurate control of the number of QDs and their relative distances to the gates is necessary.

Here, we report on the realization of a QD flash memory based on a modulation doped GaAs/AlGaAs heterostructure with site-controlled InAs QDs located in the center of a quantum wire. The central QD becomes charged at negative gate voltages. By sampling different gate voltage sweeps with variations in the minimum gate voltage and waiting time, the charge occupation number of the QDs can be controlled in a wide range. A maximal hysteresis width of 6.2 V is found. Time resolved measurements show QD charging times of several seconds.

A sketch of the device is shown in Fig. 1(a). The QD floating gate transistor was grown by molecular beam epitaxy in two steps. Starting with an undoped GaAs substrate, 30 nm of undoped $Al_{0.2}Ga_{0.8}As$ followed by 50 nm of n-doped $Al_{0.2}Ga_{0.8}As$ were grown in the first growth process. On top of the heterostructure, a 10 nm thick and undoped GaAs layer was deposited. Afterwards, nanohole arrays were processed by electron beam lithography and soft dry chemical etching with a period of 300 nm and a hole diameter of around 100 nm. The depth of the nanoholes is around 50 nm. This results in a 40 nm thick $Al_{0.2}Ga_{0.8}As$ layer between the nanohole and the two-dimensional electron gas (2DEG). The diameter of 100 nm was selected because of optimal fabrication parameters, e.g., e-beam lithography resolution and InAs quantum dot formation. In the second growth process, InAs was deposited on the structure, which leads to InAs QDs in the holes.[10] Finally, the InAs QDs were capped with GaAs. A detailed description of the growth technique is given in Refs. 2 and 11. The inset of Fig. 1(a) shows an electron microscope image conducted from a tilted angle of the structure right after the InAs growth. The sample was etched in such a way that the front cuts through a nanohole. The bright spot inside the nanohole corresponds to InAs. After the growth procedure, a Hallbar was realized by optical lithography, wet chemical etching, and alloying of Ni/AuGe/Ni/Au contacts. Finally, the QD floating gate transistor was defined by electron beam lithography in combination with a soft dry chemical etching technique. Dry chemical etching was performed to isolate the gate from the channel area via trenches with a depth of 150 nm.

An electron microscope image of the device together with the circuit diagram is shown in Fig. 1(b). The device consists of a transport channel, four laterally defined side gates and site-controlled QDs above the channel. The gate voltage V_g and the bias voltage V_b were applied to the side gates and the top contact, respectively, with the bottom contact serving as common ground. The current was measured as voltage drop across a series resistor with $R = 10\,k\Omega$. All measurements were conducted at 4.2 K in the dark. The channel width at the smallest constriction is around $w \approx 210$ nm. The position of the central site-controlled QD is highlighted by a yellow circle. In Fig. 1(c), two current-gate voltage traces $I(V_g)$ are shown. The gate voltage was swept from a minimum gate voltage $V_g = V_{gm} = -3.5$ (solid) or -3.9 V (dashed) to $V_g = 4.5$ V (up-sweep direction) and back (down-sweep direction) for a constant bias voltage $V_b = 0.1$ V. The arrows indicate the gate voltage sweep cycle directions and the corresponding threshold voltages V_{tu} for the up- and V_{td} for the down-sweep. Starting with a pinched-off channel at $V_g = V_{gm} = -3.5$ V, the channel opens when the gate voltage passes the threshold voltage V_{tu}.

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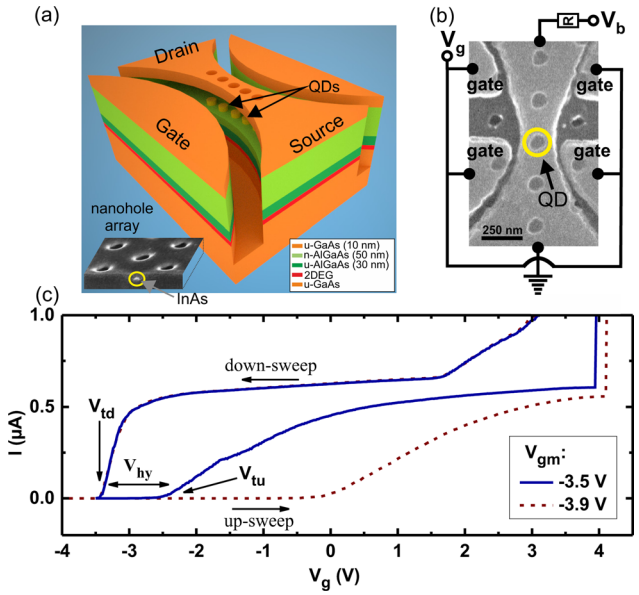

FIG. 1. (a) Scheme of the QD floating gate transistor. It is composed of a 2DEG transport channel, site-controlled InAs QDs, and laterally defined side gates. Inset: An electron microscope image taken from a tilted angle shows a cross section through a nanohole. The bright spot corresponds to InAs. (b) Electron microscope image together with electrical setup of the device. The gate voltage V_g was applied to the four side gates. The bias voltage V_b was applied to the top contact and the bottom contact was used as common ground. The QD located in the smallest constriction of the channel is highlighted by a yellow circle. (c) Current-gate voltage traces $I(V_g)$ for $V_{gm} = -3.5$ (solid) and -3.9 V (dashed) up to $V_g = 4.5$ V. The arrows indicate the up- and down-sweep directions with corresponding threshold voltages V_{tu} and V_{td} as well as the hysteresis width V_{hy}.

The current increases monotonically up to about $V_g \approx 4$ V, at which an almost instantaneous jump of the current occurs. For the down-sweep, the current decreases slightly until it drops to zero when the gate voltage passes V_{td}. A hysteresis between V_{td} and V_{tu} is evident with a hysteresis width of $V_{hy} = V_{tu} - V_{td} = 0.9$ V. At $V_g = -2.86$ V, the current is $I_h = 0.5\,\mu$A in the down-sweep and $I_l = 500$ pA in the up-sweep. Thus, the on-off current ratio I_h/I_l is 1000. One can see when the minimum gate voltage is reduced to $V_{gm} = -3.9$ V, that the down-sweep trace remains almost unaltered with a similar value V_{td}, while the up-sweep trace differs significantly. V_{tu} shifts to higher gate voltages with $V_{tu}(V_{gm} = -3.9\,\text{V}) = 3.3\,\text{V} > V_{tu}(V_{gm} = -3.5\,\text{V})$.

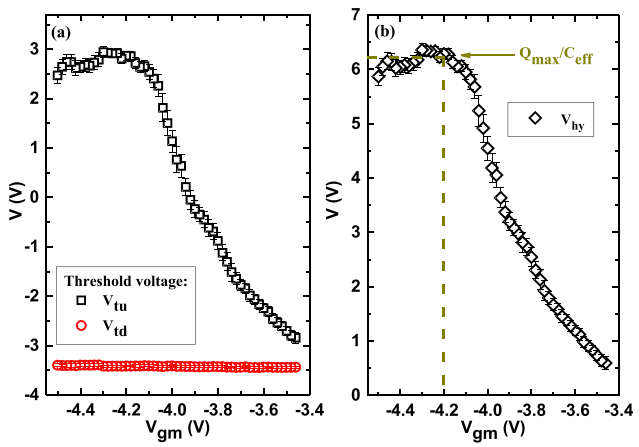

FIG. 2. (a) Threshold voltages V_{tu} and V_{td} versus minimum gate voltage V_{gm}. V_{td} is independent of V_{gm}. V_{tu} shifts from -2.8 to $+2.8$ V when V_{gm} is reduced from -3.46 to -4.50 V and saturates below $V_{gm} = -4.2$ V. (b) Hysteresis width V_{hy} versus minimum gate voltage V_{gm}. V_{hy} reaches a maximum of $V_{hy} = 6.2$ V below $V_{gm} = -4.2$ V with a maximum charge occupation Q_{max} on the QD. For $V_{gm} = -3.46$ V, the width of the hysteresis is still 0.6 V.

Experimentally determined dependencies of V_{td} and V_{tu} on V_{gm} are shown in Fig. 2(a). The measurements were conducted in the following way. V_{gm} was first set to a constant value, e.g., -3.46 V. Then, the gate voltage was swept at a constant sweep rate of $\Delta V_g/\Delta t = 0.2$ V/s from V_{gm} to $V_g = 4.5$ V and back to V_{gm}. V_{tu} and V_{td} were determined. Such measurements were repeated several times. Each data point in Fig. 2(a) represents the average value of forty closed gate voltage cycles. This procedure was performed for V_{gm} from -3.46 to -4.50 V. As depicted in Fig. 2(a), V_{tu} increases from -2.8 to $+2.8$ V when V_{gm} is lowered but saturates below $V_{gm} \approx -4.2$ V. In contrast V_{td} remains constant and is independent of V_{gm}.

The shift of the threshold voltage ΔV_{tu} to higher values for a reduction of V_{gm} is explained by the charging of the central QD with $\Delta V_{tu} = \Delta Q/C_{eff}$.[1,3,9] The capacitance C_{eff} describes the Coulomb coupling between the gate, the QD, and the channel for a given amount of QD localized charge $Q = nq$. Here, q is the elementary charge and n is the number of electrons. Thus, the $V_{tu}(V_{gm})$ curve shows that a reduction of V_{gm} corresponds to an increased amount of electrons on the QD with $Q \propto V_{gm}$. Interestingly, the charging process of the QD occurs when the quantum wire is depleted for gate voltages smaller than V_{td}. We emphasize that the observed charging process at negative gate voltages is in contrast to the typical floating gate function of transistors with a top gate structure, in which charging is observed for positive gate voltages.[1,12,13] The negative charging voltages are attributed to the side-gate geometry. Here, the in-plane gates result in a more efficient shift of the electrostatic channel potential compared to the potential change of the floating-gate. Thus, at negative gate voltages, the electrostatic channel potential exceeds the one of the quantum dot so that the QD becomes charged.

Since V_{td} is independent of V_{gm}, the charge on the centered QD remains constant during the down-sweep. The instantaneous jump of the current at the gate voltage $V_g \approx 4$ V (see Fig. 1(c)) thus corresponds to a pronounced discharging of the QD. Time-resolved measurements show that the discharging process occurs in the μs range.

Fig. 2(b) displays the width of the hysteresis $V_{hy} = V_{tu} - V_{td}$ versus the minimum gate voltage V_{gm} as obtained from the data depicted in Fig. 2(a). Since V_{td} is independent of V_{gm}, V_{hy} follows the threshold voltage V_{tu} of the up-sweep. The maximum hysteresis width is $V_{th} \approx 6.2$ V for V_{gm} smaller than -4.2 V and a maximal QD charge occupation Q_{max} is reached. For $V_{gm} = -3.46$ V, the hysteresis still has a value of $V_{hy} \approx 0.6$ V and the QD is partially charged even for $V_{gm} \approx V_{td}$. In contrast to the discharging, which results in the steep current increase, the charging of the QD occurs for a pinched-off channel. Thus, the charging time cannot be extracted directly from the I-V_g characteristic.

Fig. 3 depicts the waiting time dependence of V_{hy} for $V_{gm} = -3.60$, -3.70, and -3.75 V. The waiting time measurements were conducted in the following way. At $t = 0$ s, V_{gm} was set and kept constant for a given waiting time. Then, the gate voltage was swept from V_{gm} to $V_g = 4.5$ V

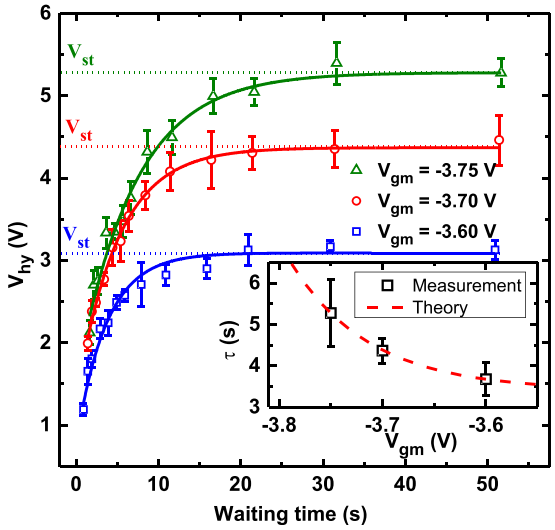

FIG. 3. Waiting time dependence of V_{hy} for $V_{gm} = -3.60$, -3.70, and -3.75 V. For constant V_{gm} and increasing waiting time, V_{hy} growths until the saturation voltage V_{st} is reached. For waiting times of 50 s, V_{st} increases when the minimum gate voltage is reduced. The solid lines are exponential fit functions according to Eq. (1). Inset: The charging time τ decays exponentially with increasing V_{gm}.

(and back) at a constant sweep rate with $\Delta V_g/\Delta t = 0.2$ V/s. For each sweep cycle, V_{td}, V_{tu}, and V_{hy} were obtained and each data point in Fig. 3 corresponds to the average of five sweep cycles. When the waiting time is varied from 0 to 50 s for $V_{gm} = -3.60$ V, V_{hy} increases from 1.19 V until it saturates at $V_{hy}(t = 50\,\text{s}) = V_{st} = 3.10$ V. For a reduction of V_{gm}, the V_{hy}-waiting time curves behave qualitatively similar but V_{st} increases to 4.37 ($V_{gm} = -3.70$ V) and 5.27 V ($V_{gm} = -3.75$ V).

We interpret the time evolution of V_{hy} in the following way. By setting V_{gm} at $t = 0$ s, the electrochemical potentials of the QD μ_q and the source contact μ_s differ with $\mu_s > \mu_q$. The electrochemical potentials then start to align by charging of the QD via electron tunneling from the source contact until $\mu_s = \mu_q$. Fig. 3 thus resembles the time resolved charging of a capacitor and the time evolution of V_{hy} for each V_{gm} can be described by[15]

$$V_{hy} = (V_{st} - V_0)\left[1 - \exp\left(\frac{-t}{\tau}\right)\right] + V_0, \qquad (1)$$

where τ is the charging or RC time constant given by the capacitance C and resistance R. V_{st} is the saturation threshold voltage and V_0 considers dynamic effects of charging. The fit functions of the data from Fig. 3 with Eq. (1) lead to charging times of (5.3 ± 0.8), (4.4 ± 0.3), and (3.6 ± 0.4) s for $V_{gm} = -3.75$, -3.70, and -3.60 V, respectively. Remarkably, τ is in the order of a few seconds. τ versus V_{gm} is shown in the inset of Fig. 3. One can estimate the tunneling resistance R by $\tau = RC$. The capacitance C of the QD is approximated by a planar disk with diameter $d = 100$ nm. With the dielectric constant of AlGaAs $\varepsilon_r = 12.3 \times \varepsilon_0$ (ε_0 is the vacuum permittivity) we obtain $C = 4\varepsilon_r d = 43$ aF.[16] The corresponding resistances R are 1.2, 1.0, and 0.8×10^{17} Ω for $V_{gm} = -3.75$, -3.70, and -3.60 V, respectively. According to our observations an increase of the QD diameter would lead to larger capacitances, which in turn increases the charging times. We associated the

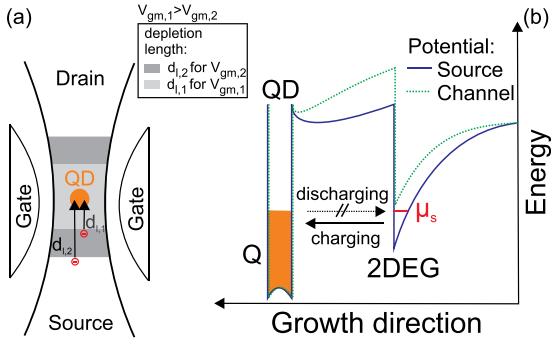

FIG. 4. Schemes of the charging time-gate voltage relation for $V_{gm,1} > V_{gm,2}$. (a) The central QD is charged when the 2DEG below the QD is depleted by the applied gate voltage. The electron tunneling distance from the source to the QD is enhanced with $d_{l,2} > d_{l,1}$ when $V_{gm,1} > V_{gm,2}$. The QD is charged over a distance of several 100 nm from the source contact of the device. The discharging of the QD to the channel is blocked, because the electrostatic potential of the channel below the QD (b) is above the electrochemical potential of the QD. This results in a blockade for discharging the QD.

observed charging times τ in the order of seconds with huge tunneling resistances. For clarity, Fig. 4 shows schemes of the device from the top (a) and conduction band profiles (b).

The top view image in Fig. 4(a) depicts the depletion region for two minimum gate voltages $V_{gm,1}$ and $V_{gm,2}$ with $V_{gm,1} > V_{gm,2}$. The depletion length d_l from the center of the QD to the contacts of the wire increases from $d_{l,1}$ to $d_{l,2}$ when the gate voltage is reduced from $V_{gm,1}$ to $V_{gm,2}$. We assume that the voltage dependent barrier width can be described by $d_l = \alpha(V_{gm} - V_{td})$ for $V_{gm} < V_{td}$ and $\alpha < 0$. We further assume that the charging can be explained by tunneling through a single barrier for which the tunneling resistance R is proportional to $\exp(2d\sqrt{2m * \Delta E}/\hbar)$,[14,17] where d is the barrier thickness which equals $\sqrt{d_l^2 + (40nm)^2}$, m^* is the effective mass, and $\hbar$ is the reduced Planck constant. ΔE is the energetic difference between the top of the barrier and the electron energy. Thus, with $\tau = RC$, the charging time is proportional to $\exp(\beta(V_{gm} - V_{td}))$. β accounts for the constants α, m^*, $\hbar$, and ΔE. This exponential dependence of τ on the gate voltage is shown in the inset of Fig. 3.

In Fig. 4(b), schemes of the conduction band along the growth direction are shown for the source region and the channel below the central QD. The QD becomes charged with electrons from the source contact up to the electrochemical potential μ_s. The electrochemical potential of the channel remains constant and thus no free electron states exist directly below the QD as the conduction band minimum is above μ_s. Thus, increasing the gate voltage results in free electron states in the channel and the QD becomes discharged at $V_g \approx 4$ V. At this gate voltage, electrons can overcome the AlGaAs/GaAs barrier at the interface which reduces the tunneling barrier to about 20 nm, which leads to a significantly faster discharging process compared to the charging process. This is reflected in the steep current increase in Fig. 1(c).

To summarize, we have fabricated and measured a QD floating gate transistor based on a modulation doped GaAs/AlGaAs heterostructure with site-controlled InAs QDs. The central QD becomes charged at negative and discharged at positive gate voltages. We observed charging times in the

order of several seconds when the gate voltage is in a critical range between −3.5 and −3.9 V. The presented single QD floating gate transistor may be used to realize low energy consuming memories or logic functions.

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