Chemical Vapor Deposition of α-Boron Layers on Silicon for Controlled Nanometer-Deep p^+n Junction Formation

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Nanometer-thick amorphous boron (α-B) layers were formed on (100) Si during exposure to diborane (B_2H_6) in a chemical vapor deposition (CVD) system, either at atmospheric or reduced pressures, at temperatures down to 500°C. The dependence of the growth mechanism on processing parameters was investigated by analytical techniques, such as transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS), in conjunction with extensive electrical characterization. In particular, devices fabricated by B deposition effectively demonstrated that p^+ doping of the silicon substrate can be achieved within 10 nm from the surface in a manner that is finely controlled by the B_2H_6 exposure conditions. High-quality, extremely ultrashallow, p^+n junctions were fabricated, and their saturation current was tuned from high Schottky-like values to low deep pn junction-like values by the increasing of the deposited B layer thickness. This junction formation exhibited high selectivity, isotropy, spatial homogeneity, and compatibility with standard Si device fabrication.

Key words: Boron (B), diborane (B_2H_6), chemical vapor deposition (CVD), silicon doping, ultrashallow junctions

INTRODUCTION

In the semiconductor industry, diborane (B_2H_6) gas is widely used for in situ p-doping during epitaxial growth of silicon layers. Other conventionally used p-doping techniques are based on diffusion into the silicon from a gas source, and they implement B diffusion in an oxidizing ambient. As an alternative to these techniques, a few studies have demonstrated p-like doping behavior of n-type (100) Si surfaces after exposure solely to B_2H_6 in an oxygen-free atmosphere.[1–4] In this case, the diborane-based doping reaction relies on the thermal decomposition of the source gas, whereby the available boron atoms may stick to the surface, chemically react with silicon atoms, and diffuse into the substrate. At the same time, the exposure can promote the segregation of the dopants and the formation of a distinct boron layer.[5,6] While the temperature and the resulting reaction kinetics mainly determine the final composition of the deposited film and the actual boron doping of the silicon substrate,[7,8] the boron concentration at the Si surface can be significantly increased beyond the solid solubility in Si by the appropriate variation of the source gas parameters and the exposure time. Although, in these earlier studies, a few experiments were performed at approximately 600°C, where a few nanometers-thick B layer was shown to form,[4,7] the bulk of the work focused on temperatures around 800–900°C, where substantial B doping of the Si is expected and silicidation of the surface is achieved, rather than the formation of a pure amorphous (α) B layer.

In this paper we show that the deposition of pure B at temperatures from 500°C to 700°C can be very attractive for the direct formation of extremely ultrashallow junctions, i.e., no subsequent (rapid) thermal anneals are necessary. Deposition is performed on a (100) Si surface during exposure to diborane in a commercially available atmospheric chemical vapor deposition (CVD) reactor.[9] An α-B

layer is readily deposited at these low temperatures. It was used in our experiments both as an abundant source of dopants and as an instrument to tune the saturation current of the diodes from high Schottky-like values to low deep *pn* junction-like values. The latter can be achieved even in situations where the actual doping of the silicon may be far less than 10 nm deep. This property has been exploited with advantage in p^+n diodes fabricated at 700°C for application as deep ultra-violet (DUV) photodiodes. The penetration depth of DUV light of 193 nm wavelength is only about 5.5 nm in Si, but, with these diodes, the theoretically maximum sensitivity is practically obtained.[10]

Here, the focus was placed on an extensive investigation of the B-deposited layers: an analytical characterization employing transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) was coupled to the electrical characterization of test structures incorporating the layers. The results were assessed with respect to reliable implementation of this type of junction in Si devices.

EXPERIMENTAL PROCEDURES

Deposition of the B layers was performed in an ASM Epsilon One reactor by CVD at either atmospheric pressure (AP), i.e., 760 Torr, or reduced pressures (RP), such as 60 Torr or 36 Torr. The deposition itself was monitored for processing temperatures ranging from 500°C to 800°C. Diborane (B_2H_6) was injected into the reactor chamber as the dopant gas with a typical flow rate of 490 standard cubic centimeters per minute (sccm), while hydrogen (H_2) was used as the carrier gas and for dilution of the doping source. Rotation of the sample can provide homogeneous exposure, preventing gas depletion phenomena. Nevertheless, the influence of the doping gas flow on the deposition process was also investigated for various diborane partial pressures (10^{-8}–10^{-3} Torr). For a given temperature, ambient pressure and diborane concentration, the boron coverage of the Si surface and the doping of the crystalline silicon substrate can be controlled by the variation of the deposition time. The results presented here correspond to exposures in the range of 1 s to 30 min.

It is known that the boron atoms will not be adsorbed on SiO_2,[2,7,8] so it is crucial that an oxide-free Si surface be provided for the deposition. This is achieved by first treating the substrates by conventional wet cleaning and HF dipping. In the reactor itself, any remaining native SiO_2 is removed before B_2H_6 exposure by an in situ thermal cleaning step in H_2 ambient at 900°C for 30 min. In the case of a patterned SiO_2 layer being used as a hard mask for selective B deposition, the pre-bake step should be carried out at AP to avoid high-temperature silicon dioxide decomposition.[11] With appropriate wafer pre-cleaning, for example with Marangoni

drying as the last step, it is also possible for the in situ thermal cleaning to be performed at lower temperatures, such as 700°C.

The number of boron atoms in the as-deposited layers was monitored by SIMS, with an O_2^+ primary ion beam at 2 keV or, alternatively, at 1 keV or 750 eV for higher resolution. On the other hand, oxygen levels were monitored by the use of Cs^+ primary ions at 3 keV. To obtain an accurate SIMS signal from the surface, we sputtered a 100 nm layer of amorphous silicon (α-Si) onto the samples at room temperature after the boron deposition. The same was done on the specimens used for analysis by transmission electron microscopy (TEM), where 20 nm physical vapor deposition (PVD) α-Si was used as a contrasting layer.

All our experiments were performed on (100) Si wafers. Electrical test structures were fabricated on either *n*- or *p*-type 2–5 Ω cm substrates. The former were used for the sheet resistance and capacitance–voltage measurement structures, for which the B layer was prepared uniformly over the wafer and covered with a 230 nm plasma-enhanced chemical vapor deposition (PECVD) tetraethylorthosilicate (TEOS) oxide. The B layer itself was in contact with pre-fabricated implanted p^+ plugs, via contact windows, and PVD Al/Si(1%) metallization of both the front and back of the wafer provided electrodes to the *n*-wafer as well as the *p*-type regions and gates on the front. The sheet resistance of the B layers was determined by differential electrical measurements on ring-shaped test structures similar to those described by Evseev et al.[12]

For diode fabrication, we reduced the series resistance by processing *p*-type wafers with a 0.9 μm *n*-doped epitaxial layer ($\sim10^{16}$ cm^{-3}) on an n^+ buried layer that was in contact with implanted n^+ plugs. In some cases the surface doping was increased to a concentration of $\sim10^{17}$ cm^{-3} by the implanting of phosphorus through a 30 nm-thick thermal oxide. Then, a 300 nm low-pressure chemical vapor deposition (LPCVD) TEOS oxide surface isolation layer was deposited, in which the contact windows to be treated by B deposition were plasma etched with wet landing on the Si. Different boron layers were deposited at AP with a B_2H_6 flow rate of 490 sccm, after which the contact windows were metallized with PVD Al/Si(1%). After metal patterning of all types of electrical test structures, a 400°C alloy step in forming gas was performed.

TEM ANALYSIS

Boron Layer Morphology and Growth Rate

A high-resolution TEM image of a B layer formed after 10 min B_2H_6 exposure at 700°C in a 760 Torr ambient is shown in Fig. 1. During thermal decomposition of diborane, the high gas-source injection (490 sccm) causes boron atoms to segregate readily on the bare silicon surface in the amorphous phase, thus forming an α-B layer. In
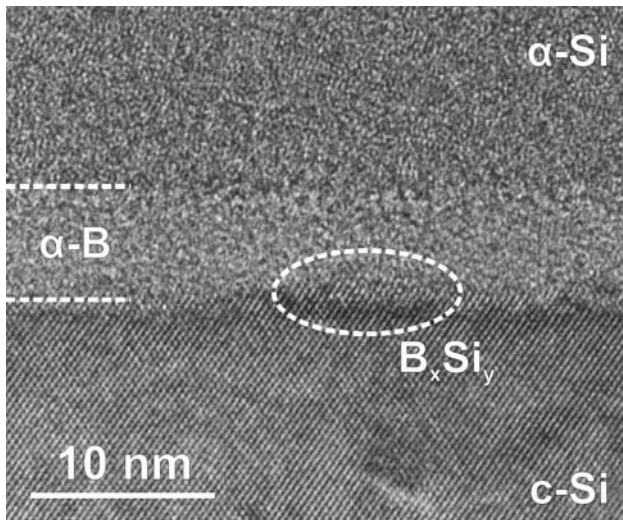
Fig. 1. High-resolution TEM image of a B layer formed after 10 min of B_2H_6 exposure at 700°C.

Fig. 2. The average B layer thickness as a function of B_2H_6 exposure time at 700°C determined from HRTEM images. For the 10 min as-deposited sample shown in Fig. 1, the physical thickness is also compared with the full width at half maximum (FWHM) of the corresponding SIMS (1 keV O_2^+) boron profile. The analytical characterization was performed on samples where B layers were deposited either (a) on blanket (100) Si surfaces or (b) in contact windows.

addition, the very high and uniform B content at the Si interface induces boron atoms to react with the silicon in a boron–silicon phase. Thus, a boron silicide B_xSi_y layer is formed, which is seen as a roughening of the c-Si surface.

Similar layer formation has been reported in the literature under comparable deposition conditions but at higher temperatures.[5–8] The segregation of the boron was shown both to prevent re-evaporation of adsorbed boron into the atmosphere and promote the reactivity of chemically adsorbed species with the surface silicon atoms. In our work it was shown that this could also be achieved with high diborane concentrations at lower temperatures, such as the 500–700°C that we used here. This suggests that the growth mechanism of the α-B/B_xSi_y layer stack is predominantly determined by the exposure time when the processing conditions are chosen so that there is a high probability that the dopant species will stick to the Si surface.

The average film thickness determined from high-resolution transmission electron microscopy (HRTEM) images is shown in Fig. 2 as a function of the B_2H_6 exposure time at 700°C. Apart from the 5 s exposure point, the time dependence of the B layer thickness for CVD on blanket Si surfaces was quite linear with a calculated growth rate of 0.4 nm/min. The deviation between the 10 min B-doped samples was probably due to the temperature calibration of the reactor chamber, which had been performed at different times.

Topography Dependence: Selectivity, Uniformity, and Isotropy

We used TEM imaging to investigate the growth of B layers performed directly in contact windows of various sizes ranging from $1 \times 1 \ \mu m^2$ to $450 \times 450 \ \mu m^2$. The windows were wet-etched into 100 nm
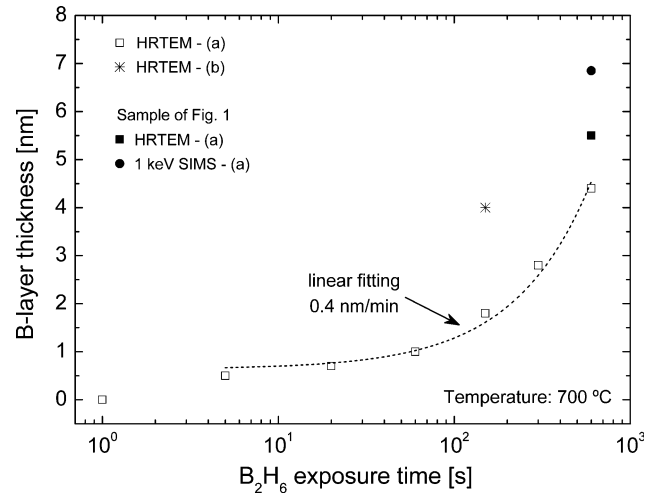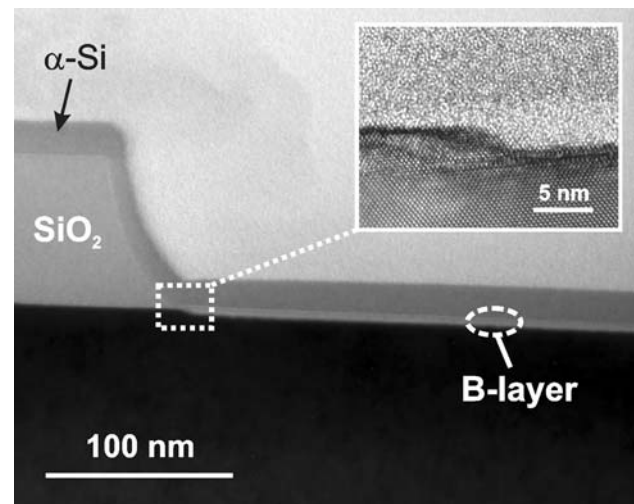

Fig. 3. TEM image of a B layer formed directly in a contact window during a 2.5 min exposure to B_2H_6 at 700°C. The CVD process is selective with respect to SiO_2 and also ensures uniform coverage of Si substrates in large area contact windows. The inset shows an enlarged view of the edge periphery and reveals an $\sim$3 nm recession of the Si with respect to the Si/SiO_2 interface.

thermal silicon oxide. The pattern dependence was studied for samples with 4 min in situ pre-bake step at 700°C followed by a 2.5 min B_2H_6 exposure at the same temperature.

The TEM image in Fig. 3 shows that the exposure to pure B_2H_6 provided selective deposition on Si: no boron can be observed on the flat or beveled SiO_2 surfaces. In the window the boron layer is seen to be continuous and uniform across the Si, with an average thickness of 4 nm independent of the
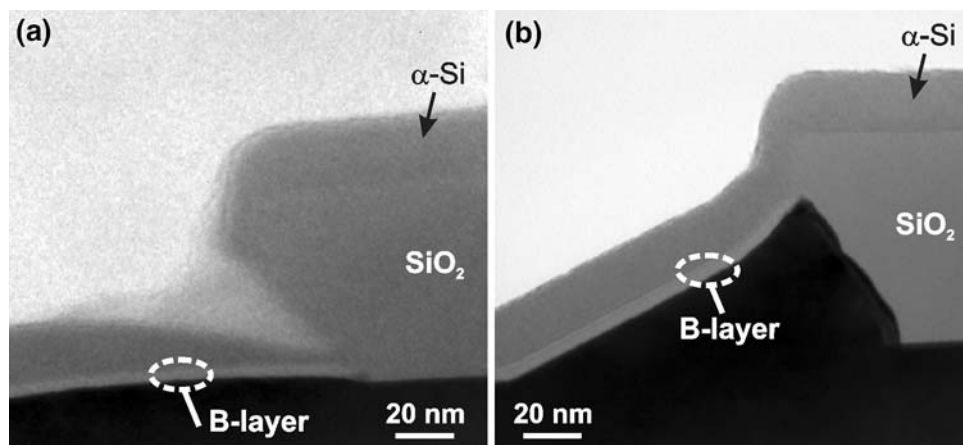
Fig. 4. TEM images of contact windows after 2.5 min of B deposition at 700°C. The SiO$_2$ etch geometry was generated by low pressure *in situ* thermal cleaning at 900°C before diborane exposure.

window sizes investigated. The film is, however, thicker than the corresponding layers in Fig. 2 that were deposited on the bare Si surface at a time when another temperature calibration of the reactor was effective.

An inspection of the window periphery revealed an ~3 nm recession of the Si with respect to the Si/SiO$_2$ interface, which, at least in part, was due to the cleaning performed before and after the sample was loaded into the reactor. Some Si consumption may also be due to the reaction with B atoms during formation of the boron silicide layer.[7]

Three different types of contact window perimeters after the 2.5 min deposition of boron can be compared in Figs. 3 and 4. The non-conventional topographies of the window edges seen in Fig. 4 were formed after in situ thermal cleaning at low pressure and at a temperature of 900°C. Under these conditions, the oxide sidewalls were steadily undercut as a result of SiO$_2$ decomposition at the perimeter of the contact opening. This was due to the reaction Si + SiO$_2$ → 2SiO, where the SiO is a volatile product.[11,13] In addition to this, on a clean Si surface, as obtained here by *in situ* H-baking, the Si atoms will be mobile and can accumulate at the perimeter of patterned areas. In all cases the CVD ensured excellent boron coverage of the silicon surface up to the oxide edge, whether a cavity or a Si mound was formed. In the latter case the B-layer thickness appeared to be independent of the c-Si surface orientation, which was evidence that the growth mechanism was isotropic.

Low-Temperature Deposition

The growth rate of the B layers, as well as the resulting layer-stack composition, is dependent on the deposition temperature.[7] At temperatures below 600°C the decomposition of diborane, although not completely dissociative, has been found to result in the formation of pure boron layers, while, at 700°C,
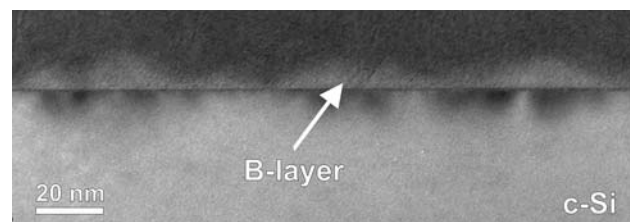

Fig. 5. TEM image of a B layer formed after a 10 min exposure to B$_2$H$_6$ at 500°C. The analysis was performed with the electron beam directed a few degrees away from [110] so that the 220 reflection was in the Bragg condition.

some reactivity with the silicon atoms is initiated and the consequent silicidation of the B layer increases with temperature.

In Fig. 5, a TEM image is shown of a substrate treated with a 10 min exposure to B$_2$H$_6$ at 500°C. A B layer was formed with an average thickness of ~6 nm, although the uniformity along the Si surface was poor in comparison with that of deposition at 700°C. In fact, at low temperatures, boron preferentially forms B-rich grains separated by regions of clean silicon, while larger rough islands are formed by coalescence of several grains after longer exposures.[8,14] On the other hand, deposition at higher temperatures, even for shorter times, exhibited better spatial homogeneity. Therefore, it is probable that high temperatures enhance the migration of species along the Si surface, besides promoting the reactivity of boron with Si atoms.

Furthermore, the bending contours of the TEM diffraction contrast image revealed the presence of local stress between the B layer and the c-Si substrate. The stress might have been induced by an altered lattice parameter at the Si surface due to the deposited B atoms. Variation in lattice plane distances could not really be discerned, although a tendency toward a lower {110} lattice plane distance, i.e., horizontal compression, was observed.

SIMS ANALYSIS

In Fig. 6 SIMS profiles are shown of B layers formed at 700°C for various deposition times. The B_2H_6 exposure was performed at AP with a flow rate of 490 sccm. Both the B peak concentrations and the integrated surface densities were extracted, and the corresponding values are presented in Fig. 7 as a function of deposition time. The SIMS analysis of these ultrashallow and highly doped layers will have been affected by the knock-on effect, which gave errors in the determination of the absolute value of boron concentration. Nevertheless, the increase in B content seen in these measurements was similar for both surface density and peak concentration, and the time dependence had a grading coefficient of 1.2. The concentration peak of the SIMS profiles seemed to saturate at the equivalent atom density of pure amorphous boron for very long exposures. On the other hand, the time dependence of the surface density showed that the saturation coverage occurred within the first 20 s, followed by a transition to the non-self-limiting segregation of boron. As is also visible from TEM images and indicated in Fig. 2, after 5 s the boron coverage started to exceed the surface atomic density of one monolayer (ML), which corresponded to 6.78×10^{14} cm^{-2} on (100) Si. High-resolution SIMS profiling was performed on the sample with a 10 min B deposition time, and the full width at half maximum (FWHM) value is also included in Fig. 2.

Besides the silicon–boron reaction at the c-Si interface, impurity diffusion into the substrate also occurs during layer growth. To study this effect, we obtained better depth resolution by removing the as-deposited α-B layer in the standard cleaning solution of boiling HNO_3 (110°C, 65%). The corresponding B and O profiles are shown in Fig. 8. This cleaning step completely dissolved the high boron peak region ($>10^{23}$ cm^{-3}), which supports the assumption that it is a metal-like boron layer.[7,15] The oxygen delta profile, which was only ~3 nm wide, was most likely due to cleaning-induced oxidation of about 1.3 nm of Si (assuming that the Si thickness was 0.455-times the oxide thickness). A 4 min dip-etch in an HF solution (0.55%) removed the oxide.

After the HNO_3 treatment, the boron SIMS profile revealed a concentration peak of 6×10^{20} cm^{-3} that was slightly reduced by HF dipping, showing that some boron atoms were also incorporated into the cleaning-induced oxide. A similar high boron concentration (8×10^{20} cm^{-3}) was also seen in a
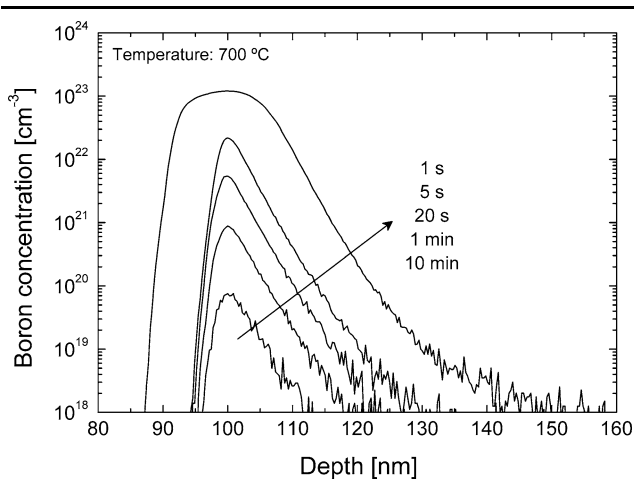

Fig. 6. SIMS profiles of B layers formed by CVD for 1 s to 10 min at 700°C. For comparison, the point of peak B concentration has been moved to 100 nm in all cases.
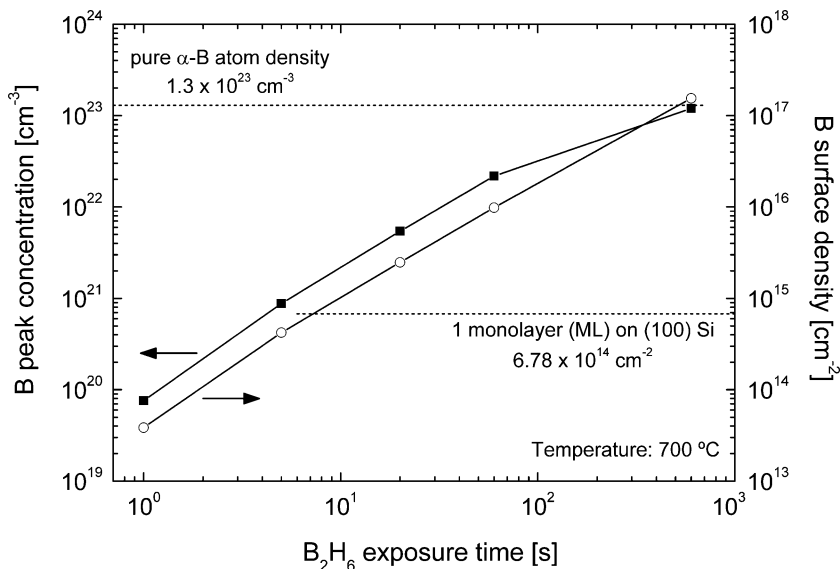

Fig. 7. B_2H_6 exposure time dependence at 700°C of boron peak concentration (left side y-axis) and surface density (right side y-axis) as determined from SIMS profiles.
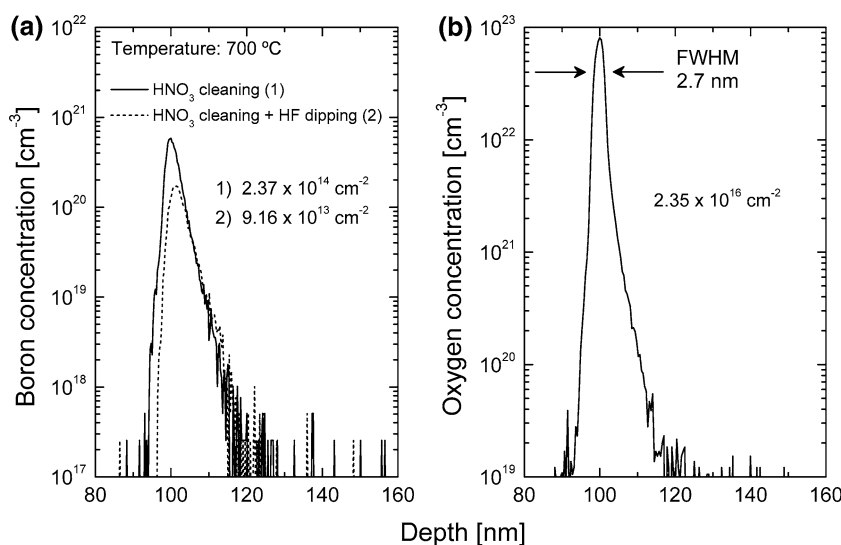
Fig. 8. (a) Boron and (b) oxygen SIMS profiles of as-deposited B-doped layer after 10 min B_2H_6 exposure and standard cleaning in boiling HNO_3. The boron profile resulting from the removal of the cleaning-induced oxide with an HF dip is also shown.

750 eV SIMS analysis. Since these levels considerably exceeded the B solid solubility at 700°C in bulk Si,[16] the surface peak was attributed to the high boron content in the B_xSi_y layer, which was only partly oxidized and removed during the HNO_3 + HF cleaning sequence.

The inherent SIMS widening of the profiles might have been limiting the resolution, and the actual extent of B diffusion into the silicon substrate could not be accurately determined. However, it is noteworthy that the point at which the doping concentration was equal to 10^{18} cm^{-3} was within 10 nm of the surface.

ELECTRICAL CHARACTERIZATION OF SURFACE DOPING

In this section we describe the electrical measurement of sheet resistances and depletion-type metal-oxide-semiconductor (MOS) capacitors that were used to determine the active boron concentration in the silicon substrate. The corresponding junction depth was extracted from capacitance–voltage profiling. The boron layer was deposited at AP with a B_2H_6 flow rate of 490 sccm.

Sheet Resistance Measurements

In Fig. 9 the extracted sheet resistance ρ_s is shown for samples with a 10 min deposition time at temperatures ranging from 500°C to 800°C. In addition, the time dependence of ρ_s is also shown for B_2H_6 exposures performed at 700°C. The reduction of the sheet resistance with either the deposition temperature or time was reasonably consistent with the expected diffusion rate of boron into the silicon. Higher dopant activation was obtained with increasing temperatures, and this, in turn, reduced the influence of the substrate bias voltage on ρ_s, as

seen in Fig. 9a. Above 700°C, a boron silicide film is formed,[7,8] but of relatively thin layers of a few nanometers. The lateral conductivity should still be dominated by impurity diffusion if the reported resistivity values for B-Si phases of 0.2–20 Ω cm apply.[17,18]

Sheet resistance measurements of B-exposed areas were also performed after HNO_3 cleaning and HF dipping until a hydrophobic surface was achieved. This removal of the B layer significantly increased the sheet resistance. In particular, for exposure times shorter than 5 min, the p^+ boron-doped region was either largely removed or depleted by charges in the field isolation oxide. The latter observation was confirmed by capacitance–voltage measurements, described in the following section. A summary of sheet resistance for B layers formed at 700°C with and without the HNO_3 + HF cleaning process is given in Table I.

Depletion-Type MOS Capacitors

The active boron dose diffused in the c-Si substrate during the deposition process was analyzed quantitatively by capacitance–voltage measurement of depletion-type p-channel MOS devices, since variation of the doping underneath the gate oxide can readily affect the C–V characteristics in terms of either threshold or flatband voltages.[19]

However, since the presence of the B layer was found to screen any influence of the metal/SiO_2/Si system, we removed the α-B layer before performing gate oxide deposition. Normalized C–V characteristics are shown in Fig. 10 at a measurement frequency of 500 Hz, and a schematic cross-section of the device structure is also displayed. Similar results were also achieved at higher frequencies, such as 1 MHz, and during quasi-static measurements. Nevertheless, in all cases, a shift of the C–V curve
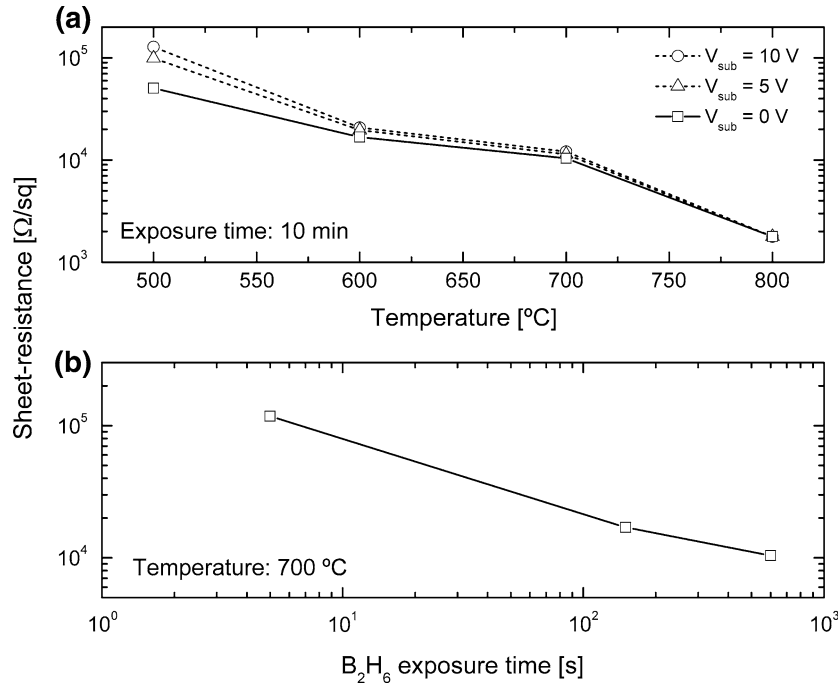
Fig. 9. Sheet resistance of B layers as a function of (a) deposition temperature and (b) B_2H_6 exposure time.

Table I. Sheet resistance of the boron layers deposited at 700°C before and after the HNO$_3$ cleaning and HF dipping sequence

Sample Description		Sheet Resistance (Ω/sq)
Exposure Time	Layer Removal	
2.5 min	No	1.7×10^4
10 min	No	1.0×10^4
≤5 min	Yes	n.l.[a]
10 min	Yes	2.5×10^5
30 min	Yes	5.9×10^4

[a]No linear I–V characteristics.

Fig. 10. Normalized C–V characteristics of depletion-type MOS structures fabricated for various minute-long B_2H_6 exposures followed by an HNO$_3$ + HF cleaning sequence. The corresponding device cross-section is shown as an inset. The measurement frequency was 500 Hz. The shift of the flatband voltage due to boron doping of the c-Si substrate is also indicated. The 1 min B-doped sample has been assumed as reference. The simulated C/C_{OX} curve (open circles) is of an equivalent enhancement-type MOS structure with $D_B = 0$.

was constantly observed for increasing deposition times. This result indicated the presence of higher boron content in the n-type c-Si substrate. Therefore, the boron doping density D_B (cm^{-2}) can be derived from the flatband voltage V_{FB} shift according to the following expression:

$$\Delta V_{FB} = V_{FB}(D_B) - V_{FB}(D_B = 0) = \frac{qD_B}{C_{OX}} \quad (1)$$

where q is the electron charge and C_{OX} is the oxide capacitance per unit area. However, the presence of a positive oxide charge density D_{OX} can shift the V_{FB} in the opposite direction. This effect is particularly visible in the C–V curve of a 1 min B-doped sample where the flatband voltage has been found to be -1.2 V. In fact, by neglecting the influence on V_{FB} of the boron doping, we could interpret the measured

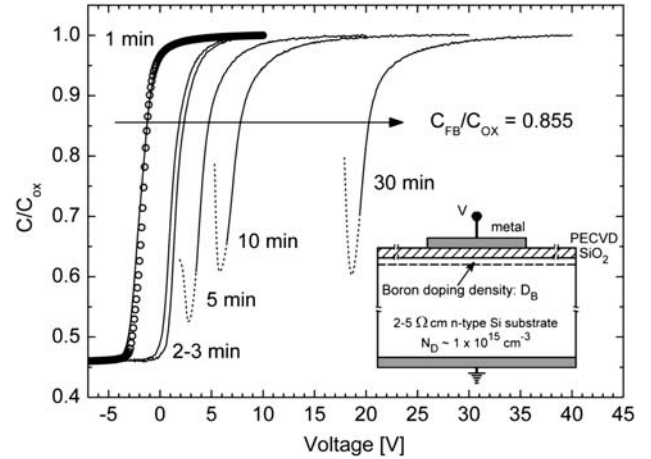curve as being an enhancement type p-MOS structure $(D_B = 0)$ with $D_{OX} = 9.25 \times 10^{10}$ cm^{-2}, as shown in Fig. 10. Therefore, this device was used as the flatband voltage reference, i.e., V_{FB} $(D_B = 0)$. Under the assumption of similar D_{OX} in all other samples, we calculated the relative boron doping densities as a function of exposure time according to Eq. 1, and they are plotted in Fig. 11 for various
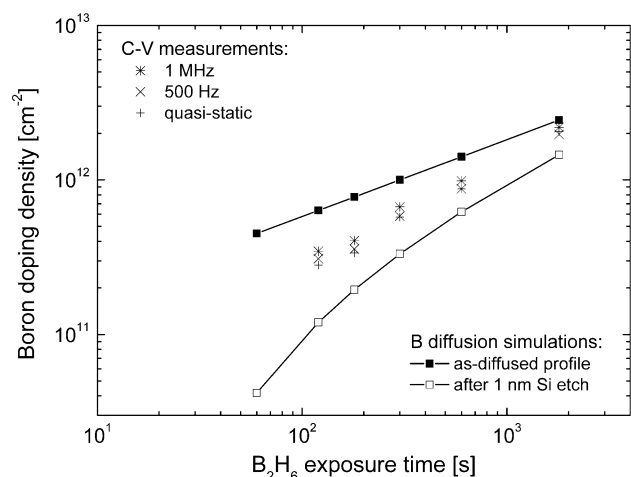
Fig. 11. Boron doping density as a function of B_2H_6 exposure time determined from the flatband voltage shift at $C_{FB}/C_{OX} = 0.855$ of the C–V characteristics for three different measurement frequency conditions. For comparison, the simulation results of boron diffusion at 700°C with a surface source are also displayed for either as-diffused profiles or after removal of a 1 nm surface Si layer.
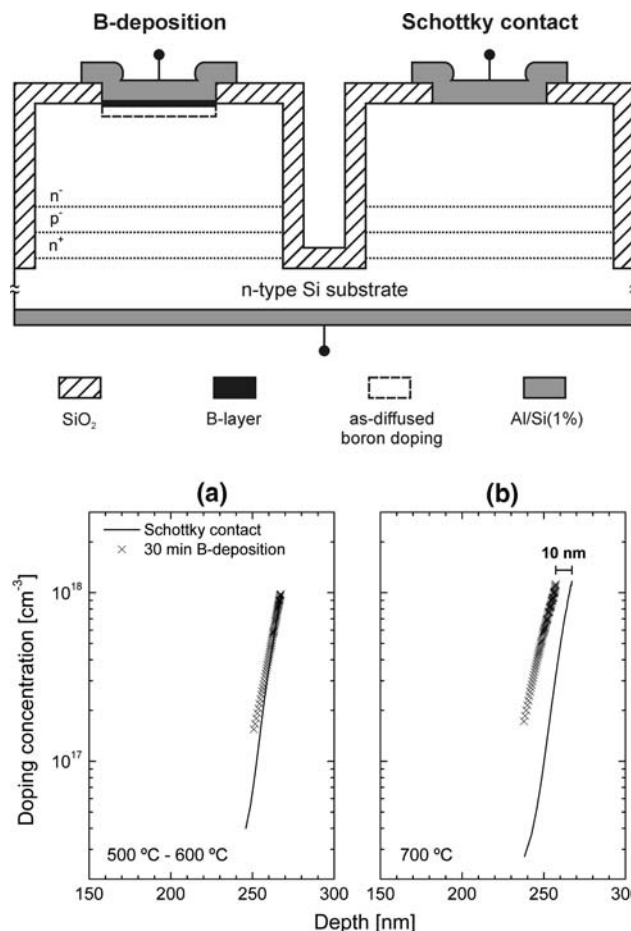

Fig. 12. (Top) Schematic cross-section of the fabricated test structure for the capacitance–voltage profiling technique, with, on the right, the Schottky diode and, on the left, the B-deposited p^+n diode. (Bottom) C–V doping profiles of the abrupt n^+ buried layer. The boron has been deposited for 30 min at temperatures of (a) 500°C and 600°C, and (b) 700°C, respectively.

measurement frequencies. In comparison, simulation results of boron diffusion at 700°C are also reported for either as-diffused profiles or after removal of a 1 nm Si surface layer, which would be a plausible effect of the cleaning sequence.

Both diffusion and Si etching were simulated with Taurus TSUPREM-4™.[20] In particular, a diffusion process can be modeled when the concentration of one or more impurities in the ambient gas is specified at the surface of the structure. In our case the growing B layer acts as the source of boron for the adjacent bulk silicon.[21] Therefore, the dopant surface concentration was varied during the simulated diffusion cycle according to the time dependence of the B-layer peak concentration as determined by the SIMS results shown in Fig. 7. The diffusion temperature and time were then defined as the experimental B_2H_6 exposure conditions. The diffusion equations and the activation of boron impurities were solved by the use of the most comprehensive models available with the default material parameters. Besides information on the diffused profile, such as boron dose and junction depth, the software is also capable of extracting electrical characteristics, as demonstrated by the simulated high-frequency capacitance–voltage curve in Fig. 10 for the enhancement-type MOS structure.

The time dependence of the measured boron densities was in good agreement with the 0.5 grading coefficient of the simulated doping process, although, for short exposures, the removal of the B layer might also have slightly reduced the number of active boron atoms incorporated into the c-Si surface. The C–V method thus overcame the limitation of sheet resistance measurements, since boron doping was also revealed to be present for deposition times of fewer than 5 min.

Capacitance–Voltage Profiling

In order to confirm that the B deposition process is suitable for fabrication of nanometer-deep junctions, the diffusion of boron atoms into the c-Si substrate has been determined with an in-house capacitance–voltage profiling technique that uses an abrupt n^+ buried layer to profile the tail of B-doped junctions at the wafer surface.[22] A schematic cross-section of the test structure is shown in Fig. 12. It is composed of two adjacent junction capacitors, one an Al to n-Si Schottky diode and the other a p^+n diode formed by the B deposition and in contact with Al. Before the patterning of these structures, the n-Si substrate was processed with an $n^- – p^- – n^+$ epitaxial layer. We isolated each diode by etching shallow trenches into the n^+-layer. By comparing the C–V profiles of the n^+-layer extracted from measuring each diode, one can set an upper limit for the depth and abruptness of the p-doping from the B deposition.

The B_2H_6 exposure was carried out at temperatures ranging from 500°C to 700°C for 30 min. In Fig. 12 the extracted profiles are shown for a test structure designed to examine a 30 min deposition of boron. For both 500°C and 600°C exposures, the curves of both the Schottky and p^+n diode essentially coincide, which suggests that a p^+-like layer was formed without any significant diffusion of dopant atoms. For the 700°C deposition, the 10 nm difference in the position of the two curves verifies that the junction depth remained limited, even after prolonged deposition times.

ELECTRICAL CHARACTERIZATION OF P^+N DIODES

Exposure Time Dependence

The diode I–V characteristics for various B deposition times at either 500°C or 700°C are shown in Fig. 13, which also includes the case without a deposited B layer, i.e., a Schottky contact directly to the substrate. First, it should be noted that all diodes show near-ideal behavior with ideality factors lower than ~1.02, thus confirming that the
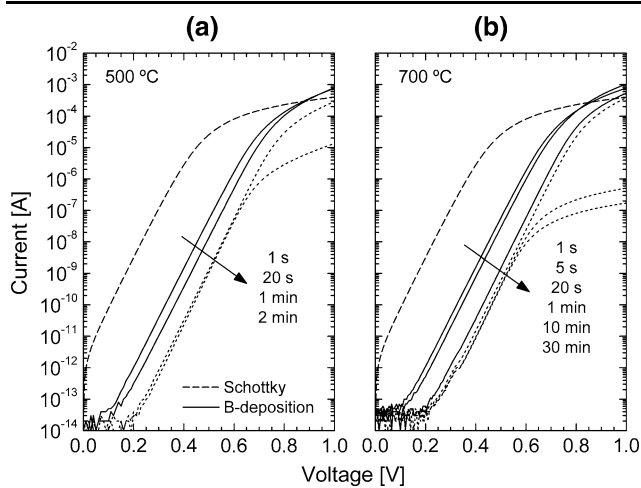

Fig. 13. Diode I–V characteristics for various deposition times at either (a) 500°C or (b) 700°C. The anode area is 2×1 μm^2. For comparison, the I–V curve of a Schottky diode is also included.

fabrication of the B layer did not introduce any defects that caused significant leakage currents. Secondly, at both deposition temperatures, an increase in the B deposition time led to a decrease in the saturation current, and a transition is seen from the high-current Schottky diode case to a low-current p^+n diode characteristic. The saturation current level reaches a minimum that is dominated by the hole injection into the substrate as governed by the Gummel number of this n-region. Electron injection from the substrate, which is normally already very significant for junctions less than approximately 20 nm deep, is apparently being suppressed by the boron surface coverage, which for the minute-long depositions is mainly composed of α-B. This is confirmed by the results reported in Table II that compares the saturation current densities of diodes fabricated with minute-long B depositions with that of a 0.7 μm-deep junction that was fabricated by the annealing of a high-dose B^+ implant. The saturation current density after 1 min of B deposition was only 3.7-times higher than that of the annealed B-implanted device, and the thicker α-B layer formed for longer exposures was instrumental in reducing the current level even further.

In addition, the series resistance that attenuated the current at high forward voltages decreased significantly with B deposition, and a minimum was reached for the 5 s deposition at 700°C. However, after 20 s the B coverage exceeded 1 ML, i.e., the α-B layer began to form, and the series resistance started to increase considerably. Similar behavior could be observed for diodes processed at 500°C, although the lower temperature delayed the boron coverage and the corresponding effect on the I–V characteristics.

From the measured series resistance and the thickness of the B layer determined by HRTEM images, it can be concluded that the grown layer had a resistivity on the order of 10^4 Ω cm. This value was in the resistivity range of 10^3–10^5 Ω cm reported in the literature for various α-B layers,[17,23] while boron–silicon compounds are generally characterized by higher conductivity. For a 30 min deposition time, the series resistance was increased

Table II. Saturation current density and junction depth of as-deposited boron diodes compared with a deep p^+n junction

Sample Description		Saturation Current Density $(A/\mu m^2)^a$	Junction Depth $(nm)^b$
Doping Technique	**Process Conditions**		
B deposition at 700°C	1 min	8.97×10^{-20}	2.5
	10 min	5.45×10^{-20}	7.5
	30 min	4.97×10^{-20}	13
B^+ implantation	3×10^{15} cm^{-2}, 15 keV, annealing: 950°C—20 min	2.44×10^{-20}	700

^{a}Extracted from measured I–V characteristics. ^{b}Determined from simulation of boron diffusion in an n-type Si substrate with uniform arsenic doping of 10^{16} cm^{-3}.

by a factor of ∼3 as compared to that obtained with a 10 min B_2H_6 exposure time. This was in good agreement with the linear time dependence of the film growth rate.

Temperature Dependence

In Fig. 14 the diode series resistance is shown as a function of CVD processing temperature for a 1×1 μm^2 diode fabricated with a 30 min B deposition. Three different regions can be distinguished, and they reveal a change in the growth mechanism and the layer composition, in agreement with the results reported by Saitoh et al.[7]

In fact, at temperatures lower than 650°C, a pure boron layer is expected to be formed by thermal decomposition of diborane, which is enhanced by increasing temperatures. Indeed, the measured series resistance confirmed the presence of a high-ohmic B film. In addition, the positive temperature coefficient suggested that the deposition of boron atoms on the silicon surface was more efficient as the temperature increased. This could be explained by an increase in hydrogen desorption from the adsorbed layer, i.e., more sites were open for further boron adsorption.[1]

The second growth regime was from about 650°C to 700°C and was characterized by a slightly lower series resistance with negligible temperature dependence. In this temperature regime, silicon began to react with the segregated boron atoms on the surface. Therefore, the high-ohmic pure boron layer was partly converted into a more conductive boron silicide region.

Finally, B_2H_6 exposure at temperatures higher than 700°C resulted in a rapid decrease in the series resistance, since the silicon–boron reaction was significantly promoted, along with faster diffusion of boron atoms into the substrate, which reduced the probability of B segregating on the surface in a pure phase.
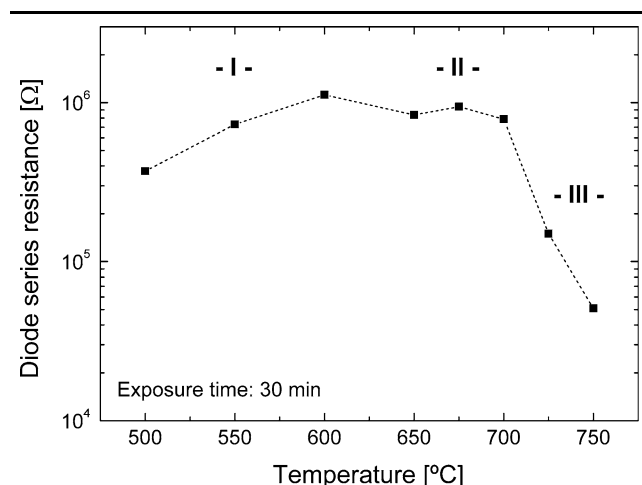
Flow Rate and Pressure Dependence

The influence of the diborane flow rate in the CVD process was investigated for three different reactor pressures, namely 760 Torr, 60 Torr, and 36 Torr, at the deposition temperature of 700°C. For a 30 min B_2H_6 exposure time, the measured diode series resistance is plotted in Fig. 15 as a function of the boron mole fraction, which, for a given B_2H_6 flow rate, was defined here as the ratio between the resulting boron partial pressure and the total ambient pressure. Diode I–V characteristics revealed that pn-junctions were formed for all these processing conditions, and the current levels decreased with increasing boron mole fraction. However, the typical high-ohmic behavior of the B layer was achieved only for B_2H_6 injection at levels as high as 490 sccm, either at atmospheric pressure or reduced pressure (RP). On the other hand, lower gas-source flow rate did not induce any segregation of boron atoms in an amorphous phase, even for long exposure times such as 30 min, and the series resistance was limited by the substrate resistivity. This dependence was similar to that reported by Kiyota and Inada,[6] where a change in the surface reaction kinetics was observed to occur for B_2H_6 concentrations higher than 6 ppm. In fact, for lower gas-source flow, the substrate was doped just as it would have been by conventional diffusion from a source with constant surface concentration. In contrast, for a higher gas flow, an adsorbed boron layer was formed and the surface boron concentration became dependent on the exposure time. Additionally, it is worth noting that the hydrogen carrier gas played an important role in the sticking of boron atoms to the Si surface. Changing the

Fig. 14. The diode series resistance as a function of deposition temperature for a 30 min B_2H_6 exposure time. The anode size is 1×1 μm^2.
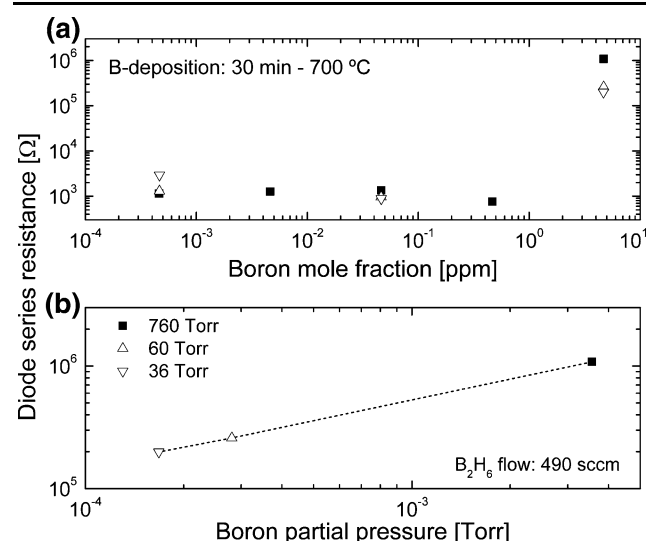

Fig. 15. The diode series resistance as a function of (a) boron mole fraction, i.e., the ratio between boron partial pressure and ambient pressure, and (b) the boron partial pressure for a B_2H_6 flow rate of 490 sccm. Deposition was performed at 700°C for 30 min by varying the total pressure from 36 Torr to 760 Torr. The anode size was 1×1 μm^2.
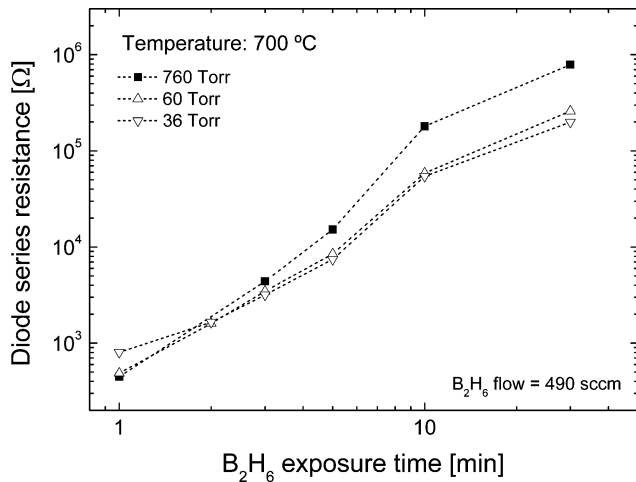
Fig. 16. The diode series resistance as a function of B_2H_6 exposure time at 700°C for three ambient pressures. The anode size is $1 \times 1 ~\mu m^2$.

carrier gas to, for example, nitrogen has been demonstrated to induce boron segregation even at lower diborane flow rate.[5]

For a diborane flow rate of 490 sccm, the series resistance increased almost linearly with the boron partial pressure, also shown in Fig. 15b. This was consistent with the theory of molecular gas dynamics, where the number of molecules impinging on a plane per unit area and time is proportional to the partial pressure of the precursor.[6] The difference between B deposition at atmospheric and RP can also be distinguished in Fig. 16 for various exposure times.

CONCLUSIONS

It has been demonstrated that the growth of boron layers on (100) Si substrates during diborane (B_2H_6) exposure in a CVD reactor can be performed such that high selectivity, excellent isotropy, and uniform coverage can be achieved. The thermal dissociation of B_2H_6 at high gas flow rates forms a reproducible and high-quality electrically active p^+-like layer, the composition of which varies from a pure boron phase to a boron–silicon compound for increasing temperatures.

Either the deposited or diffused B atoms can be quantitatively controlled by variation of the exposure time, while temperatures below 700°C can ensure an extremely limited junction depth, even after prolonged deposition times. The electrical properties were also studied by the fabrication of pn diodes that exhibited excellent characteristics in terms of ideality and saturation currents as low as those obtained with conventional deep pn-junctions. The latter is to be attributed to the presence of the α-B layer, since the current levels decrease as boron segregation occurs. With this technique, ultrashallow junctions with low series resistance can be fabricated at low thermal processing temperatures

in a manner that is compatible and attractive for many Si device configurations.

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