CHAPTER 2

Chip-Package Interaction and Reliability Impact on Cu/Low-k Interconnects

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2.1 Introduction

The exponential growth in device density has yielded high-performance microprocessors containing two billion transistors [1]. The path toward such integration continues to require the implementation of new materials, processes, and design for interconnect and packaging structures. Since 1997, copper (Cu), which has a lower resistivity than aluminum (Al), has been selected as an interconnect material to reduce the RC delay. At the 90 nm technology node, dielectric materials with k (dielectric constant) lower than silicon dioxide (SiO_2, k ~ 4) were implemented with Cu interconnects [2, 3]. As the technology advances, the interconnect structure continues to evolve with decreasing dimensions and an increasing number of layers and complexity. At this time, the effort of the semiconductor industry is focused on implementing ultralow-k (ULK) porous dielectric material ($k < 2.5$) in Cu interconnects to further reduce the RC delay (Figure 2.1) [4]. However, mechanical properties of the dielectric materials deteriorate with increase in the porosity, raising serious concerns about the integration and reliability of Cu/low-k interconnects.

For advanced integrated circuits (ICs), the packaging technology is mainly based on the area-array packages, or the flip-chip solder interconnects. This type of first-level structure interconnects the active device side of the silicon (Si) die face

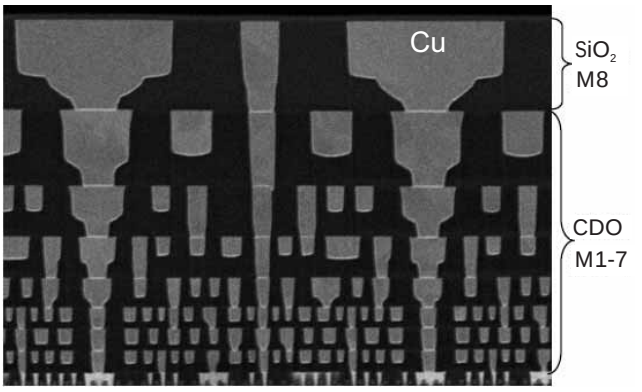


Figure 2.1 SEM image of Intel 45nm Cu/low-k interconnect structure [4].

down via solder bumps on a multilayered wiring substrate. The area-array configuration has the ability to support the required input/output (I/O) pad counts and power distribution due to the improvement of the device density and performance. With the implementation of Cu/low-k interconnects, the flip-chip package has evolved, including the implementation of organic substrates with multilayered high-density wiring and solder bumps with pitch reducing from hundreds of microns to tens of microns. Furthermore, environmental safety mandates the change from Pb-based solders to Pb-free solders, which are more prone to thermal cyclic fatigue failures and electromigration reliability problems [5, 6].

Structural integrity is a major reliability concern for Cu/low-k chips during fabrication and when they are integrated into high-density flip-chip packages. The problem can be traced to the thermomechanical deformation and stresses generated by the mismatch in thermal expansion between the silicon die with Cu/low-k interconnects and the organic substrate in the package [7]. Although the origin of the stresses in the interconnect and packaging structures is similar, the characteristics and the reliability impact for the low-k interconnects are distinctly different. At the chip level, the interconnect structure during fabrication is subjected to a series of thermal processing steps at each metal level, including film deposition, patterning, and annealing. The nature of the problem depends to a large degree on the thermal and chemical treatments used in the fabrication steps. For instance, for deposition of metal and barrier layers, the temperature can reach 400°C and for chemical-mechanical polishing (CMP), the chip is under mechanical stresses and exposed to chemical slurries simultaneously. When subjected to such process-induced stresses, the low-k interconnects with weak mechanical properties are prone to structural failure. Such mechanical reliability problems at the chip level have been extensively investigated [8].

When incorporated into the organic flip-chip package, the fabrication of the silicon die containing the interconnect structure is already completed, so the interconnect structure as a whole is subjected to additional stresses induced by the packaging and/or assembly processes. Here the maximum temperature is reached during solder reflow for die attach. Depending on the solder materials, the reflow temperature is about 160°C or higher for eutectic Pb alloys and about 250°C for Sn-based Pb-free solders. During accelerated or cyclic thermal tests, the temperature varies from –55°C to 125°C or 150°C. Although the assembly or test temperatures of the package are considerably lower than the chip processing temperatures, the thermomechanical interaction between the chip and the package structures can exert additional stresses onto the Cu/low k interconnects. The thermal stress in the flip-chip package arises from the mismatch of the coefficients of thermal expansion (CTEs) between the chip and the substrate, which are 3 ppm/°C for Si and about 17 ppm/°C for an organic substrate. The thermally induced stresses on the solder bumps increase with the distance to the die center and reach a maximum at the outermost solder row. By using underfills, the stresses at the solder bumps can be effectively reduced to improve package reliability [9]. However, the underfill causes the package to warp, resulting in large peeling stresses at the die-underfill interfaces [10, 11]. The thermomechanical deformation of the package can be directly coupled into the Cu/low-k interconnect structure, inducing large local stresses to drive interfacial crack formation and propagation, as shown in Figure 2.2. This has generated exten-

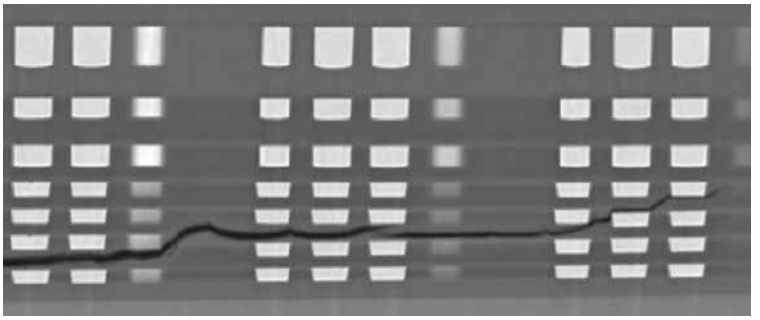


Figure 2.2 Crack propagation in a multilevel interconnect.

sive interest recently in investigating chip-package interaction (CPI) and its reliability impact on Cu/low-k structures [12–19].

In this chapter, we first review two experimental techniques important for the study of CPI and reliability, followed by a general discussion of fracture mechanics in Section 2.3. Then, a three-dimensional (3D), multilevel, submodeling method based on finite element analysis (FEA) is introduced in Section 2.4 to calculate the CPI-induced crack-driving force for interfacial delamination in the low-k interconnect structure. The chip-package interaction was found to be maximized at the die-attach step during packaging assembly and most detrimental to low-k chip reliability because of the high thermal load generated by the solder reflow process before underfilling. The discussion of the chip-package interaction in Sections 2.5 and 2.6 is first focused on the effects of dielectric and packaging materials, including different low-k dielectrics and Pb-based and Pb-free solders. The discussion is then extended in Section 2.6 to the study of the scaling effect, where the reduction of the interconnect dimension is accompanied by more metal levels and the implementation of ultralow-k porous materials. Finally, some recent results on CPI-induced crack propagation in the low-k interconnect and the use of crack-stop structures to improve chip reliability are discussed.

2.2 Experimental Techniques

2.2.1 Thermomechanical Deformation of Organic Flip-Chip Package

Thermal deformation of a flip-chip package can be determined using an optical technique of moiré interferometry. This is a whole-field optical interference technique with high resolution and high sensitivity for measuring the in-plane displacement and strain distributions [20]. This method has been successfully used to measure the thermal-mechanical deformation in electronic packages to investigate package reliability [7, 10, 21]. The sensitivity of standard moiré interferometry is not sufficient for measuring thermal deformation in high-density electronic packages, particularly for small features, such as solder bumps. For such measurements, a high-resolution moiré interferometry method based on the phase-shifting technique was developed, which measured the displacement field by extracting the phase angle as a function of position from four precisely phase-shifted moiré interference patterns [7, 11]. Once the phase angle is obtained, the continuous displace-

ments in the horizontal (u) and vertical (v) directions can be determined. The strain components can then be evaluated accordingly:

$$\varepsilon_x = \frac{\partial u}{\partial x}, \quad \varepsilon_y = \frac{\partial v}{\partial y}, \quad \gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \tag{2.1}$$

The high-resolution moiré analysis was carried out for an experimental flip-chip package. The package was first sectioned and polished to reach the cross section of interest. A schematic of the experimental flip-chip package with the cross section that was analyzed is shown in Figure 2.3.

The moiré experiment was performed at room temperature (22°C), and the grating was attached to the cross section of the specimen at the temperature of 102°C, providing a reference (zero) deformation state and a thermal loading of –80°C, which can generate good deformation signals without introducing large noises from the epoxy [22]. An optical micrograph of the right half of the package cross section is shown in Figure 2.4.

The displacement field (u and v) phase-contour maps generated from the phase-shifting moiré interferometer with fringe spacing of 208 nm are shown in Figure 2.5. An outline of the interfaces obtained from the optical micrograph is superimposed onto the phase contour to highlight the local change of the displacement field in various packaging components. The global deformation of the u and v

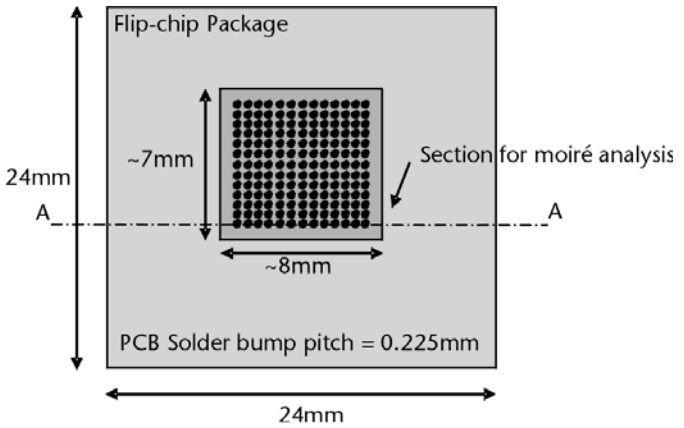
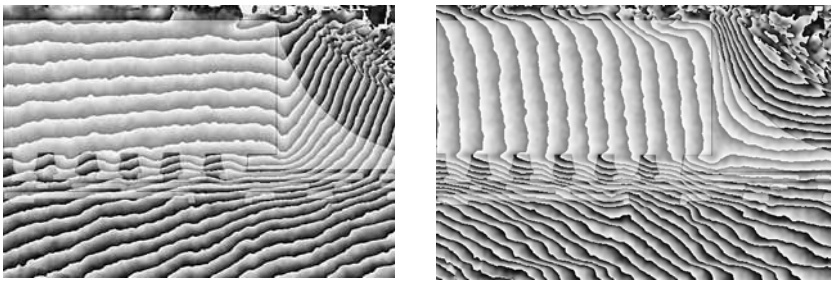


Figure 2.3 Schematic of a flip-chip package for moiré interferometry study, where the optical grating was attached to the cross section as indicated for moiré measurements.

Figure 2.4 Optical micrograph for the package cross-section used for moiré interferometry study.



(a) (b)

Figure 2.5 Phase contour maps obtained by high-resolution moiré interferometry for the flip-chip package in Figure 2.3: (a) *u* field and (b) *v* field.

fields shows overall bending contours of the package due to warpage. This gives rise to the *u* field with relatively smooth horizontal (*x*) displacement distribution, while the *v* field displays high-density fringes in the solder bump/underfill layer, which is caused by the high coefficient of thermal expansion (CTE) in this layer. The die corner at the lower right has the highest shear strain, which can be seen from the large displacement gradient along the vertical (*y*) direction in the *u* field.

The phase contours in Figure 2.5 were used to map the displacement and strain distributions in the flip-chip package. The results are illustrated in Figure 2.6, where the displacement and strain distributions are determined along three lines: the sili-

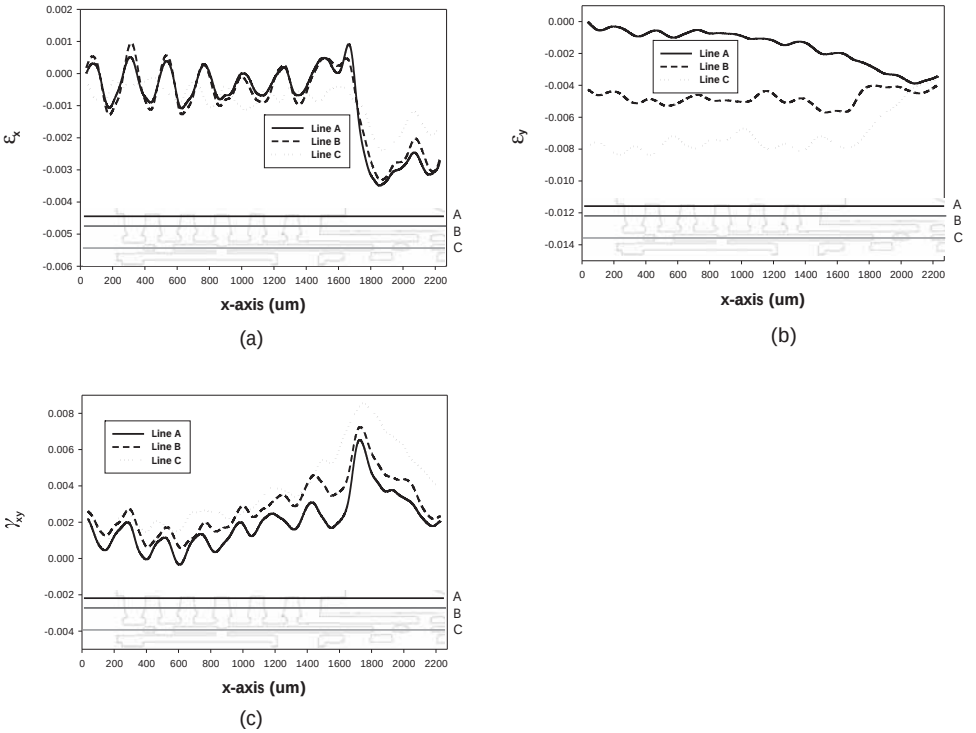


Figure 2.6 (a–c) Distributions of strains induced by chip-package interaction along three lines: the silicon-solder interface (Line A), the centerline of solder bumps (Line B) and the centerline of the high density interconnect wiring layer above the substrate (Line C).

con-solder interface (line A), the centerline of solder bumps (line B), and the centerline of the high-density interconnect wiring layer above the bismaleimide triazine (BT) substrate (line C). Overall, the normal strains ε_x and ε_y show the existence of a positive peeling stress in the bottom fillet area, while the shear strain γ_{xy} reaches a maximum in the fillet of the underfill near the lower die corner, corresponding to the most critical stress concentration in the package. The strain components generally increase toward the edge of the packaging as expected and can reach a value as high as 0.6% under a thermal load of –80°C for the outermost solder bump. Thus, the strain induced by the package deformation is about three to five times larger than the thermal strain caused by thermal mismatch between the die and Cu/low-k interconnect. It can be directly coupled into the low-k interconnect structure near the outermost solder bumps to drive crack formation. This underscores the importance of chip-package interaction in causing interfacial delamination in the interconnect structure, particularly with the incorporation of the low-k dielectric with weak thermomechanical properties.

2.2.2 Measurement of Interfacial Fracture Toughness

As a thermodynamic process, crack growth is driven by the release of stored strain energy in the material. The driving force for fracture is hence defined as the amount of strain energy released per unit area of crack growth, namely, the *energy release rate* (ERR). On the other hand, the resistance to crack growth is the energy required to break the bonds, create new surfaces, and generate dislocations or other defects near the crack tip. The total energy required to grow the crack by a unit area is defined as the *fracture toughness* of the material. A fracture criterion is thus established by comparing the energy release rate with the fracture toughness [8].

Fracture toughness (or critical energy release rate) is a key component for the reliability assessment of microelectronic devices. Measuring fracture toughness as a property of the material or interface is thus a critical procedure for materials characterization for interconnects and packaging. Over the last 20 years, advances in fracture mechanics for thin films and layered materials [8, 23] have provided a solid foundation for the development of experimental techniques for the measurement of both cohesive and interfacial fracture toughness. This section discusses experimental techniques commonly used to measure fracture toughness of low-k interfaces.

While a single-valued fracture toughness is typically sufficient for characterizing cohesive fracture in a homogeneous material, the interface toughness must be properly characterized as a function of the mode mix, namely, the ratio between shearing and opening stresses near the crack tip. Consequently, different test structures and load conditions are often necessary for interface toughness measurements [23, 24].

Among many different measurement techniques, the double cantilever beam (DCB) [25, 26] and four-point bend (FPB) techniques [26–28] are most popular in microelectronics applications. Both techniques sandwich one or more layers of thin-film material between two thick substrates (typically Si) so that the whole specimen is easy to load. Because the substrates are much thicker than the films, the energy release rate for an interfacial crack advancing between a film and a substrate or between two films can be calculated from the far-field loading on the substrates (i.e., the homogeneous solutions given by Hutchinson and Suo [23]), neglecting the

thin films. For the DCB test (Figure 2.7), the energy release rate (J/m^2) under a symmetric loading (i.e., $F_1 = F_2 = P$) is given by

$$G = \frac{12\left(1 - v^2\right)P^2 a^2}{EB^2 H^3} \tag{2.2}$$

where E and v are the Young's modulus (N/m^2) and Poisson's ratio of the substrate, respectively; P is the applied force (N); a is the crack length (m); H is the substrate thickness (m); and B is the beam width (m). With a predetermined crack length, a critical load P_c to advance the crack can be determined from the load-displacement curve, and the interface toughness is then calculated by (2.2) as the critical energy release rate (i.e., $\Gamma = G(P_c)$). For the FPB test (Figure 2.8), the crack growth along the interface reaches a steady state with the energy release rate independent of the crack length:

$$G = \frac{21\left(1 - v^2\right)P^2 L^2}{16EB^2 H^3} \tag{2.3}$$

where L is the distance (m) between inner and outer loading points. The load P at the steady state can be determined from the plateau in the load-displacement diagram.

The mode mix for the sandwich specimen depends on the local conditions, including the materials and thickness of the thin films. It is rather cumbersome to

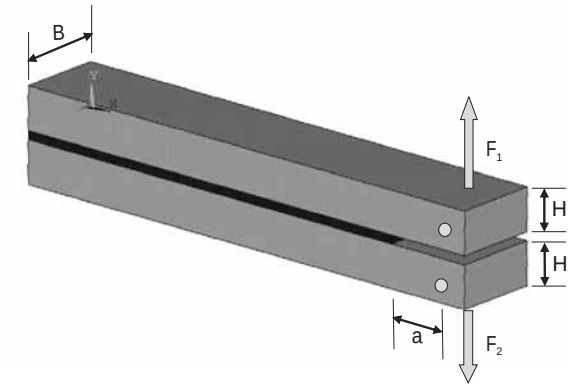


Figure 2.7 Schematic of a double cantilever beam specimen. For symmetric DCB tests, $F_1 = F_2 = P$; for mixed-mode DCB tests, the two forces can be adjusted independently (see Figure 2.9).

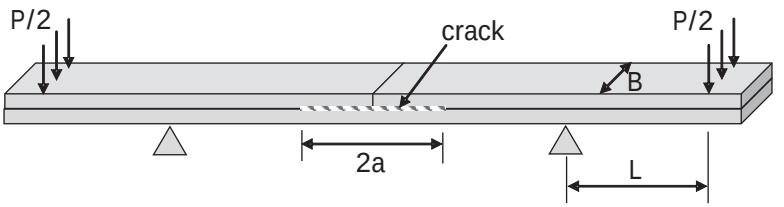


Figure 2.8 Schematic of a four-point bending test.

calculate the local mode mix when several films are sandwiched. A common practice has been to specify the mode mix for the sandwich specimens by the far-field phase angle, $\psi_\infty = \tan^{-1}\left(K_{II}^\infty / K_I^\infty\right)$, where K_I^∞ and K_{II}^∞ are, respectively, the opening and shearing modes stress-intensity factors at the crack tip [8]. For the symmetric DCB test, $\psi_\infty = 0$, hence a nominally mode I far field. For the FPB test, $\psi_\infty \approx 41°$. Other mode mixes can be obtained by using generalized laminated beam specimens loaded under cracked lap shear (mixed mode) or end-notched flexure (mode II) conditions [29] or by a modified DCB test configuration as described later.

An instrument to measure interfacial fracture energy under arbitrarily mixed-mode loading was developed using the approach originally conceived by Fernlund and Spelt [30]. This instrument utilizes a double cantilever beam (DCB) sample with a loading fixture as illustrated in Figure 2.9. By changing the positions of the different links in the link-arm structure, the forces, F_1 and F_2, applied respectively on the upper and lower beams, can be changed to adjust the mode mix. The instrument allows interfacial fracture measurements for phase angles ranging from 0° (pure tension, $F_1 = F_2$) to 90° (pure shear, $F_1 = -F_2$). Additionally, multiple tests can be run on the same sample. The challenge of this technique resides in the crack length measurement, which is required for deducing the fracture energy for the DCB configuration. The energy release rate can be calculated as

$$G = \frac{6\left(1-\nu^2\right)F_1^2 a^2}{EB^2H^3}\left[1+\left(\frac{F_2}{F_1}\right)^2 - \frac{1}{8}\left(1-\frac{F_2}{F_1}\right)^2\right] \tag{2.4}$$

The phase angle varies as a function of the ratio F_1/F_2:

$$\psi = \arctan\left(\frac{\sqrt{3}}{2}\frac{\left(\frac{F_1}{F_2}-1\right)}{\left(\frac{F_1}{F_2}+1\right)}\right) \tag{2.5}$$

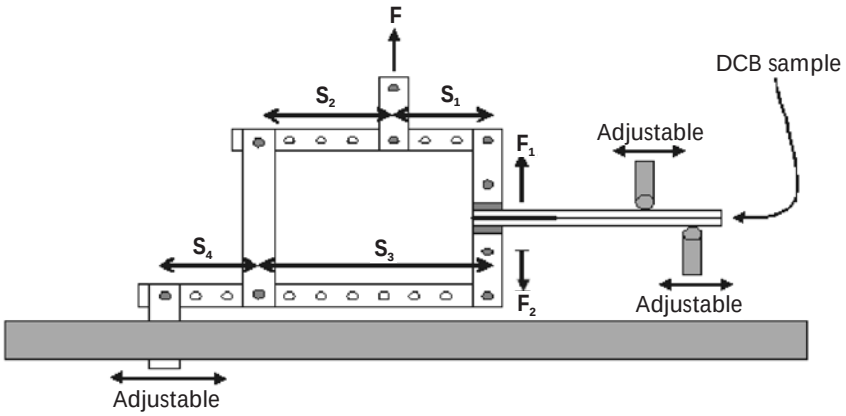


Figure 2.9 Mixed-mode double cantilever beam test loading fixture.

This mixed-mode DCB test can measure the interface toughness as a function of the phase angle (from 0° to 90°), as shown in Figure 2.10 for a porous low-k (k ~ 1.9) thin-film structure. The measured interface toughness in general exhibits a trend to increase as the phase angle increases. It is understood that the shearing mode promotes inelastic deformation in the constituent materials and near-tip interface contact/sliding, both contributing to the energy dissipation during the crack growth [31].

The measurements of interface fracture toughness provide a tool for materials selection and process control in the microelectronics industry. One typically measures the fracture toughness for specific interfaces under various process conditions, then selects the material and condition that gives an adequate toughness. In the development of Cu interconnects, new barrier layers were required to prevent copper diffusion into dielectrics and to provide adhesion of copper to the dielectrics. Using the FPB technique, Lane et al. [32] measured the interface toughness and subcritical cracking for a range of Tantalum (Ta) and Tantalum Nitride (TaN) barrier layers and showed that the presence of N significantly improves the adhesion and resistance to subcritical cracking. Moreover, a cap layer is typically used to suppress mass transport and thus improve the electromigration (EM) reliability of the Cu interconnects. A correlation between the EM lifetime and interface toughness was demonstrated so that the interface toughness measurements can be used as a screening process to select cap-layer materials and processes [33, 34]. Sufficient interface toughness is also a requirement for the integration of low-k dielectric materials in interconnect structures. Recently, the FPB technique has been adapted to quantitatively determine the effective toughness of different designs of crack-stop structures to prevent dicing flaws at the edge of chips from propagating into the active areas under the influence of thermal stresses during packaging [35].

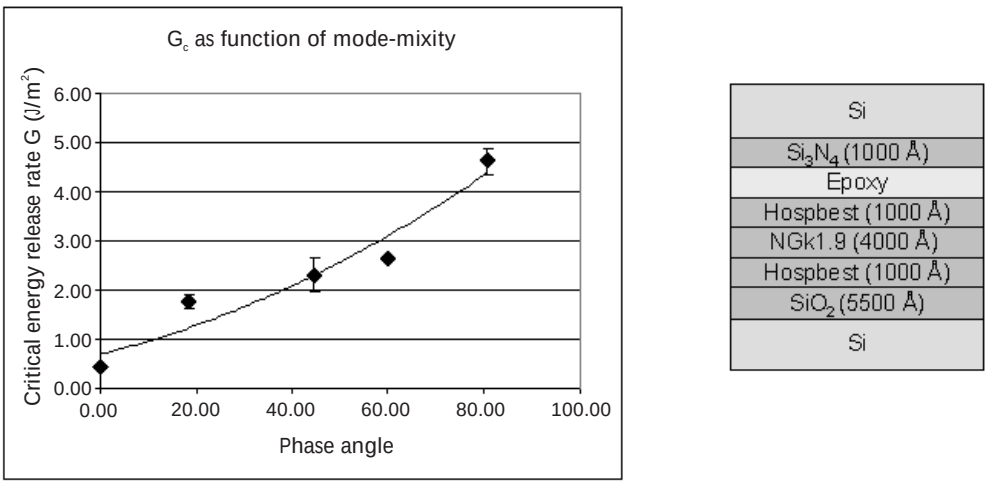


Figure 2.10 Interface toughness as a function of the mode mix measured by the mixed-mode DCB tests. The inset shows the Si/SiO_2/Hospbest/low-k(NGk1.9)/Hospbest film stack with the film thicknesses, where Hospbest is a siloxane-based hybrid material.

2.3 Mechanics of Cohesive and Interfacial Fracture in Thin Films

Integration of low-k and ultralow-k dielectrics in advanced interconnects has posed significant challenges for reliability issues due to compromised mechanical properties. Two types of failure modes have been commonly observed: cohesive fracture of the dielectrics [36–38] and interfacial delamination [39, 40]. The former pertains to the brittleness of low-k materials, and the latter manifests as a result of poor adhesion between low-k and surrounding materials. This section briefly reviews the mechanics underlying fracture and delamination in thin films with applications for integrated Cu/low-k interconnects.

In a generic thin-film structure with an elastic film on an elastic substrate, the mismatch in the elastic properties between the film and the substrate plays a critical role in the mechanical behavior and can be described by using two Dundurs' parameters [23]:

$$\alpha = \frac{\overline{E}_f - \overline{E}_s}{\overline{E}_f + \overline{E}_s} \text{ and } \beta = \frac{\overline{E}_f (1-\nu_f)(1-2\nu_s) - \overline{E}_s (1-\nu_s)(1-2\nu_f)}{2(1-\nu_f)(1-\nu_s)(\overline{E}_f + \overline{E}_s)} \tag{2.6}$$

where $\overline{E} = E/(1-\nu^2)$ is the plane-strain modulus (N/m^2) and ν is Poisson's ratio, with the subscripts f and s for the film and substrate, respectively. When the film and the substrate have identical elastic moduli, we have $\alpha = \beta = 0$, while $\alpha > 0$ for a stiff film on a relatively compliant substrate (e.g., a SiN cap layer on low-k dielectrics) and $\alpha < 0$ for a compliant film on a relatively stiff substrate (e.g., a low-k film on a Si substrate). The role of β is often considered secondary compared to that of α and sometimes ignored for simplicity.

2.3.1 Channel Cracking

A tensile stress in an elastic film can cause cohesive fracture by channel cracking. Unlike a freestanding sheet, fracture of the film bonded to a substrate is constrained. As a result, the crack arrests at a certain depth from the film surface (often at or close to the film/substrate interface) and propagates in a direction parallel to the surface, forming a "channel crack," as illustrated in Figure 2.11 [23, 41]. Figure 2.12(a) shows an array of parallel channel cracks, and Figure 2.12(b) shows the cross section in the wake of a channel crack [42].

For an elastic thin film bonded to an elastic substrate, the energy release rate for steady-state growth of a channel crack takes form [23, 41]:

$$G_{ss} = Z(\alpha, \beta)\frac{\sigma_f^2 h_f}{\overline{E}_f} \tag{2.7}$$

where σ_f is the tensile stress in the film, h_f is the film thickness, and the dimensionless coefficient Z depends on the elastic mismatch between the film and the substrate. At steady state, the energy release rate is independent of the channel length. The value of Z represents the constraint effect on channel cracking due to the substrate and can be determined using a two-dimensional (2D) model [41, 43],

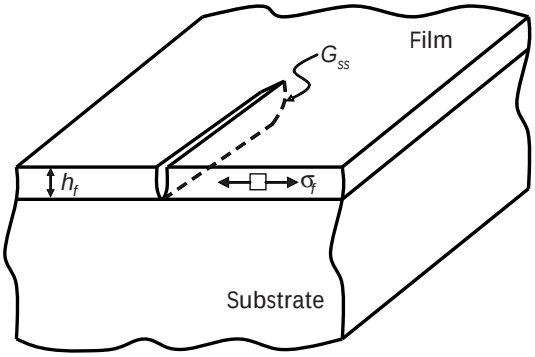


Figure 2.11 Illustration of a channel crack.

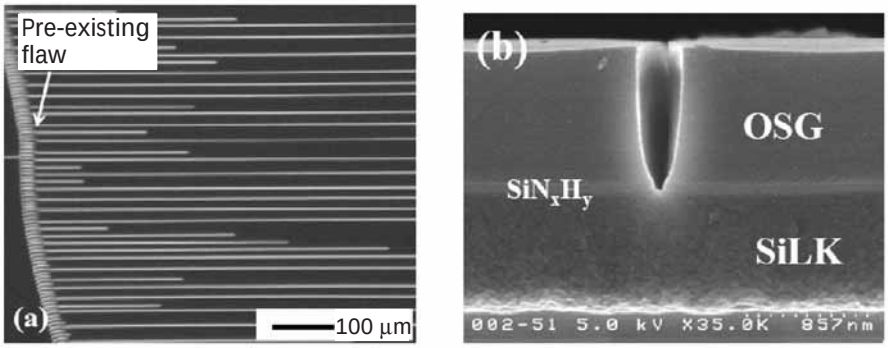


Figure 2.12 Top view (a) and cross-sectional view (b) of channel cracks in thin film stacks of low-k materials [42].

which is plotted in Figure 2.13 as a function of α. When the film and the substrate have identical elastic moduli, $Z = 1.976$. It deceases slightly for a compliant film on a relatively stiff substrate ($\alpha < 0$). A more compliant substrate, on the other hand, provides less constraint, and Z increases. For very compliant substrates (e.g., a SiN cap layer on low-k dielectrics), Z increases rapidly, with $Z > 30$ for $\alpha > 0.99$.

A three-dimensional analysis showed that the steady state is reached when the length of a channel crack exceeds two to three times the film thickness [44]. When the substrate material is more compliant than the film, however, the crack length to achieve the steady state can be significantly longer [45]. With all the subtleties aside, the steady-state energy release rate for channel cracking offers a robust measure for the reliability of thin-film structures, which has also been used for experimental measurements of cohesive fracture toughness of dielectric thin films [27] and crack-driving forces in integrated low-k interconnects [42]. Recently, channel cracking has been investigated in more complex integrated structures with low-k materials, such as multilevel patterned film structures [37] and stacked buffer layers [40].

In addition to the elastic constraint effect, the roles of interface debonding, substrate cracking, and substrate plasticity on film cracking have been studied [45–49]. As shown by Tsui et al. [38], while a brittle film cracks with no delamination on a

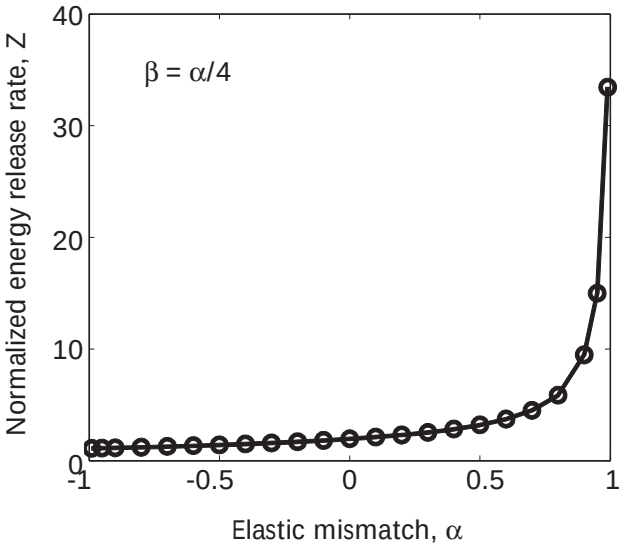


Figure 2.13 Normalized energy release rate for steady state channel crack growth.

stiff substrate, interfacial delamination was observed when the film lies on a more compliant buffer layer. Furthermore, the constraint effect can be significantly relaxed over time if the substrate creeps [50, 51], leading to higher energy release rates.

When the steady-state energy release rate of channel cracking reaches or exceeds the cohesive fracture toughness of the film, fast crack growth in the film is expected. In the subcritical regime ($G < G_c$), however, slow growth of channel cracks in thin films may be facilitated by environmental effects or thermal cycles. The consequence of slow crack growth can be critical for the long-term reliability and lifetime of devices. Several mechanisms for the slow growth of channel cracks in thin films have been studied, including environmentally assisted cracking [36, 38], creep-modulated cracking [50–53], and ratcheting-induced cracking [54, 55].

2.3.2 Interfacial Delamination

Integration of diverse materials relies on interfacial integrity. Typically, an interfacial crack nucleates from a site of stress concentration such as a free edge of the film or a geometric or material junction in a patterned structure. Under tension, a channel crack in a film may lead to delamination from the root of the channel [47]. Under compression, buckling of the film can drive propagation of buckle-delamination blisters (e.g., telephone cord blisters) [23].

Due to asymmetry in the elastic moduli with respect to a bimaterial interface, propagation of an interfacial crack occurs in general under mixed-mode conditions. As a result, the fracture toughness of an interface is necessarily expressed as a function of the mode mix. However, the stress field around an interfacial crack tip in general cannot be decoupled into pure mode I (opening) and mode II (shearing) fields, due to the oscillatory singularity at the crack tip [56, 57]. For a two-dimensional interfacial crack between two isotropic elastic solids joined along

the x-axis, as illustrated in Figure 2.14, the normal and shear tractions on the interface directly ahead of the crack tip are given by [23]

$$\sigma_{yy} = \frac{K_1 \cos(\varepsilon \ln r) - K_2 \sin(\varepsilon \ln r)}{\sqrt{2\pi r}}, \sigma_{xy} = \frac{K_1 \sin(\varepsilon \ln r) + K_2 \cos(\varepsilon \ln r)}{\sqrt{2\pi r}} \tag{2.8}$$

where r is the distance from the crack tip, and ε is the index of oscillatory singularity depending on the second Dundurs' parameter,

$$\varepsilon = \frac{1}{2\pi} \ln\left(\frac{1-\beta}{1+\beta}\right) \tag{2.9}$$

The stress-intensity factors, K_1 and K_2, are the real and imaginary parts of the complex interfacial stress-intensity factor, $K = K_1 + iK_2$.

When $\varepsilon = 0$, the interfacial crack-tip stress field reduces to the homogeneous crack-tip field with tractions, $\sigma_{yy} = \frac{K_1}{\sqrt{2\pi r}}$ and $\sigma_{xy} = \frac{K_2}{\sqrt{2\pi r}}$, where K_1 and K_2 are the conventional mode I and mode II stress-intensity factors. In this case, the ratio of the shear traction to the normal traction is simply K_2 / K_1, which defines the mode mix. When $\varepsilon \neq 0$, however, the mode mix as a measure of the proportion of mode II to mode I requires specification of a length quantity since the ratio of the shear traction to the normal traction varies with the distance to the crack tip. As suggested by Rice [57], an arbitrary length scale (l) may be used to define a phase angle of the mode mix for interfacial delamination, namely,

$$\psi = \tan^{-1}\left[\left(\frac{\sigma_{xy}}{\sigma_{yy}}\right)_{x=l}\right] = \tan^{-1}\left[\frac{\mathrm{Im}\left(Kl^{i\varepsilon}\right)}{\mathrm{Re}\left(Kl^{i\varepsilon}\right)}\right] \tag{2.10}$$

The choice of the length l can be based on the specimen geometry, such as the film thickness, or on a material length scale, such as the plastic zone size at the crack tip. Different choices will lead to different phase angles. A simple transformation

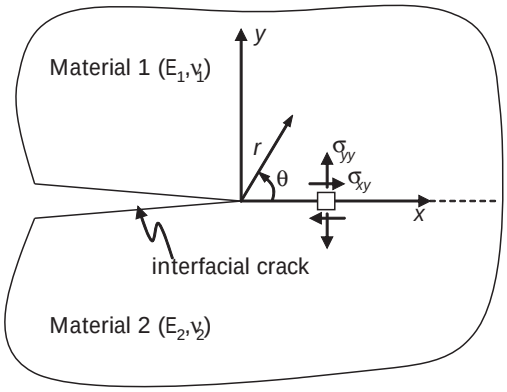


Figure 2.14 Geometry and convention for an interfacial crack.

rule was noted by Rice [57] that transforms the phase angle defined by one length scale to another, namely,

$$\psi_2 = \psi_1 + \varepsilon \ln\left(l_2 / l_1\right) \tag{2.11}$$

where ψ_1 and ψ_2 are the phase angles associated with lengths l_1 and l_2, respectively. Therefore, so long as a length scale is clearly presented for the definition of the phase angle, experimental data for the mode-dependent interface toughness can be unambiguously interpreted for general applications (i.e., $\Gamma\left(\psi_1, l_1\right) = \Gamma\left(\psi_2, l_2\right)$).

The energy release rate for a crack advancing along an interface is related to the interfacial stress-intensity factors by [23]

$$G = \frac{1-\beta^2}{E^*}\left(K_1^2 + K_2^2\right) \tag{2.12}$$

where $E^* = 2\left(\overline{E}_1^{-1} + \overline{E}_2^{-1}\right)^{-1}$. The criterion for interfacial delamination can then be stated as $G = \Gamma(\psi, l)$, where the same choice of the length l has to be used in the definition of the phase angle for the interface toughness and in the calculation of the phase angle for the specific problem along with the energy release rate G. For 3D problems, a mode III term must be added into the energy release rate, and another phase angle may be defined for the 3D mode mix.

For delamination of an elastic thin film from a thick elastic substrate under the plane-strain condition, a steady state is reached when the interfacial crack length is much greater than the film thickness. The energy release rate for the steady-state delamination is independent of the crack length:

$$G_{ss}^d = \frac{\sigma_f^2 h_f}{2\overline{E}_f} \tag{2.13}$$

Taking the film thickness as the length scale ($l = h_f$), the phase angle of mode mix at the steady state depends on the elastic mismatch as a function of the Dundurs' parameters (i.e., $\psi_{ss} = \omega(\alpha, \beta)$). This function was determined numerically and tabulated by Suo and Hutchinson [58]. When the film and the substrate have identical elastic moduli, $\psi_{ss} = \omega(0,0) = 52.1°$.

Yu et al. [59] have shown that the energy release rate for an interfacial crack emanating from a free edge can be significantly lower than the steady-state energy release rate. Consequently, there exists a barrier for the onset of delamination, which depends on the materials and geometry near the edge. For interfacial delamination from the root of a channel crack [46, 47], the energy release rate approaches the same steady-state value but follows a power law at the short crack limit [60]:

$$G_d \sim \left(\frac{d}{h_f}\right)^{1-2\lambda} \tag{2.14}$$

where d is the crack length, and λ depends on the elastic mismatch determined by

$$\cos \lambda\pi = \frac{2(\alpha-\beta)}{1-\beta}(1-\lambda)^2 - \frac{\alpha-\beta^2}{1-\beta^2} \tag{2.15}$$

As shown in Figure 2.15, the energy release rate approaches zero as $d / h_f \to 0$ when $\alpha < 0$ (compliant film on stiff substrate). Thus, there exists a barrier for the onset of delamination. On the other hand, when $\alpha > 0$ (stiff film on compliant substrate), the energy release rate approaches infinity as $d / h_f \to 0$, suggesting that interfacial delamination always occurs concomitantly with channel cracking. In Cu/low-k interconnects, the low-k dielectric is usually more compliant compared to the surrounding materials. Therefore, channel cracking of low-k dielectrics is typically not accompanied by interfacial delamination. However, when a more compliant buffer layer is added adjacent to the low-k film, interfacial delamination can occur concomitantly with channel cracking of the low-k film [38]. Moreover, a relatively stiff cap layer (e.g., SiN) is often deposited on top of the low-k film. Channel cracking of the cap layer could be significantly enhanced by interfacial delamination.

The energy release rate and mode mix of interfacial delamination in more complex integrated structures are commonly calculated for device reliability analysis. Here, finite-element-based models are typically constructed to compute the stress-intensity factors or energy release rates of interfacial cracks literally introduced into the model. Nied [61] presented a review focusing on applications in electronic packaging. Liu et al. [39] analyzed delamination in patterned interconnect structures. As one of the emerging reliability concerns for advanced interconnects and packaging technology, the impacts of chip-package interactions on interfacial delamination have been investigated by multilevel finite element models, which will be discussed in the next section.

The experimental techniques to measure interface toughness as the critical energy release rate ($\Gamma = G_c$) for fast fracture have been discussed in Section 2.2.2. In addition, interfacial cracks are often susceptible to environmentally assisted crack growth in the subcritical regime ($G < G_c$) [25, 27, 28, 31, 62, 63]. The kinetics of

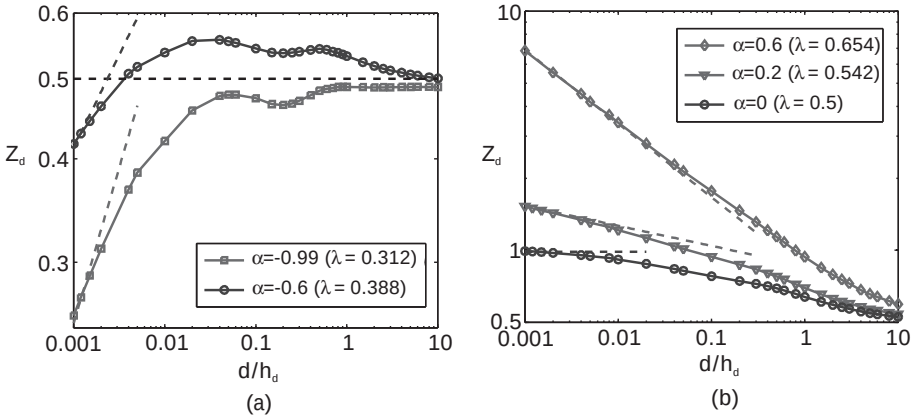


Figure 2.15 Normalized energy release rate of interfacial delamination $Z_d = G_d \bar{E}_f / \left(\sigma_f^2 h_f\right)$ from the root of a channel crack as a function of the interfacial crack length. (a) $\alpha < 0$, and (b) $\alpha \geq 0$. The dashed lines indicate the asymptotic solution given by Eq. (2.14), and $Z_d = 0.5$ for the steady-state delamination.

subcritical interfacial delamination have been understood as controlled by stress-dependent chemical reactions in stage I and by mass transport of environmental species (e.g., water molecules) to the crack tip in stage II [31]. Recently, by combining the kinetics of subcritical cracking and water diffusion, Tsui et al. [40] proposed a model to predict degradation of adhesion in thin-film stacks as a function of exposure time to water and found good agreement with experimental data for film stacks containing a low-k dielectric material.

2.4 Modeling of Chip-Packaging Interactions

Finite element analysis (FEA) is commonly used to evaluate the thermomechanical deformation and stress distributions in electronic packages and their impact on reliability. For stand-alone silicon chips, the modeling results show that thermal stresses in the Cu lines depends on the aspect ratio (i.e., the width versus height ratio) and the degree of confinement from the dielectric materials as well as the barrier and cap layers (Figure 2.16). For an aspect ratio greater than 1, the stress state is triaxial and behaves almost linear elastically under thermal cycling [64]. Wafer processing can induce additional residual stresses in the interconnect structures, which has also been investigated using FEA [65]. The general behavior is in quantitative agreement with results from X-ray diffraction measurements [64, 66]. After the silicon die is assembled into a flip-chip package, the package deformation can increase the thermomechanical stresses in the interconnect structures. Modeling the packaging effect on the thermal stress of the interconnect structure is challenging due to the large difference in the dimensions of the packaging and interconnect structures. For this reason, researchers from Motorola first introduced a multilevel submodeling technique to evaluate the energy release rate for interfaces in the interconnect structure after assembling the die into a flip-chip package [12, 13]. This technique bridges the gap between the packaging and wafer levels. The energy release rates for various

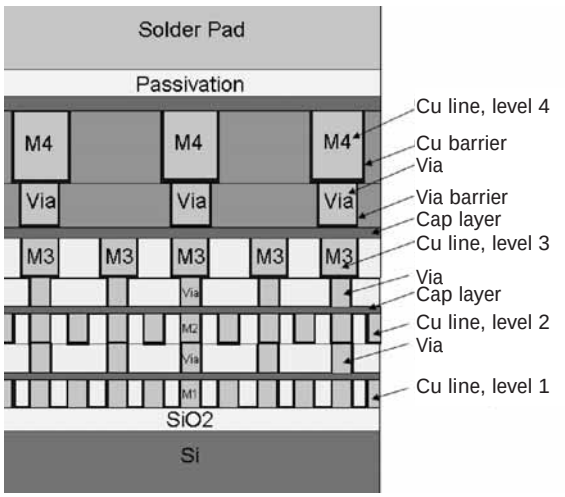


Figure 2.16 Cu/low-k structure schematics.

interconnect interfaces during packaging assembly were calculated using 2D FEA models. However, a flip-chip package is a complicated 3D structure that cannot be properly represented using a 2D model. We developed, therefore, a 3D FEA model based on a four-level submodeling technique to investigate the packaging effect on interconnect reliability, particularly focusing on the effects of low-k dielectrics and other materials used to form the Cu interconnect structures [14, 17].

2.4.1 Multilevel Submodeling Technique

Level 1. Starting from the package level, the thermomechanical deformation for the flip-chip package is first investigated. At this package level, a quarter-section of the package is modeled using the symmetry condition as illustrated in Figure 2.17(a). No interconnect structure detail was considered at this level because its thickness is too small compared to the whole package. Simulation results for this package-level model are verified with experimental results obtained from moiré interferometry.

Level 2. From the simulation results for the package-level modeling, the most critical solder bump is identified. A submodel focusing on the critical solder bump region with much finer meshes is developed, as shown in Figure 2.17(b). The built-in cut boundary technique in ANSYS [67] is used for submodeling. At this

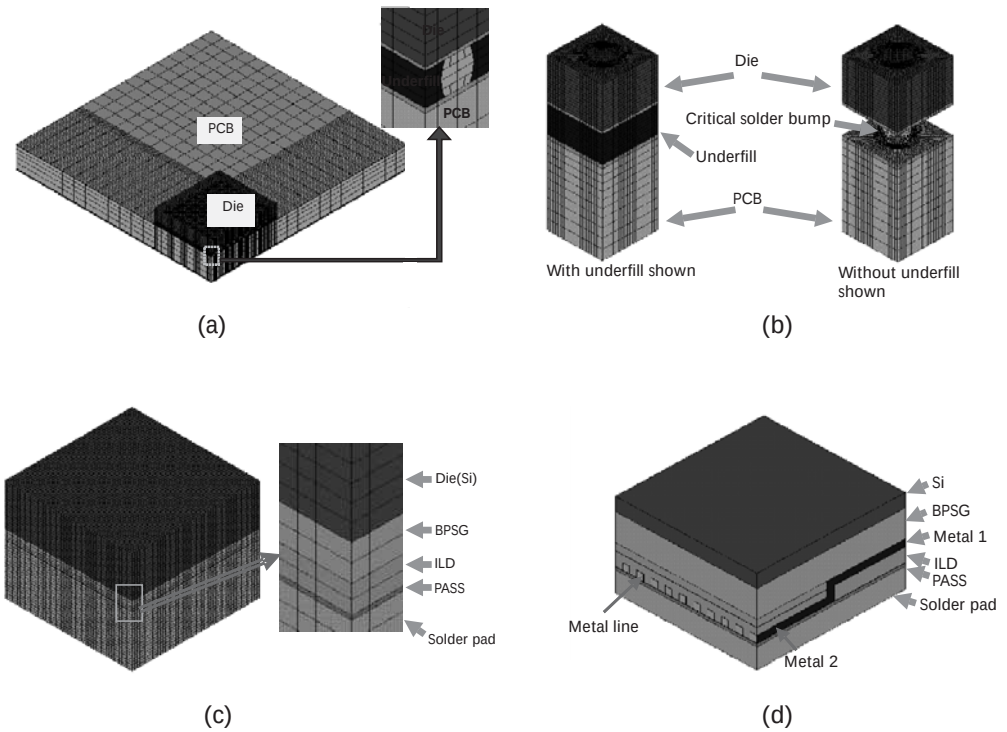


Figure 2.17 Illustration of four-level sub-modeling: (a) package level; (b) critical solder level; (c) die-solder interface level; and (d) detailed interconnect level.

submodel level, a uniform interlevel dielectric (ILD) layer at the die surface is considered, but still no detailed interconnect structure is included.

Level 3. Based on the level 2 submodeling results, a large peeling stress is found at the die-solder interface. At the critical die-solder interface region with the highest peeling stress, a submodel is created using the cut boundary technique, as shown in Figure 2.17(c). This submodel focuses on the die-solder interface region (a small region of level 2) containing a portion of the die, the ILD layer, and a portion of the solder bump. Still only a uniform ILD layer at the die surface is considered at this level, and no detailed interconnect structure is included.

Level 4. This submodel zooms in further from the level 3 model, focusing on the die-solder interface region as shown in Figure 2.17(d). Here, a detailed 3-D interconnect structure is included. An interconnect with two metal levels and vias is considered first, and effects of multilevel stacks are discussed in Section 2.6. The submodel is set up accordingly, and a crack with a fixed length is introduced along several interfaces of interest. The energy release rate and mode mix for each crack are determined using a modified virtual crack closure technique as discussed in the next section.

2.4.2 Modified Virtual Crack Closure Method

To investigate the impact of CPI on the reliability of low-k interconnect and packaging structures, interfacial cracks are introduced into the models, and both the energy release rates and mode mix are calculated as a measure of the crack-driving force for interfacial delamination. Several methods have been developed for calculating the interfacial fracture parameters within the framework of finite element analysis. The J-integral method has been widely used [68–70] and is a standard option in some commercially available FEA codes (e.g., ABAQUS [71]). This method is capable of calculating both the energy release rate and the mode mix for 2-D and 3-D interfacial cracks, but it requires relatively fine meshes near the crack tip to achieve convergence and path independence of the numerical results. A set of special finite element methods has also been developed to improve the numerical accuracy without requiring fine meshes, including the singular element method [72], the extended finite element method (XFEM) [73], and an enriched finite element method [74, 75]. Implementation of these methods, however, is very involved numerically and has been limited to problems with relatively simple geometry and material combinations. Alternatively, Liu et al. [19, 39] calculated stress-intensity factors by comparing the crack surface displacement to the analytical crack-tip solution, from which both the energy release rate and mode mix were determined. This approach requires very fine meshes near the crack tip for the accuracy of the displacement calculation and is not readily applicable to 3D problems. With the material and geometrical complexities in the four-level modeling of CPI, a simple method using standard FEA codes along with relatively coarse meshes is desirable for the fracture analysis. A modified virtual crack closure (MVCC) technique [14, 76] has emerged to meet such a need and is described as follows.

As illustrated in Figure 2.18, the MVCC method calculates the components of the energy release rate corresponding to the three basic fracture modes (I, II, and III) separately. With the local stress-strain and displacement distributions obtained by the finite element modeling, both the energy release rate and the mode mix for the interfacial cracks can be calculated accordingly. For the eight-node solid elements shown in Figure 2.18, the three energy release rate components G_I, G_{II} and G_{III} can be obtained as

$$\begin{aligned} G_I &= \sum_i F_z^{(i_1)} \delta_z^{(i_2)} / (2\Delta A) \\ G_{II} &= \sum_i F_x^{(i_1)} \delta_x^{(i_2)} / (2\Delta A) \\ G_{III} &= \sum_i F_y^{(i_1)} \delta_y^{(i_2)} / (2\Delta A) \end{aligned} \tag{2.16}$$

where $F_x^{(i_1)}$, $F_y^{(i_1)}$, and $F_z^{(i_1)}$ are nodal forces at node i_1 along the x-, y-, and z-directions, respectively, and $\delta_x^{(i_2)}$, $\delta_y^{(i_2)}$, and $\delta_z^{(i_2)}$ are relative displacements between node i_2 and node i_3 in the x-, y-, and z-directions, respectively. Note that, for simplicity, only one element set is shown along the crack front direction (y-direction). The total energy release rate is then

$$G = G_I + G_{II} + G_{III} \tag{2.17}$$

and the phase angles of mode mix may be expressed as

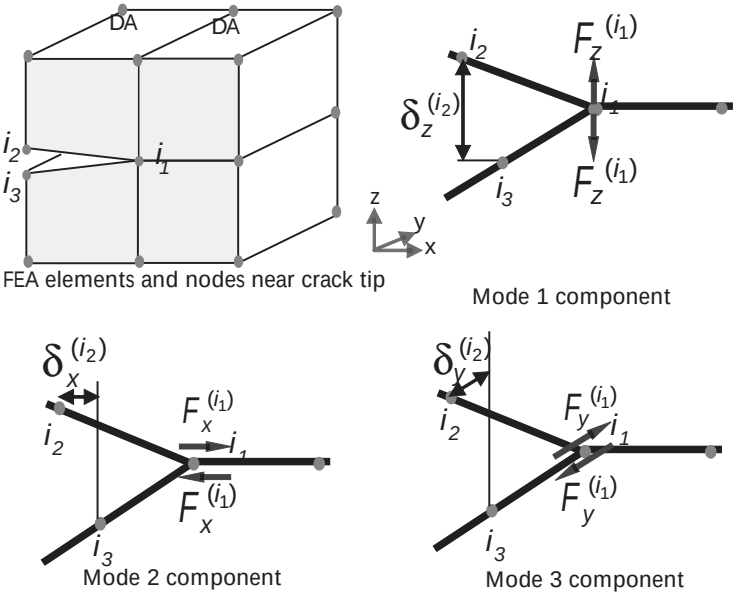


Figure 2.18 Illustration of the modified virtual crack closure (MVCC) technique.

$$\psi = \arctan - 1\left[\left(G_{II}/G_{I}\right)^{1/2}\right]$$
$$\varphi = \arctan - 1\left[\left(G_{III}/G_{I}\right)^{1/2}\right] \tag{2.18}$$

The criterion for interfacial delamination can thus be established by comparing the total energy release rate to the experimentally measured mode-dependent interface toughness [i.e., $G = \Gamma(\psi, \varphi)$].

While the original virtual crack closure technique (VCCT) was proposed for cracks in homogeneous materials [77–79], it has been shown that care must be exercised in applying the technique for interfacial cracks [79–83]. As noted by Krueger [79], due to the oscillatory singularity at the interfacial crack tip, the calculated energy release rate and mode mix may depend on the element size at the crack tip. It was suggested that the element size shall be chosen to be small enough to assure a converged solution by the finite element model but also large enough to avoid oscillating results for the energy release rate. Furthermore, as discussed in Section 2.3.2, mode I and mode II in general cannot be separated for interfacial cracks (except for cases with $\beta = 0$). The separation of the energy release rate components in (2.16) is therefore dependent on the element size, as is the definition of the phase angles in (2.18). The total energy release rate on the other hand was found to be less sensitive to the element size [80, 81]. Several approaches have been suggested to extract consistent phase angles of mode mix independently of the element size using the VCCT [82, 83], following the standard definition in (2.10). For simplicity, the phase angles defined in (2.18) are used in the subsequent discussions.

2.4.3 Package-Level Deformation

The FEA results for the package-level modeling can be verified using results from moiré interferometry. Since the thermal load used in the moiré measurement was from 102°C to 22°C, we applied the same thermal load (102°C to 22°C) in the package-level modeling in order to compare the moiré and FEA results. Figure 2.19 shows the *z*-displacement (package warpage) distribution along the die centerline (line A-A in Figure 2.3). The FEA and moiré results are found to be in good agreement. Detailed moiré results can be found in [22].

2.4.4 Energy Release Rate for Stand-alone Chips

After verification with moiré interferometry, FEA was applied to evaluate the energy release rates for stand-alone wafer structures as well as the packaging effect. Both Al and Cu interconnect structure with tetraethyl orthosilicate (TEOS) and a spin-on polymer SiLK as ILD were investigated. The material properties used in the modeling analysis are listed in Table 2.1. All materials in the wafer structure were assumed to be linear elastic except at the package level, where plasticity was considered for solder materials. To calculate the energy release rate, a crack was introduced at several relevant interfaces, as shown in Figure 2.20. The crack has a rectangular shape with a fixed length of 1.5 μm along the metal line direction and a width of 0.5 μm,

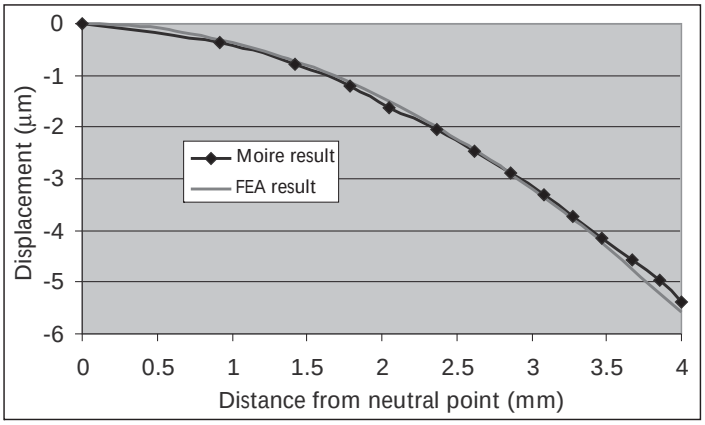


Figure 2.19 Comparison of FEA and Moiré results of thermal deformation for the flip-chip package in Figure 2.3.

Table 2.1 Mechanical Properties of Interconnect Materials [18, 22]

Material	*E (GPa)*	*ν*	*α (ppm/°C)*
Si	162.7	0.28	2.6
Al	72	0.36	24
Cu	122	0.35	17
TEOS (k = 4.2)	66	0.18	0.57
SiLK (k = 2.62)	2.45	0.35	66
MSQ (k = 2.7)	7	0.35	18
CVD-OSG (k = 3.0)	17	0.35	8
tblPorous MSQ-A (k < 2.3)	2	0.35	10
Porous MSQ-B (k < 2.3)	5	0.35	10
Porous MSQ-C (k ~ 2.3)	10	0.35	12
Porous MSQ-D (k ~ 2.3)	15	0.35	18
Porous MSQ-E (k ~ 2.3)	10	0.35	6
Porous MSQ-F (k ~ 2.3)	10	0.35	18

the same as the metal line width and thickness. In general, the energy release rate depends on the number of the metal levels and the crack dimension used in the calculation. In the following discussion, a fixed crack size in a two-level structure is used in order to simplify the CPI computation in the study of the material and processing effects. This point should be kept in mind as the crack-driving force is compared, particularly when the CPI study is extended to four-level interconnect structures with a different crack size to study scaling and ultralow-k effects in Section 2.6.

The energy release rates for interfacial fracture along the six interfaces shown in Figure 2.20 were first calculated for the stand-alone chip subjected to a thermal load of 400°C to 25°C, typical for wafer processing. The results summarized in Figure 2.21 show that the energy release rates for all the interfaces in Al/TEOS and Cu/TEOS structures are generally small, less than 1 J/m^2. The Cu/SiLK structure has the highest energy release rates for the two vertical cracks along the SiLK/barrier sidewall (crack 2) and along the barrier/Cu interfaces (crack 3), both exceeding 1

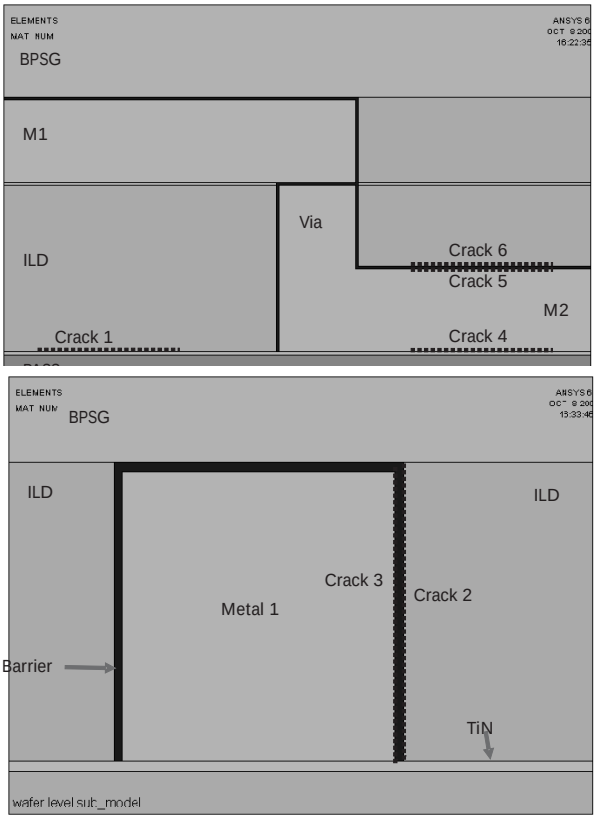


Figure 2.20 Cracks introduced along interfaces of interest.

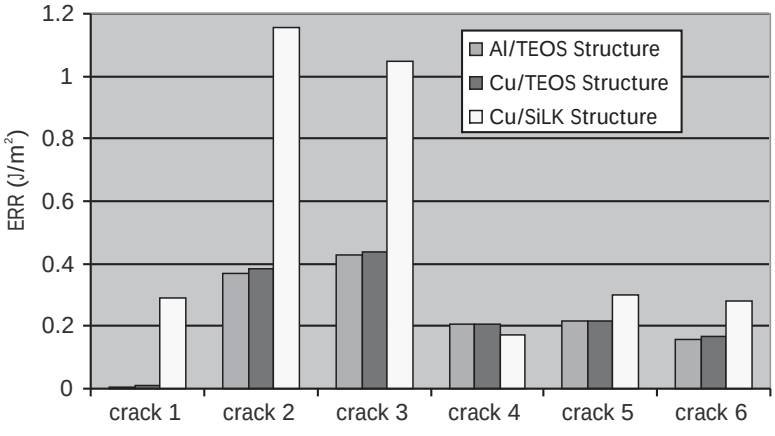


Figure 2.21 Energy release rates for interfaces in interconnect structures in stand-alone chip before packaging assembly (from 400°C to 25°C).

J/m^2. The fracture mode for these two cracks is almost pure mode I, indicating that for the stand-alone chip, the tensile stresses driving crack formation act primarily on the vertical interfaces due to the large CTEs of the low-k ILDs in comparison to the CTEs of the silicon substrate and metal lines. Compared to the critical energy release

rates for low-k interfaces obtained from experiments (usually about 4 to 5 J/m^2 [84]), these values are considerably lower. Hence, interfacial delamination in Cu/low-k interconnect structures during wafer processing is not expected to be a serious problem, although the result does not rule out the possibility of delamination due to subcritical crack growth.

2.5 Energy Release Rate under Chip-Package Interactions

2.5.1 Effect of Low-k Dielectrics

The energy release rates induced by CPI were evaluated using the four-step multilevel submodel. A stress-free state was assumed at –55°C for the flip-chip package, and the crack-driving force was obtained at 125°C to simulate a test condition of –55°C to 125°C. The package used has the same dimensions as the one used for moiré measurements, which has an organic substrate with a die size of 8 × 7 mm^2 and lead-free solders (95.5 Sn/3.8 Ag/0.7 Cu). The critical solder bump with the highest thermal stress is the outermost one at the die corner. The interconnect structure located at this critical solder bump–die interface was investigated. The results are given in Figure 2.22, which reveals a small CPI effect for Al/TEOS and Cu/TEOS structures. In contrast, the effect is large for the Cu/SiLK structure with the crack-driving force G reaching 16 J/m^2. Interestingly, the interfaces parallel to the die surface (cracks 1, 4, 5, and 6) are more prone to delamination, instead of the vertical interfaces 2 and 3 as is the case for the stand-alone chip. For these parallel interfaces, the mode mix is close to being pure mode I, although for the Cu/passivation interface, both mode I and III components are present. As compared with the results for the stand-alone wafers and after packaging, not only is a large increase in the crack-driving force evident due to chip-package interactions but the interfaces most prone to delamination also change to those parallel to the die surface. This indicates that the crack-driving force becomes dominated by thermal

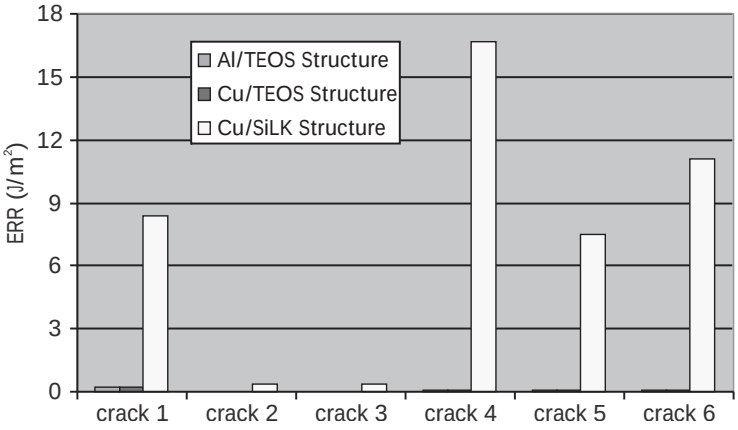


Figure 2.22 Energy release rates for interfaces in on-chip interconnect structures after assembly into packages with Pb-free solders.

stresses imposed by the package deformation where the package warpage has the most significant effect for the parallel interfaces.

These results indicate that the delamination induced by CPI occurs near the outermost solder bumps under mostly a mode I condition. As the crack propagates, both the energy release rate and the mode mix at the crack tip vary. The crack follows a path that maximizes G / Γ, the ratio between the energy release rate and the fracture toughness. Depending on the local material combination and wiring geometry, the crack may zigzag through the interconnect structure toward the lower Cu levels with weaker low-k dielectrics. As the crack propagates, the energy release rate will increase while the phase angle changes to mixed mode, depending on the local wiring geometry. The crack-propagation problem in a multilayer interconnect network is complex and will be further discussed in Section 2.6.

2.5.2 Effect of Solder Materials and Die Attach Process

As the semiconductor industry shifts from Pb-based solders to Pb-free solders, the effects of solder materials on CPI and low-k interconnect reliability become of interest. The energy release rates for the six interfaces are compared in Figure 2.23 for high-lead (95 Pb/5 Sn), eutectic lead alloy (62 Sn/36 Pb/2 Ag), and lead-free solder (95.5 Sn/3.8 Ag/0.7 Cu). The material properties used in these calculations are listed in Table 2.2. The mismatch in CTE between the lead-free solder and underfill is larger than that between the high-lead or eutectic solder and underfill. The Young's modulus of the lead-free solder is also larger than the high-lead and eutectic solders. Thus, larger thermal stresses are induced at the die surface for the lead-free solder package as compared to the high-lead and eutectic solder packages, resulting in the highest driving force for interconnect delamination in lead-free packages.

The processing step with the highest thermal load in flip-chip package assembly is the die attach before underfilling the package. The solder reflow occurs at a temperature higher than the solder melting point, and afterwards the package structure is cooled down to room temperature. Without the underfill serving as a stress buffer, the thermal mismatch between the die and the substrate can generate a large thermal

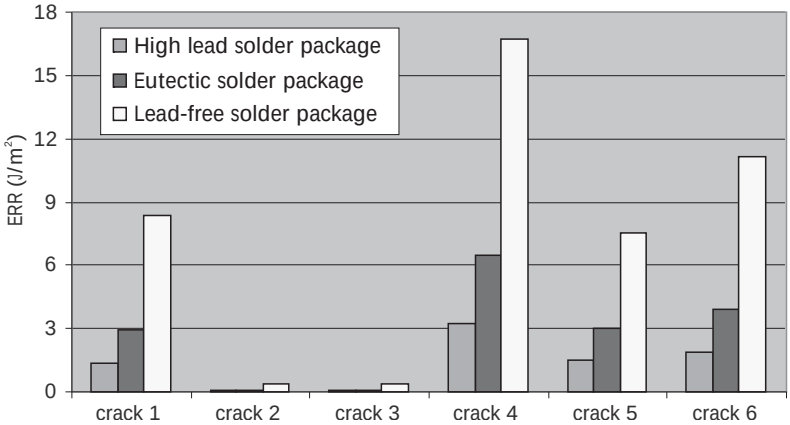


Figure 2.23 Energy release rates for Cu/SiLK interconnect structures in high-lead, eutectic solder and lead-free solder packages after underfilling.

Table 2.2 Material Properties for High-Lead, Eutectic Lead, and Lead-Free Solders [22] (Modulus Values Are a Function of Temperature *T*)

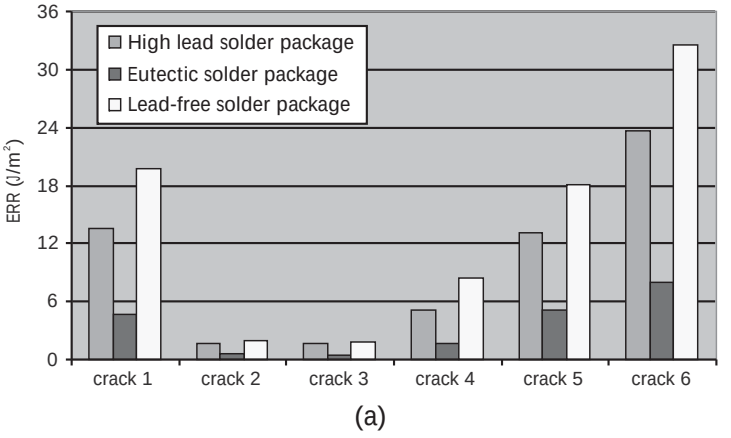
Solder Material	*E (GPa)*	ν	α *(ppm/°C)*
Eutectic	$75.84 - 0.152 \times T$	0.35	24.5
High lead	$39.22 - 0.063 \times T$	0.35	29.7
Lead free	$88.53 - 0.142 \times T$	0.40	16.5
Underfill	6.23	0.40	40.6
Organic substrate	Anisotropic elastic		16 (in plane) 84 (out of plane)

stress at the solder-die interface near the die corner, driving interfacial delamination. The CPI effect of the die-attach step for low-k structure was investigated for Cu/SiLK and Cu/MSQ structures for different solder materials. Here, the study was again performed for the high-lead, eutectic lead, and lead-free solders with different reflow cycles: 160°C to 25°C for eutectic solder, 250°C to 25°C for lead-free solder, and 300°C to 25°C for high-lead solder. The substrate in the package was organic with a die size of 8×7 mm^2, and the study assumed that the high-lead solder could be assembled onto an organic substrate in order to compare these solders on the same substrate. The results are summarized in Figure 2.24(a) for Cu/SiLK chips assembled on an organic substrate. The eutectic solder package has the lowest crack-driving force for interfacial delamination due to its lowest reflow temperature. In contrast, the lead-free solder package is most critical due to the high reflow temperature and the high Young's modulus of the lead-free solder material. For the high-lead solder, although it has the highest reflow temperature yet the lowest Young's modulus, the crack-driving force is lower than that for the lead-free solder package. For comparison, the results for the Cu/MSQ structure with eutectic and lead-free solders are shown in Figure 2.24(b). The energy release rate for the Cu/MSQ structure is generally about a factor of three lower than that of the Cu/SiLK structure. This can be attributed to the threefold higher Young's modulus of the MSQ dielectrics, indicating that the mechanical property of the low-k is an important factor to consider for the packaging effect.

Comparing Figure 2.23 and Figure 2.24(a), it is clear that the crack-driving force in the Cu/SiLK structure during the die-attach process is generally larger than that in an underfilled package during thermal cycling from –55°C to 125°C. This indicates that the die-attach process with a larger thermal load is a more critical step than thermal cycling in driving critical interfacial delamination in Cu/low-k structures.

2.5.3 Effect of Low-k Material Properties

To investigate the effect of dielectric properties, we first compare the CPI for a CVD-OSG (k = 3.0) [9] with an MSQ [10] and a spin-on polymer SiLK [7] to investigate how better material properties can improve interconnect reliability. Both MSQ and SiLK are fully dense with k ~ 2.7. The energy release rates were computed using the two-level interconnect structure with cracks 1 to 6, and the results are plotted in Figure 2.25. Among the dielectric materials, the energy release rates



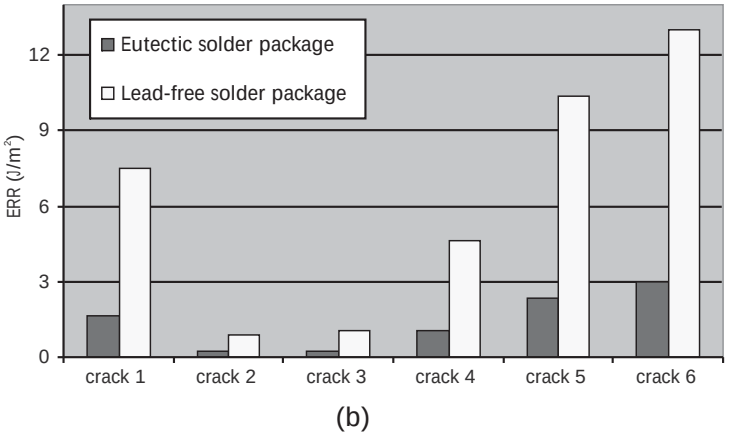


Figure 2.24 Energy release rates for interconnect interfaces in (a) Cu/SiLK and (b) Cu/MSQ structures in die attach process.

(ERRs) are the lowest for CVD-OSG, which has the highest Young's modulus (E). For the spin-on polymer, which has the lowest E, the ERR values for cracks 1 and 6 are about six times higher than those of CVD-OSG. This indicates that the on-chip interconnect fabricated with spin-on polymer needs about six times more adhesion strength at the interfaces of cracks 1 and 6 in order to obtain a mechanical reliability equivalent to interconnects fabricated using CVD-OSG.

Next, the study is extended to several porous MSQ materials (A to D) [11], which are being developed for interconnect structures of the 65 nm node and beyond. These porous low-k materials have $k < 2.3$ but with different thermomechanical properties, which are listed in Table 2.1. The results are plotted in Figure 2.26(a), which shows a good correlation between ERR and E. Comparing porous MSQ-D ($k \sim 2.3$) with fully dense CVD-OSG ($k = 3.0$), both with similar mechanical properties, their ERR values are similar. Interestingly, for the porous MSQ-E and the MSQ-F, even though they have very different CTE but similar E, their ERR values are about the same, too, as shown in Figure 2.26(b). Overall, there seems to be little effect due to the CTE of the low-k materials. In contrast, the ERR

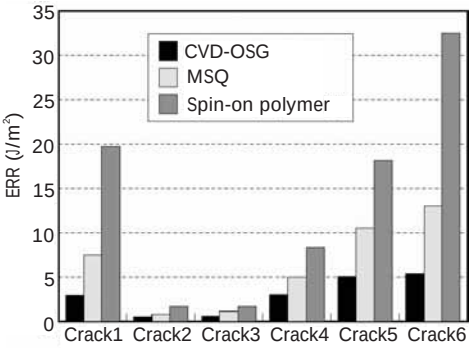
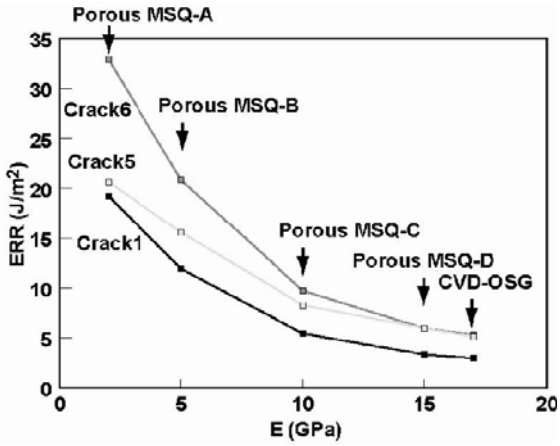
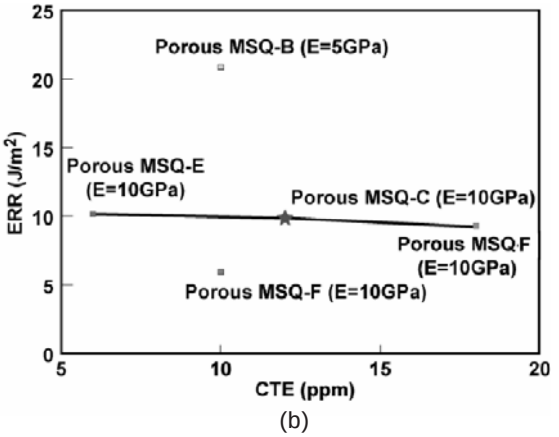


Figure 2.25 Comparison of ERR for low-k dielectrics of CVD-OSG, MSQ and a spin-on polymer. The cracks are the same as shown in Fig. 2.20.



(a)



(b)

Figure 2.26 (a) Values of ERR as a function of Young's modulus for low-k dielectrics; (b) Values of ERR as a function of CTE for low-k dielectrics.

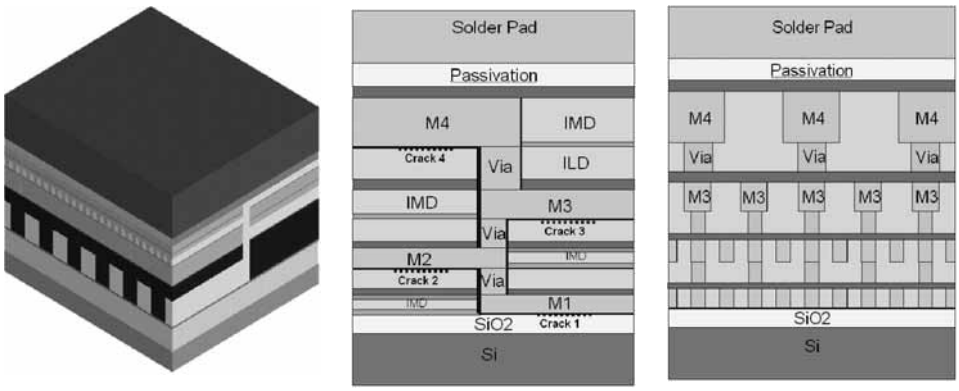
increases considerably with decreasing E. Therefore, for low-k dielectrics, increasing E seems to be effective for improving the mechanical reliability.

The interconnect structure used to calculate ERR in this study is a simple two-layer structure. The actual interconnect structure for low-k chips for the 65 nm technology node has more than 11 layers with complex geometry and material combinations [84, 85]. There will be other interesting and important factors contributing to ERR to affect package reliability. Of particular interest is channel cracking induced by thermal stress in compliant low-k layers, which depends on the interconnect geometry and layer stack structure. There will also be the effect due to residual stresses generated by thermal processing during chip fabrication, which can superimpose onto the CPI stresses to affect the ERR driving force [42, 65].

2.6 Effect of Interconnect Scaling and Ultralow-k Integration

The scaling of interconnect structures has led to highly complex architectures with over 10 metal layers, sub–50 nm dimensions, and ultralow-k dielectrics (ultimately, air gap structures). There are important questions regarding the effect of interconnect scaling and the implementation of ultralow-k dielectric on chip-package interaction and low-k interconnect reliability. The study of the scaling effect is focused on two issues: the effect of the implementation of ultralow-k dielectric and the effect of interconnect geometry on the ERR as the crack propagates through the Cu/low-k structure. Previous studies have investigated the effect of increasing stacking layers based on 2D multilevel submodels and found that the ERR increases with the addition of more wiring levels [12]. The study reported here is based on a 3D multilevel interconnect model with four metal levels, as shown in Figure 2.27. We found that a four-level 3D structure provides a realistic wiring structure to analyze the effect of porous low-k implementation in the interconnect structure. In this structure, the pitch and line dimensions in the first two metal layers (M1 and M2) are doubled in the third layer (M3), which are doubled again in the fourth layer (M4), approximately simulating the hierarchical layers in real interconnect structures.

The effect of ultralow-k implementation was investigated using different stacking of low-k and ultralow-k dielectric layers. In this study, we are interested to find



3D View X-section View Side View

Figure 2.27 FEA model of 3D 4-layer interconnect.

out whether different combinations of low-k and ultralow-k dielectrics in selective metal layers could improve mechanical reliability without sacrificing electrical performance (RC delay). Energy release rates were calculated for horizontal cracks placed at each metal level at the interface between the etch stop/passivation (ESL) and the low-k dielectric, which is known to be one of the interfaces most prone to delamination [12–14]. Each crack has a width of 0.1 μm and a length of 2 μm extending in the multiple wiring directions, as shown in Figure 2.27. Results of the ERRs of the interfacial cracks in the four-level interconnect models with three different ILD combinations are summarized in Figure 2.28. The first model [Figure 2.28(a)] uses ultralow-k materials in all layers for which the interfacial crack at the uppermost level (crack 4) has the largest ERR. This is to be expected since the uppermost level is the thickest, being four times larger than M1 in thickness, and thus the maximum crack-driving force. In the second model [Figure 2.28(b)], SiO_2 is used to replace ULK at level 4. In this case, the high E of SiO_2 significantly reduces the ERR of crack 4 but raises the ERRs in the other three interfaces. This reflects the effect on the crack-driving force of the elastic mismatch between SiO_2 and the ULK layer as discussed in Section 2.3.2. In this structure, the ERR is highest for crack 3 in the M3 level, which is thicker than M1 and M2. In model 3 [Figure 2.28(c)], a fully dense low-k CVD-OSG is used at level 3, which has a higher E than the ULK. Consequently, the ERR of crack 3 is reduced, and the effect of elastic mismatch shifts the largest ERR to crack 2 in the M2 level with a magnitude comparable to that of crack 3 in model 2. This set of results indicates that the ultralow-k interface at the upper-

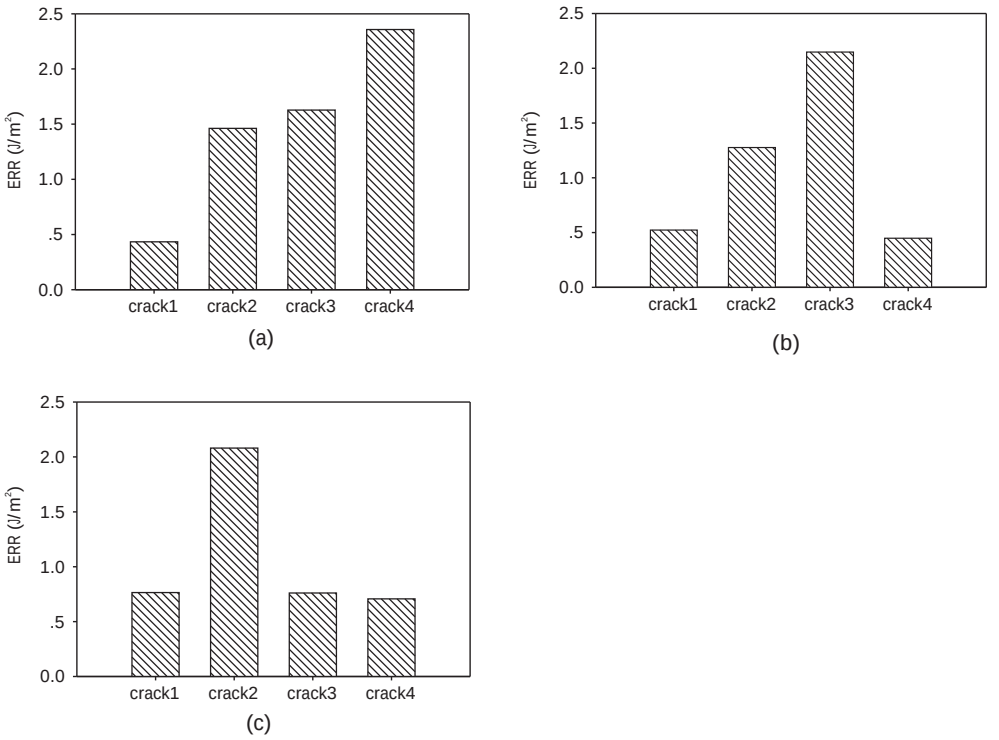


Figure 2.28 CPI-induced energy release rates for four-level interconnect models with different combinations of interlevel dielectrics: (a) ULK in all levels; (b) SiO_2 in the M4 level and ULK in others, and (c) SiO_2 in M4 and CVD OSG in M3 and ULK in others.

most level is the most critical, and the multilevel stacking structure has to be optimized in order to minimize the CPI effect on ULK interconnect reliability.

As shown in Figure 2.29, the calculated energy release rates increase dramatically from low-k (OSG and porous MSQ) to ultralow-k ILDs, especially for cracks 2 and 3. This trend is consistent with the results from the two-level interconnect model, which has shown increasing ERRs with decreasing ILD modulus (Figure 2.26). However, the magnitudes of the ERRs in the four-level model are considerably lower that those obtained from the two-level model, possibly due to denser metal lines providing stronger constraint on the cracks. Since ultralow-k materials are required for 45 nm technology and beyond, this result indicates that CPI will be a major concern due to the weak mechanical properties of the ultralow-k materials.

As a crack propagates in a multilevel interconnect structure, both the energy release rate and the mode mix at the crack tip vary. As illustrated by a two-dimensional model in Figure 2.30, as the crack grows from right to left along one interface, the energy release rate oscillates as a function of the crack length. When the crack tip is located close to the left corner of a metal line, the energy release rate peaks due to the peeling stress concentration. The magnitude of the peak increases with the crack length but seems to saturate toward a steady state. The phase angle of mode mix oscillates as well, but within a relatively small range. Apparently, the local material combinations and geometry complicate the stress field near the crack tip and thus the crack propagation along the interface. As a conservative design rule, the maximum energy release rate must be kept below the interface toughness at the corresponding mode mix to avoid interfacial delamination.

A crack propagation in a real interconnect structure due to CPI is shown in Figure 2.2. Apparently, the crack does not always propagate along one interface. Depending on the local material combination and geometry, an interfacial crack may kink out of the interface, causing cohesive fracture of low-k materials. Similarly, a cohesive crack may deflect into a weak interface. The selection of the crack propagation path depends on the loading conditions as well as material properties (including interfaces) and geometrical features in the interconnect structure. A general rule of crack propagation, as suggested by Hutchinson and Suo [23] for

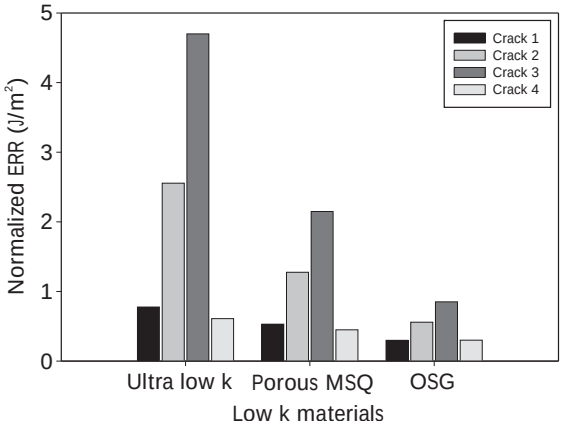


Figure 2.29 Comparison of CPI-induced energy releases rates in the four-level interconnects with low-k and ultralow-k ILDs.

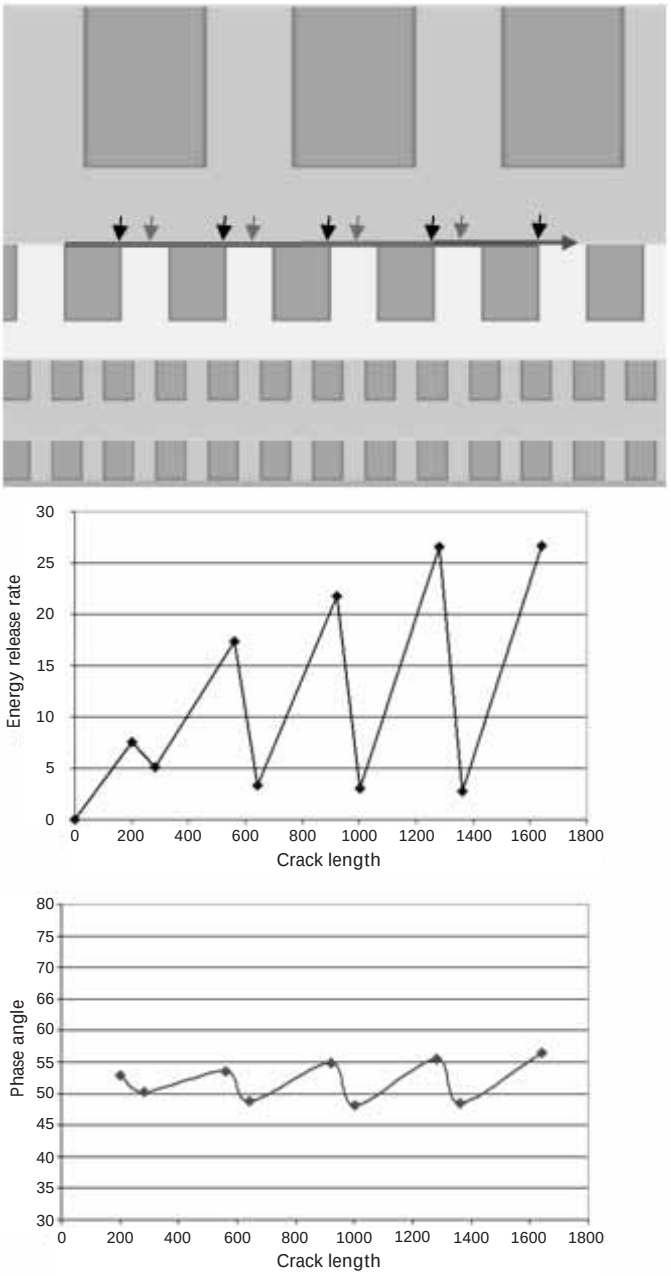


Figure 2.30 Crack length dependence of the energy release rate and mode mix of an interfacial crack.

anisotropic materials and composites, may be stated as follows: a crack propagates along a path that maximizes G / Γ, the ratio between the energy release rate and the fracture toughness. While cohesive fracture in an isotropic material typically follows a path of mode I ($\psi = 0$), the mode mix along an interfacial path varies, as does the interfacial fracture toughness. Therefore, the crack propagation not only seeks a path with the largest energy release rate but also favors a path with the lowest fracture toughness, either interfacial or cohesive. Due to the complexity of the materials

and structures, modeling of crack propagation in multilevel interconnects has not been well developed. Experiments have shown that cracks often propagate from upper levels to lower levels, eventually causing failure by die cracking. Figure 2.31 depicts a simple model of crack propagation in a multilevel interconnect due to CPI. The crack initiates at an upper-level interface, which has been shown to have a higher energy release rate compared to the same crack in a lower-level interface. As the crack propagates toward the lower levels and the total crack length increases, the energy release rate increases. Without detailed data of the interface toughness, the calculation of the energy release rate alone is not sufficient to predict the crack propagation path. Nevertheless, it illustrates a possible scenario in consistency with experimental observations.

2.7 Summary

Chip-package interaction has become a critical reliability issue for Cu/low-k chips during assembly into organic flip-chip packages, particularly for ultralow-k porous dielectrics to be implemented beyond the 65 nm node. In this chapter, we review the experimental and modeling studies to investigate the chip-package interaction and its impact on low-k interconnect reliability. The problem is explored using

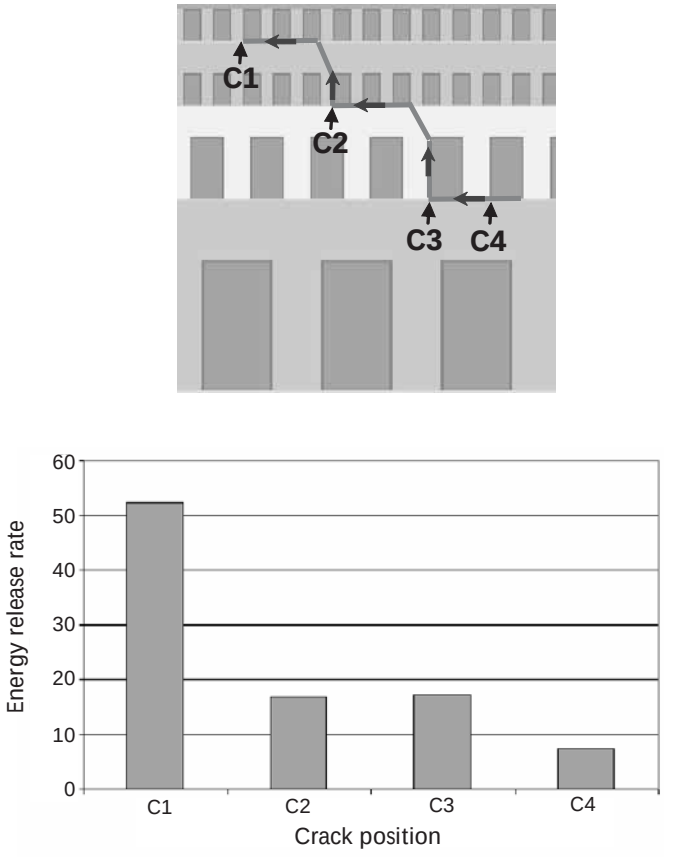


Figure 2.31 CPI induced crack propagation in a multilevel interconnect.

high-resolution moiré interferometry and multilevel submodeling, and its origin is traced to the large thermal stress induced by package deformation to drive crack propagation and the weak thermomechanical properties of the low-k dielectric material. The nature of interfacial delamination and crack growth in multilayered dielectric structures was discussed based on fracture mechanics. The chip-package interaction was investigated using 3D finite element analysis (FEA) based on a multilevel submodeling approach. The packaging-induced crack-driving force for relevant interfaces in Cu/low-k structures was deduced. The die-attach process was found to be a critical step, and the energy release rate was found to depend on the solder, underfill, and low-k material properties. Implementation of lead-free solder and ultralow-k material poses great threats to the Cu interconnect reliability by increasing the low-k delamination driving force. Finally, the effect of scaling and crack propagation in multiple Cu/dielectric line structures was investigated. Crack propagation was found to be a complex phenomenon depending on the local material combinations and geometry, which control the stress field near the crack tip and thus the crack propagation along the interface.

Recent efforts from within the industry and universities have significantly advanced the present understanding of chip-package interaction and its reliability impact on Cu/low-k interconnects. Many questions remain, and a major challenge in microelectronics packaging is to prevent cracks initiated at the edge of a chip from propagating into the functional area of the chip under thermomechanical loadings during packaging processes and service. The use of low-k and ultralow-k dielectrics in the interconnects presents even more of a challenge due to chip-package interactions and the significantly lower toughness of the low-k materials. One approach to preventing propagation of the edge cracks is to incorporate patterned metal structures around the perimeter of a chip as a crack-stop structure [19]. If designed properly, the metal structures can increase the fracture toughness along the path of crack propagation. A four-point-bend experiment has been used to determine the effective toughness of crack-stop structures [35]. The optimal design of crack-stop structures requires better understanding of crack propagation under the influence of chip-package interactions.

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