Circuit Analysis and Optimization of GAA Nanowire FET Towards Low Power and High Switching

V. Bharath Sreenivasulu (vbharathsree818@gmail.com)
National Institute of Technology Warangal https://orcid.org/0000-0003-3064-1522
Vadthiya Narendar
National Institute of Technology Warangal

Research Article

Keywords: Junctionless, GAA nanowire FET, Spacer length, ION/IOFF, SS.

Posted Date: November 11th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-954572/v1

Version of Record: A version of this preprint was published at Silicon on March 5th, 2022. See the published version at https://doi.org/10.1007/s12633-022-01777-6.

Abstract

The main aim of this work is to study the effect of symmetric and asymmetric spacer length variations towards source and drain on n-channel SOI JL vertically stacked (VS) nanowire (NW) FET at 10 nm gate length (L_G). Spacer length is proved to be one of the stringent metrics in deciding device performance along with width, height and aspect ratio (AR). The physical variants in this work are symmetric spacer length (L_{SD}), source side spacer length (L_S) and drain side spacer length (L_D). The simulation results give highest I_{ON}/I_{OFF} ratio with L_D variation compared to L_S and L_{SD}, whereas latter two variations have similar effect on I_{ON}/I_{OFF} ratio. At 25 nm ($2.5 \times L_G$) of L_D, the device gives appreciable ON current with the highest I_{ON}/I_{OFF} ratio (2.19×10^8) with optimum subthreshold slope (SS) and ensures low power and high switching drivability. Moreover, it is noticed that among optimal values of L_S and L_D, the device I_{ON}/I_{OFF} ratio has an improvement of 22.69% as compared to other variations. Moreover, the effect of various spacer dielectrics on optimized device is also investigated. Finally, the CMOS inverter circuit analysis is performed on the optimized symmetric and asymmetric spacer lengths.

1. Introduction

Increased growth in semiconductor market improved the transistor performance but with the impact od SCEs. Various attempts to overcome the SCE problem have resulted in radical changes in transistor structural design. Many researchers predict that the vertically stacked nanowire (VS-NW) structure, is future option to drive electronic industry, which has good gate controllability and great packing density, will be the eventual destination of the shrinking transistor. The VS superior NW performance is due to its gate-all-around (GAA) based architecture. Recent research [1–3] has shown that VS-NWs are capable of balancing outstanding low off-state and high on-state properties. However, none of these studies have taken into account the VS-NW structure's spacer optimization, which is an unavoidable for sub-10 nm nodes for better gate controllability [4]. Moreover, to increase device efficiency at sub-10 nm regime JL devices are formed. Simple manufacturing method, Junction free nature, low thermal budgets, doping concentration gradient, improved scalability, and immunity to short channel effects (SCEs) are all advantages of JL based devices. [5–8].

Moreover, the JL devices exhibits better I_{OFF} characteristics due to volume depletion nature. For volume depletion in JL FETs the need of channel thickness less than 10 nm is fundamental and advanced architectures like trigate, double gate, Gate all Around (GAA) structure is essential. Moreover, higher gate work function is also required for full depletion [9, 10]. Since JL device use volume conduction phenomena hence improves carrier transit speed and minimize surface roughness through scattering [11].

To minimize SCEs for sub-20 nm device's, the introduction of spacers is fundamental [4]. The addition of spacers, on the other hand, enhances series resistance and so minimizes drive current (I_{ON}) current performance. The flow of gate-source/drain carriers is restricted as the spacer length increases, even at

high V_{DS}. High-k spacers increase switching ratios (I_{ON}/I_{OFF}) by inducing field coupling via the fringing effect [12]. However, in order to achieve superior performance metrics, spacer length should be carefully chosen. Aside from thickness and width, spacer length is also carefully adjusted to improve transistor performance. According to research [13], the effect of drain asymmetry variation reduces leakages by 57 %. The inclusion of spacer reduces leakages mostly due to edge tunnelling of carriers. This paper explores symmetric and asymmetric spacer length variation on GAA NW FET at nano regime. Various performance metrics like I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, and SS are analyzed.

The paper is organized as follows. The section 2 describes device physics and device geometrical parameters. In section 3.1 symmetrical dielectric variation of spacer length optimization is performed on SS and I_{ON}/I_{OFF}. In section 3.2 source spacer length is varied (L_S) by keeping drain spacer length (L_D) constant. In section 3.3 drain spacer length is varied (L_D) by keeping L_S as constant. Section 4 illustrates the CMOS inverter performance of symmetric and asymmetric spacers.

2. Device Structure And Simulation Methodology

Figure 1 depicts the 3-D JL SOI nanowire FET and 2-D view of symmetric spacer. In this paper we have considered 3-D JL SOI VS NW FET to understand the effect of spacer length on device DC performance. The high-k dielectric HfO_2 is used as a spacer material to increase switching performance. Although the use of spacer length improves subthreshold performance, but reduces ON current. As a result, a spacer length with a high-k dielectric is provided to compensate for this impact, increasing ON current by increasing electron flow from source to drain. Furthermore, introducing high-k gate dielectric along with interfacial oxide (SiO_2) achieves a lower EOT and better gate electrostatics, the suppression of leakages, and the suppression of random threshold voltage changes [14, 15]. The OFF current is maintained <100 pA for all variations with a fixed work function of 4.8 eV. With Titanium (Ti) as the gate metal, continuous and uniform doping is maintained.

TABLE 1. Various Device Parameters Used for Simulation

Parameters	**JL VS NW FET**
Gate Length (L_G)	10 nm
Gate oxide thickness(t_{ox})-SiO_2	0.5 nm
Gate oxide thickness- HfO_2	3 nm
Metal Gate Thickness	5 nm
EOT (Equivalent Oxide Thickness)	0.75 nm
Each channel thickness and height	10 nm
Source/drain length	20 nm
Length of source or drain extensions (L_S/L_D/L_{SD})	Varied
Work function	4.8 eV
Source/channel/drain doping	10^{19} cm^{-3}

Higher channel doping concentrations activate Fermi Dirac statistics. Since carrier degradation phenomena are produced by surface roughness, acoustic phonon scattering, and doping dependency mobility reduction, the Lombardi mobility model is taken into account. A band-to-band tunnelling model is included to handle the band gap narrowing effect that can occur as a result of increased channel doping. To account for carrier production and recombination events, the Shockley-Read-Hall (SRH) model is used. To account for quantum correction effects, quantum models are used. The threshold voltage is extracted at (W/L) × 10^{-7} A at V_{DS} = 0.9 V and V_{GS} = 1.2 V. The simulation models have been thoroughly calibrated using experimental data [17]. The simulations are carried out through 3D Cogenda Visual TCAD simulator [16].

3. Result Analysis And Discussion:

3.1 Symmetric variation of Spacer Length

Fig 2 depicts the ON-OFF parameters and subthreshold characteristics received from the TCAD simulator are examined. The VS NW FET demonstrates behavioral change with modification in spacer length, as shown in Fig. 2(a) and (b), with both I_{ON} and I_{OFF} decreasing as spacer length increases. Longer spacers produce good subthreshold behavior but result in a decrease in ON current due to the increased series resistance. Due to downfall in edge tunnelling from source to drain and gate overlap results in lowering of I_{OFF} with more spacer distance i.e., higher L_{SD}/L_G ratio.

From Fig. 3 it is observed that the symmetric spacer exhibits highest I_{ON}/I_{OFF} of 2.65×10^8 and lower SS of 63 mV/dec at $L_{SD} = 1.5 \times L_G$. Moreover, the device exhibits diminished I_{ON}/I_{OFF} at $L_{SD} = 2 \times L_G$ and thus removed from design of symmetric spacer perspective.

3.2 *L_S variation with fixed L_D*

The length of the spacer dielectric is asymmetrically altered in this section. The source side spacer length is adjusted while the drain spacer length is kept constant at 1.5 × L_G, because the device achieves the maximum I_{ON}/I_{OFF} ratio and mild SS at this symmetric spacer length. From the Fig.4(a) and (b) increase in L_S length the ON current decreases at fixed L_D length of 15 nm. From the Fig.5 the I_{ON}/I_{OFF} ratio increases with raise in L_S/L_G value and reaches to highest value at 1.5 × L_G.

Fig 5 depicts the asymmetric spacer variation of L_S in ON state. The device exhibits highest I_{ON}/I_{OFF} ratio at $L_S = 1.5 \times L_G$. The I_{ON}/I_{OFF} of 2.6×10^8 is obtained at source spacer length optimization which is permissible for driving logic applications. However, the device exhibits down fall after $L_S = 1.5 \times L_G$ due to increase of OFF state electron tunneling with more L_S.

3.3 L_D variation with fixed L_S

In this section, the same analysis as in section 3.2 is carried out, but the drain side spacer length is altered while the source side spacer length is fixed at 1.5 × L_G. The greater the L_D/L_G, the lower the I_{OFF} and the lower the I_{ON}, as shown in Fig. 6(a) and (b). The I_{ON} increases with lower L_D length. Since higher L_D of device leads to higher resistance to electron flow. Moreover, the I_{OFF} which is significant for low stand by power applications is reduced with higher L_D/L_G value. Since in OFF state the spacer dielectric fringing fields increase the potential barrier height and restrict tunneling of electrons.

From Fig.7, increase in spacer length the I_{ON}/I_{OFF} ratio increases up to $2.5 \times L_G$ and then degrades. The device achieves the highest I_{ON}/I_{OFF} ratio at $L_S = 15$ nm and $L_D = 25$ nm at $L_G = 10$ nm with acceptable SS. Moreover, the device I_{ON}/I_{OFF} ratio falls after $2.5 \times L_G$ due to reduced fringing effect with larger L_D. Thus, spacer optimization is vital for enhanced performance at nano regime.

3.4. *Comparisonof source/drain sidespacerlengthvariation*

The performance metrics of L_S and L_D variation on I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, and SS are compared in this section and displayed in Figs. 8 and 9. Both L_S and L_D variation on VS NW FET shows contrasting effect on performance metrics. From Fig.8(a) and
(b), both ON current and OFF current decreases with increase in L_S and L_D. The ON current of L_S is higher compared to L_D up to $1 \times L_G$, whereas opposite behavior results from $1.5 \times L_G$ to $2.5 \times L_G$.

The OFF current of L_S is more compared to L_D with spacer distance variation. The lowest OFF current for L_S and L_D takes place at highest spacer length i.e., at $2.5 \times L_G$ whereas, the highest OFF current occurs at lowest spacer distance i.e., $0.2 \times L_G$. Since the highest OFF current occurs at $0.2 \times L_G$, $0.5 \times L_G$ and hence

they are discarded for device design prospective. The permissible L_S and L_D values for device design are 1 × L_G, 1.5 × L_G, 2 × L_G, and 2.5 × L_G respectively. However, the best optimized device set is at L_S = 1.5 × L_G and L_D = 2.5 × L_G with acceptable SS.

Figure 9(a) and (b) shows the I_{ON}/I_{OFF} and SS performance of the VS NW FET with both L_S and L_D versions. The I_{ON}/I_{OFF} ratio diminishes after 2 × L_G for L_S whereas it increases up to 1.5 × L_G for both L_S and L_D spacer length variations, whereas the ratio degrades. So, the maximum allowable range of L_S variation is are limited to L_S = 1.5 × L_G to drive device for better switching and low power applications.

Figure 9(a) shows the SS performance of the VS NW FET for both L_S and L_D variations, with the highest SS value at 0.2 × L_G and the lowest value at 2.5 × L_G. Except at 0.2 × L_G, the device achieves the lowest SS among L_S, L_D variations.

4. Spacer Dielctric Optimization

The Figure 9(a) and (b) show the I_D-V_{GS} characteristics with symmetric (L_S = 15 nm and L_D = 15 nm) and asymmetric (L_S = 15 nm and L_D = 25 nm) combinations.

The simulated transfer characteristics (I_D-V_{GS}) with different spacer dielctrics of JL nanowire FET with symmetric spacer are shown in Figure 10(a). With all spacer dielectrics, the device has an I_{OFF} of less than nA. With spacer dielectrics, however, the I_{ON} varies from 60 to 75 A. The I_D-V_{GS} of asymmetric spacer variation follow the same pattern as symmetric variation, as shown in Fig. 10(b). For all spacer combinations, the I_{OFF} of the device with asymmetric spacer is less than nA. With the HfO_2 spacer, the I_{ON} reaches a maximum of 68 A, while with no spacer, it reaches 54 A. According to the results, a rise in the '*k*' value causes a decrease in I_{OFF}. Stronger fringing fields result in lower I_{OFF} when the '*k*' value is higher. Due to the spacer fringing electric fields, the depletion region improves. The p-n junctions form the depletion zone in inversion mode FETs, whereas energy barrier generation owing to depletion in the OFF state occurs in JL devices. The subthreshold current decreases as the spacer dielectric value increases because of high vertical electric field at V_{DS} = 0.9 V and V_{GS} = 0 V i.e., in the OFF state. Furthermore, the I_D is marginally affected in the ON state due to the zero electric field induced by the flat band situation. In comparison to Air and SiO_2 spacers, the HfO_2 followed by Si_3N_4 spacer has good switching behavior and a lower I_{OFF} at nano-regime. As a consequence of the analysis, high-k spacer dielectrics such as Si_3N_4 and HfO_2 excel with better subthreshold and switching behavior at nano-regime, ensuring potential candidate for low-power applications [17].

The I_{ON} for a device is calculated at V_{DS} = 0.9 V and V_{GS} = 1.2 V whereas, I_{OFF} is calculated at V_{DS} = 0.9 V and V_{GS} = 0 V. As seen in Fig. 11(a), the I_{ON} is much lower with the asymmetric spacer than with the symmetric spacer. HfO_2 has the smallest I_{ON} decrease of all the spacer combinations, at 11.24%. The Si_3N_4 spacer and no spacer materials had a 13.26 percent and 15.8 percent drop, respectively. Because

higher fringing fields with a high-k spacer diminish the I_{ON} decrement with asymmetric spacer compared to a low-k spacer, the I_{ON} decrement with asymmetric spacer is minimized. The IOFF for various spacer dielectrics is shown in Figure 11(b). Although symmetric spacers improve ION, asymmetric spacers diminish direct tunnelling of electrons in the OFF state due to the greater distance between the channel and drain. The I_{ON}/I_{OFF} ratio of a device with varied spacer dielectrics is shown in Figure 11(c). With only SiO_2, Si_3N_4, and HfO_2 spacers, the asymmetric spacer has a greater I_{ON}/I_{OFF} ratio than the symmetric spacer. In comparison to Air and no spacer, the symmetric spacer exhibits a modest increase in the I_{ON}/I_{OFF} ratio due to increased I_{ON} and marginal I_{OFF} fluctuation. The negligible difference in I_{OFF} between symmetric and asymmetric spacers for Air and no spacer is attributed to ineffective leakage control due to decreased dielectric fringing fields. Furthermore, the asymmetric spacer aims to improve the I_{ON}/I_{OFF} ratio while lowering coupling and parasitic capacitances [18, 19]. With HfO_2 spacer, the asymmetric spacer improves the I_{ON}/I_{OFF} ratio by 19.6% and reduces IOFF by 34.13% when compared to the symmetric spacer. Furthermore, as seen in Fig. 11(d), the performance of SS is poorer with an asymmetric spacer. Although the I_{ON} is lowered by 11.24% with the asymmetric spacer, the subthreshold behavior and switching performance are improved thanks to a spectacular reduction in I_{OFF}.

The electric field on the channel region of the symmetric spacer is higher than that of the asymmetric spacer, as shown in Fig. 12(a) and (b). Due to larger distance between the channel and drain in the asymmetric spacer the electric field lines are minimized into the silicon and thus enhanced tunnelling width. Figures 12(c) and 12(d) demonstrate the potential distribution of JL nanowire FETs with symmetric and asymmetric spacers. Because of the long distance between channel and drain, an asymmetric spacer ensures lower SCEs.

4. CMOS Inverter Performance Analysis

Figure 13 depicts the I_D-V_{GS} characteristics of both NMOS and PMOS with optimized symmetric and asymmetric spacers. The gate length L_G = 10 nm, EOT (high-k+SiO_2) = 0.75 nm, Si channel thickness =10 nm, and HfO_2 as spacer material have all been maintained same as in NMOS. The design for PMOS symmetric spacer is L_S = L_D = 15 nm and L_S = 15 nm and L_D = 25 nm for asymmetric spacer, which is maintained same as NMOS. The V_t is matched for both NMOS and PMOS by work function engineering. The SS and DIBL of symmetric and asymmetric spacers NMOS are depicted inside Fig. 13. Furthermore, the delay performance is calculated by CMOS inverter as shown in Fig 14.

The CMOS inverter delay (T_D) is calculated using the effective drive current model, such as in equation 1 [20], where I_{EFF} is the effective drive current, C_L is the load capacitance, and V_{DD} is the supply voltage of the first stage inverter at the output node.

$$T_D = 0.5C_L \times \frac{V_{DD}}{I_{EFF}} \quad (1)$$

The evaluation of C_L is carried through parasitic first stage output and input capacitance of second stage as (2) and a value of 1.5 is considered for miller coefficient (M) [21]. The C_{IN2} is calculated by using the weighted distribution of NMOS and PMOS during input transitions of the OFF and ON-state capacitances. During the output-fall transition to $0.5V_{DD}$, the transistor P2 remains ON while N2 switches from OFF to ON. As a result, the OFF to ON ratio of 0.25: 0.75[20-22] is utilized to calculate C_{IN2} (3).

$$C_L = M\,C_M + C_{IN2} \quad (2)$$

$$C_{IN2} = 0.25\,C_{G\_OFF} + 0.75\,C_{G_{ON}} \quad (3)$$

Where, $I_{EFF} = (I_L + I_H + I_M)/3$, $I_M = I_{DS}$ ($V_{DS} = 0.75V_{DD}$, $I_H = I_{DS}$ ($V_{GS} = V_{DD}$, $V_{DS} = 0.5V_{DD}$), $V_{GS} = 0.75V_{DD}$) and $I_L = I_{DS}$ ($V_{GS} = 0.5V_{DD}$, $V_{DS} = V_{DD}$,) as defined in [21], and are taken from the individual I_D-V_{GS} characteristics.

Figure15 depicts the CMOS inverter delay of symmetric and asymmetric spacer dielectrics. The terms t_{PHL} and t_{PLH} defines the speed of the logic and detrimental in calculating propagation delay (t_P). The symmetric spacer exhibits lower delay compared to asymmetric spacers. Since in asymmetric spacer the L_D is 25 nm which is higher compared to symmetric spacer which is 15 nm. Thus, symmetric spacer is better for circuit applications at nano regime. However, asymmetric spacer outperforms symmetric spacer in terms of OFF current, subthreshold performance, and good switching behavior.

Conclusion

In thiswork detailed study of spacer length has been presented on n-channel SOI JL VS NW FET. According to the performance optimization metrics, spacer length modification has a serious effect on SCE reduction. By result analysis the I_{ON}/I_{OFF} ratio with L_S =1.5 nm and L_D = 2.5 nm exhibits best performance. Among optimized L_S and L_D values an improvement of 22.69 % in I_{ON}/I_{OFF} ratio is noticed with $L_D = 2.5 \times L_G$, whereas the SS is reduced i.e., 63 mV/dec to 62 mV/dec. The highest OFF current with $0.2 \times L_G$ and $0.5 \times L_G$ for both L_S and L_D variations are not considered for device design considerations. For L_S variations $2 \times L_G$ and $2.5 \times L_G$ are neglected, whereas for L_D the spacer length $3 \times L_G$ is not considered since the device I_{ON}/I_{OFF} ratio tends to down fall. From the result analysis with L_S = 15 nm L_D = 25 nm and high-k spacer for 10 nm n-channel JL VS NW FET shows best optimized results. Hence optimized asymmetric VS NW FET exhibit low OFF current, higher I_{ON}/I_{OFF} ratio and hence assures low standby power requirements and low power applications. Moreover, symmetric spacer exhibits higher I_{ON} and lower delay and assures high performance applications.

Declarations

Author Contributions

V. Bharath Sreenivasulu: Writing- Original draft preparation, Formal Analysis, Investigation, Simulation, Data Curation.

V. Narendar: Supervision, Resources.

Financial interests: The authors declare they have no financial interests.

Funding: No Funding Received.

Conflict of Interest: The author has no conflicts of interest to declare that are relevant to the content of this article.

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Availability of data and material: Not applicable.

Consent to Participate: Not applicable.

Consent for Publication: Not applicable.

Acknowledgements: The authors thank to the department of Electronics and Communications Engineering, NIT Warangal for providing the TCAD Tools.

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Figures

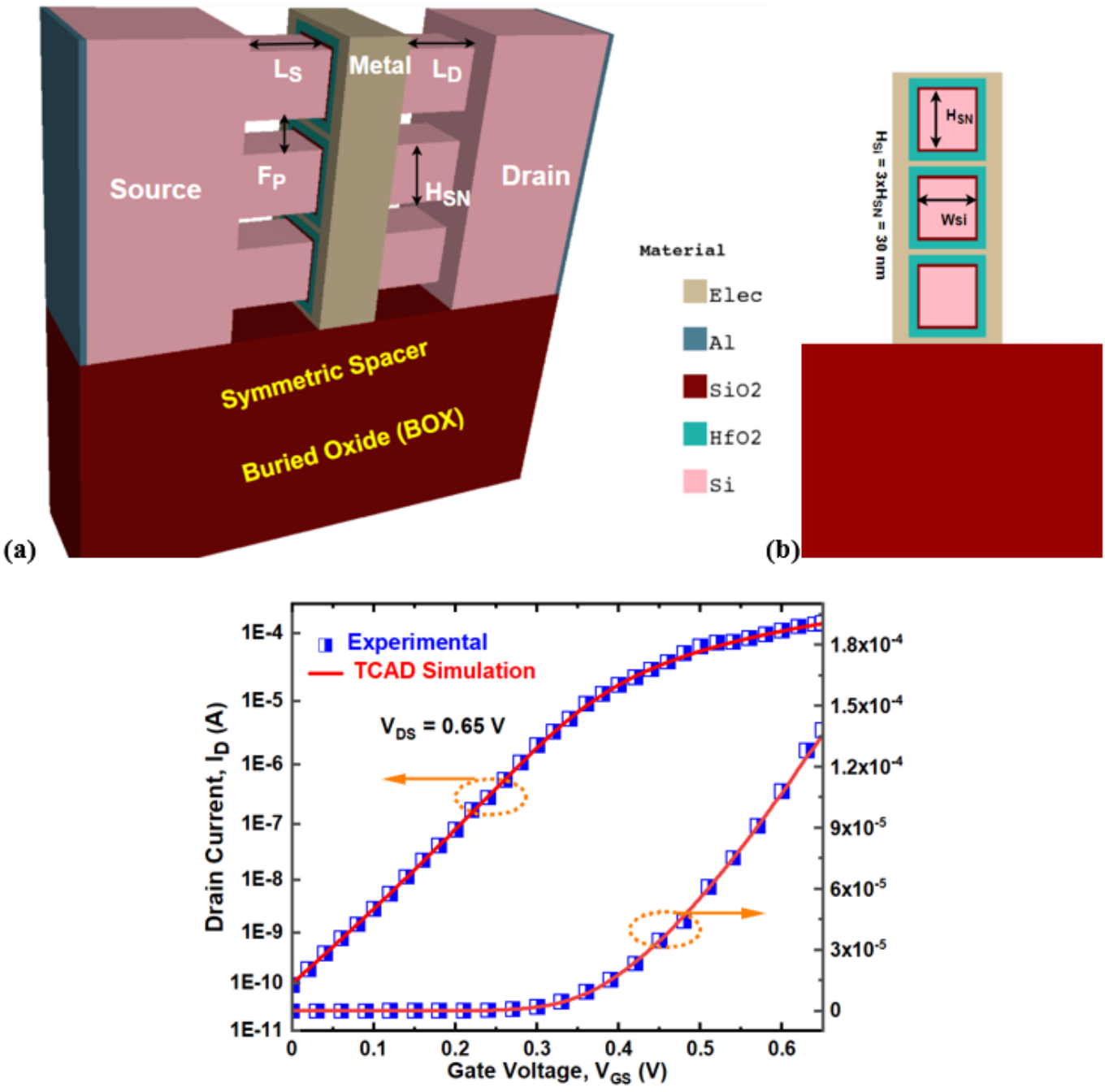


Figure 1

(a) 3-D (b) 2-D view of JL SOI vertically stacked nanowire FET (c) Calibration.

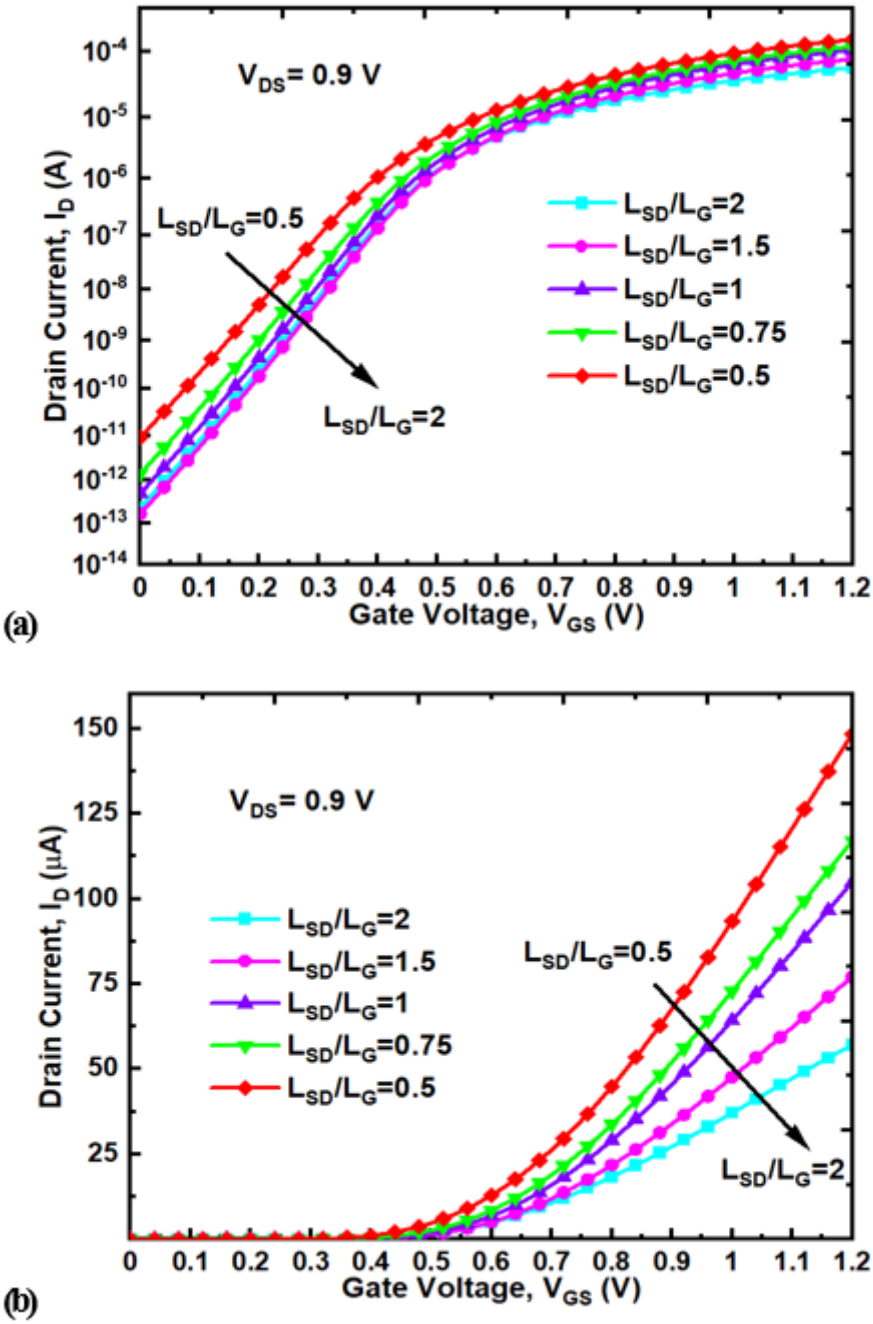


Figure 2

Symmetric variation of source side spacer (LS) length with fixed drain spacer (LD) length (a) Log scale (b) Linear scale.

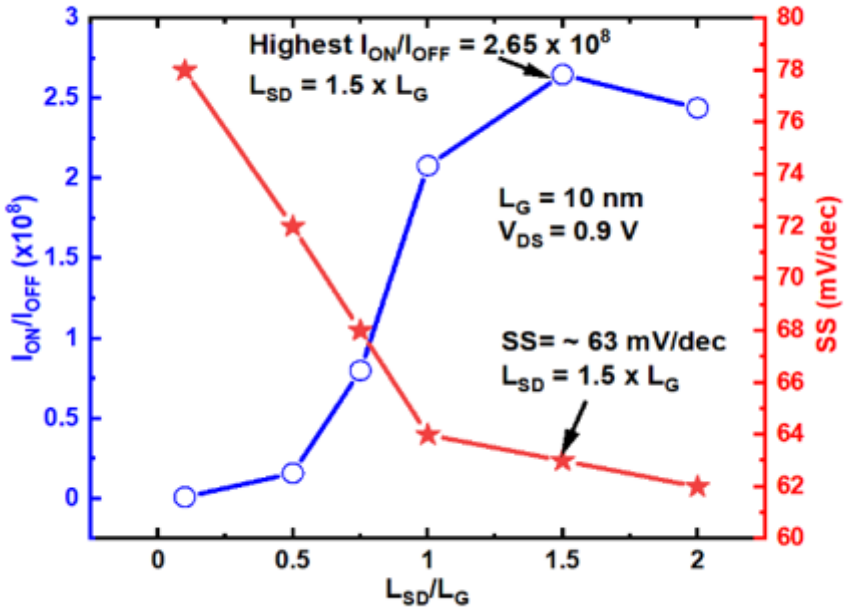


Figure 3

Symmetric variation and its ION/IOFF and SS.

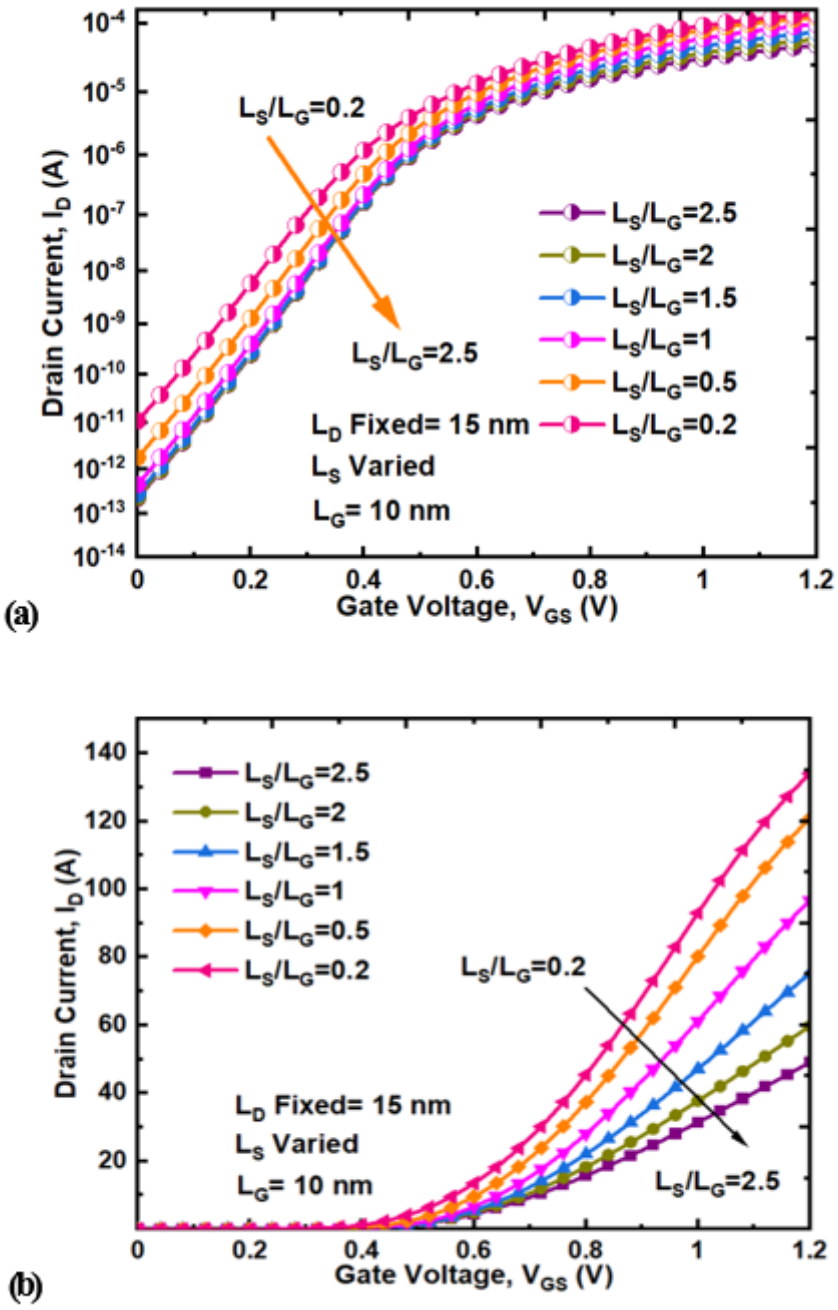


Figure 4

ID-VGS variation (a) Log scale (b) Linear scale.

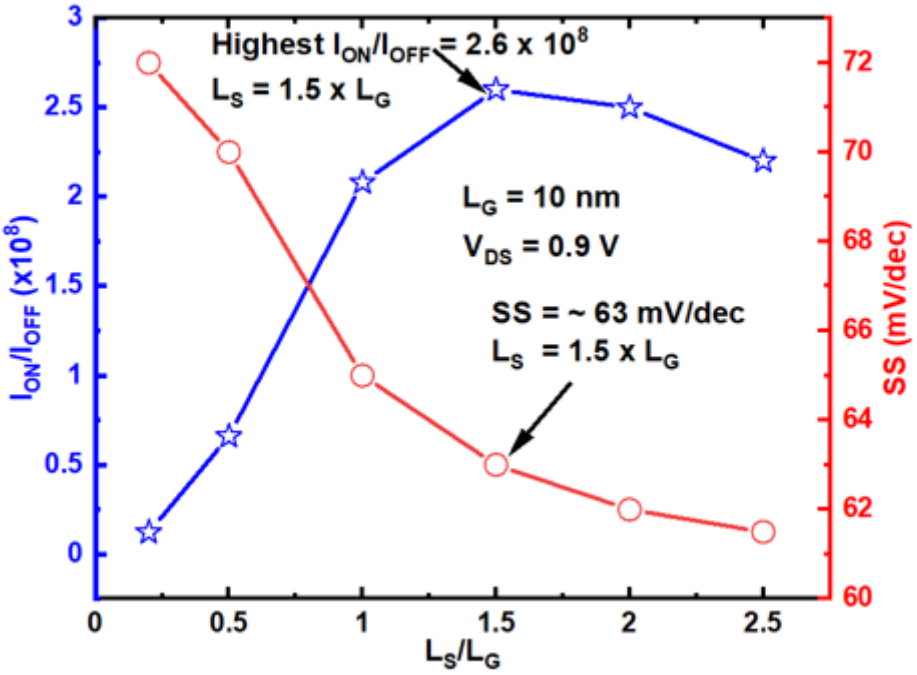
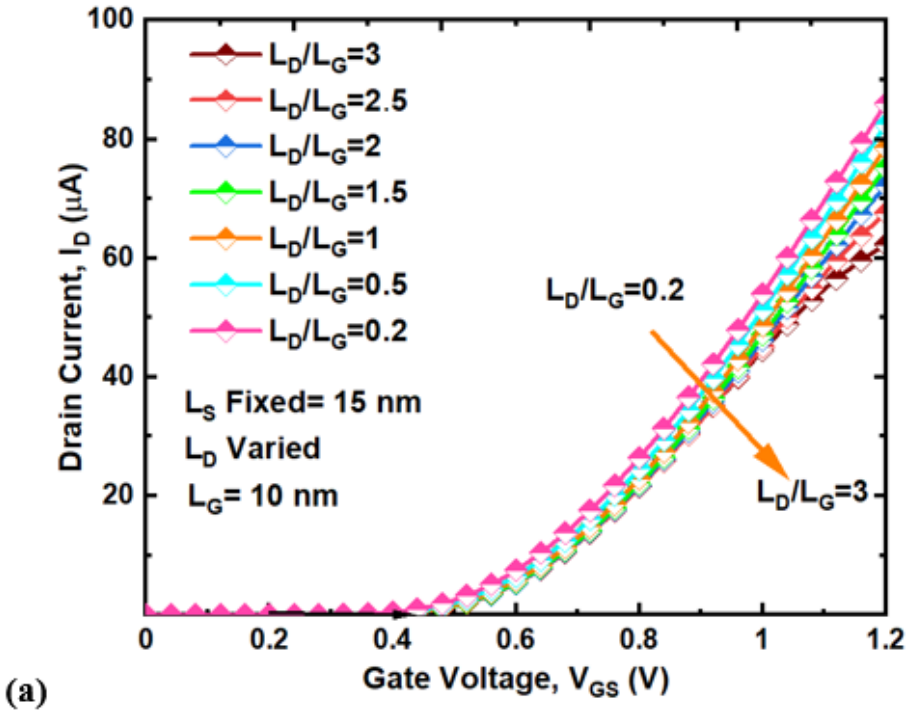


Figure 5

The SS and ION/IOFF variation of VS NS FET at VDS=0.9 V and VGS=1.2 V.



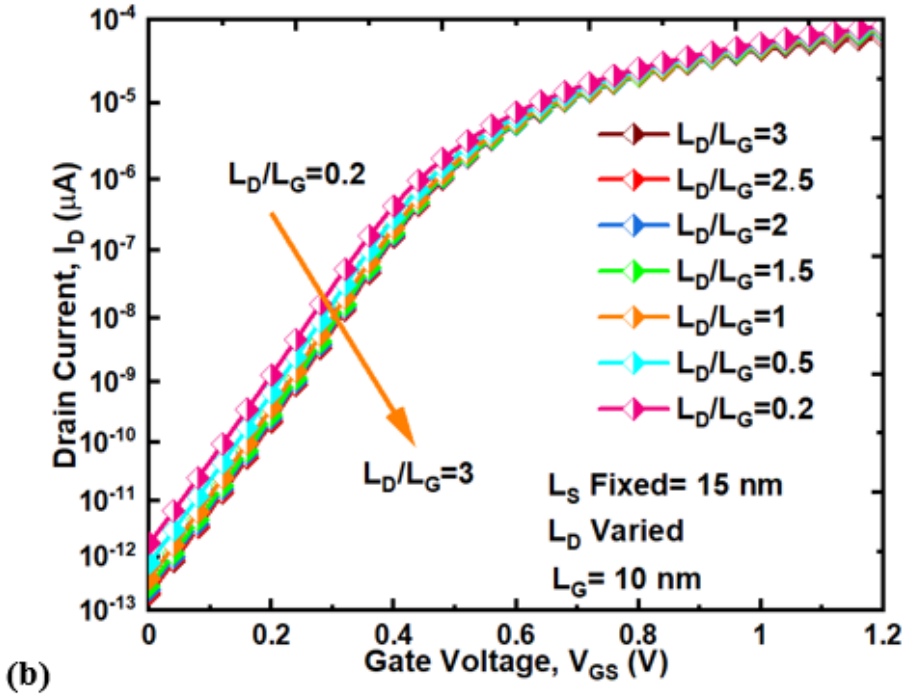


Figure 6

LD variation (a) Linear (b) Log characteristics.

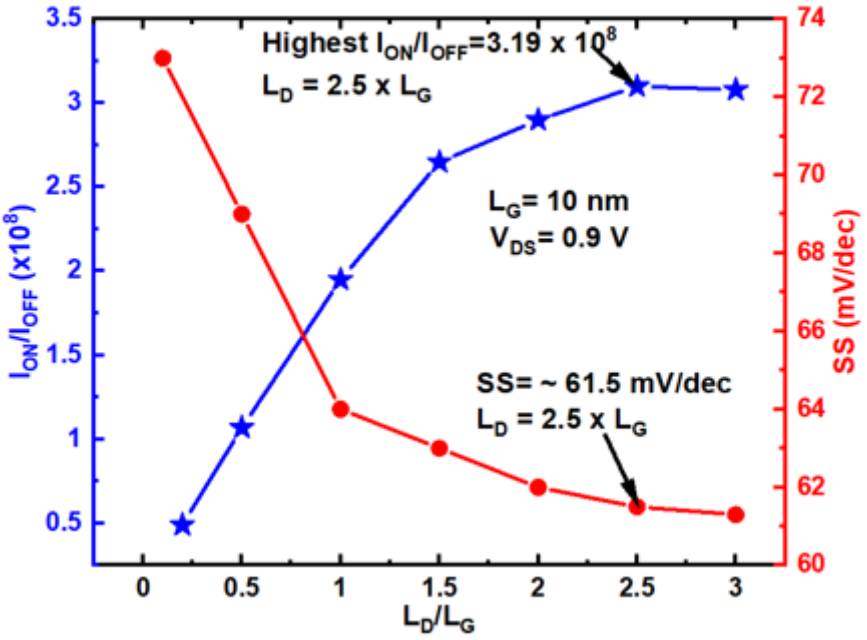


Figure 7

LS and LD variation of spacer length (a) ION/IOFF ratio and Subthreshold slope (SS).

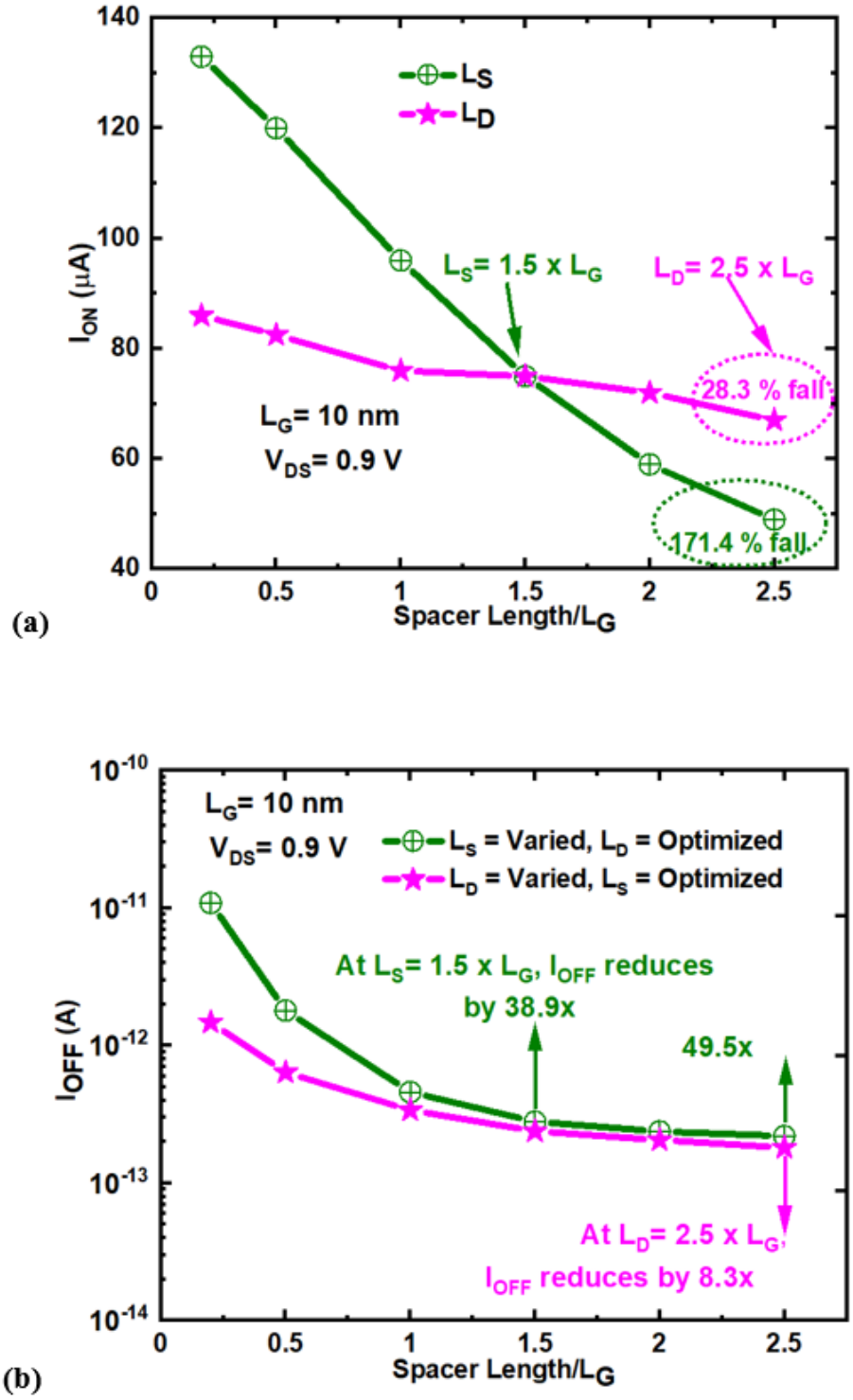


Figure 8

LS and LD variation of spacer length (a) ION/IOFF ratio (b) Subthreshold slope (SS).

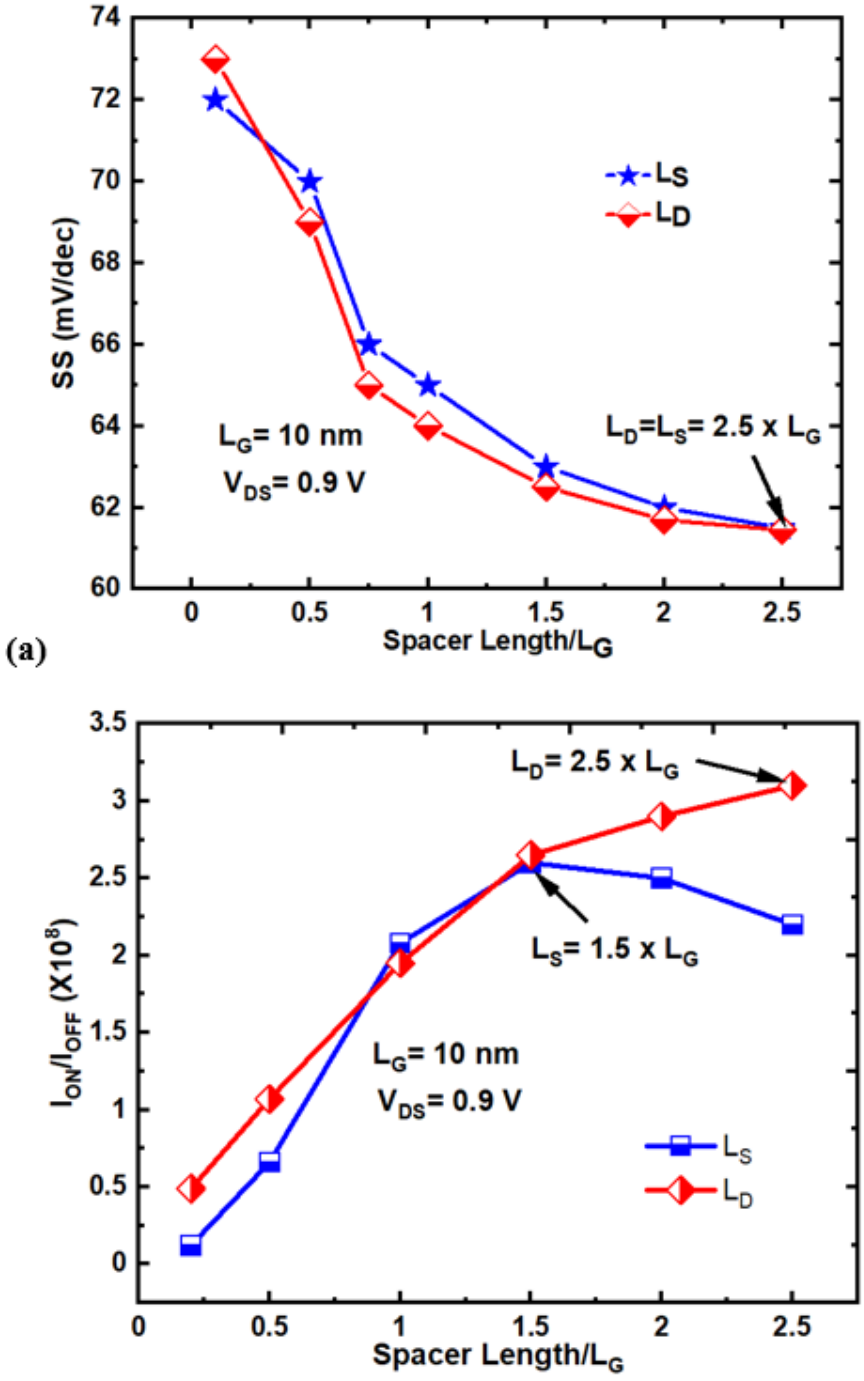


Figure 9

LS and LD variation of spacer length (a) ION/IOFF ratio (b) Subthreshold slope (SS).

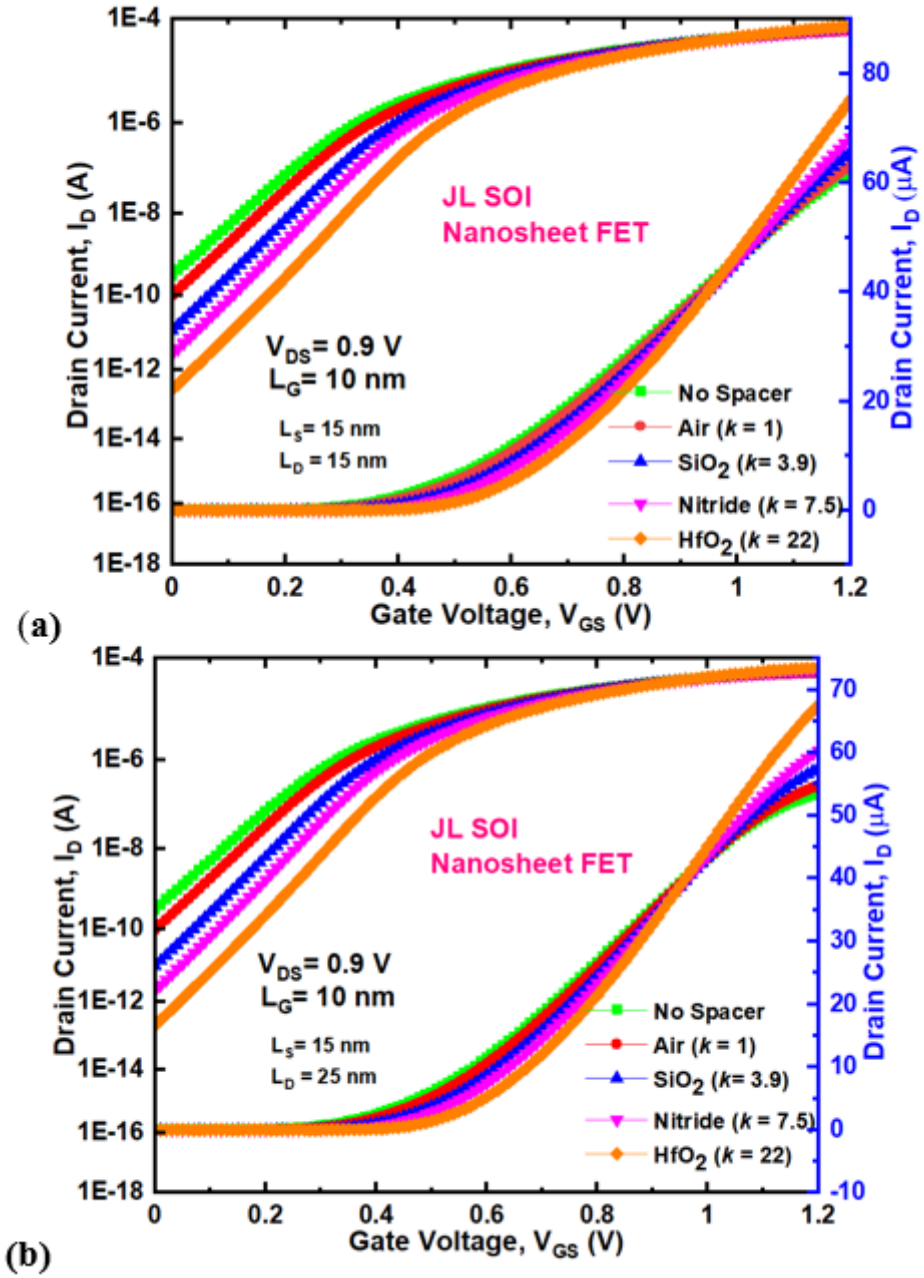


Figure 10

(a) LS=LD=15 nm (b) LS=15 nm LD= 25 nm in log scale and linear scale.

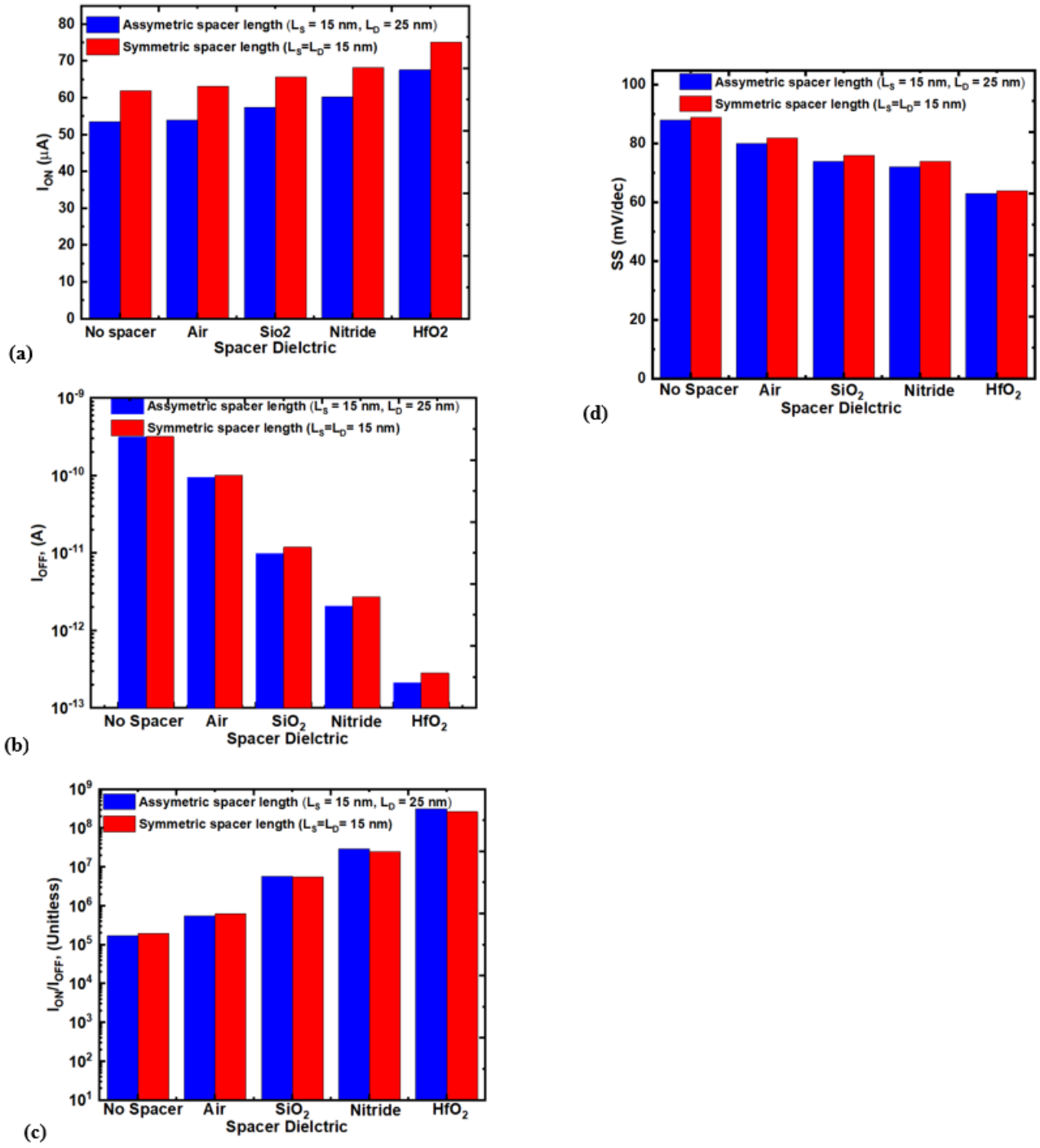


Figure 11

Nanowire FET electrical characteristics (a) ION (b) IOFF (c) ION/IOFF and (d) SS.

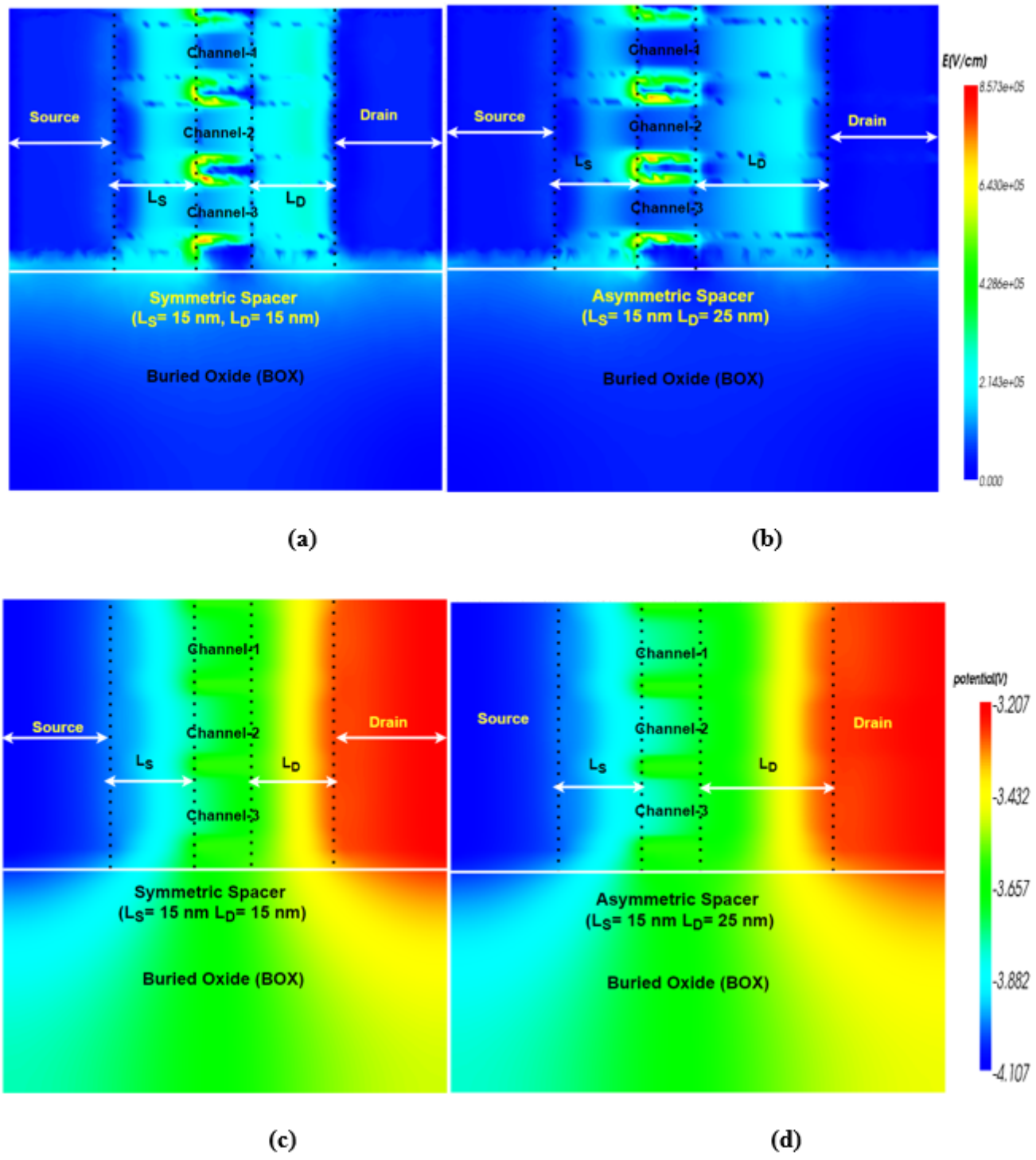


Figure 12

Electric field and potential distribution contour plots (a, c) LS = LD = 15 nm (b, d) LS = 15 nm LD = 25 nm in ON state with HfO2 spacer.

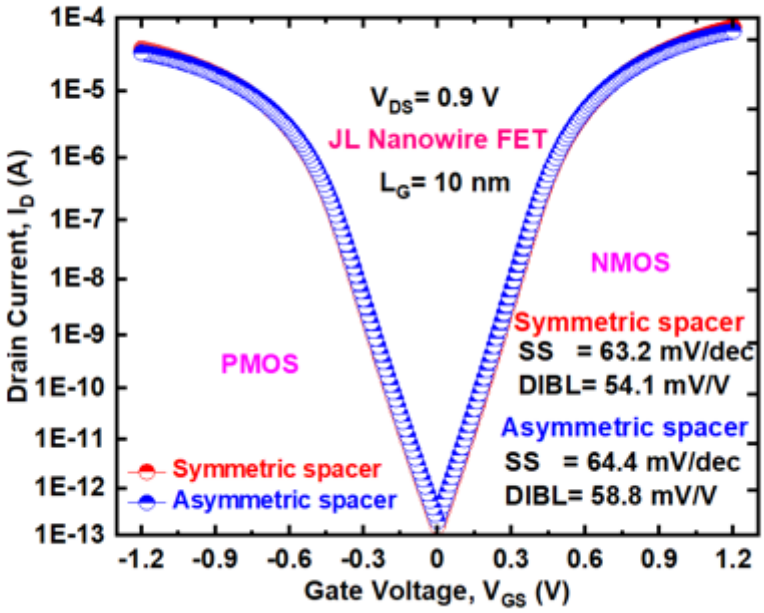


Figure 13

PMOS and NMOS ID-VGS characteristics of symmetric and asymmetric spacer.

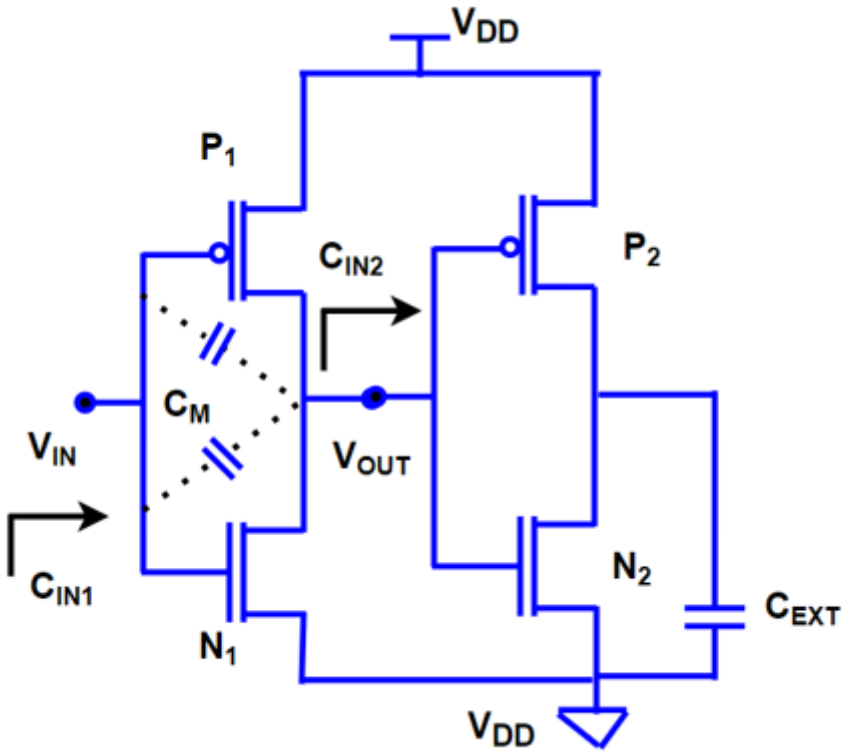


Figure 14

Schematic view of CMOS inverter.

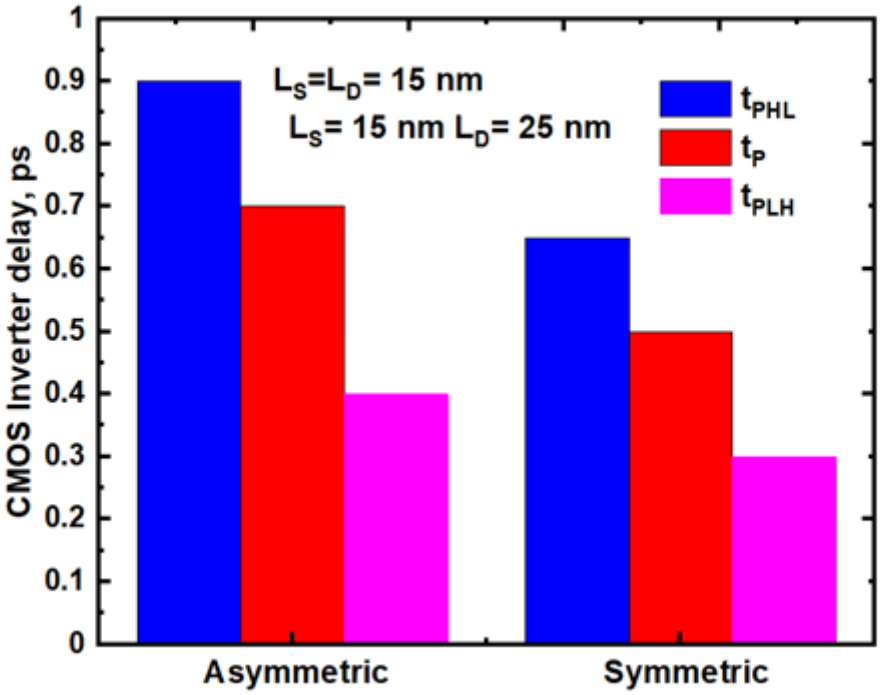


Figure 15

Symmetric and asymmetric CMOS inverter delay.