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Circuit Implementation of Variable-Order Scaling Fractal-Ladder Fractor with High Resolution

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Abstract: Extensive research has been conducted on the scaling fractal fractor using various structures. The development of high-resolution emulator circuits to achieve a variable-order scaling fractal fractor with high resolution is a major area of interest. We present a scaling fractal-ladder circuit for achieving high-resolution variable-order fractor based on scaling expansion theory using a high-resolution multiplying digital-to-analog converter (HMDAC). Firstly, the circuit configuration of variable-order scaling fractal-ladder fractor (VSFF) is designed. A theoretical demonstration proves that VSFF exhibits the operational characteristics of variable-order fractional calculus. Secondly, a programmable resistor–capacitor series circuit and universal electronic component emulators are developed based on the HMDAC to adjust the resistance and capacitance in the circuit configuration. Lastly, the model, component parameters, approximation performance, and variable-order characteristics are analyzed, and the circuit is physically implemented. The experimental results demonstrate that the circuit exhibits variable-order characteristics, with an operational order ranging from −0.7 to −0.3 and an operational frequency ranging from 7.72 Hz to 4.82 kHz. The peak value of the input signal is 10 V. This study also proposes a novel method for variable-order fractional calculus based on circuit theory. This study was the first attempt to implement feasible high-resolution continuous variable-order fractional calculus hardware based on VSFF.

Keywords: fractional calculus; variable order; fractional-order circuits/systems; analog realization; emulator

1. Introduction

Fractional calculus, a branch of mathematics, has been widely implemented in the various fields of science and engineering [1–3]. Although it typically has a constant order, its application in describing new phenomena and problems with an operational order dependent on variables such as time and space is difficult. These problems can be better described using variable-order fractional calculus [4–6], which was first proposed by Samko and Ross [7] in 1993. Variable-order fractional calculus is expressed through mathematical functions that can be used to model natural phenomena and processes. The studies conducted on variable-order fractional calculus were primarily focused on the mathematical description of variable-order phenomena and processes and on the theory of variable-order fractional calculus application system design [4–6,8–12]. However, studies on the implementation of flexible and controllable physical entities of variable-order fractional calculus are scarce.

The solid-state fractor can be used as the physical entity of variable-order fractional calculus operation. However, it faces certain limitations, such as a narrow range of operational order variation, limited temperature control, and difficulty in operational order adjustment [13,14]. Analog circuit implementation is an important approach that enables the flexible

and controllable physical implementation of variable-order fractional calculus operation. Sierociuk et al. conducted several pioneering studies [15–17]. They use analog circuits to implement many kinds of variable-order fractional calculus circuits. These studies primarily employed the switching strategy to switch between two or three-order types. Constant-order fractor has been used in variable-order circuits and systems [15–18]. Variable-order fractional impedance (variable-order fractor) is a basic unit circuit or element that can perform variable-order fractional calculus. Variable-order fractional calculus can be realized by changing the operational order while maintaining the structure of the variable-order fractor circuit. In [19], a fractor circuit was designed based on rational approximation, and the order was changed by adjusting the transconductance operational amplifier control current. The operational order was switched between 0.2, 0.5, and 0.8; however, a physical circuit was not implemented. The studies conducted on variable-order fractor with a low operational order variation, narrow range, and regulation difficulties remain limited, to the best of our knowledge. Additionally, the studies conducted on circuit implementation are scarce.

To date, the studies conducted on fractor primarily focused on constant-order fractor circuits. These studies primarily involved two types of constant-order fractor [20]. The first type is constructed either directly or by modeling the phenomena of electrochemistry or other scientific fields, such as Liu-Kaplan [21], 2h-type fractal-tree [20], fractal-ladder [22,23], and fractal-chuan fractor [22–24]. The second type is constructed by designing a circuit-realizable rational function to approximate the performance of fractional-order operators such as the Oustaloup algorithm [25,26], Dutta Roy's fractor [27], and Carlson's iterating rational approximation algorithm [28,29].

In a previous study, we developed scaling expansion theory [30,31]. This theory can be used to extend multiple fractors, thereby overcoming the limitation of only realizing half- to arbitrary-order operations [30,32,33]. Scaling expansion theory can also be used in mathematics to extend the algebraic iterative equation, which describes the rational approximation of half-order operators into an irregular scaling equation describing arbitrary fractional operators. This theory can be used to construct the scaling fractal-lattice [30,31], scaling fractal-chuan [32], scaling fractal-chain [33], and scaling fractal-ladder fractor [34]. The scaling fractal fractor presents a high operating frequency bandwidth.

Scaling expansion theory is used to extend the semi-order fractor to a fixed scaling structure based on the required constant order. The theory is employed to realize the circuit of a fractional memristor of the scaling fractal-lattice [30] and scaling fractal-ladder fractor [34]. The lumped parameter value adjustment with the port flux or charge must be solved to achieve the scaling fractal fractional memristor [34]. It is similar to that the operational order adjustment must be solved to achieve the variable-order fractor.

Several studies have been conducted on scaling fractal fractor by using various structures [30–34]. However, the design of high-resolution emulator circuits to achieve high-resolution variable-order scaling fractal fractor is theoretically challenging. A variable-order scaling fractal-ladder fractor (VSFF) circuit implementation method is proposed to overcome this issue. The main contributions of this study are as follows:

- The proposed circuit can realize the VSFF, thereby overcoming the limitations faced by the existing variable-order fractor, such as limited operational order variation, narrow range, and difficult adjustment [13,14,19].
- A programmable resistor–capacitor series circuit and programmable universal electronic component emulators are designed based on the high-resolution multiplying digital-to-analog converter (HMDAC). These emulators can also be applied to other variable-order fractor circuits, memristor emulators, and memcapacitor emulators [35–37].
- This paper also proposes a method for variable-order fractional calculus based on circuit theory.

The remainder of this paper is organized as follows. Section 2 presents the VSFF circuit configuration. A programmable resistor–capacitor series circuit emulator and a

universal electronic component emulator are designed based on the requirements of the circuit configuration. Section 3 presents the model and component parameters in the VSFF and the calculation of the relative error of equivalent parameters of the programmable circuit. The approximation performance and variable-order characteristics of the VSFF are analyzed in the frequency domain. The VSFF is implemented, and the variable-order operation characteristic of the circuit is experimentally validated. Sections 4 and 5 present the discussions and conclusions, respectively.

2. VSFF Design

This section describes the design of the proposed VSFF. Firstly, the circuit configuration is presented. Subsequently, the emulators required to realize the programmable resistor–capacitor series circuit, universal electronic capacitor, and resistor components are described.

2.1. VSFF Circuit Configuration

Scaling fractal-ladder fractor is a classic constant-order fractor circuit [34]. It is employed to achieve the scaling fractal fractional memristor and design the lumped parameter value of the fractor with the port flux or charge [34]. Similarly, the constant-order fractor circuit component parameters must be adjusted based on the required change in the operational order to design a variable-order fractor circuit for solving the problem. Therefore, the design of the VSFF circuit configuration requires only the resistor and capacitor to be replaced in the constant-order scaling fractal-ladder fractor with the variable resistor and capacitor controlled by the microcontroller.

This subsection presents the VSFF circuit configuration and explains the parameters and calculation of the admittance function. Subsequently, the equivalent operation order expression of the VSFF in the characteristic frequency range is calculated to prove that the VSFF possesses characteristics of variable-order fractional calculus operations. Furthermore, it presents a method to optimize the VSFF and improve the approximation performance. Lastly, it explains the correlation between the circuit parameters and operation order.

2.1.1. Circuit Configuration and Admittance

Figure 1 depicts the VSFF circuit configuration. The n-th subcircuit comprises a variable resistor, r_n, in series with a variable capacitor, c_n. k denotes the total number of subcircuits. The serial number, $n = 1, 2, \ldots, k$. $R(C)$, denotes the reference resistance (capacitance). Resistor r_o and capacitor c_o are used for circuit optimization. The n-th subcircuit, r_o, and c_o denote the programmable resistor–capacitor series circuit, programmable resistor, and programmable capacitor emulators, respectively, which are controlled by the microcontroller. $\alpha(\beta)$ denotes the resistance (capacitance) progression ratio. The parameter [15,31],

$$\sigma = \alpha\beta(\alpha \in \mathbb{R}^+, \beta \in \mathbb{R}^+, 0 < \delta \neq 1) \tag{1}$$

represents the scaling factor of the circuit, where α, β, and σ denote the scaling parameters. The scaling parameters are positive real numbers and $\alpha \neq 1$, $\beta \neq 1$. The case in which all the scaling parameters are greater than 1 corresponds to the direct proportion extension VSFF. However, the case in which all the scaling parameters are between 0 and 1 corresponds to the inverse proportion extension VSFF.

The VSFF can realize any real fractional operation in the approximation frequency range. When resistor r_o and capacitor c_o are not considered, the admittance of the VSFF function can be obtained as follows:

$$Y_k(s) = \frac{1}{\tilde{Z}_k(s)} = \sum_{n=1}^{k} \frac{\beta^{n-1}Cs}{1 + \sigma^{n-1}RCs}, \tag{2}$$

s denotes the Laplace or the operational variable, where $\tau = RC$, $w = \tau s$, and $\bar{Y}_k(w) = Y_k(w/\tau)R$. The admittance function is normalized as follows:

$$\bar{Y}_k(w) = \sum_{n=1}^{k} \frac{\beta^{n-1}w}{1 + \sigma^{n-1}w}.$$ (3)

The iterative algorithm formula of the normalized admittance function is expressed as follows:

$$\bar{Y}_k(w) = \frac{w}{1+w} + \frac{\bar{Y}_{k-1}(\sigma w)}{\alpha}.$$ (4)

When $k \to +\infty$, the equation,

$$\bar{y}(w) = \frac{w}{1+w} + \frac{\bar{y}(\sigma w)}{\alpha}$$ (5)

corresponding to the formula of the iterative algorithm, which is the VSFF scaling equation. Equation (5) can be used to analyze the electrical characteristics of the VSFF, including the frequency characteristics and operational order.
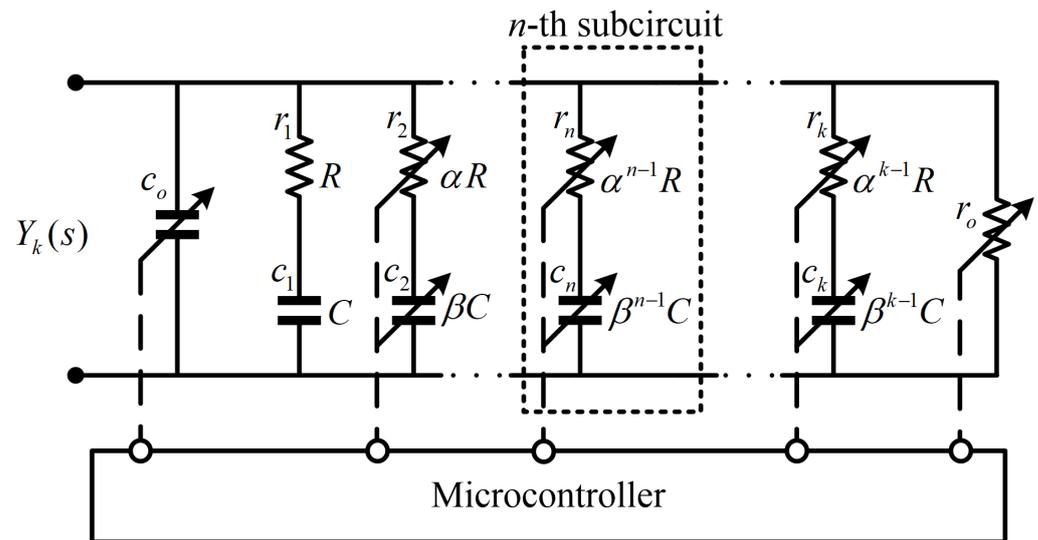

Figure 1. Circuit configuration of VSFF.

2.1.2. Characteristic Frequency and Operational Order

The theoretical expression of the operational order of VSFF in the characteristic frequency range can be calculated. The characteristic frequency of the n-th subcircuit can be expressed as follows:

$$\omega_n = \frac{1}{\alpha^{n-1}\beta^{n-1}} = \sigma^{1-n} (n = 1, 2 \cdots, k).$$ (6)

Therefore, when $1 < \sigma < \infty$ is a direct proportion extension, ω_n is extended to the lower-frequency range. In an inverse proportion extension, $0 < \sigma < 1$, ω_n is extended to the higher-frequency range. When

$$1 < \sigma < +\infty, \quad \omega_k \ll \omega_1 = 1,$$ (7)

at high frequencies ($1 < |\omega| \to \infty$), the circuit exhibits resistive characteristics. At low frequencies ($1 > |\omega| \to 0$), the circuit exhibits capacitive characteristics, that is

$$0 \leftarrow \frac{1-\beta^k}{1-\beta} \cdot w \overset{0 \leftarrow |\omega| < 1}{\longleftarrow} \bar{Y}_k(w) \overset{1 < |\omega| \to \infty}{\longrightarrow} \frac{1-\alpha^{-k}}{1-\alpha^{-1}}.$$ (8)

When the frequency band meets

$$0 \leftarrow \omega_k < |\omega| \ll 1, \tag{9}$$

the resistive and capacitive components interact, and the circuit exhibits fractional calculus operational performance. The operational order can be expressed as follows [34]:

$$\mu \approx -\frac{\lg \alpha}{\lg \sigma} = -\frac{\lg \alpha}{\lg \alpha + \lg \beta}, \tag{10}$$

where μ denotes the operational order. A VSFF can be constructed by adjusting the values of α and β, as shown in (10).

2.1.3. VSFF Optimization

The parallel-connected resistor, r_o, and capacitor, c_o, in the circuit are used to optimize the VSFF to achieve a better variable-order fractional calculus performance. It is assumed that an infinite number of subcircuits exist before the 1-th subcircuit and behind the k-th subcircuit since the total number of subcircuits is limited. When $\alpha, \beta > 1$. The resistance and capacitance decrease progressively with decreasing number of n at each subcircuit before the 1-th circuit. The capacitor of each subcircuit plays a significant role. The capacitor connected in parallel before the 1-th subcircuit is expressed as follows:

$$c_o = \sum_{n=-\infty}^{-1} \beta^n C = \frac{C}{\beta - 1} (\beta > 1). \tag{11}$$

For each subcircuit behind the k-th circuit, both the resistance and capacitance increase with increasing number of n. The resistor of each subcircuit plays a significant role. The resistor connected in parallel behind the k-th subcircuit is expressed as follows:

$$r_o = \frac{1}{\sum_{n=k}^{\infty} 1/(\alpha^n R)} = \frac{(\alpha - 1)R}{\alpha^{1-k}} (\alpha > 1). \tag{12}$$

Similarly, when $0 < \alpha, \beta < 1$, the capacitor connected in parallel before the 1-th subcircuit and the resistor connected in parallel behind the k-th subcircuit are $\frac{\beta^k C}{1-\beta}$ and $\frac{(1-\alpha)R}{\alpha}$, respectively.

Without loss of generality, the VSFF circuit uses a direct proportion extension ($\alpha, \beta > 1$ and $\sigma > 1$) .

2.1.4. Component Parameter Calculation

The parameter values of each component and its variation rule of the circuit configuration can be calculated based on the operational order, μ, and its variable-order range. $\mu_{\min}$ and $\mu_{\max}$ denote the minimum and maximum values of the variable-order range, respectively. The resistance progressive ratio, $\alpha = \sigma^{-\mu}$, and capacitance progressive ratio, $\beta = \frac{\sigma}{\alpha} = \sigma^{\mu+1}$, are calculated based on the variable-order range, $-1 < \mu_{\min} \le \mu \le \mu_{\max} < 0$, and scaling parameter, σ. The n-th variable resistor,

$$r_n = R\alpha^{n-1} = R\sigma^{(1-n)\mu}, \tag{13}$$

and the n-th variable capacitor,

$$c_n = C\beta^{n-1} = C\sigma^{(n-1)(\mu+1)}. \tag{14}$$

The resistor,

$$r_o = \frac{(\alpha - 1)R}{\alpha^{1-k}} = \left(1 - \alpha^{-1}\right)\alpha^k R = (1 - \sigma^\mu)\sigma^{-\mu k} R, \tag{15}$$

and the capacitor,

$$c_o = \frac{C}{\beta - 1} = \frac{C}{\sigma^{\mu+1} - 1}.$$

(16)

The partial derivative of the n-th variable resistor r_n with respect to the operational order μ can be obtained as follows:

$$\frac{\partial r_n}{\partial \mu} = (1 - n) R \sigma^{(1-n)\mu} \ln \sigma.$$

(17)

If $n = 1$, $\frac{\partial r_n}{\partial \mu} = 0$. If $n = 2, 3, \ldots, k$,

$$\frac{\partial r_n}{\partial \mu} < 0.$$

(18)

The resistance of r_n decreases with an increase in μ apart from the fixed value of r_1. The partial derivative of c_n corresponding to μ can be obtained as follows:

$$\frac{\partial c_n}{\partial \mu} = (n - 1) C \sigma^{(n-1)(\mu+1)} \ln \sigma.$$

(19)

If $n = 1$, $\frac{\partial c_1}{\partial \mu} = 0$. If $n = 2, 3, \ldots, k$,

$$\frac{\partial c_n}{\partial \mu} > 0.$$

(20)

Except for the fixed value of c_1, the capacitance of c_n increases with an increase in μ.

2.2. Programmable Resistor–Capacitor Series Circuit Emulator

Figure 1 depicts the n-th subcircuit, which is composed of a variable resistor, r_n, in series with a variable capacitor, c_n. If the variable resistor, r_n, and variable capacitor, c_n, are equivalent when using separate emulators, each emulator must be controlled separately, and the variable capacitor emulator circuit must be operated by floating. The n-th programmable resistor–capacitor series circuit emulator ($n = 2, 3, \ldots, k$) was designed to avoid using more hardware circuits and separately control each emulator. r_n and c_n can be controlled by a single HMDAC, and a separate floating emulator circuit is not required.

This subsection presents the circuit schematic of the programmable resistor–capacitor series circuit emulator and explains the parameters involved. The theory proves that the circuit schematic can achieve the aim of the emulator. The expression of the control variable, $K^{(n)}$, is then theoretically deduced to fulfill the variable-order requirement. Lastly, the expressions of the relative errors of $\tilde{r}_n$ and $\tilde{c}_n$ are derived theoretically.

2.2.1. Circuit Schematic

Figure 2 depicts the circuit schematic of the n-th programmable resistor–capacitor series circuit emulator ($n = 2, 3, \ldots, k$), where $U_1^{(n)}$ represents the HMDAC. The electrical characteristics between ports, $a^{(n)}$ and $b^{(n)}$, are considered as the equivalent electrical characteristics of the n-th subcircuit, as shown in Figure 1. $R_1^{(n)} = R_2^{(n)} = R_3^{(n)} = R_4^{(n)}$, $R_x^{(n)} = R_y^{(n)}$, the operational amplifier, ($A_3^{(n)}$, $A_4^{(n)}$, $A_5^{(n)}$, and $A_6^{(n)}$), and the resistor, ($R_1^{(n)}$, $R_2^{(n)}$, $R_3^{(n)}$, $R_4^{(n)}$, $R_x^{(n)}$, and $R_y^{(n)}$) form the current follower. The current flowing through the capacitor current, $C_x^{(n)}$, is equal to the current flowing through the resistor, $R_x^{(n)}$. If the voltage across the capacitor, $C_x^{(n)}$, is 0 V in $t = 0$, the voltage is obtained as $u_c^{(n)}(t) = \frac{1}{C_x^{(n)}} \int_0^t i_{in}^{(n)}(t) dt$.
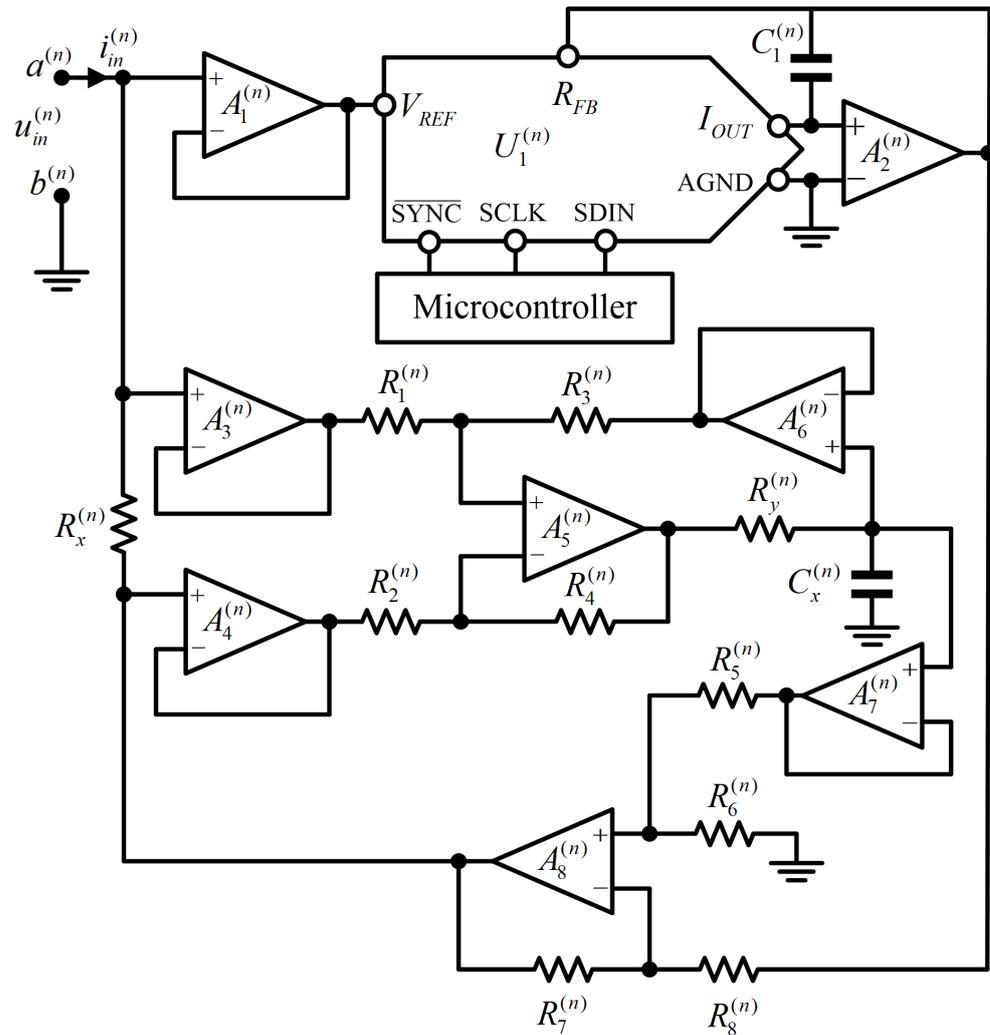
Figure 2. Circuit schematic of the n-th programmable resistor–capacitor series circuit emulator ($n = 2, 3, \ldots, k$).

Most digital-to-analog converters (DACs) operate at a fixed reference voltage, where the output voltage or current corresponds to the product of the reference voltage and the value of a set control variable. The reference voltage of a multiplicative DAC typically varies within the range of ± 10 V. $U_1^{(n)}$ for the output current, $A_2^{(n)}$, and the integrated feedback resistor inside the $U_1^{(n)}$ constitute a precision current-voltage conversion amplifier. The output voltage of $A_2^{(n)}$ is $-K^{(n)} u_{in}^{(n)}(t)$ and the control variables,

$$K^{(n)} = \frac{DATA^{(n)}}{2^m} \left(0 \leq K^{(n)} \leq 1 \right) \tag{21}$$

are controlled by the microcontrollers. $K^{(n)}$ corresponds to the digital quantity, $DATA^{(n)} (0 \leq DATA^{(n)} \leq 2^m)$, provided by the microcontroller. m is expressed as the number of bits of the HMDAC. $R_5^{(n)} = R_6^{(n)} = R_7^{(n)} = R_8^{(n)}$, $A_8^{(n)}$, $R_5^{(n)}$, $R_6^{(n)}$, $R_7^{(n)}$, and $R_8^{(n)}$ constitute a differential amplifier circuit. The output voltage of $A_8^{(n)}$ is

$$u_o^{(n)}(t) = u_c^{(n)}(t) + K^{(n)} u_{in}^{(n)}(t) = u_{in}^{(n)}(t) - i_{in}^{(n)}(t) \cdot R_x^{(n)}. \tag{22}$$

Therefore,

$$u_{in}^{(n)}(t) = i_{in}^{(n)}(t) \cdot \frac{R_x^{(n)}}{1 - K^{(n)}} + \frac{1}{\left(1 - K^{(n)}\right)C_x^{(n)}} \int_0^t i_{in}^{(n)}(t)dt = i_{in}^{(n)}(t) \cdot \tilde{r}_n + \frac{1}{\tilde{c}_n} \int_0^t i_{in}^{(n)}(t)dt. \tag{23}$$

According to (23), the circuit illustrated in Figure 2 is equivalent to the series connection of the programmable resistance,

$$\tilde{r}_n = \frac{R_x^{(n)}}{1 - K^{(n)}}. \tag{24}$$

Furthermore, the programmable capacitance,

$$\tilde{c}_n = \left(1 - K^{(n)}\right)C_x^{(n)}. \tag{25}$$

According to (24) and (25), both $\tilde{r}_n$ and $\tilde{c}_n$ correspond to the control variables, $K^{(n)}$ and $\tilde{r}_n$, and $\tilde{c}_n$ are controlled by the microcontroller.

2.2.2. Calculating the Control Variable of $K^{(n)}$

The equivalent $\tilde{r}_n$ and $\tilde{c}_n$ of Figure 2 can be achieved by adjusting the value of the control variable, $K^{(n)}$, using the microcontroller based on the VSFF, which decreases the number of DACs and presents considerable advantages. According to

$$\frac{\partial \tilde{r}_n}{\partial K^{(n)}} = \frac{R_x^{(n)} K^{(n)}}{\left(1 - K^{(n)}\right)^2} > 0, \frac{\partial \tilde{c}_n}{\partial K^{(n)}} = -C_x^{(n)} < 0, \tag{26}$$

$\tilde{r}_n$ gradually increases and $\tilde{c}_n$ gradually decreases with an increase in $K^{(n)}$. When $K^{(n)} = 0$, the minimum programmable resistance, $\tilde{r}_n$ is $R_x^{(n)}$. According to (13) and (18), when $\tilde{r}_n$ is the minimum value within the change range, μ must be the maximum value, i.e.,

$$\tilde{r}|_{K^{(n)}=0} = R_x^{(n)} = R\sigma^{(1-n)\mu_{\max}} = r_n|_{\mu=\mu_{\max}}. \tag{27}$$

When $K^{(n)} = 0$, the maximum value of $\tilde{c}_n$ is $C_x^{(n)}$. According to (14) and (20), when $\tilde{c}_n$ is the maximum value within the change range, the operational order, μ, must be the maximum value, that is

$$\tilde{c}_n|_{K^{(n)}=0} = C_x^{(n)} = C\sigma^{(n-1)(\mu_{\max}+1)} = c_n|_{\mu=\mu_{\max}}. \tag{28}$$

Equation (27) is substituted into (24) to obtain

$$\tilde{r}_n = \frac{R}{1 - K^{(n)}} \sigma^{(1-n)\mu_{\max}}. \tag{29}$$

Equation (28) is substituted into (25) to obtain

$$\tilde{c}_n = \left(1 - K^{(n)}\right)C\sigma^{(n-1)(\mu_{\max}+1)}. \tag{30}$$

When $\tilde{r}_n = r_n$,

$$R\sigma^{(1-n)\mu} = \frac{R}{1 - K^{(n)}}\sigma^{(1-n)\mu_{\max}} \tag{31}$$

can be obtained from (13) and (29). When $\tilde{c}_n = c_n$,

$$C\sigma^{(n-1)(\mu+1)} = \left(1 - K^{(n)}\right)C\sigma^{(n-1)(\mu_{\max}+1)} \tag{32}$$

can be obtained from (14) and (30). Remarkably, (31) and (32) produce the same result:

$$K^{(n)} = 1 - \sigma^{(n-1)(\mu - \mu_{max})}. \tag{33}$$

Only one control variable, $K^{(n)}$, is required to satisfy the change in the resistance, r_n, and capacitance, c_n, of the n-th subcircuit in the VSFF, as shown in (33). When compared to the programmable resistance and capacitance circuits, which require HMDAC control, the number of HMDAC is halved, the circuit is simpler, and the I/O port resources of the microcontroller are reduced.

2.2.3. Calculating the Relative Errors of $\tilde{r}_n$ and $\tilde{c}_n$

Figure 2 depicts the relative errors of $\tilde{r}_n$ and $\tilde{c}_n$ of the circuit, which correspond to μ_{min}, μ_{max}, n, and m. According to (24), the correlation between the relative error, $\delta^{(\tilde{r}_n)}$, of $\tilde{r}_n$ and the resolution, $\Delta K^{(n)} = \frac{1}{2^m}$, of the HMDAC is expressed as:

$$\delta^{(r_n)} = \frac{\Delta \tilde{r}_n}{\tilde{r}_n} = \frac{\partial \tilde{r}_n \Delta K^{(n)}}{\tilde{r}_n \partial K^{(n)}} = \frac{1}{2^m \left(1 - K^{(n)}\right)}. \tag{34}$$

According to (25), the correlation between the relative error, $\delta^{(\tilde{c}_n)}$, of $\tilde{c}_n$ and $\Delta K^{(n)} = \frac{1}{2^m}$ is expressed as:

$$\delta^{(\tilde{c}_n)} = \frac{\Delta \tilde{c}_n}{\tilde{c}_n} = \frac{\partial \tilde{c}_n \Delta K^{(n)}}{\tilde{c}_n \partial K^{(n)}} = \frac{-1}{2^m \left(1 - K^{(n)}\right)}. \tag{35}$$

According to (33)–(35), when $\mu = \mu_{max}$, $K^{(n)} = 0$, $\tilde{r}_n$, and $\tilde{c}_n$ are the minimum relative errors within the change range:

$$\delta_{min}^{(\tilde{r}_n)}\Big|_{\mu = \mu_{max}} = \mid \delta_{min}^{(\tilde{c}_n)} \mid\mid_{\mu = \mu_{max}} = \frac{1}{2^m}. \tag{36}$$

When $\mu = \mu_{min}$, $K^{(n)}$ is the maximum value within the change range, and $\tilde{r}_n$ and $\tilde{c}_n$ can be used to obtain the maximum relative error within the change range:

$$\delta_{max}^{(\tilde{r}_n)}\Big|_{\mu = \mu_{min}} = \mid \delta_{max}^{(\tilde{c}_n)} \mid\mid_{\mu = \mu_{min}} = \frac{\sigma^{(n-1)(\mu_{max} - \mu_{min})}}{2^m}. \tag{37}$$

The maximum relative error of the programmable resistor–capacitor series circuit emulator corresponds to the ranges of μ, n, and m. The larger the range of μ, the larger the maximum relative error of the equivalent programmable parameter. The larger the serial number, n, the larger the maximum relative error of the equivalent programmable parameter. The larger the number of bits, m, the smaller the resolution, $\Delta K^{(n)}$, and the maximum relative error of the equivalent programmable parameters.

2.3. Programmable Universal Electronic Component Emulator–Programmable Resistor and Capacitor for Circuit Optimization

Figure 1 illustrates the programmable resistor, r_o, and programmable capacitor, c_o. Fewer schematics are used to simplify the overall circuit schematic. A programmable universal electronic component emulator was also designed.

This subsection presents a circuit schematic of the programmable universal electronic component emulator and explains the parameters involved. The theory proves that the circuit schematic can achieve the aim of the emulator. Subsequently, the expressions of the control variables, $K^{(r_o)}$ and $K^{(c_o)}$, are deduced theoretically to fulfill the variable-order requirement. Lastly, the expressions of the relative errors of $\tilde{r}_o$ and $\tilde{c}_o$ are derived theoretically.

2.3.1. Circuit Schematic

Figure 3 depicts the circuit schematic of the programmable universal electronic component emulator. $U_1^{(x_o)}$ represents the HMDAC. If $x_o = r_o$ and $X^{(x_o)}$ represent the resistance, $R_x^{(r_o)}$, the electrical characteristics between ports $a^{(r_o)}$ and $b^{(r_o)}$ are considered to be equivalent to the electrical characteristics of the resistor, r_o, as shown in Figure 1. If $x_o = c_o$ and $X^{(x_o)}$ represent the capacitance, $C_x^{(c_o)}$, the electrical characteristics between the ports, $a^{(c_o)}$ and $b^{(c_o)}$, are used as the equivalent electrical characteristics of capacitor, c_o, as shown in Figure 1. The operational amplifier, $A_1^{(x_o)}$, constitutes the voltage follower. The operational amplifiers, $A_3^{(x_o)}$, and resistors, ($R_1^{(x_o)}$ and $R_2^{(x_o)}$), constitute the inverse proportional amplifiers. When $R_1^{(x_o)} = R_2^{(x_o)}$ and $A_3^{(x_o)}$, the output voltage is $K^{(x_o)}u_{in}^{(x_o)}$. For port, $a^{(x_o)}$, the input current is expressed as

$$I_{in}^{(x_o)}(s) = \frac{U_{in}^{(x_o)}(s) - K^{(x_o)}U_{in}^{(x_o)}(s)}{X^{(x_o)}(s)}, \tag{38}$$

that is

$$\frac{U_{in}^{(x_o)}(s)}{I_{in}^{(x_o)}(s)} = \frac{X^{(x_o)}(s)}{1 - K^{(x_o)}}, \tag{39}$$

where s denotes the complex frequency variable. According to (39), the equivalent component parameter value of the circuit shown in Figure 3 can be adjusted by adjusting the control variables, $K^{(x_o)}$, using the microcontroller. If $x_o = r_o$ and $X^{(x_o)} = R_x^{(r_o)}$, the equivalent programmable optimized resistance is expressed as

$$\tilde{r}_o = \frac{R_x^{(r_o)}}{1 - K^{(r_o)}}, \tag{40}$$

where $\tilde{r}_o$ corresponds to the control variable, $K^{(r_o)}$, and is controlled by the microcontroller. If $x_o = c_o$ and $X^{(x_o)} = C_x^{(c_o)}$, the equivalent programmable optimized capacitance is expressed as:

$$\tilde{c}_o = \left(1 - K^{(c_o)}\right) \cdot C_x^{(c_o)}, \tag{41}$$

where $\tilde{c}_o$ corresponds to the control variable, $K^{(c_o)}$, and is controlled by the microcontroller. If $X^{(x_o)}$ represents circuit parameters other than the resistance and capacitance, such as the inductance, fractance, and transtance [38], the circuit shown in Figure 3 can also be used to realize a programmable circuit with more component parameter values, thereby improving its applicability.
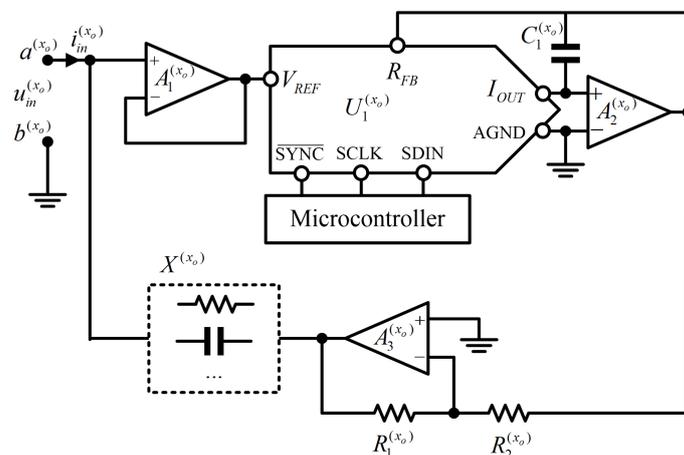

Figure 3. Circuit schematic of the programmable universal electronic component emulator.

2.3.2. Calculating the Control Variables of $K^{(r_o)}$ and $K^{(c_o)}$

The equivalent programmable optimized resistance, $\tilde{r}_o$, or the programmable optimized capacitance, $\tilde{c}_o$, shown in Figure 3 can be realized through a microcontroller by adjusting $K^{(r_o)}$ or $K^{(c_o)}$. The partial derivative of $\tilde{r}_o$ corresponding to $K^{(r_o)}$ can be obtained as $\frac{\partial \tilde{r}_o}{\partial K^{(r_o)}} = \frac{-R_x^{(r_o)}}{\left(1-K^{(r_o)}\right)^2} < 0$. This indicates that, with an increase in $K^{(r_o)}$, $\tilde{r}_o$ decreases progressively. The partial derivative of r_o, shown in (15), to μ can be obtained as $\frac{\partial r_o}{\partial \mu} > 0$. This indicates that r_o increases with an increase in μ. When $K^{(r_o)} = 0$ is used, the maximum $\tilde{r}_o$ obtained is r_o when $\mu = \mu_{\max}$. That is,

$$\tilde{r}_o|_{K^{(r_o)}=0} = R_x^{(r_o)} = (1 - \sigma^{\mu_{\max}})\sigma^{-\mu_{\max}k}R = r_o|_{\mu=\mu_{\max}}. \tag{42}$$

Assuming $\tilde{r}_o = r_o$ can be obtained from (15), (40) and (42),

$$K^{(r_o)} = 1 - \frac{(1 - \sigma^{\mu_{\max}})\sigma^{(\mu-\mu_{\max})k}}{1 - \sigma^\mu}. \tag{43}$$

The partial derivative of $\tilde{c}_o$ corresponding to $K^{(c_o)}$ is obtained as follows:

$$\frac{\partial \tilde{c}_o}{\partial K^{(c_o)}} = -C_x^{(c_o)} < 0. \tag{44}$$

$\tilde{c}_o$ decreases with the increase in $K^{(c_o)}$. The partial derivative of c_o of (16) corresponding to μ can be obtained as

$$\frac{\partial c_o}{\partial \mu} = \frac{-C\sigma^{\mu+1}\lg\sigma}{\left(\sigma^{\mu+1} - 1\right)^2} < 0, \tag{45}$$

where c_o decreases with an increase in μ. When $K^{(c_o)} = 0$ is set, the maximum $\tilde{c}_o$ is c_o in $\mu = \mu_{\min}$. That is,

$$\tilde{c}_o|_{K^{(c_o)}=0} = C_x^{(c_o)} = \frac{C}{\sigma^{\mu_{\min}+1} - 1} = c_o|_{\mu=\mu_{\min}}. \tag{46}$$

$\tilde{c}_o = c_o$ can be obtained from (16), (41) and (46) as follows:

$$K^{(c_o)} = 1 - \frac{\sigma^{\mu_{\min}+1} - 1}{\sigma^{\mu+1} - 1}. \tag{47}$$

2.3.3. Calculating the Relative Errors of $\tilde{r}_o$ and $\tilde{c}_o$

When realizing the VSFF, the relative error of the equivalent element parameter values in Figure 3 corresponds to $\mu_{\min}$, $\mu_{\max}$, n, and m. The correlation between the relative error, δ_{r_o}, of $\tilde{r}_o$ and $\Delta K^{(r_o)} = \frac{1}{2^m}$ is expressed as follows:

$$\delta^{(\tilde{r}_o)} = \frac{\Delta \tilde{r}_o}{\tilde{r}_o} = \frac{1}{\tilde{r}_o}\frac{\partial \tilde{r}_o}{\partial K^{(r_o)}}\Delta K^{(r_o)} = \frac{1}{2^m\left(1 - K^{(r_o)}\right)}. \tag{48}$$

According to (43), $K^{(r_o)} = 0$ can be obtained when $\mu = \mu_{\max}$ and the minimum relative error of $\tilde{r}_o$ within the change range is expressed as follows:

$$\delta_{\min}^{(\tilde{r}_o)}\Big|_{\mu=\mu_{\max}} = \frac{1}{2^m}, \tag{49}$$

when $\mu = \mu_{\min}$, $K^{(r_o)}$ is the maximum value within the change range, and the maximum relative error can be obtained from (43) and (48) as follows:

$$\delta_{\max}^{(\tilde{r}_o)}\Big|_{\mu=\mu_{\min}} = \frac{1 - \sigma^{\mu_{\min}}}{2^m(1 - \sigma^{\mu_{\max}})\sigma^{(\mu_{\min}-\mu_{\max})k}}. \tag{50}$$

The correlation between the relative error of $\tilde{c}_o$ and $\Delta K^{(c_o)} = \frac{1}{2^m}$ can be given as

$$\delta^{(\tilde{c}_o)} = \frac{\Delta \tilde{c}_o}{\tilde{c}_o} = \frac{\Delta K^{(c_o)} \partial \tilde{c}_o}{\tilde{c}_o \partial K^{(c_o)}} = \frac{1}{2^m \left(K^{(c_o)} - 1 \right)}. \tag{51}$$

According to (47), when the operation, $\mu = \mu_{\min}$, the control variable $K^{(c_o)} = 0$, and $\tilde{c}_o$ is the minimum relative error within the change range,

$$\delta^{(\tilde{c}_o)}_{\min}\Big|_{\mu=\mu_{\min}} = -\frac{1}{2^m}. \tag{52}$$

When $\mu = \mu_{\max}$, $K^{(c_o)}$ is the maximum value within the change range and the maximum relative error of $\tilde{c}_o$ is obtained. That is,

$$\delta^{(\tilde{c}_o)}_{\max}\Big|_{\mu=\mu_{\max}} = \frac{1 - \sigma^{\mu_{\max}+1}}{2^m \left(\sigma^{\mu_{\min}+1} - 1 \right)}. \tag{53}$$

3. Experimental Results

This section presents the results of the experiments and the verification of the VSFF circuit. Firstly, the model and component parameters in the VSFF are provided, and the relative error of the programmable circuit is calculated. Subsequently, the approximation performance and variable-order characteristics of the VSFF are analyzed in the frequency domain. Furthermore, two equivalent methods to calculate the variable-order electrical characteristics are presented. One of these characteristics is derived from circuit theory and is presented herein. Lastly, the VSFF is implemented and the variable-order characteristic of the circuit is experimentally validated.

3.1. Circuit Implementation

This subsection presents the parameters, models, and instruments used for circuit implementation. Firstly, the values of the component parameters are presented and the model selection of the microcontroller and the HMDAC are introduced. Subsequently, a list of circuit parameters is presented, which includes the control variables of the microcontroller, equivalent parameters of the emulators, and equivalent parameter relative errors of the emulators. The influence of the different parameters is also demonstrated. Lastly, some details that were considered in the implementation of the circuit are presented.

This circuit realizes the VSFF by replacing the n-th subcircuit shown in Figure 1 with the emulator shown in Figure 2 ($n = 2, 3, \cdots k$), and by replacing the resistance, r_o, ($x_o = r_o$, $X^{(x_o)} = R_x^{(r_o)}$) and capacitance, c_o, ($x_o = c_o$, $X^{(x_o)} = C_x^{(c_o)}$) of the emulator shown in Figure 3. It was assumed that $k = 5$, $n = 2, 3, 4, 5$, $R = 330\ \Omega$, $C = 0.1\ \mu\text{F}$, $\sigma = 5$, and $\mu_{\min} = -0.7 \le \mu \le -0.3 = \mu_{\max}$. The operational amplifiers, $A_2^{(2)}$, $A_2^{(3)}$, $A_2^{(4)}$, $A_2^{(5)}$, $A_2^{(c_o)}$, and $A_2^{(r_o)}$, used OP97 and all the other operational amplifiers used OP07.

The HMDAC used AD5544 [39], $m = 16$ bits, and a resolution of $\Delta K = \frac{1}{2^m} = \frac{1}{65,536}$. Each AD5544 comprised four current output DACs, with each DAC containing an independent multiplying reference input. A load strobe enabled 4-channel, simultaneous updates for hardware-synchronized output voltage changes. Two AD5544 units were used for the implementation of the circuit.

STC8A8K64S4A12 was selected as the microcontroller, as shown in Figure 1. This microcontroller did not require an external crystal oscillator and external reset circuit for an internal clock source frequency of up to 24 MHz. According to (33), (43), (47), and the variable order μ, the control variables, $K^{(n)}$, $K^{(r_o)}$, and $K^{(c_o)}$ of AD5544 were set by the STC8A8K64S4A12 to realize the change in the operational order of the VSFF.

Table 1 lists the parameters of the circuit. $R_x^{(n)}$, $C_x^{(n)}$, $\tilde{r}_n$, $\tilde{c}_n$, $K^{(n)}$, $\delta^{(\tilde{x}_n)}_{\min}(\tilde{x}_n = \tilde{c}_n, \tilde{r}_n)$, and $\delta^{(\tilde{r}_n)}_{\max}(\tilde{x}_n = \tilde{c}_n, \tilde{r}_n)$ were calculated from (27)–(29), (30), (33), (36) and (37), respectively.

Following the circuit implementation, $R_x^{(n)}$ and $C_x^{(n)}$ took fixed values. $K^{(n)}$ was controlled by the microcontroller, and by varying this value, the microcontroller adjusted $\tilde{r}_n$ and $\tilde{c}_n$, thereby achieving variable order. $\delta_{\min}^{(\tilde{x}_n)}$ and $\delta_{\max}^{(\tilde{r}_n)}$ were the minimum and maximum relative errors of $\tilde{r}_n$ and $\tilde{c}_n$ within the range of variation. $\tilde{r}_o$, $R_x^{(r_o)}$, $K^{(r_o)}$, $\delta_{\min}^{(\tilde{r}_o)}$, and $\delta_{\max}^{(\tilde{r}_o)}$ were calculated from (40), (42), (43), (49) and (50), respectively. Following the circuit implementation, $R_x^{(r_o)}$ took fixed values. $K^{(r_o)}$ was controlled by a microcontroller, and by varying this value, the microcontroller changed $\tilde{r}_o$, thereby achieving variable order. $\delta_{\min}^{(\tilde{r}_o)}$ and $\delta_{\max}^{(\tilde{r}_o)}$ were the minimum and maximum relative errors of $\tilde{r}_o$ within the range of variation. $\tilde{c}_o$, $C_x^{(c_o)}$, $K^{(c_o)}$, $\delta_{\min}^{(\tilde{c}_o)}$, and $\delta_{\max}^{(\tilde{c}_o)}$ were calculated from (41), (46), (47), (52) and (53), respectively. Following the circuit implementation, $C_x^{(c_o)}$ took fixed values. $K^{(c_o)}$ was controlled by a microcontroller and by varying this value, the microcontroller changed $\tilde{c}_o$, thereby achieving variable order. $\delta_{\min}^{(\tilde{c}_o)}$ and $\delta_{\max}^{(\tilde{c}_o)}$ were the minimum and maximum relative errors of $\tilde{c}_o$ within the range of variation. For the capacitance, $C_1^{(2)} = C_1^{(3)} = C_1^{(4)} = C_1^{(5)} = C_1^{(r_o)} = C_1^{(c_o)} = 1.8$ pF, the resistances not marked in Table 1 were assumed to be 16 kΩ.

Table 1. Circuit parameter list.

	$-0.7 \leq \mu \leq -0.3, k = 5, \sigma = 5$	
r_o, c_o	$62.3 \text{ k}\Omega \geq \tilde{r}_o \geq 1.41 \text{ k}\Omega,$ $6.732 \times 10^{-4} \geq \delta^{(\tilde{r}_o)} \geq \frac{1}{65,536}$	$161 \text{ nF} \geq \tilde{c}_o \geq 48.0 \text{ nF},$ $\frac{1}{65,536} \leq \delta^{(\tilde{c}_o)} \leq 5.126 \times 10^{-5}$
	$R_x^{(r_o)} = 1.41 \text{ k}\Omega$	$C_x^{(c_o)} = 161 \text{ nF}$
	$0.9773 \geq K^{(r_o)} \geq 0$	$0 \leq K^{(c_o)} \leq 0.7023$
1-st subcircuit	$R = 330 \Omega$	$C = 0.1 \text{ }\mu\text{F}$
2-nd subcircuit	$1.02 \text{ k}\Omega \geq \tilde{r}_2 \geq 535 \Omega,$ $2.905 \times 10^{-5} \geq \delta^{(\tilde{r}_2)} \geq \frac{1}{65,536}$	$162 \text{ nF} \leq \tilde{c}_2 \leq 309 \text{ nF},$ $2.905 \times 10^{-5} \geq \delta^{(\tilde{c}_2)} \geq \frac{1}{65,536}$
	$R_x^{(2)} = 535 \Omega, C_x^{(2)} = 309 \text{ nF}$	
	$0.4747 \geq K^{(2)} \geq 0$	
3-rd subcircuit	$3.14 \text{ k}\Omega \geq \tilde{r}_3 \geq 867 \Omega,$ $5.530 \times 10^{-5} \geq \delta^{(\tilde{r}_3)} \geq \frac{1}{65,536}$	$263 \text{ nF} \leq \tilde{c}_3 \leq 952 \text{ nF},$ $5.530 \times 10^{-5} \geq \delta^{(\tilde{c}_3)} \geq \frac{1}{65,536}$
	$R_x^{(3)} = 867 \Omega, C_x^{(3)} = 952 \text{ nF}$	
	$0.7241 \geq K^{(3)} \geq 0$	
4-th subcircuit	$9.69 \text{ k}\Omega \geq \tilde{r}_4 \geq 1.40 \text{ k}\Omega,$ $1.053 \times 10^{-4} \geq \delta^{(\tilde{r}_4)} \geq \frac{1}{65,536}$	$426 \text{ nF} \leq \tilde{c}_4 \leq 2.94 \text{ }\mu\text{F},$ $1.053 \times 10^{-4} \geq \delta^{(\tilde{c}_4)} \geq \frac{1}{65,536}$
	$R_x^{(4)} = 1.40 \text{ k}\Omega, C_x^{(4)} = 2.94 \text{ }\mu\text{F}$	
	$0.8550 \geq K^{(4)} \geq 0$	
5-th subcircuit	$29.9 \text{ k}\Omega \geq \tilde{r}_5 \geq 2.28 \text{ k}\Omega,$ $2.004 \times 10^{-4} \geq \delta^{(\tilde{r}_5)} \geq \frac{1}{65,536}$	$690 \text{ nF} \leq \tilde{c}_5 \leq 9.06 \text{ }\mu\text{F},$ $2.004 \times 10^{-4} \geq \delta^{(\tilde{c}_5)} \geq \frac{1}{65,536}$
	$R_x^{(5)} = 2.28 \text{ k}\Omega, C_x^{(5)} = 9.06 \text{ }\mu\text{F}$	
	$0.9239 \geq K^{(5)} \geq 0$	

As shown in Table 1, $K^{(n)}$, $K^{(r_o)}$, and $K^{(c_o)}$ were within the range of achievable changes ($0 \sim 1$). The equivalent minimum relative error $\delta_{\min}^{(\hat{x}_n)} = \frac{1}{65,536} (\hat{x}_n = \tilde{c}_n, \tilde{r}_n, c_o, r_o)$ and maximum relative error $\delta_{\max}^{(\hat{x}_n)} = 6.732 \times 10^{-4}$ of the emulator met the requirements of Figure 1. If $R_x^{(n)}$ and $R_x^{(r_o)}$ were not nominal values, they were obtained in series by using the nominal resistors. If $C_x^{(n)}$ and $C_x^{(c_o)}$ were not nominal values, they were obtained in parallel by using the nominal capacitance. Figures 2 and 3 illustrate the resistors and capacitors of the

circuit, which were packaged with 0805. The rated power of the resistance was 0.125 W and the rated voltage of the capacitor was 50 V. During production, it was assumed that the power rating of the resistor did not exceed the rated power value, the capacitor voltage was less than the voltage withstand value, and that the power supply voltage, input and output voltages, and input and output currents of all the chips in the circuit were within the standard range.

3.2. Frequency Characteristic Analysis

This subsection presents the frequency domain analysis of the approximation performance and variable-order characteristics of the VSFF. The amplitude-frequency characteristic, phase-frequency characteristic, order-frequency characteristic, and F-frequency characteristic function are introduced, and the theoretical and experimental frequency domain characteristic analysis curve of the VSFF is obtained. Subsequently, the frequency domain characteristic curve is analyzed, and the range of the approximation frequency is obtained when the VSFF changes to a different operation order. Lastly, the correlation between the lumped parameter value and the operation order was solved.

The approximation performance and variable-order characteristics of the VSFF were analyzed by using the frequency characteristics. The impedance function of the VSFF was $\tilde{Z}_k(s)$ when the operational order changed to μ and the impedance $\tilde{I}^{(\mu)}(s) = F^{(\mu)}s^\mu$ was then approximated. The complex frequency variable, s, was replaced by the exponential frequency variable, ϖ [31]. That is:

$$s = \mathrm{j}2\pi f = \mathrm{j}2\pi 10^\varpi. \tag{54}$$

The amplitude-frequency characteristic functions are:

$$\Lambda_k(\varpi) = \lg\left|\tilde{Z}_k(\mathrm{j}2\pi 10^\varpi)\right| \leftrightarrow \Lambda^{(\mu)}(\varpi) = \lg\left|\tilde{I}^{(\mu)}(\mathrm{j}2\pi 10^\varpi)\right|. \tag{55}$$

The phase-frequency characteristic function is:

$$\theta_k(\varpi) = \arg\left\{\tilde{Z}_k(j2\pi 10^\varpi)\right\} \leftrightarrow \theta^{(\mu)}(\varpi) = \frac{\pi}{2}\mu. \tag{56}$$

The order-frequency characteristic function [20] is:

$$O_k(\varpi) = \frac{\mathrm{d}\Lambda_k(\varpi)}{\mathrm{d}\varpi} \leftrightarrow O^{(\mu)}(\varpi) = \frac{\mathrm{d}\Lambda^{(\mu)}(\varpi)}{\mathrm{d}\varpi} = \mu. \tag{57}$$

The F-frequency characteristic function [40] is:

$$\Gamma_k(\varpi) = \Lambda_k(\varpi) - O_k(\varpi)[\varpi + \lg(2\pi)] \leftrightarrow \Gamma^{(\mu)}(\varpi) = \lg F^{(\mu)}. \tag{58}$$

These functions were used for comparative analysis. $\Lambda_k(\varpi)$, $\theta_k(\varpi)$, $O_k(\varpi)$, and $\Gamma_k(\varpi)$ represent the frequency characteristic functions of $\tilde{Z}_k(s)$. $\Lambda^{(\mu)}(\varpi)$, $\theta^{(\mu)}(\varpi)$, $O^{(\mu)}(\varpi)$, and $\Gamma^{(\mu)}$ represent the frequency characteristic functions of $\tilde{I}^{(\mu)}(s)$. For the circuit configuration shown in Figure 1 and in the case of the parameter values shown in Table 1, when $\mu = -0.7, -0.6, \ldots, -0.3$, respectively. $r_n(n = 2,3,4,5)$, c_n, r_o, and c_o were calculated from (13), (14)–(16), respectively. These parameters are substituted into (2). Based on (55)–(58), the theoretical characteristic function curve in the frequency domain was determined, as shown in Figure 4. Figure 4 also shows the simulation experiment results obtained by Multisim 14.
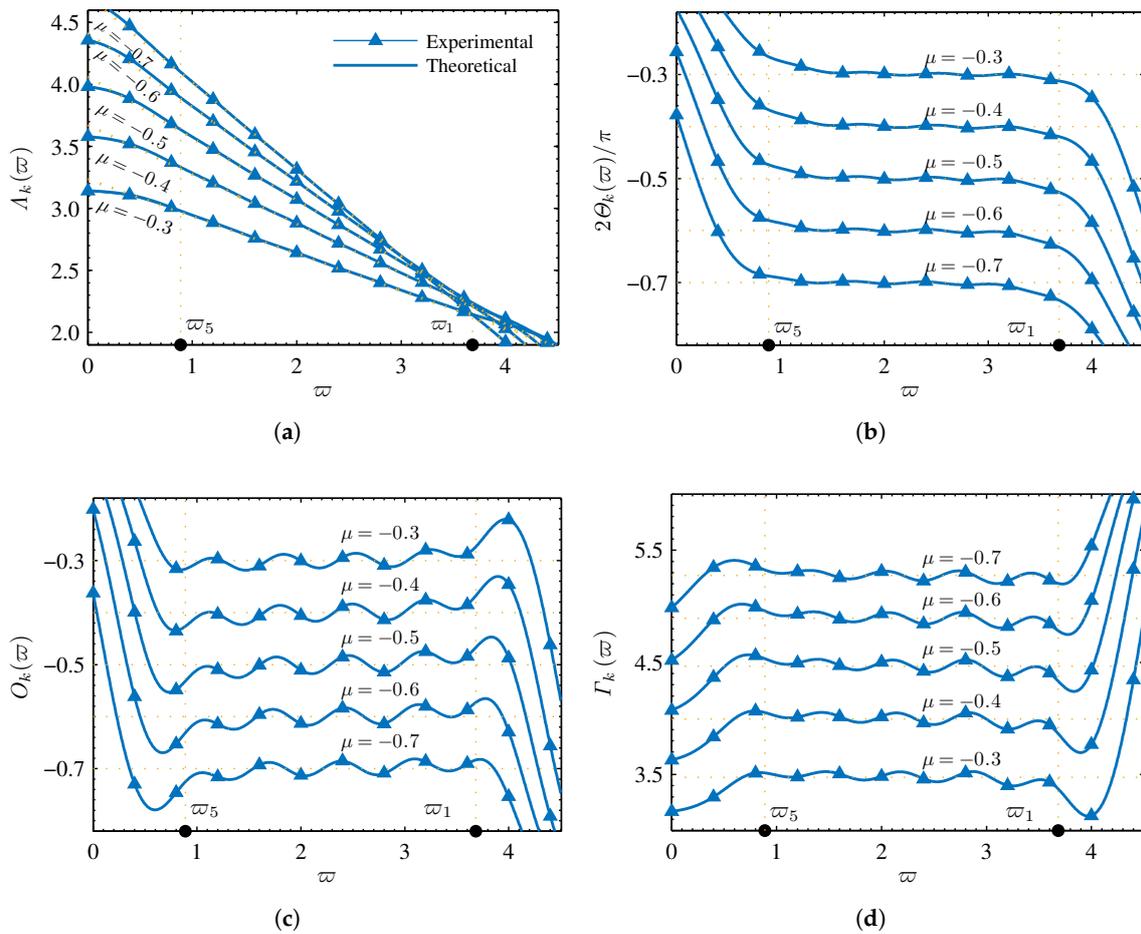
Figure 4. Frequency characteristic curves of VSFF: $k = 5$, $\sigma = 5$, R =330 Ω, and $C = 0.1$ μF: (**a**) amplitude-frequency characteristic; (**b**) phase-frequency characteristic; (**c**) order-frequency characteristic; (**d**) F-frequency characteristic.

The amplitude-frequency and phase-frequency characteristic function curves, shown in Figure 4a,b, describe the gain and phase characteristics between the voltage and current of the VSFF in the frequency domain, respectively. It can be observed from the amplitude–frequency function curve that the amplitude–frequency characteristic values decreased with increasing frequency. The smaller the operational order, the higher the rate of reduction in the amplitude–frequency characteristic values with increasing frequency. In the low-frequency range, the amplitude—frequency characteristic values decreased with increasing operational order. The phase-frequency and order-frequency characteristic curves, shown in Figure 4b,c, respectively, constitute the mathematical basis to analyze the operational performance (such as the operational order, constant phase, and approximation performance) of the VSFF.

In the case of a fixed operational order, the phase was a fixed value in the approximation frequency range ($10^{\varpi_1} \sim 10^{\varpi_5}$). When the frequency was less than 10^{ϖ_1}, the phase increased with decreasing frequency. When the frequency was greater than 10^{ϖ_5}, the phase decreased with increasing frequency. In the case of a fixed frequency, the phase decreased with decreasing operational order. The order-frequency characteristic function represents the operational order of the VSFF from the frequency domain. It can be observed from the order–frequency function curve that the operational order was a fairly constant value in the approximation frequency range ($10^{\varpi_1} \sim 10^{\varpi_5}$). When the frequency was less than 10^{ϖ_1}, the operational order increased with decreasing frequency. When the frequency was greater than 10^{ϖ_5}, the operational order decreased with increasing frequency. In the case

of a fixed frequency, the operational order decreased with decreasing operational order. The F-frequency characteristic function curve, shown in Figure 4d, represents the lumped parameter value of the VSFF in the frequency domain.

It can be observed from F-frequency function curve that the lumped parameter value was a fairly constant value in the approximation frequency range ($10^{\varpi_1} \sim 10^{\varpi_5}$). When the frequency was less than 10^{ϖ_1}, the lumped parameter value decreased with the decrease in the frequency. When the frequency was greater than 10^{ϖ_5}, the lumped parameter value increased with the increase in frequency. In the case of a fixed frequency, the lumped parameter value increased with the decrease in the operational order. The order-frequency and F-frequency characteristic functions visually represent the degree of operational order and the lumped parameter value of the VSFF approximation of the ideal fractor element. It can be observed from the order-frequency and F-frequency characteristic curves, that the VSFF realized the fractional and variable operation orders within a certain frequency range. The highest frequency index value [31],

$$\varpi_1 = \lg[1/(2\pi RC)], \tag{59}$$

and the lowest frequency index value [31],

$$\varpi_k = \varpi_1 - (k-1)\lg\sigma, k = 5, \tag{60}$$

were used to realize fractional-order operation.

Therefore, the operating frequency range of the VSFF of the parameters shown in Table 1 was obtained as ($10^{\varpi_1} \sim 10^{\varpi_5}$), i.e., (7.72 Hz$\sim$4.82 kHz). The lumped parameter value, $F^{(\mu)}$, was solved within the operating frequency range, as observed from the F-frequency characteristic curve. The correlation between the lumped parameter value, $F^{(\mu)}$, and μ was solved by using the least square method to fit the data and to obtain the following equation:

$$\Gamma^{(\mu)}(\mu) = \lg F^{(\mu)}(\mu) = -2.2444\mu^2 - 6.7431\mu + 1.6545. \tag{61}$$

The relative error of $\Gamma^{(\mu)}(\mu)$ calculated by (61) within the variation range of μ, was less than 0.05%.

3.3. Two Equivalent Methods for Calculating Variable-Order Electrical Characteristics

This subsection presents two equivalent methods to calculate the variable-order electrical characteristics to obtain the time-domain theoretical electrical characteristics of the VSFF. One of these methods is derived from circuit theory and is presented in this study. The other variable-order electrical characteristic calculation method is obtained through the Grünwald-Letnikov variable-order fractional calculus.

3.3.1. Variable-Order Electrical Characteristics Obtained through Circuit Theory

For the input voltage signal, $u(t)$, to the VSFF, the current flowing through the VSFF according to Kirchhoff's current and voltage laws can be represented as follows:

$$i(t) = \frac{C}{\beta-1}\frac{\mathrm{d}u(t)}{\mathrm{d}t} + \frac{\alpha^{1-k}u(t)}{(\alpha-1)R} + \sum_{n=1}^{k}\frac{u(t) - u_n(t)}{\alpha^{n-1}R}, \tag{62}$$

where $u_n(t)$ denotes the voltage across the capacitor, $c_n(n = 1, 2, \ldots, k)$, and is described by

$$\beta^{n-1}C\frac{\mathrm{d}u_n(t)}{\mathrm{d}t} = \frac{u(t) - u_n(t)}{\alpha^{n-1}R}, (n = 1, 2, \cdots, k). \tag{63}$$

The correlation between α and β in Equations (62) and (63) and the operation order can be obtained from Equation (10). Therefore, the variable-order electrical characteristics of the VSFF can be obtained based on (10), (62) and (63).

3.3.2. Variable-Order Electrical Characteristics Obtained through the
Grünwald–Letnikov Definition

The input voltage signal, $u(t)$, to the VSFF and the main spectral range of $u(t)$ was within the approximate frequency range of the VSFF. The input current obtained is expressed as follows [13]:

$$i(t) \approx \frac{1}{F(\mu(t))} t_o D_t^{-\mu(t)} u(t), \tag{64}$$

where t_0 is the initial time.

Grünwald-Letnikov variable-order fractional calculus was used to define the computation completion (64). It has at least three widely used definitions [15–17]. These definitions are based on replacing the constant operational order, μ, with variable operational order, $\mu(t)$. The coefficients are then obtained based on different sampling methods. If the coefficient is sampled from the order value at the corresponding time of the coefficient, then [15–17]:

$$i(t) = \frac{1}{F(\mu(t))} \lim_{h \to 0} \sum_{j=0}^{(t-t_0)/h} \frac{(-1)^j}{h^{-\mu(t-jh)}} \binom{-\mu(t-jh)}{j} u(t-jh), \tag{65}$$

where $t < t_0$, $u_{in}(t) \equiv 0$, and $\binom{-\mu(t-jh)}{j}$ are binomial coefficients. To complete the numerical calculation of (65), the step size, h, must be sufficiently small; therefore:

$$i(t) \approx \frac{1}{F(\mu(t))} \sum_{j=0}^{(t-t_0)/h} \frac{\psi_j^{(-\mu(t-jh))}}{h^{-\mu(t-jh)}} u(t-jh), \tag{66}$$

where $\psi_j^{(-\mu(t-jh))} = (-1)^j \binom{-\mu(t-jh)}{j}$ represents the polynomial coefficient of the function, $(1-z)^{-\mu(t-jh)}$, which can be directly calculated by using the following recursive formula:

$$\psi_0^{(-\mu(t))} = 1, \quad \psi_j^{(-\mu(t-jh))} = \left(1 - \frac{1-\mu(t-jh)}{j}\right) \psi_{j-1}^{(-\mu(t-jh))}, \quad j = 1, 2, \ldots \tag{67}$$

If $\mu(t)$ is constant, the calculated result of (66) must be consistent with that defined by the Grünwald-Letnikov fractional calculus of the constant operational order.

3.4. Experimental Verification

In this subsection, the variable-order characteristics of VSFF are experimentally verified. The experimental fields include steady-state, dynamic, and continuous variable order. The steady-state variable-order experiments can be used to prove that a single VSFF can be used as a constant-order fractor of different orders. The dynamic variable-order experiments can prove that the VSFF contains a variable-order process, which can be used in the cases where the operational order requires a jump. For example, in the design of programmable variable-order fractional chaos [18]. The continuous variable-order experiments can be used to demonstrate the capability of VSFF for programmable high-resolution continuous variable-order.

GPS-4303C, TBS1052B, EE16330, TCP312A, and TCPA300, were employed as the power supply, oscilloscope, signal generator, current probe, and current amplifier, respectively. The current probe and amplifier were used to convert the current waveform to a linear voltage signal and to amplify the voltage signal for the oscilloscope test, respectively. The TBS1052B is connected to a PC through a USB interface, which has the Tektronix OpenChoice PC Communications software installed on it to obtain the data that it measured by TBS1052B. Figure 5 depicts the experimental test images.
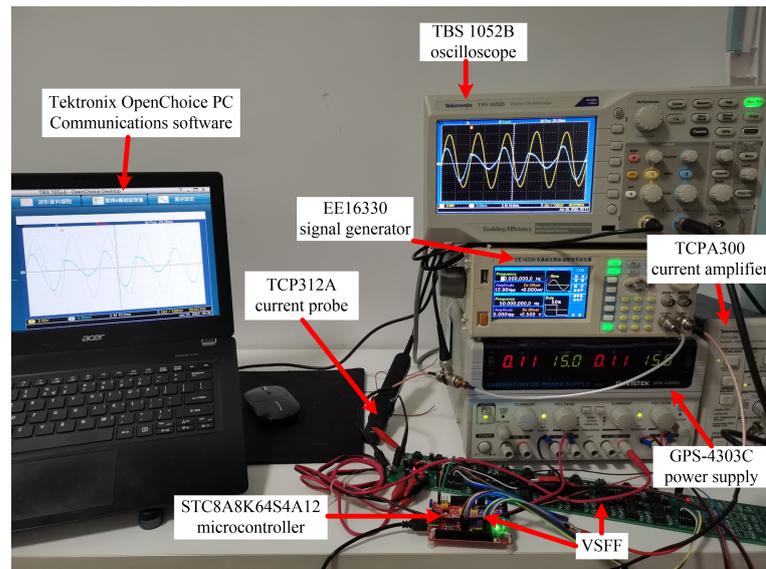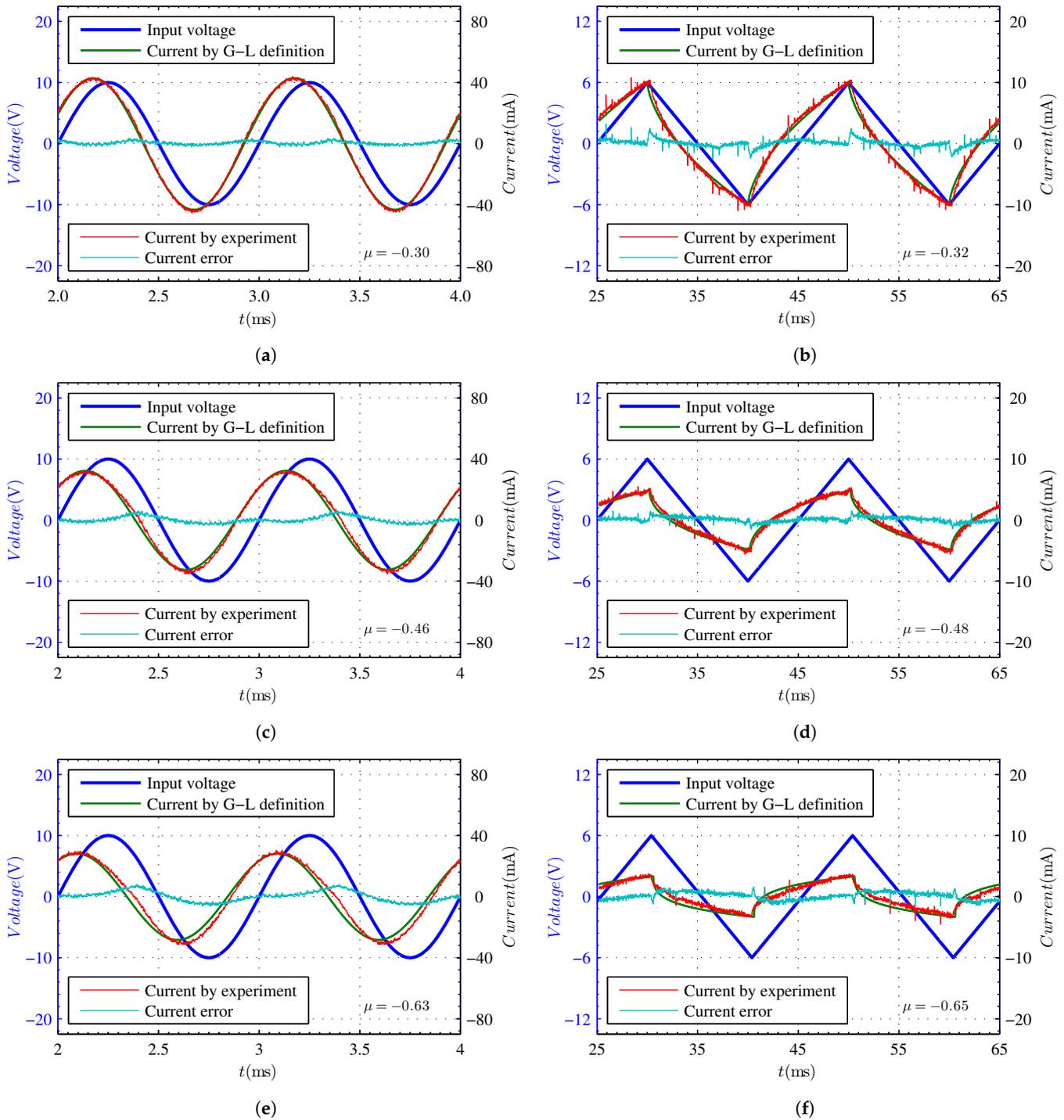
Figure 5. VSFF Experiment.

3.4.1. Steady-State Variable-Order Experiment

If the signal generator outputs a sinusoidal voltage signal,

$$u^{(S)}(t) = A^{(S)} \sin\left(2\pi f^{(S)} t\right) \tag{68}$$

to the VSFF, $A^{(S)} = 10$ V, and $f^{(S)} = 1000$ Hz. Then, $\mu(t)$ is -0.30, -0.46, and -0.63, respectively. The Grünwald-Letnikov definition method is used to calculate the current waveform obtained from (61), (66) and (67), and Figure 6a,c,e presents the corresponding experimental current waveform. If the triangular wave voltage signal, $u^{(T)}(t)$, is input into the VSFF, the peak voltage, $A^{(T)} = 6$ V, frequency, $f^{(T)} = 50$ Hz, and $\mu(t)$ change to -0.32, -0.48, and -0.65, respectively. The Grünwald-Letnikov definition method is used to calculate the current waveform, and Figure 6b,d,f depicts the corresponding experimental current waveform. Furthermore, Figure 6 depicts the current error waveform between the experimental current waveform and the Grünwald-Letnikov definition method is used to calculate the current waveform.

According to the experimental current waveform shown in Figure 6, when the input voltage signals are sinusoidal and triangular, the VSFF can perform steady-state variable-order experiments of different orders. The average values of the current error waveforms shown in Figure 6a–f are 0.4524 mA, 0.1927 mA, 0.2151 mA, 0.0913 mA, 0.1131 mA, and 0.1191 mA, respectively. The standard deviations of the current error waveforms shown in Figure 6a–f are 1.1325 mA, 2.0992 mA, 1.9526 mA, 0.6218 mA, 0.4256 mA, and 0.6348 mA, respectively. When the input amplitude of the voltage waveform is constant, the smaller the operational order, $\mu(t)$, the smaller the amplitude of the current waveform. This is consistent with the amplitude-frequency characteristic function curve depicted in Figure 4a. Figure 6a,c,e demonstrates that when $\mu(t)$ is -0.30, -0.46, and -0.63, the corresponding theoretical phase difference is $-27°$, $-41.4°$ and $-56.7°$, respectively. Figure 6a,c,e also demonstrates that when $\mu(t)$ is -0.30, -0.46, and -0.63, the corresponding experimental phase difference is $-26.6°$, $-40.5°$ and $-53.1°$, respectively. The phase error between the experimental and the theoretical phase is shown in Figure 6a,c,e are $0.4°$, $0.9°$, and $3.6°$, respectively. The phase difference decreases with a decrease in the operational order, $\mu(t)$, which is consistent with the phase-frequency characteristic curve presented in Figure 4b. The experimental results concur well with their theoretical counterparts when the input waveform, amplitude, frequency, and operational order change. The peak value of the input signal was 10 V.

Figure 6. Experimental results of VSFF of steady-state variable-order: (**a**) sine wave, $\mu = -0.30$; (**b**) triangular wave, $\mu = -0.32$; (**c**) sine wave, $\mu = -0.46$; (**d**) triangular wave, $\mu = -0.48$; (**e**) sine wave, $\mu = -0.63$; (**f**) triangular wave, $\mu = -0.65$.

3.4.2. Dynamic Variable-Order Experiment

If the voltage signal, $u^{(S)}(t)$, shown in (68) is input to the VSFF and the peak voltage, $A^{(S)} = 6$ V,

$$f^{(S)} = 50 \text{ Hz}, \mu(t) = \begin{cases} -0.33 & \frac{\tilde{n}}{f^{(S)}} \le t < (\tilde{n}+1)\frac{1}{f^{(S)}} \\ -0.66 & (\tilde{n}+1)\frac{1}{f^{(S)}} \le t < (\tilde{n}+2)\frac{1}{f^{(S)}} \end{cases}, \tilde{n} = 0,1,2,\dots \quad (69)$$

Figure 7a presents the circuit theoretical method used to calculate the current waveform obtained from (10), (62) and (63) and the Grünwald-Letnikov definition method used to calculate the current waveform obtained from (61), (66) and (67). Figure 7a presents the corresponding experimental current waveforms. When the triangle wave voltage signal, $u^{(T)}(t)$, is input into the VSFF, the peak voltage, $A^{(T)} = 6$ V, frequency, $f^{(T)} = 50$ Hz, and $\mu(t)$ vary between -0.33 and -0.66. Figure 7b illustrates the circuit theoretical method used to calculate the current waveform obtained from (10), (62) and (63) and the Grünwald-Letnikov definition method used to calculate the current waveform obtained from (61), (66) and (67). Figure 7b illustrates the corresponding experimental current waveform. Additionally, Figure 7a,b presents the current error waveform between the experimental current waveform and the circuit theoretical method calculated current waveform.

According to the experimental current waveform shown in Figure 7, when the input voltage signals are sinusoidal and triangular, the VSFF can complete dynamic variable-order experiments of different orders. The circuit theoretical method and the Grünwald-Letnikov definition method used to calculate the current waveform overlap perfectly. The accuracy of the variable-order electrical characteristics obtained through circuit theory is verified. The average values of the current error waveforms shown in Figure 7a,b are 0.0517 mA and 0.0723 mA, respectively. The standard deviations of the current error waveforms shown in Figure 7a,b are 0.9938 mA and 0.7473 mA, respectively. At the moment when the operation order jumps, the circuit theoretical method calculated current waveform and the Grünwald-Letnikov definition method calculated current waveform also jump. However, the corresponding experimental waveform jump is not obvious. This is due to parasitic resistance and capacitance parameters in VSFF, test cables, and experimental apparatus, which filter out the high-frequency spectrum during the current waveform jump. According to the experimental current waveform shown in Figure 7, the VSFF completed the change of order within the approximation frequency and operational order ranges.

3.4.3. Continuous Variable-Order Experiment

A continuous variable-order experiment was conducted to fully demonstrate the variable-order capability of the VSFF and to reflect its advantages. If the voltage signal, $u^{(S)}(t)$, shown in (68) is input to the VSFF and the peak voltage, $A^{(S)} = 6$ V, the frequency, $f^{(S)} = 50$ Hz, and $\mu(t)$ change from -0.3 to -0.7. The variable-order range included the maximum and minimum values of the designed operational order. Figure 8 depicts the circuit theoretical method used to calculate current waveform obtained from (10), (62) and (63) and the Grünwald-Letnikov definition method used to calculate the current waveform obtained from (61), (66) and (67). Figure 8 depicts the corresponding experimental current waveform. Additionally, Figure 8 depicts the current error waveform between the experimental current waveform and the circuit theoretical method used to calculate the current waveform.
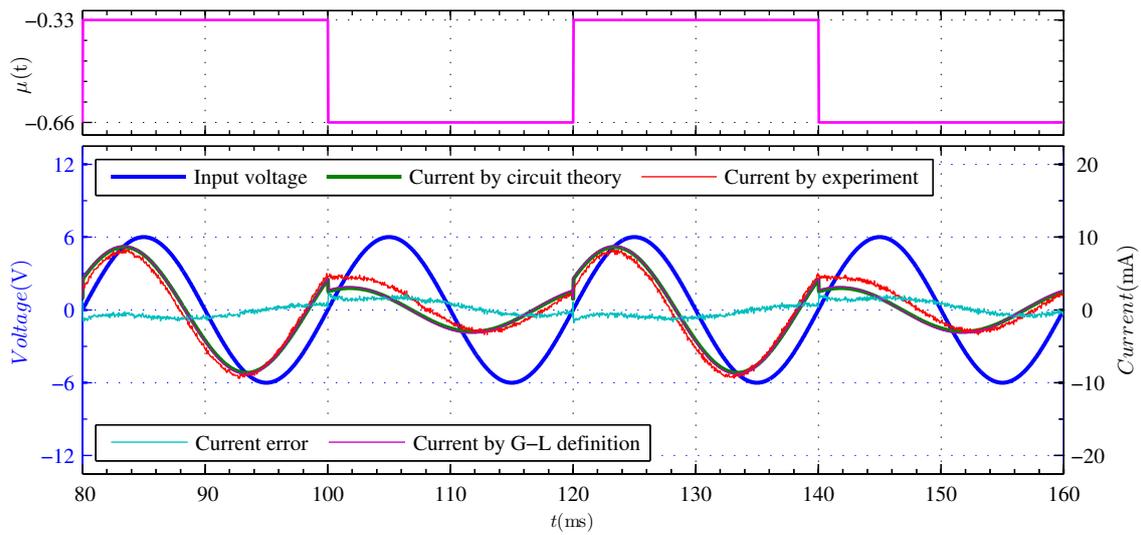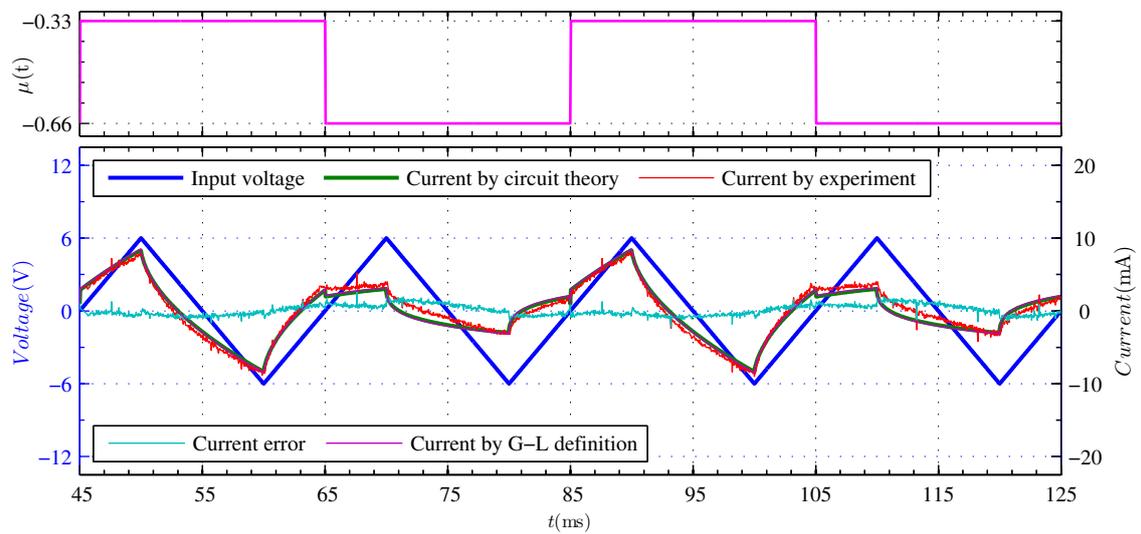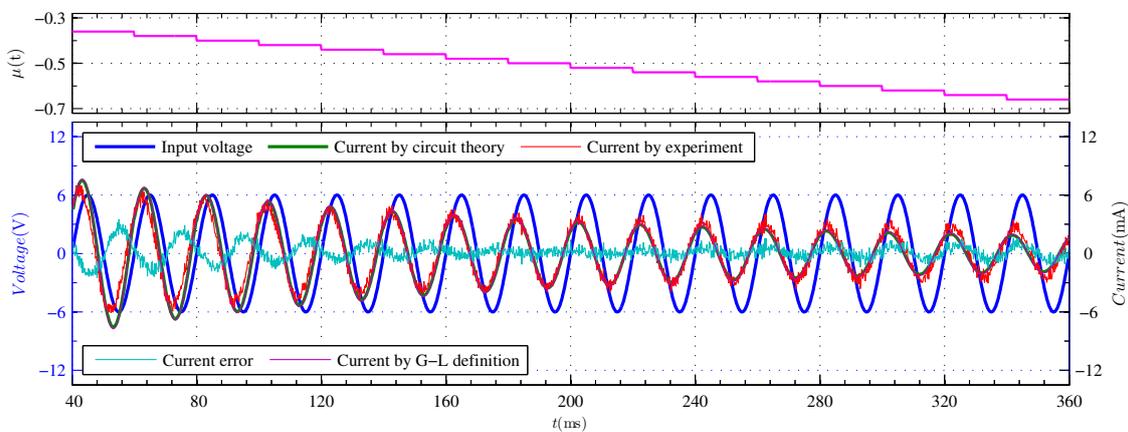
Figure 7. Experimental results of VSFF of dynamic variable-order: (**a**) sine wave; (**b**) triangular wave.

Figure 8. Experimental results of VSFF of continuous variable-order.

The VSFF can perform continuous variable-order experiments based on the experimental current waveform depicted in Figure 8. The circuit theoretical method and the Grünwald-Letnikov definition method used to calculate the current waveform overlap perfectly. The accuracy of the variable-order electrical characteristics obtained through circuit theory is confirmed once again. The larger current error waveforms are partly due to small phase errors. In essence, the current error is not large. The average value and standard deviations of the current error waveforms shown in Figure 8 are 0.1167 mA and 0.7094 mA, respectively. Errors may be caused by many factors such as circuit components, experimental instruments, and frequency domain approximation errors. Errors in circuit components include resistors, capacitors, operational amplifiers, and AD5544. The relative errors of various equivalent parameters of AD5544 caused by resolution have been given in Table 1. Integral non-linearity is also an important factor causing error of AD5544. There is a non-linear relationship between integral non-linearity and digital quantity of AD5544 [39]. The frequency characteristic curves shown in Figure 4 also indicate that there are frequency domain errors that fluctuate with frequency within the approximate frequency range. When the input amplitude of the voltage waveform is constant, $\mu(t)$ changes from -0.3 to -0.7, the smaller the amplitude of the current waveform. This is consistent with the amplitude-frequency characteristic function curve shown in Figure 4a. It can also be observed from Figure 8 that when the operation order reduces, the smaller the operation order, the larger the relative error between the experimental current waveform and the theoretical waveform. This is similar to the equivalent relative error variation rule shown in Table 1. It is observed that the equivalent relative error changes from minimum to maximum as the operation order changes from maximum to minimum. It can be observed from Figure 8 that the variable-order scaling fractal-ladder fractor can perform high-resolution continuous variable-order experiments within the range of the operation order. This is because the HRMDAC and other devices can support the requirement of device indicators for continuous operational order varying.

It can also be observed from Figure 8 that when the operation order is large, the amplitude of the experimental current waveform is smaller than that of the theoretical current waveform. When the operation order is small, the amplitude of the experimental current waveform is larger than that of theoretical current waveform. A similar situation is observed in the steady-state variable-order and dynamic variable-order experiments. The error between the experimental waveform and the theoretical waveform, and the operation order exhibit a stable regularity; this type of error is called a systematic error. System errors must be calibrated often in circuit and system design. Therefore, when the results of Figures 6 and 7 are presented, the same systematic error calibration parameters are implemented for the circuit theoretical method, which is used to obtain the current waveform from (10), (62) and (63) and the Grünwald-Letnikov definition method used to obtain the current waveform from (61), (66) and (67). The calibration results used while constructing an application system using VSFF must be more accurate.

4. Discussion

This study implemented the VSFF superior to existing related studies in multiple indicator dimensions. In [13], when the temperature of the solid-state fractor changed within the range of 25~60 °C, and the operational order changed within a range of only 0.909~0.949. In [14], when the temperature of the solid-state fractor changed within the range 100~150 °C, the operational order changed within a range of only 0.77~0.86. The VSFF implemented in this study used a microcontroller, which is more convenient and efficient than the temperature control method [13,14]. In [19], the operational order switched between 0.2, 0.5, and 0.8. However, the studies conducted on circuit implementation are limited. The variable-order range of the circuit realized in this study was from -0.7 to -0.3. This significantly exceeds the operational order range of the variable-order fractor [13,14,19] and exhibits high-resolution characteristics. The HMDAC is crucial in the implementation of the VSFF.

In this study, the scaling fractal fractor used in the VSFF exhibited a classic structure. The voltage-controlled resistance and capacitance circuits used the AD633 multiplier as the core in the memristor and memcapacitor emulators [35–37]. The resolution and precision requirements of the VSFF for variable circuit parameter adjustment could not be easily satisfied since the accuracy of the AD633 was approximately 2%. The HMDACs are typically used in the DAC conversion and in multiplier circuits. The HMDAC uses the AD5544, $m = 16$ bits, and a resolution of $\Delta K = \frac{1}{2^m} = \frac{1}{65,536}$. For the emulator, the equivalent minimum relative error $\delta_{\min}^{(\hat{x}_n)} = \frac{1}{65,536}(\hat{x}_n = \tilde{c}_n, \tilde{r}_n, c_o, r_o)$ and maximum relative error $\delta_{\max}^{(\hat{x}_n)} = 6.732 \times 10^{-4}$. The programmable resistor–capacitor series circuit and programmable universal electronic component emulators designed using the HMDAC as the core can better meet the requirements of the VSFF parameter adjustment.

In this study, the selection of component parameters is merely an example of the circuit implementation of the VSFF. The technical specifications of VSFF can be adjusted based on the requirement of the actual system. The frequency range of the operations can be increased by increasing the total number of subcircuits. The accuracy can be improved by decreasing the value of the scaling parameter, σ. The VSFF accuracy can also be improved by selecting components with higher precision and resolution. Furthermore, the speed of the variable order can be increased by using faster microcontrollers.

Despite the various advantages presented by the implemented VSFF, it faces certain limitations that must be addressed. Firstly, VSFF is larger and thus requires more space, although it is more flexible and has a wider range of steps when compared to the existing solid-state fractor. Secondly, the VSFF variable-order speed is limited by the control speed of the microcontroller. Lastly, it can be observed from the F-frequency characteristic function curve presented in Figure 4d, that when the operational order of VSFF changes, the lumped parameter value also changes.

5. Conclusions

Variable-order fractor is an important unit or component for realizing variable-order fractional calculus operations. Based on previous studies on scaling fractal fractor with various structures [30–34], the theoretical problem of developing high-resolution emulator circuits to achieve VSFF is a major challenge. This study proposed a VSFF circuit configuration based on the scaling expansion theory [30,31]. A programmable resistor–capacitor series circuit and programmable universal electronic component emulators with HMDAC were designed based on the requirements of the circuit configuration. The experimental content includes steady-state, dynamic and continuous variable-order. The operational order ranged from -0.7 to -0.3. The operation frequency of the VSFF ranged from 7.72 Hz to 4.82 kHz and the peak value of the input signal was 10 V.

The programmable resistor–capacitor series circuit and the programmable universal electronic component emulators were designed based on the HMDAC. Furthermore, these emulators can be applied to other variable-order fractor circuits, memristor emulators, and memcapacitor emulators. The proposed implementation method can also be used to design the existing scaling fractal-chain [33], fractal-chuan [32], and fractal-lattice [30,31] circuits with variable-order fractor. The VSFF can be used to model natural phenomena and processes of the variable order. The proposed variable-order fractional calculus method that is based on circuit theory can be used as a new time-domain approximation method. More circuit theoretical calculation formulas of variable-order fractional calculus operation can be obtained based on the proposed circuit theoretical calculation method of variable-order fractional calculus operation. The variable-order fractional calculus using circuit theory requires further analysis since it is a novel calculation method.

Author Contributions: Conceptualization, B.Y. and Y.P.; methodology, B.Y. and X.Y.; software, B.Y. and Q.H.; validation, B.Y.; writing—original draft preparation, B.Y.; writing—review and editing, B.Y. and Y.P.; supervision, Y.P.; funding acquisition, Y.P. and B.Y. All authors have read and agreed to the published version of the manuscript.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

VSFF   Variable-Order Scaling Fractal-Ladder Fractor
HMDAC   High-Resolution Multiplying Digital-to-Analog Converter

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