Circuit Solutions on ESD Protection Design for Mixed-Voltage I/O Buffers in Nanoscale CMOS

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***Abstract*—Electrostatic discharge (ESD) protection for mixed-voltage I/O interfaces has been one of the major challenges of system-on-a-chip (SOC) implementation in nanoscale CMOS processes. Moreover, the gate leakage current across thin gate-oxide devices has serious degradation on circuit performance while circuits implementing in nanoscale CMOS processes. The on-chip ESD protection circuit for mixed-voltage I/O buffers should meet the gate-oxide reliability constraints and be designed with consideration of gate leakage current. This paper presents the effective ESD protection scheme with circuit solutions to protect the mixed-voltage I/O buffers in nanoscale CMOS processes against ESD stresses. The proposed ESD protection scheme and the specific ESD clamp circuits with low standby leakage current have been successfully verified in nanoscale CMOS processes. Effective on-chip ESD protection scheme should be early planed and started in the beginning phase of chip design in order to achieve good enough ESD robustness for IC products.**

I. Introduction

For commercial IC products, to achieve the electrostatic discharge (ESD) specification is necessary duirng product qualification. On-chip ESD protection has become a design challenge for CMOS ICs implemented in nanoscale CMOS technologies. The thickness of the gate oxide and the device dimension of transistors have scaled down to improve the circuit performance; meanwhile, the power supply voltage has been also decreased to reduce the power consumption and to meet the gate oxide reliability. On-chip ESD protection should be developed with more aggressive method to protect such a thin gate-oxide devices against ESD damage [1]. Recently, some process optimizations on MOSFETs in nanoscale CMOS processes have been reported to improve the device-level ESD robustness [2], [3].

From the perspective of circuit design for whole system integration, the core circuit designs have been migrated to lower VDD voltage level such as 1V in a 65-nm CMOS process while some peripheral components or other ICs in a microelectronic system are still operated at the higher voltage levels (1.8V/2.5V). Therefore, the I/O buffers for such mixed-voltage interfaces may drive or receive high-voltage signals to communicate with other ICs. Several problems arise when traditional I/O buffer is used in the mixed-voltage I/O buffers between these ICs, such as the gate-oxide breakdown [4] and the undesirable leakage current paths across the parasitic forward diode in the pull-up PMOS.

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To solve the gate-oxide reliability issue without using the additional thick gate-oxide process (called dual gate oxide in some CMOS processes), the stacked-NMOS configuration had been widely used in the mixed-voltage I/O buffer to reduce the process complexity and fabrication cost of the chip [5]. However, the stacked NMOS configuration has a lower ESD level and slower turn-on speed, as compared with the single NMOS [6]. Therefore, additional ESD protection design must be provided to protect the stacked NMOS in the mixed-voltage I/O buffer without additional leakage current path and the problem of gate-oxide reliability.

In addition to the requirement of the specific ESD protection scheme for the mixed-voltage I/O buffers, a more serious problem in gate leakage issue occurs while thin gate-oxide devices implemented in nanoscale CMOS processes. Such a thin gate-oxide of only ~2nm in a 130nm CMOS technology has been reported to result in a substantial fraction of the overall leakage current in the chip due to its gate leakage current [7]. To reduce the gate leakage current, the high-k metal gate technology is applied in 45-nm generation and beyond [8], [9]. Nevertheless, the gate leakage issue still exists in the 90-nm and 65-nm CMOS technologies which are currently used in major production without using high-k/metal-gate structure. The gate current of MOSFET has been modeled in BSIM4 model [10], and the foundries have also supported the corresponding SPICE parameters in their nanometer CMOS processes to circuit designers. Recently, some work has been reported on how to reduce the gate leakage current for digital circuits in advanced CMOS processes [11], [12]. In the traditional power-rail ESD clamp circuit which is used to protect the core circuits [13], the large-sized ESD clamp device and the MOS capacitor will suffer serious gate leakage problem and induce huge whole-chip standby leakage current while implementing in nanoscale CMOS process [14]. New designs on the power-rail ESD clamp circuit should be developed to further reduce such standby leakage current in nanometer CMOS processes.

In this paper, the ESD protection schemes and high-voltage-tolerant ESD clamp circuits designed to protect the mixed-voltage I/O interfaces against ESD stresses without suffering the gate-oxide reliability issue are presented [15], [16]. With consideration of gate-leakage issue, a new high-voltage-tolerant low-leakage ESD clamp circuit has been designed and successfully verified in the nanoscale CMOS processes with only thin gate-oxide devices [17]. High ESD robustness for mixed-voltage I/O buffers can be achieved with the proposed circuit solutions.

II. ESD Proection Design For Mixed-Voltage I/O Interfaces

A. ESD Protection Schemes

The ESD protection schemes with only 1×VDD thin gate-oxide devices for the mixed-voltage I/O interfaces to drive or receive 2×VDD high-voltage signals, with power supply voltage of 2×VDD or VDD are shown in Figs. 1(a) and 1(b), respectively. From Fig. 1(a), the ESD protection scheme can be implemented by placing diode from I/O pad to the power pad of 2×VDD with an efficient 2×VDD-tolerant ESD clamp circuit between 2×VDD and VSS. However, this protection scheme can not be applied if the power supply voltage is only VDD due to the leakage current path across the top-side diode Dp. The ESD bus (realized by wide metal line in CMOS process) is applied to solve this problem, as shown in Fig. 1(b). The ESD bus is not directly connected to an external power pad, but is initially biased at VDD through the diode D1 after the chip has been powered on. When the 2×VDD input signals reach to the I/O pad (Fig. 1(b)), the ESD bus line will be charged up to 2×VDD through Dp. Therefore, the ESD clamp circuit between ESD bus and VSS should be also designed to tolerant 2×VDD supply voltage during normal circuit operating conditions. Both ESD protection schemes (Fig. 1(a) and Fig. 1(b)) need a 2×VDD-tolerant ESD clamp circuit to protect the stacked-NMOS in the mixed-voltage I/O buffer. The R_{ESD} is used to avoid damage on the stacked-NMOS before the ESD current is discharged through this ESD protection scheme. The diode D1 connected between the VDD and ESD bus is used to block the leakage current path from the I/O pad to VDD.

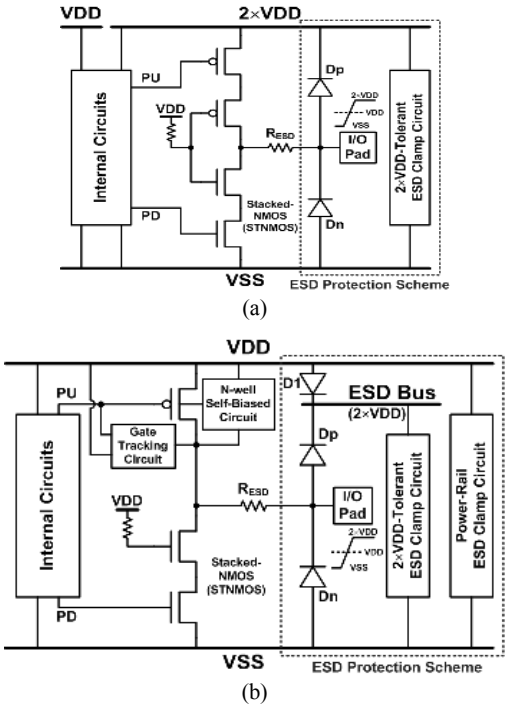

Fig. 1. ESD protection schemes for mixed-voltage I/O interface with 2×VDD-tolerant ESD clamp circuit, where the power supply is powered by voltage level of (a) 2×VDD or (b) VDD.

For the ESD protection scheme with ESD bus, under positive-to-VSS (PS-mode) ESD stress on I/O pad, the ESD current can be discharged through the diode Dp to the ESD bus and then through the 2×VDD-tolerant ESD clamp circuit to the grounded VSS, instead of through stacked NMOS in the I/O buffer to ground. Under positive-to-VDD (PD-mode) ESD stress on I/O pad, the ESD current can be discharged through Dp, ESD bus, and the 2×VDD-tolerant ESD clamp circuit to VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. Under negative-to-VSS (NS-mode) ESD stress on I/O pad, the negative ESD current can be discharged through the diode Dn in forward-biased condition to the grounded VSS. Under negative-to-VDD (ND-mode) ESD stress on I/O pad, the negative ESD current can be discharged through Dn to the floating VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. These four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the ESD protection scheme with ESD bus.

B. Design of 2×VDD-tolerant ESD Clamp Circuit

The 2×VDD-tolerant ESD clamp circuit realized with only 1×VDD thin gate-oxide devices is shown in Fig. 2, composed of the ESD detection circuit and the stacked-NMOS (STNMOS) as ESD clamp device. The gate of Mn1 is biased at VDD through a resistor to avoid the gate-oxide reliability issue, and the gate of Mn2 is connected to VSS to ensure the off state of the STNMOS. Therefore, the STNMOS will be kept off without gate-oxide reliability during normal circuit operating conditions. During the normal circuit operating condition, the ESD detection circuit is kept inactive and does not interfere with the functions of internal circuits. Nevertheless, it becomes active to provide the substrate-triggered current to quickly trigger on the STNMOS under ESD stress condition.

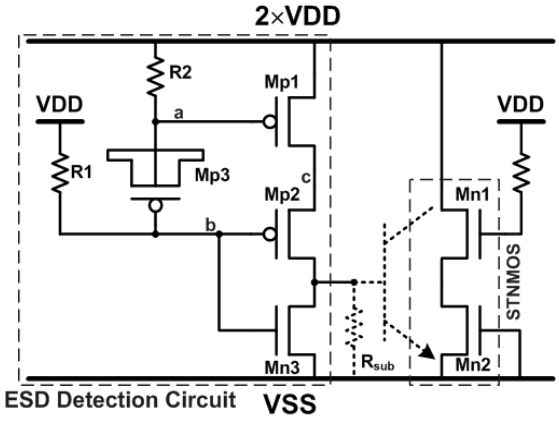

Fig. 2. The 2×VDD-tolerant ESD clamp circuit with only 1×VDD thin gate-oxide devices.

During normal circuit operating conditions, the gate of Mp1 (node a) is biased at 2×VDD through the resistor R2, and the gate of Mp2 and Mn3 (node b) are biased at VDD through the

resistor R1. Therefore, Mp1 and Mp2 are kept in off state but Mn3 is turned on to bias the substrate of STNMOS at VSS. There is no trigger current generated from the ESD detection circuit into the STNMOS, so the STNMOS is guaranteed to be kept off during normal circuit operating conditions. The source-gate voltage of Mp2 is less than the threshold voltage of 1×VDD PMOS transistor (|Vtp|), so the source voltage of Mp2 (node c) is kept between VDD and VDD+|Vtp|. In this situation, all 1×VDD devices are free from gate-oxide reliability issue during normal circuit operating condition with voltage level on the ESD bus of 2×VDD in the mixed-voltage I/O interfaces.

When ESD transient voltage is applied to 2×VDD with VSS relatively grounded, the RC delay of R2 and C (Mp3) in the ESD detection circuit will keep the gate (node a) of Mp1 at a relatively low voltage for a long time. The VDD is initially floating with an initial voltage level of 0V before the ESD transient voltage is applied across 2×VDD and VSS. Some ESD transient voltage would be coupled to VDD through the parasitic capacitance during ESD zapping, but the R1 and the parasitic capacitance at the gates of Mp2 and Mn3 will hold the gate of Mp2 at a low voltage level for a long time to keep Mp2 in on state. Therefore, Mp1 and Mp2, whose initial gate voltages are at a low voltage level, can be quickly turned on by the ESD energy to generate the substrate-triggered current into the substrate of the STNMOS. After the base-emitter voltage of the lateral n-p-n BJT in the STNMOS is greater than its cut-in voltage, the STNMOS will be triggered into its snapback region to discharge ESD current from 2×VDD to VSS.

C. *Experimental Results*

The ESD protection scheme with 2×VDD-tolerant ESD clamp circuit for 1.2/2.5-V mixed-voltage I/O interfaces has been successfully verified in a 130nm CMOS process with only 1.2-V devices. Transmission line pulsing (TLP) generator [18] is used to verify the secondary breakdown current (It2) of STNMOS with or without ESD detection circuit. The measured TLP I–V curves of STNMOS with device dimension (W/L) of 360μm/0.2μm are shown in Fig. 3. The STNMOS with ESD detection circuit can be triggered on at a lower voltage level than that without ESD detection circuit. In addition, the turn-on uniformity among the multiple fingers of STNMOS can be improved to enhance its ESD robustness by the substrate-triggered effect [19], such that the It2 of STNMOS with ESD detection circuit can be increased from 2A to 2.6A.

The human-body-model (HBM) and machine-model (MM) ESD levels of STNMOS devices with different device dimensions are shown in Table I. In these ESD verifications, the HBM and MM ESD levels are measured by *KeyTek ZapMaster* where the failure criterion is defined as the I-V characteristic curve shifting over 30% from its original curve after three continuous ESD discharges at every ESD test level. With the substrate-triggered current generated from the ESD detection circuit, the turn-on uniformity of STNMOS can be effectively improved. The HBM (MM) ESD levels of the STNMOS with the ESD detection circuit in the 2×VDD-tolerant ESD clamp circuit under channel widths of 240, 360, and 480μm with a channel length of 0.2μm are improved from 3, 4, and 5kV (175, 250, and 275V) to 4, 5, and 6.5kV (225, 300, and 400V), respectively, as compared with the stand-alone STNMOS. Therefore, the ESD levels of these 1.2/2.5V mixed-voltage I/O interfaces can be effectively improved by the ESD protection scheme with ESD bus and the 2×VDD-tolerant ESD clamp circuit.

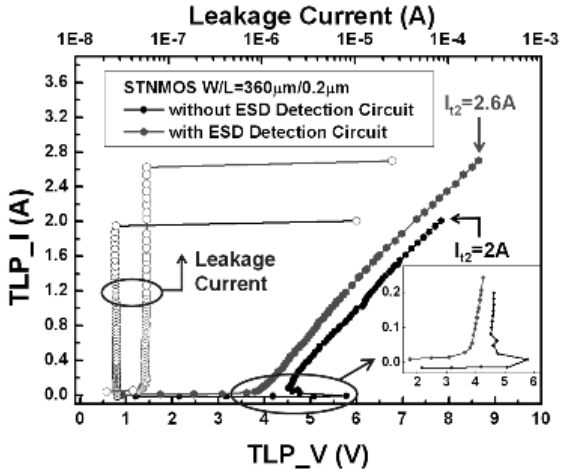

Fig. 3. The TLP-measured I-V curve of the STNMOS with or without ESD detection circuit under device dimension (W/L) of 360μm/0.2μm.

TABLE I
HBM AND MM ESD LEVELS OF STNMOS WITH OR WITHOUT ESD DETECTION CIRCUIT

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)	
	Without detection circuit	With detection circuit	Without detection circuit	With detection circuit
240/0.2	3	4	175	225
360/0.2	4	5	250	300
480/0.2	5	6.5	275	400

III. 3×VDD-TOLERARNT ESD PROECTION DESIGN

Recently, the mixed-voltage I/O buffer to receive 3×VDD input signals by using only 1×VDD thin gate-oxide devices without suffering gate-oxide reliability issue has been proposed [20]. Nevertheless, the ESD protection design for such a 3×VDD-tolerant mixed-voltage I/O buffer was not considered. Therefore, how to design an effective ESD protection circuit with only 1×VDD thin gate-oxide devices without suffering gate-oxide reliability for mixed-voltage I/O buffer with 3×VDD input tolerance is also a challenge. With the ESD protection scheme with ESD bus for mixed-voltage I/O buffer, an efficient 3×VDD-tolerant ESD clamp circuit is needed.

A. *Design of 3×VDD-tolerant ESD Clamp Circuit*

The 3×VDD-tolerant ESD clamp circuit with only 1×VDD thin gate-oxide devices is shown in Fig. 4. The p-type substrate-triggered silicon-controlled rectifier (SCR) device with three diodes in series is used as the main ESD clamp

device [21]. The SCR device, which is composed of cross-coupled n-p-n and p-n-p BJTs with regenerative feedback loop, with a low holding voltage can sustain a high ESD level within a smaller silicon area in CMOS process. However, the main concerns of the SCR device as the ESD clamp device are the slow turn-on speed, high trigger voltage, and latchup issue. The most common method to solve the latchup issue is to connect with several diodes in series. To avoid the damage of I/O buffer before ESD clamp device is turned on, the ESD detection circuit is also used to provide the substrate-triggered current to quickly trigger on the SCR device.

During normal circuit operating condition, the diode-connected PMOS (Mp1~Mp3) are used as the voltage divider to bias the substrate driver (Mn1, Mp4, and Mp5) of the ESD detection circuit, where a deep N-well is used in Mn1 to avoid the gate-oxide overstress between gate and bulk. The NMOS (Mn2) is used to keep the voltage level of the trigger node at VSS, so the ESD clamp device is guaranteed to be kept off. All devices in the ESD detection circuit with 1×VDD thin gate-oxide can be free from gate-oxide reliability issue during the normal circuit operating condition.

When ESD voltage is applied to 3×VDD with VSS relatively grounded, and VDD floating, the capacitor (Mp6) will couple some ESD transient voltage to the node 1 to turn on Mn1 and to pull up the node 3. The RC delay from R1 and Mp7 in the ESD detection circuit will keep the gate of Mp4 (node 4) at a relatively lower voltage level (compared to the node 3) for a long time. The VDD is initially floating with an initial voltage level of 0V during ESD stress. Some ESD transient voltage would be coupled to VDD through the parasitic capacitance during ESD zapping, but the R2 and the parasitic capacitance at the gates of Mp5 and Mn2 will hold the gate of Mp5 at a low voltage level for a long time to keep Mp5 in on state. Therefore, Mp4 and Mp5**,** whose initial gate voltages are at low voltage level, can be quickly turned on by ESD energy to generate the substrate-triggered current into the substrate of SCR. Then, the ESD clamp device can be quickly triggered on to discharge ESD current from 3×VDD to VSS.

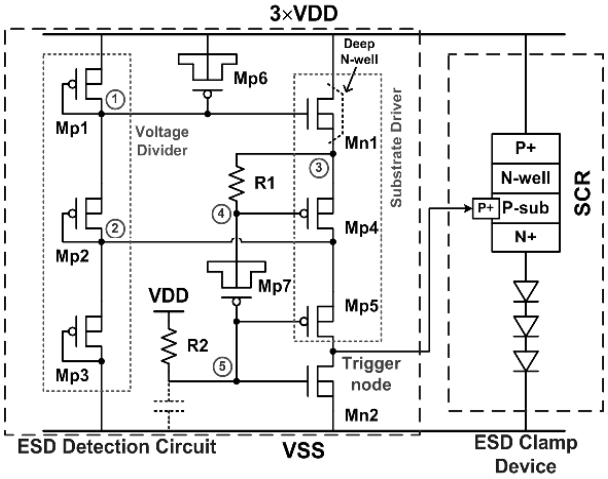

Fig. 4. Circuit implementation of the 3×VDD-tolerant ESD clamp circuit realized with only 1×VDD thin gate-oxide devices.

B. Experimental Results

The ESD protection design with 3×VDD-tolerant ESD clamp circuit for 1.2/3.3-V mixed-voltage I/O interfaces has been successfully verified in a 130nm CMOS process with only 1.2-V devices. Fig. 5 shows the measured voltage waveforms under the PS-mode ESD stress and the normal circuit operating condition with overshooting noise pulse by applying a 0-to-6V voltage pulse with a rise time of 10ns to I/O pad. During PS-mode ESD stress (VDD is floating), the overshooting voltage waveform at I/O pad is clamped by the Dp and ESD clamp device to ~4V, which is lower than the breakdown voltage of the stacked NMOS in the mixed-voltage I/O buffer. Therefore, the 3×VDD-tolerant I/O buffer can be effectively protected by the proposed ESD protection design. Under normal circuit operating condition (VDD is biased at 1.2V), the voltage waveform at I/O pad is still kept at 6V, so the ESD clamp device is not triggered on even with an overshooting noise at I/O pad. From the measured voltage waveforms in Fig. 5, the excellent turn-on efficiency in ESD-stress condition and high enough noise immunity in normal circuit operating condition has been successfully verified in the ESD protection design.

The TLP-measured secondary breakdown current (It2) and HBM ESD level of the 3×VDD-tolerant I/O buffer with and without the ESD protection circuit under PS-mode ESD stress are compared in Table II. When the width of SCR device in ESD clamp device is 45μm, the It2 of the I/O buffer with the ESD protection circuit can be increased from 0.2A to 4A, as comparing with the I/O buffer without ESD protection. In addition, the HBM ESD level of the I/O buffer with the ESD protection scheme can be improved from 500V to 6kV. When the width of SCR device in ESD clamp device is increased to 90μm, the It2 and HBM ESD level of the I/O buffer with the ESD protection scheme can be further increased larger than 6A and 8kV, respectively. The ESD protection scheme with 3×VDD-tolerant ESD clamp circuit can significantly improve the It2 and HBM ESD level of the 3×VDD-tolerant I/O buffer.

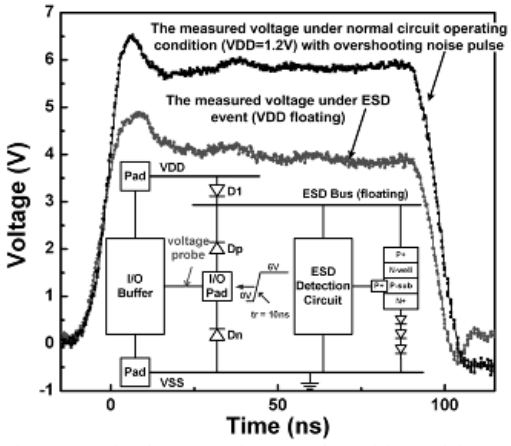

Fig. 5. The measured voltage waveforms at I/O pad by applying a 0-to-6V overshooting voltage pulse to I/O pad under the PS-mode ESD stress (VDD floating) and the normal circuit operating condition (VDD = 1.2V).

TABLE II
ESD ROBUSTNESS OF I/O BUFFER WITH OR WITHOUT ESD PROTECTION

3×VDD-Tolerant I/O Buffer	It2	HBM ESD Level
I/O Buffer without ESD Protection Circuit	0.2A	< 500V
I/O Buffer with ESD Protection Circuit (SCR Width = 45μm)	4A	6kV
I/O Buffer with ESD Protection Circuit (SCR Width = 90μm)	> 6A	> 8kV

IV. ESD CLAMP CIRCUIT WITH CONSIDERATION OF GATE LEAKAGE CURRENT

The gate leakage current cannot be neglected when the gate oxide thickness is scaled down to 3nm and below. The oxide thickness and the total gate current across the gate-oxide of N/P MOSFET with W/L of 1μm/1μm under 1-V bias in 90-nm, 65-nm, and 45-nm CMOS processes are compared in Table III. The gate current of a MOS capacitor with W/L of 5μm/5μm used in ESD detection circuit in a 65-nm CMOS process will be as high as 2μA. Such a leakage current across the MOS capacitor could cause the ESD detection circuit abnormal function and induce a significant leakage current across the whole ESD protection circuit.

To solve the problem of malfunction in the traditional RC-based ESD detection circuit [13], the timer level restorer was ever reported [14]. However, even with the additional timer level restorer, the gate current of ESD clamp MOSFET and MOS capacitor still result in a total standby leakage current of several ten micro-amperes at 125°C in a 130nm CMOS process. Another design using the PMOS and NMOS feedback technique to decrease the leakage current of the power-rail ESD clamp circuit and to improve the trigger ability had also been reported [22]. However, such feedback network used in power-rail ESD clamp circuit might suffer transient latchup failure during the system-level ESD test [23]. To solve the gate leakage current without suffering transient latchup issue from feedback network, a new design solution for ESD clamp circuit has been proposed in the following.

A. Gate Leakage Current in the 2×VDD-Tolerant ESD Clamp Circuit

Based on BSIM4 model, the STNMOS in Fig. 2 with large device size as ESD clamp device generates some leakage current from 2×VDD to VDD via the gate of Mn1. Furthermore, the sub-threshold leakage current of the STNMOS in a nanoscale CMOS technology is also large. In the ESD detection circuit, the MOS capacitor with gate oxide of large area will induce a large amount of gate current from node a to VDD during the normal circuit operating condition. Therefore, the leakage current path exists from 2×VDD through R1, Mc1, and R to VDD. Such gate current causes a voltage drop across the resistor R1, and therefore the PMOS Mp1 in the ESD detection circuit can not be completely turned off. With a non-turned-off PMOS, node d could be charged up to some voltage level higher than VSS, and that in turn provides some triggered current into the substrate of STNMOS under the normal circuit operating condition. The STNMOS with weak triggered current could further induce extra leakage current. Both the ESD detection circuit and STNMOS suffer serious leakage current issue when this ESD clamp circuit is implemented in a nanoscale CMOS technology. Such a leaky ESD protection circuit is barely tolerable for low power requirements.

TABLE III
OXIDE THICKNESS AND GATE CURRENT OF GATE-OXIDE OF N/P MOSFET UNDER 1-V BIAS IN DIFFERENT CMOS TECHNOLOGIES

Generation	MOS Type	Oxide Thickness	Gate Leakage @ 1V Bias (W/L = 1μm/1μm)
90nm	NMOSFET	~2.3nm	~11nA
	PMOSFET	~2.5nm	~3nA
65nm	NMOSFET	~2.0nm	~140nA
	PMOSFET	~2.2nm	~80nA
45nm	NMOSFET	~1.9nm	~260nA
	PMOSFET	~2.1nm	~95nA

B. New Proposed 2×VDD-Tolerant Low-Leakage Power-Rail ESD Clamp Circuit

The proposed 2×VDD-tolerant low-leakage ESD clamp circuit is shown in Fig. 6. The 2×VDD-tolerant low-leakage ESD clamp circuit is composed of ESD detection circuit and p-type substrate-triggered SCR as ESD clamp device. The SCR device without poly gate structure has good immunity against the gate leakage problem. The new ESD detection circuit with only 1×VDD thin gate-oxide devices is designed with consideration of the gate current and gate-oxide reliability in this work. By utilizing the gate current to bias the ESD detection circuit and optimizing the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor during the normal circuit operating condition can be reduced. The total leakage current, which is resulted from the MOS capacitor, in the ESD detection circuit can be minimized. Therefore, the leakage currents through the ESD clamp device (SCR) and the ESD detection circuit can be well controlled and minimized by this new proposed design.

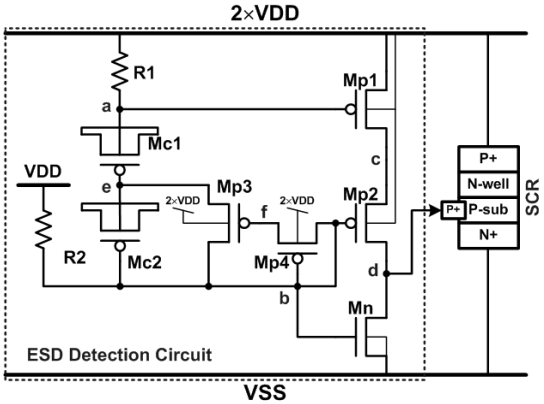

Fig. 6. The 2×VDD-tolerant low-leakage ESD clamp circuit with only 1-V thin gate-oxide devices.

In the proposed ESD detection circuit, the PMOS Mp1 and Mp2 are used as substrate driver to generate the substrate-triggered current into the trigger node of the SCR device during ESD stress event, but the substrate driver is kept off under the normal circuit operating condition. The NMOS Mn is used to keep the trigger node (node d in Fig. 6) at VSS, so the ESD clamp device (SCR) is guaranteed to be turned off during the normal circuit operating condition. The RC time constant from R1, Mc1, Mc2, and the parasitic gate capacitance of Mn is designed around the order of ~μs to distinguish ESD stress event from the normal power-on condition. The diode-connected Mp3 and Mp4 are acted as a start-up circuit with initial gate-to-bulk current from 2×VDD into the ESD detection circuit, and in turn to conduct some gate current of Mc1 to bias the nodes e and f. After that, the voltage level at node e will be biased at a specified voltage level to reduce the voltage difference across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors. In this bias condition, all devices with thin gate oxide in the ESD detection circuit are free from gate-oxide reliability issue under normal circuit operating condition.

When a positive fast-transient ESD voltage is applied to 2×VDD with VSS grounded and VDD floating (with an initial voltage level of ~0V), the RC delay keeps the node a at a relatively low voltage level compared to the fast rising voltage level at 2×VDD. The Mp1 and Mp2, whose initial gate voltages are kept at relatively low voltage levels compared to their source voltages, can be quickly turned on to generate the substrate-triggered current into the trigger node of the SCR device. Finally, the SCR device can be fully turned on into holding state to discharge ESD current from 2×VDD to VSS.

With a foundry provided SPICE model in a 1-V 65-nm CMOS process, the circuit operation of the ESD detection circuit can be simulated. The Hspice-simulated voltage waveforms at the nodes of the proposed ESD detection circuit during and after the normal power-on transition are shown in Fig. 7. 2×VDD and VDD are powered on to 1.8V and 1V, respectively, with a simultaneous rise time of 1ms. From the simulation results, the voltage differences across the gate-to-drain, gate-to-source, and gate-to-bulk terminals of all devices in the proposed ESD detection circuit do not exceed the process limitation (1.1V for 1-V devices in a 65-nm CMOS process). Therefore, the ESD detection circuit can be ensured against gate-oxide reliability issue under the normal circuit operating condition.

Fig. 8 shows the transient simulated voltage and substrate-triggered current of the ESD detection circuit during the ESD transition, where a 0-to-5V voltage pulse with a rise time of 10ns is applied to 2×VDD. With a limited voltage height of 5V in the voltage pulse, the voltage transition on each node in the ESD detection circuit can be simulated to check the desired circuit function before device breakdown. From the simulated results, the source-to-gate voltages of Mp1 and Mp2 are around 1.5V, which is much higher than their threshold voltage, and the substrate-triggered peak current generated from substrate driver is higher than 30mA during the ESD transition. With the proposed ESD detection circuit, the SCR device can be triggered on by the adequate substrate-triggered current before device breakdown during the ESD stress event.

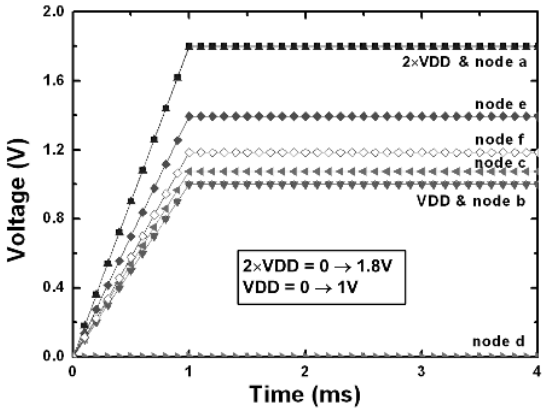

Fig. 7. Hspice-simulated voltage on the nodes of the ESD detection circuit in a 65-nm CMOS process under the normal power-on condition with 2×VDD of 1.8V and VDD of 1V.

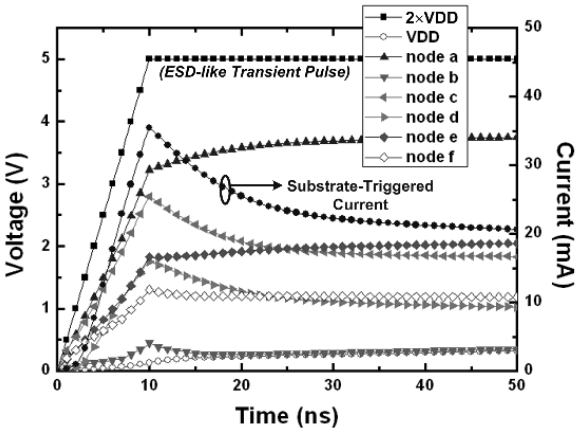

Fig. 8. Hspice-simulated voltages on the nodes of the ESD detection circuit and the substrate-triggered current which flows into the SCR device under 0-to-5V ESD-like transition on 2×VDD.

C. Experimental Results

The proposed 2×VDD-tolerant low-leakage ESD clamp circuit has been fabricated in a 65-nm CMOS process. All devices used in this design are 1-V fully-silicided devices, including the p-type substrate-triggered SCR device. The prior work of 2×VDD-tolerant ESD clamp circuit without consideration of gate current (shown in Fig. 2) has also been fabricated in the same 65-nm CMOS process to compare the standby leakage current and ESD performance.

The measured standby leakage current of the fabricated 2×VDD-tolerant low-leakage ESD clamp circuit at 25°C is shown in Fig. 9, where the width of the SCR device is 45μm. The standby leakage current is measured by increasing the voltage of 2×VDD from 0V to 1.8V and VDD from 0V to 1V simultaneously. The standby leakage current of the prior work (Fig. 2) is measured under the same bias condition, and the result is also shown in Fig. 9. From the measured results, the standby leakage current of the 2×VDD-tolerant low-leakage ESD clamp circuit is only 0.15μA. However, the standby

leakage current of the ESD detection circuit in the prior work is as high as 1.18μA. With the STNMOS, the standby leakage current of the prior work increases up to 5.59μA. The standby leakage current of both the ESD detection circuit and the ESD clamp device (SCR) in this work (Fig. 6) are much smaller than that in the prior work (Fig. 2). The proposed 2×VDD-tolerant low-leakage ESD clamp circuit can successfully achieve a low standby leakage current.

The TLP-measured I-V characteristics of low-leakage 2×VDD-tolerant ESD clamp circuit with SCR device of different widths are shown in Fig. 10. The ESD clamp circuit with SCR widths of 45μm can achieve second breakdown current (It2) of 4.71A. The HBM ESD levels and MM ESD levels of the 2×VDD-tolerant low-leakage ESD clamp circuit are listed in Table IV. The low enough trigger voltage (3~4V) and high It2/HBM/MM values can ensure the effective ESD protection capability.

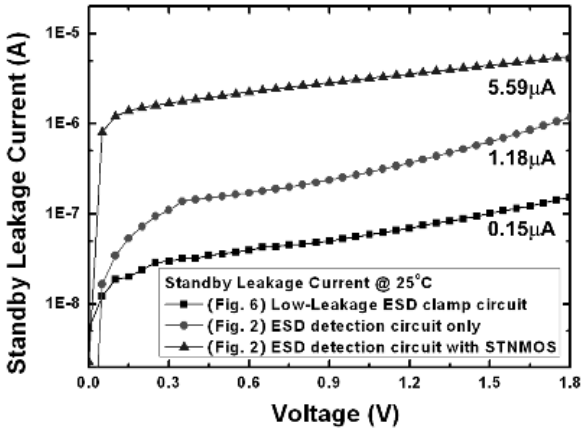

Fig. 9. The standby leakage current of the proposed low-leakage ESD clamp circuit (in Fig. 6) and the work of ESD detection circuit with and without STNMOS (in Fig. 2) at 25°C.

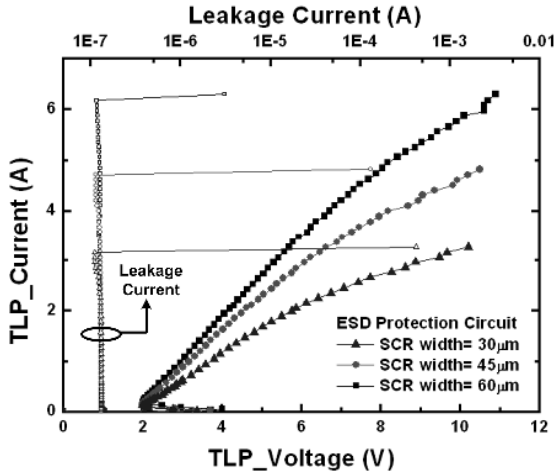

Fig. 10. The TLP-measured I-V characteristics of the 2×VDD-tolerant low-leakage ESD clamp circuit with SCR device of different widths under positive 2×VDD-to-VSS ESD stress.

The performance comparison between the prior work (Fig. 2) and the 2×VDD-tolerant low-leakage ESD clamp circuit (Fig. 6) is shown in Table V. With consideration of ESD robustness and standby leakage current, the 2×VDD-tolerant low-leakage ESD clamp circuit has provided an excellent ESD solution for mixed-voltage I/O interfaces in advanced nanoscale CMOS technologies.

TABLE IV
ESD ROBUSTNESS OF THE 2×VDD-TOLERANT LOW-LEAKAGE ESD CLAMP CIRCUIT WITH SCR OF DIFFERENT WIDTHS

SCR Width	It2	HBM ESD Level	MM ESD Level
30μm	3.15A	4.25kV	225V
45μm	4.71A	6.5kV	350V
60μm	6.17A	> 8kV	450V

TABLE V
COMPARISON BETWEEN THE PROPOSED 2×VDD-TOLERANT LOW-LEAKAGE ESD CLAMP CIRCUIT AND PRIOR WORK

	2×VDD-Tolerant ESD Clamp Circuit		
	Without consideration of gate current (Fig. 2)		With consideration of gate current (Fig. 6)
	ESD detection circuit only	With STNMOS W = 320μm L = 0.12μm	ESD detection circuit with SCR W_{SCR} = 45μm
Standby leakage current at 25°C	1.18μA	5.59μA	0.15μA
Standby leakage current at 125°C	12.6μA	66.6μA	1.71μA
HBM ESD Level	n/a	4kV	6.5kV
MM ESD Level	n/a	250V	350V

D. Design of 1×VDD Low-Leakage ESD Clamp Circuit

The design concept of low-leakage ESD detection circuit can be applied to power-rail ESD clamp circuit between VDD and VSS. The modified low-leakage power-rail ESD clamp circuit with only 1×VDD thin gate-oxide devices is shown in Fig. 11. While implementing in a 1-V 65-nm CMOS process, the node c in Fig. 11 is initially biased at some voltage level (~0.45V) to turn on Mn and then to keep the trigger node grounded. The diode-connected Mp2 and Mp3 conduct the gate current of Mc1 to bias the nodes c, d, and e. After that, the voltage level at the node d will be biased at some voltage level (~0.7V) to reduce the voltage drop across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors (Mc1 and Mc2). Without using a feedback network to reduce the device dimension of MOS capacitor, the low-leakage power-rail ESD clamp circuit can achieve high enough ESD robustness in a small layout area with a lower standby leakage current to efficiently protect the core logics with 1×VDD power supply against ESD stresses in nanoscale CMOS technologies.

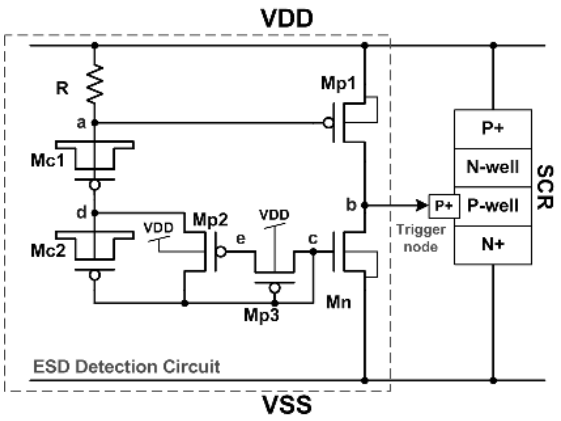

Fig. 11. The low-leakage power-rail ESD clamp circuit designed for ESD protection between VDD and VSS.

V. Conclusion

The challenges of ESD protection designs for mixed-voltage I/O buffers and design consideration of gate leakage current in nanoscale CMOS technologies have been presented. The ESD protection scheme with ESD bus and high-voltage-tolerant power-rail ESD clamp circuit is recommended to protect the mixed-voltage I/O buffers. The high-voltage-tolerant power-rail ESD clamp circuit needs to meet the gate-oxide reliability constraints without suffering the undesired standby leakage current during the normal circuit operating condition. To solve the gate leakage current issue, the design of 2×VDD-tolerant power-rail ESD clamp circuit with lower standby leakage current, no gate-oxide reliability issue, and high robust ESD level has been successfully verified in a 65-nm CMOS process. The proposed 2×VDD-tolerant low-leakage ESD clamp circuit is an excellent circuit solution for on-chip ESD protection design for mixed-voltage I/O buffers in the nanoscale CMOS technologies.

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