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Circuit theory of power factor correction in switching converters

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SUMMARY

This paper discusses the circuit theory aspects of power factor correction in switching converter circuits. The discussion begins with an examination of the requirement of power factor correction in dc/dc converters. Using the concept of zero-order converter circuits, sufficient conditions for a dc/dc converter circuit to provide power factor correction are derived. The duality principle is applied to generate new converter circuits that can achieve power factor correction. The practical application of power factor correction is considered in conjunction with the requirement of tight output voltage regulation. Detailed study of the circuit configuration that can simultaneously provide power factor correction and output regulation is given. Based on a general three-port model, the voltage regulator with power factor correction capability is studied in terms of the power flow between the input port, output port and energy storage port. A detailed consideration of the power flow among the three ports leads to the derivation of all possible minimal configurations that can achieve power factor correction and voltage regulation. The efficiencies of these minimal configurations are studied theoretically, leading to the concept of 'reduced redundant power processing' which provides important clue to efficiency improvement. Another issue addressed in this paper is the synthesis of practical circuits that can provide power factor correction and output regulation. In particular, four practical minimal configurations that achieve reduced redundant power processing are considered. A systematic synthesis procedure is derived for creating converter circuits that achieve power factor correction and output voltage regulation. The control issue is also investigated in depth, pinpointing the basic requirement on the number of control parameters needed and its relationship with the operating mode. Copyright © 2003 John Wiley & Sons, Ltd.

KEY WORDS: power factor correction; switching converters; power flow; efficiency; circuit synthesis

1. INTRODUCTION

Traditional linear-type power regulators have largely given way to switching power supplies which are more efficient and less bulky. However, switching power supplies, due to their non-linear operation, cause substantial harmonic distortion to the line current and emit electromagnetic noise via conduction and radiation, interfering the operations of nearby equipments. Recently, the term *power quality* has been introduced to describe the overall level of

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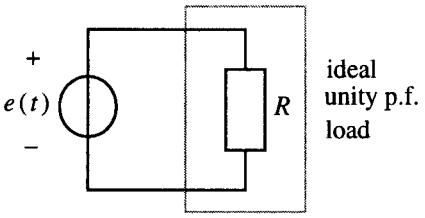

Figure 1. Ideal unity power factor load.

satisfaction of power supplies and systems in such areas of performance as harmonic distortion and electromagnetic interference. In many countries, in order to ensure a sufficiently high quality of power supplies, design standards have been tightened to restrict the level of harmonic distortion. A useful measure of the power quality is the *power factor* (p.f.), which is defined as the ratio of the real power to the apparent power [1], i.e.

$$\text{p.f.} = \frac{P_{\text{in}}}{E_{\text{rms}} I_{\text{rms}}} \tag{1}$$

where P_{in} is the input real power, E_{rms} is the root-mean-square (rms) input voltage and I_{rms} is the rms input current. Two factors affect the power factor. First, if the input voltage and current are not in phase, P_{in} will be less than the product of E_{rms} and I_{rms}, leading to a low power factor. The worst case corresponds to a 90° phase shift between E_{rms} and I_{rms}. Second, if the current contains a high harmonic content, I_{rms} becomes large, again leading to a low power factor. Mathematically we can express the power factor as the product of a displacement factor and a distortion factor [2], i.e.

$$\text{p.f.} = \underbrace{\cos\phi}_{\text{displacement factor}} \times \underbrace{\sqrt{\frac{1}{1 + (I_2/I_1)^2 + (I_3/I_1)^2 + \cdots}}}_{\text{distortion factor}} = \frac{\cos\phi}{\sqrt{1 + \text{THD}^2}} \tag{2}$$

where ϕ is the phase difference between the fundamental input voltage and current, I_i is the rms ith harmonic input current, and THD is the total harmonic distortion.

Theoretically, unity power factor, in the case of a simple one-port network, requires that the phase shift between the voltage and the current be zero, and that the current be free from harmonic distortion. In circuit terms, these requirements call for an input impedance resembling a linear resistor, i.e. a zero-order linear one-port, as shown in Figure 1. Although quite a number of switching circuits are already being used in practical power factor correction (PFC), they are scattered in the literature as isolated cases of innovative circuit designs [3–5]. Moreover, little formal work has been reported on the basic topological requirements of these circuits that can shed light on the creation of new PFC topologies. In the first part of this paper we attempt to derive sufficient conditions for which a switching network has a zero-order input impedance. We will also examine some simple zero-order networks that form the basis of a range of PFC circuits being used in practical power supplies. To illustrate the usefulness of the theory, we derive some 'new' possibilities for PFC, by application of duality, which are rarely known to the power electronics engineers.

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In practice, power supplies are required to regulate output voltage. This basic requirement is often combined with the requirement of PFC. This issue is formally studied in this paper, beginning with a simple viewpoint based on the flow of power from the input to the output. Since the instantaneous input power is not the same as the output power, instantaneous power surplus and deficit has to be stored in an energy storage element. This leads to a three-port model, from which we derive the minimal circuit configurations that achieve simultaneously PFC and output regulation. A main result of this paper shows that 16 minimal configurations, each consisting of two basic switching converters, are possible. We compare these configurations in terms of their theoretical efficiency. The comparison of efficiency leads to the concept of *reduced redundant power processing* (R^2P^2), which is useful for designing efficient power supplies that provide PFC and output regulation.

Another issue addressed in this paper is the synthesis of practical circuits. Among the minimal configurations, we select four particular configurations which enjoy *reduced redundant power processing,* and for which isolation can be easily achieved. Specifically we develop a systematic synthesis procedure for creating new efficient switching converter circuits that can achieve PFC and voltage regulation. Finally, we present a comparative study of control requirements which provides important insights into the choice of control parameters and its relationship with the operating mode.

2. ZERO-ORDER SWITCHING CONVERTER CIRCUITS

Before embarking on a discussion of PFC, the concept of energy storage elements has to be renewed. Specifically, when a capacitor (inductor) forms a loop (cutset) periodically with closed (open) switches, it stores zero energy over one complete switching period. However, within a switching period, it does store energy. Thus, it has no energy storage capability in the low-frequency sense, but remains as a reactive element at switching frequency or higher. As will become apparent, zero-order input impedance is required at low frequencies for PFC. Hence, we may exploit the periodically closed capacitors or opened inductors to create circuits that give zero-order input impedance for low-frequency operations. It should be borne in mind that high-frequency components (near and above switching frequency) are usually removed by filtering, and the main concern is the low-frequency behaviour. The essential tool that allows us to focus on the low-frequency behaviour is the averaging principle [6], of which we will make free use throughout the paper.

Switching power converters in general consist of linear inductors, capacitors and ideal switches. The input is typically a voltage source and the output a parallel combination of a capacitor and a load resistor. We now begin with the definitions of topological arrangements that prevent capacitors and inductors from behaving as low-frequency storage elements.

Definition 1

A zero-order switching inductor (L^0) is an inductor which forms a cutset periodically with only open switch(es) and/or current source(s).

Definition 2

A zero-order switching capacitor (C^0) is a capacitor which forms a loop periodically with only closed switch(es) and/or voltage source(s).

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Having defined these important elements, we may now formally state our first result concerning the topological requirement of a zero-order network. To avoid confusion, we should stress that a zero-order network does not in general imply a zero-order input impedance, the latter being a subject yet to be examined.

Theorem 1
Suppose all capacitors have finite current and all inductors have finite voltage. A switching converter circuit is zero order if it is composed of only zero-order switching inductors, zero-order switching capacitors, and switches.

Proof
Since, from the hypothesis, each inductor forms a cutset periodically with open switches and/or current sources, its current is fixed periodically by KCL. Likewise, KVL fixes each capacitor voltage periodically. □

The simplest zero-order switching converter consists of one inductor and two switches. The reason for choosing the inductor (instead of the capacitor) is that the input is a voltage source and the output is a capacitor, both of which can only be switched abruptly onto an inductor (not capacitor). At least two complementary on-off switches are needed because inductor cannot be left open while current is flowing. This leads to three possible topologies which happen to be the well-known buck, buck–boost and boost converters. From Theorem 1, the inductor is required to be an L^0. Hence, there must exist a sub-interval in a period for which a cutset is formed exclusively of the inductor and the two open switches. This corresponds to the well-known discontinuous-mode operation.

3. NEAR-ZERO-ORDER INPUT IMPEDANCE AND POWER FACTOR CORRECTION

A well established approach to modelling switching converters is via averaging [6,7]. For example, the input current can be written as the average of the input current observed over one switching period.

$$I_{\text{in}} = \frac{1}{T}\int_0^T i_{\text{in}}(t)\,\mathrm{d}t \tag{3}$$

We are now ready to present the second result concerning the topological requirement of zero-order input impedance.

3.1. Topological requirements

Theorem 2
The input impedance of a zero-order switching converter as represented in Figure 2 is of zero order if no loop is formed that contains both the input port and the output port for the entire switching period.

Proof
Observe that if there exists no loop containing two branches, b_1 and b_2, of a graph, then the two branches are contained separately in two *disconnected* sub-graphs or in two *separable*

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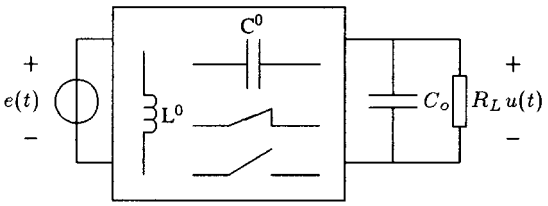

Figure 2. Zero-order switching converter.

sub-graphs [8]. In particular the current in b_1 and the voltage of b_2 will be independent of each other. Now consider the circuit of Figure 2. We observe that only the output port voltage involves a storage element. Therefore, the averaged input current in the sense of (3) will not contain a time-derivative term if the hypothesis is true. □

Corollary 1
The buck–boost converter operating in discontinuous mode has a zero-order (i.e. resistive) input impedance. Moreover, both the buck converter and the boost converter operating in discontinuous mode do not have a zero-order impedance.

Proof
By inspection of all three constituent linear networks corresponding to the three switch states of the buck–boost converter, there exists no loop that contains both the input port and the output port (see Figure 3). Moreover, for the buck and the boost converter, such a loop exists in at least one sub-interval of the switching period. The result follows directly from Theorem 2. □

3.2. Averaged models for zero-order impedance

Suppose there exists a loop that contains the input port and the output port during a sub-interval of the switching period. From basic circuit theory, any voltage or current in a circuit can be written as a function of the input source(s) and the state variable(s). In this case, I_{in} generally depends on both u and e, and if u is a dynamic variable, so is I_{in}. The average model, in general, is a non-linear controlled current source as shown in Figure 4(a). If the function $g(.)$ is separable to two terms, each dependent upon one port voltage only, then the model of Figure 4(b) is valid. Finally, the model reduces to that of Figure 4(c) for the case where $g(.)$ is independent of u.

For the case of the simple zero-order switching circuits, the input current is given by

$$I_{\text{in}} = \frac{1}{T}\left(\int_0^{dT} i_{\text{in}}(t)\,\mathrm{d}t + \int_{dT}^{d'T} i_{\text{in}}(t)\,\mathrm{d}t + \int_{d'T}^{T} i_{\text{in}}(t)\,\mathrm{d}t\right) \tag{4}$$

where $i_{\text{in}}(t)$ is a function of the input voltage and the output voltage. According to the waveform of the inductor current, we can write down the averaged input current for the three

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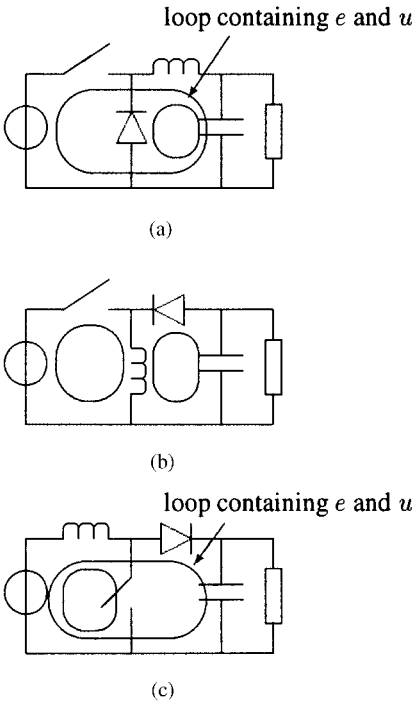

Figure 3. Corollary 1. (a) Buck converter has a loop that contains input port and output port; (b) Buck–boost converter has no such loops; (c) Boost converter has such a loop.

simple converter circuits as

Buck converter:

$$I_{\text{in}} = \frac{d^2 T}{2L}(e - u) \tag{5}$$

Buck–boost converter:

$$I_{\text{in}} = \frac{d^2 T}{2L} e \tag{6}$$

Boost converter:

$$I_{\text{in}} = \frac{d^2 T}{2L} \frac{ue}{u - e} \tag{7}$$

The circuit models for the input impedances are exactly as given in Figure 4, with (a) corresponding to the boost converter, (b) to the buck converter, and (c) to the buck–boost converter.

3.3. Application to power factor correction

It should be apparent that any switching converter would have PFC capability if its input impedance is resistive or near resistive. Furthermore, if the input resistance is linear, unity

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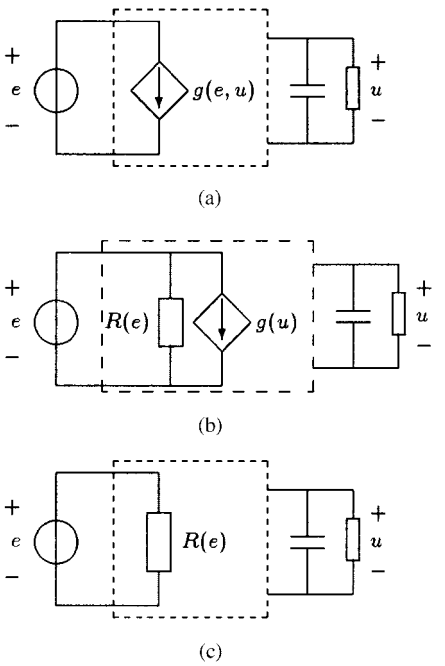

Figure 4. Averaged models of impedance. (a) General model; (b) Variable separable; (c) zero-order impedance (resistive). Dependence on d and T of all functions omitted for brevity.

power factor is expected. Thus, from Equation (6), the buck–boost converter operating in discontinuous mode is a perfect choice for PFC if d and T are constant, i.e.

$$R_{\text{in, buck-boost}} = \frac{2L}{d^2 T} \tag{8}$$

For the buck converter, we can see from Equation (5) that something close to a resistance can indeed be achieved.

$$Z_{\text{in, buck}} = \frac{2L}{d^2 T}\left(1 + \frac{u}{e} + \frac{u^2}{e^2} + \cdots\right) \tag{9}$$

$$\Rightarrow \quad R_{\text{in, buck}} \approx \frac{2L}{d^2 T} \quad \text{if } u \ll e \tag{10}$$

Likewise, the boost converter can serve as a PFC circuit though not as perfectly as the buck–boost converter. The equivalent resistance can be found as

$$Z_{\text{in, boost}} = \frac{2L}{d^2 T}\left(1 - \frac{e}{u}\right) \tag{11}$$

$$\Rightarrow \quad R_{\text{in, boost}} \approx \frac{2L}{d^2 T} \quad \text{if } u \gg e \tag{12}$$

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Use of the discontinuous-mode boost or buck converter for PFC is expectedly subject to distortion, as can be seen from Equations (9) and (11). (See Reference [4] for a general procedure for deriving the actual power factors and harmonic distortions.) Fortunately, it is possible to compensate for unity power factor in both the buck and the boost converter. Suppose the duty cycle is reserved for some mandatory control function, e.g. voltage regulation in the case of single-stage PFC regulators [3,4]. Then, the switching frequency becomes the only parameter that may be varied to obtain unity power factor. At this point, a legitimate question arises: Is it possible to derive a frequency control law that can achieve unity power factor? For the simple buck and boost converters, the answer is 'yes', since the form of Equations (9) and (11) clearly permits a closed form expression to be written for T in terms of e and u, assuming constant input resistance. Specifically, the control laws required for achieving unity power factor are

$$T = \frac{2L}{d^2 R_{\text{in}}} \left(1 + \frac{u}{e} + \mathcal{O}\left(\frac{u^2}{e^2}\right)\right) \tag{13}$$

for the buck converter, and

$$T = \frac{2L}{d^2 R_{\text{in}}} \left(1 - \frac{e}{u}\right) \tag{14}$$

for the boost converter, where R_{in} is a constant consistent with the output power. The above idea can be used to improve power factor for discontinuous-mode converters [9].

3.4. *Choice of topology for power factor correction*

Generally speaking, any of the basic converters operating in discontinuous mode can be chosen as a PFC stage, the buck–boost converter being the perfect choice as far as power factor is concerned. However, if we take into account the peak current stress and efficiency, the boost converter is more favourable. Firstly, the lower peak input current, as compared to the buck–boost converter delivering the same amount of power, is easily appreciated by inspecting the typical input current waveforms shown in Figures 5(a) and 5(b). Secondly, the efficiency of the buck–boost converter is usually lower. This is because the input is never coupled directly with the output, and energy is transferred to the load indirectly via circulating loops. Also, as seen from Equation (11), high power factor is possible for the discontinuous-mode boost converter if e/u is small. This means that the switching device must stand a high voltage during its off-state, implying a possible design tradeoff between power factor and voltage stress. As regards the buck converter, high power factor requires small u/e which implies small duty cycle values. The consequence is, however, unfavorably high peak current stress, as illustrated in Figure 5(c). We may now draw some interim conclusions based on the above discussion:

- The discontinuous-mode buck–boost converter represents a 'perfect' PFC stage, but is a less efficient topology.
- The discontinuous-mode boost converter can achieve very high power factor at the expense of high switching device voltage stress. It enjoys low peak current stress.
- The discontinuous-mode buck converter can achieve very high power factor with small duty-cycle values. It suffers high peak current stress.

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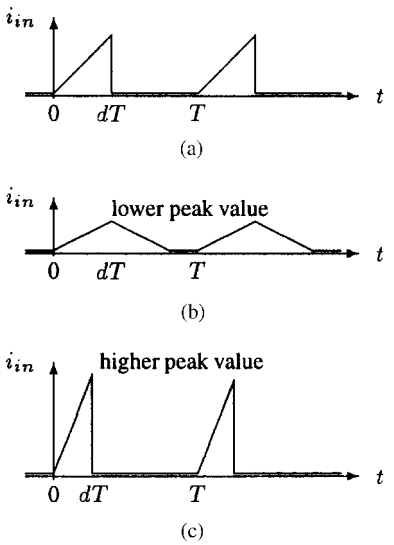

Figure 5. Input current waveforms comparison. (a) Buck–boost converter; (b) Boost converter (lower peak); (c) Buck converter (higher peak).

- The power factor of the discontinuous-mode buck and boost converters can be further improved by application of appropriate frequency control schemes.

4. EXTENSION TO HIGHER ORDER CONVERTERS

4.1. Generalization of Theorem 2

Zero-order switching converters that satisfy the hypothesis of Theorem 2 have a zero-order (resistive) input impedance, and hence are natural unity power factor circuits. Can a higher order switching converter also provide a zero-order input impedance under certain conditions? Intuitively speaking, if the input port 'sees' no reactive elements, zero-order input impedance can be maintained. To avoid confusion, we shall refer to an inductor as 'reactive inductor' if it is not an L^0, and to a capacitor as 'reactive capacitor' if it is not a C^0. Unlike L^0 and C^0 which are not storage elements below switching frequency, 'reactive inductors and capacitors' remain as storage elements at all frequencies.

Theorem 3
A general voltage switching converter has a zero-order input impedance if the input port does not form loops with any reactive inductor, reactive capacitor, or the output port.

Proof
The same argument as in the proof of Theorem 2 applies here. The hypothesis implies that the input port branch is, in any sub-interval of time, disconnected from all reactive elements. Thus, the input of the converter is resistive. □

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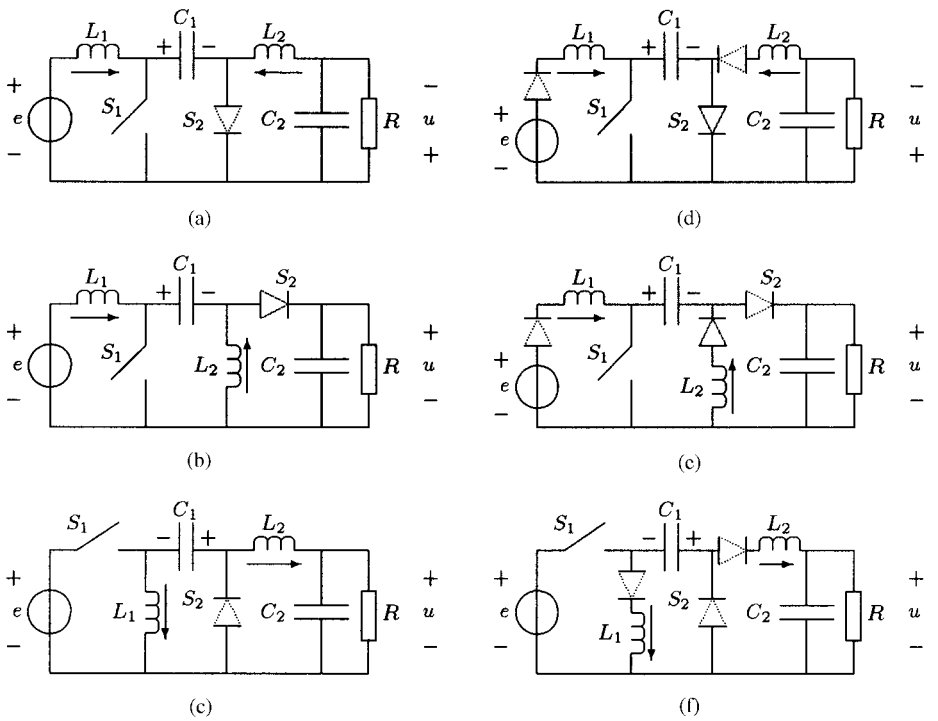

Figure 6. Higher order converters. (a) Ćuk converter; (b) SEPIC converter; (c) Zeta converter; (d)–(f) Converters with additional diodes to create L^0.

The hypothesis of the above theorem essentially means that the input is only allowed to be directly connected to zero-order elements such as L^0 and C^0. The classic example is the buck–boost converter, in which the on-time circulating loop contains the input and an L^0, and the off-time circulating loop contains the L^0 and the reactive output port, the two loops being non-overlapping in time. In higher order converters, however, the presence of reactive elements play important roles in the energy conversion process. As we shall see later, energy storage capability remains a key property of single-stage PFC regulators. Although one can design to avoid connecting the input with any reactive element by introducing more circulating loops that transfer energy sequentially within a period, the price is poor efficiency. Thus, direct connection between input and reactive elements is often inevitable. The following sub-sections consider some common examples.

4.2. The discontinuous-mode Ćuk, SEPIC and Zeta converters

The Ćuk, SEPIC and Zeta converters are shown in Figures 6(a)–(c). Here, unlike in simple converters, the discontinuous-mode operation does not make the inductors behave as L^0. In fact, as shown in Figure 7(a) the inductor currents do not necessarily touch the zero level although their sum is periodically zero. So, they are still 'free to vary' (hence not L^0) although their combined dynamics is reduced to first order.

The derivation of the expression for the averaged input current is complicated by the variable diode conduction time. (See Reference [7] for full details.) Moreover, we know that

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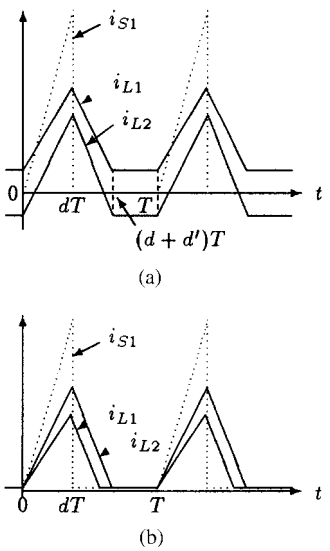

Figure 7. Inductor currents in Ćuk, SEPIC and Zeta converters operating in discontinuous mode, (a) without, and (b) with additional diodes in series with inductors.

the input impedance is not zero-order because the inductors are not L^0. But high power factor is still possible if the inductor dynamics is negligible.

4.3. Power factor correction by Ćuk, SEPIC and Zeta converters

Suppose we can make the inductors, in the Ćuk, SEPIC and Zeta Converters, behave as L^0. The circuits can then be viewed as some cascade combination of the basic converters in discontinuous mode. This can be accomplished by inserting a diode in series with each inductor, as in Figures 6(d)–(f). Under such conditions, the inductors are L^0 as illustrated in Figure 7(b). Clearly, the kind of discontinuous-mode operation differs fundamentally from that described in the previous sub-section when series diodes are not present. Note that it is also possible for i_{L_2} to assume continuous-mode operation while keeping i_{L_1} discontinuous. We shall deal with this case later in the paper.

We now focus on the Ćuk, SEPIC and Zeta converters of Figures 6(d)–(f) operating with both inductors being L^0 (as in Figure 7(b)). First, the Ćuk converter's input current is similar to the boost converter's, and can be derived by replacing u with v_{C1} in (7):

$$I_{\text{in, Ćuk}} = \frac{d^2T}{2L_1}\left(\frac{e}{1-(e/v_{C1})}\right) \tag{15}$$

The input resistance is

$$R_{\text{in, Ćuk}} = \frac{2L_1}{d^2T}\left(1-\frac{e}{v_{C1}}\right) \tag{16}$$

$$\approx \frac{2L_1}{d^2T} \quad \text{if} \quad \left|\frac{e}{v_{C1}}\right| \ll 1 \tag{17}$$

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Thus, the Ćuk converter under the specified operating mode can provide PFC if $|e/v_{C1}|$ is small. This again implies a possible tradeoff between voltage stress and power factor.

In a likewise fashion, we can derive, for the SEPIC converter under the specified operating mode, the input current by replacing u with $v_{C1}+u$ in (7), i.e.

$$I_{\text{in, SEPIC}} = \frac{d^2T}{2L_1}\left(\frac{e}{1-\dfrac{e}{v_{C1}+u}}\right) \tag{18}$$

Hence, we have the input resistance as

$$R_{\text{in, SEPIC}} = \frac{2L_1}{d^2T}\left(1-\frac{e}{v_{C1}+u}\right) \tag{19}$$

$$\approx \frac{2L_1}{d^2T} \quad \text{if} \quad \left|\frac{e}{v_{C1}+u}\right| \ll 1 \tag{20}$$

Thus, the SEPIC converter can provide PFC if $|e/(v_{C1}+u)|$ is small. Compared to the Ćuk converter, the SEPIC converter seems to suffer less voltage stress since the fact that $u>0$ tends to improve the approximation given in Equation (20).

For the Zeta converter, the input current when S_1 conducts is the sum of the two inductor currents, and is zero when S_1 is switched off. Thus, the averaged input current, in the specified operating mode, is

$$I_{\text{in, Zeta}} = \frac{d^2T(L_1+L_2)e}{2L_1L_2}\left(1+\frac{L_1}{L_1+L_2}\frac{v_{C1}-u}{e}\right) \tag{21}$$

The input resistance is

$$R_{\text{in, Zeta}} = \frac{2L_1L_2}{d^2T(L_1+L_2)}\left[1-\frac{L_1}{L_1+L_2}\frac{v_{C1}-u}{e}+\mathcal{O}\left(\left(\frac{L_1}{L_1+L_2}\frac{v_{C1}-u}{e}\right)^2\right)\right] \tag{22}$$

$$\approx \frac{2L_1L_2}{d^2T(L_1+L_2)} \quad \text{if} \quad \left|\frac{L_1(v_{C1}-u)}{(L_1+L_2)e}\right| \ll 1 \tag{23}$$

Here, high power factor requires that the magnitude of $L_1(v_{C1}-u)/(L_1+L_2)e$ be small. This remains a fairly weak condition since the factor $L_1/(L_1+L_2)$ further reduces the magnitude of $(v_{C1}-u)/e$.

Remark

As mentioned before, it is possible that L_2 operates in continuous mode while L_1 in discontinuous mode. This situation may or may not affect the PFC property depending upon the topology. For the Ćuk and SEPIC converters, the input current is actually i_{L1} which is independent of i_{L2}. As long as L_1 remains in discontinuous mode (Figure 7(b)), the input is still

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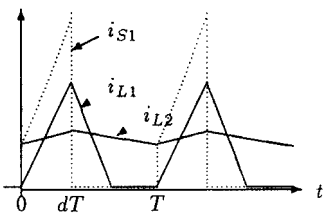

Figure 8. Current waveforms with L_2 in continuous mode. $i_{\text{in}} = i_{L1}$ for Ćuk and SEPIC. $i_{\text{in}} = i_{S1}$ for Zeta.

nearly resistive. However, for the Zeta converter, operating L_2 in continuous mode will affect the input current as shown in Figure 8. Specifically, during the interval when S_1 is on, the input port is connected to L_2 which is not an L^0. Thus, from Theorem 3, the Zeta converter must lose its PFC capability.

5. POWER FACTOR CORRECTION BY CURRENT PROGRAMMING—A BRUTE FORCE APPROACH

It should be noted that the foregoing basically exploits the discontinuous-mode operation to provide near zero-order input impedance for PFC. The obvious advantage is simplicity since no additional control is needed. However, the use of discontinuous-mode operation for power factor correction does not exhaust all possibilities of providing zero-order input impedance. Clearly, the foregoing study pinpoints an important requirement for PFC which is the destruction of the dynamics of the inductor [11]. In fact, if active control is allowed, it is theoretically possible to destroy the inductor dynamics by forcing its current to follow some desired wave shape. Thus, even when the converter operates in continuous mode, power factor correction is possible through active current programming. Commercial IC controllers are available for this purpose. Typically, the inductor current is forced to follow the input voltage wave shape in an appropriate magnitude for power balance. An example is shown in Figure 9.

6. DERIVATION OF NEW TOPOLOGIES BY THE DUALITY PRINCIPLE

Much has been said about zero-order switching converters which are based on zero-order switching inductors, L^0. Would it be possible to develop new topologies based on zero-order switching capacitors, C^0? This section examines such possibilities.

6.1. Near zero-order switching converters based on zero-order switching capacitors

A short-cut to the design of C^0-based PFC circuits is via duality transformation. Figure 10 shows the duals of the basic converter circuits. Note that duality effectively reverses the switch state, i.e. 'on' becomes 'off', and *vice versa*. Therefore, if we employ the same definition for duty cycle (percentage of time duration when active switch is on), the discontinuous-mode

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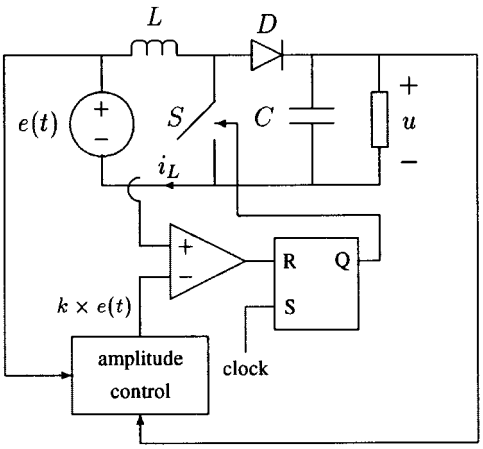

Figure 9. Active current programming to achieve PFC in continuous-mode operation.

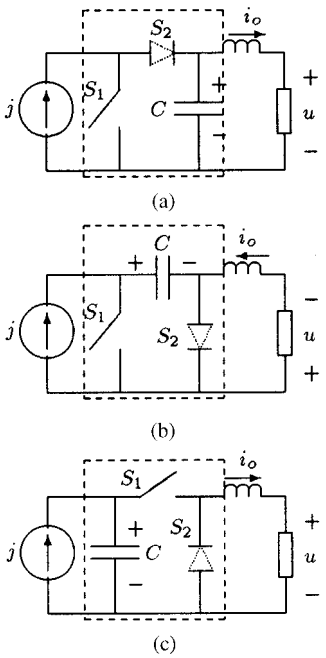

Figure 10. Zero-order and near zero-order switching converters based on C^0. Direct duals of (a) buck, (b) buck–boost, and (c) boost converters.

operation is characterised by zero capacitor voltage during a portion of the on-time as shown in Figure 11. Since the capacitor C forms a loop periodically with closed switches, it qualifies as a C^0. From Theorem 1, the converters are zero-order switching converters.

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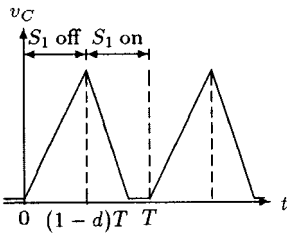

Figure 11. Capacitor voltage waveform for circuits of Figure 10.

Duality allows us to obtain the low-frequency input resistance for the circuits of Figure 10 by interchanging current and voltage, resistance and conductance, capacitance and inductance, d and $(1-d)$, etc., in previously derived expressions for the buck, buck–boost and boost converters. Specifically, from (9), (8) and (11), the input conductances of the circuits of Figure 10, in the averaged sense, are given by

$$G_{\text{in, dual-buck}} = \frac{2C}{(1-d)^2 T}\left(1 + \frac{i_o}{j} + \frac{i_o^2}{j^2} + \cdots\right) \tag{24}$$

$$G_{\text{in, dual-buck-boost}} = \frac{2C}{(1-d)^2 T} \tag{25}$$

$$G_{\text{in, dual-boost}} = \frac{2C}{(1-d)^2 T}\left(1 - \frac{j}{i_o}\right) \tag{26}$$

where j and i_o are the input and output currents of the dual converters. Finally, for the sake of conciseness, we state that all conclusions drawn in Section 5 are valid here, provided the appropriate duality translations are made for the involving quantities.

6.2. Justification of the current source assumption

Although the dual converters (Figure 10) inherit the PFC property, their suitability for practical applications is questionable because mains inputs are seldom current sources, and regulated voltage is normally required of the output. Thus, the dual circuits necessitate modification in two respects, namely, inserting a 'substantial' inductor in the input and plugging a 'small' capacitor on the load as shown in Figure 12.

From duality, high power factor is maintained only at the input of the dual converter (i.e. dashed box shown in Figure 12). Thus, the input impedance seen by the voltage source e would have a series inductive component, implying a possible degradation in power factor due to the additional phase shift caused by the inductance. However, if the extent of phase shift is insignificant, these circuits may still be considered.

Since the current source j in the basic dual converters (Figure 10) is required to remain as a constant current source during a switching period, the rate of change of j should be an order of magnitude lower than the switching frequency. Now observe that $L_s/R_L T = \mathcal{O}(1)$ and $R_{\text{in}}/R_L = \mathcal{O}(1)$, where R_L represents the load resistance. In practice, the mains frequency

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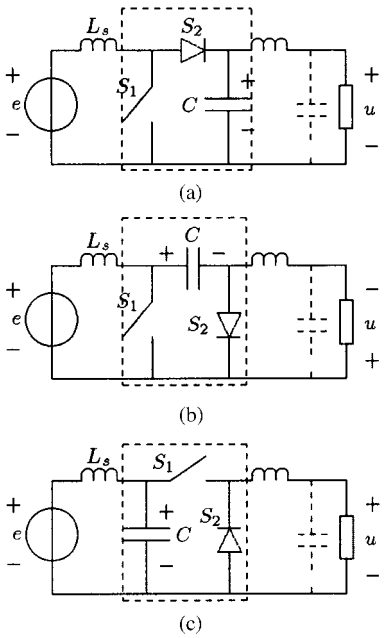

Figure 12. Modified dual converters for practical source and load. Capacitor C operates in discontinuous mode.

is several orders of magnitude below the switching frequency, i.e. $\mathcal{O}(f_m T) \ll 1$. Clearly, the phase shift ϕ caused by L_s is given by

$$\tan\phi = \frac{2\pi f_m L_s}{R_{\text{in}}} = \frac{2\pi f_m T(L_s/R_{\text{L}}T)}{R_{\text{in}}/R_{\text{L}}}$$
$$= \frac{2\pi\mathcal{O}(f_m T)\mathcal{O}(1)}{\mathcal{O}(1)} = 2\pi\mathcal{O}(f_m T) \ll 1 \tag{27}$$

Thus, we have $\phi \approx \tan\phi \ll 1$. In short, due to the wide separation of the mains frequency and the switching frequency, the reactance of L_s can be considered insignificant at the mains frequency, thus justifying the possible use of the dual converters in practical PFC applications.

7. SWITCHING REGULATORS WITH POWER FACTOR CORRECTION—CONVENTIONAL CASCADE CONFIGURATIONS

We now move on to consider the use of a PFC converter in practical situations where the output voltage is required to be tightly regulated. A straight-forward construction involves a simple zero-order switching network followed by a switching regulator [12–16]. Figure 13

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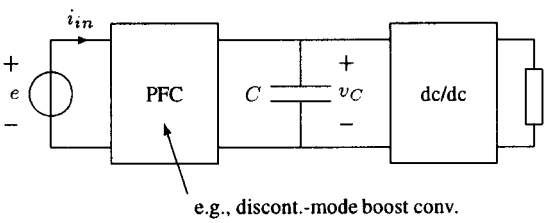

Figure 13. Block diagram of a two-converter PFC voltage regulator.

shows the block diagram of such a circuit. We will refer to this combined circuit as a *PFC voltage regulator.*

7.1. Energy balance consideration

In the following analysis we assume that the input voltage is a rectified sinusoid, the power factor is maintained unity, and the output voltage is constant. The instantaneous input power is $p_{\text{in}}(t) = \hat{e}\hat{i}_{\text{in}} \sin^2 2\pi f_m t$, where f_m is the mains frequency, usually 50 or 60 Hz. Letting P_o be the output power, we have $\hat{e}\hat{i}_{\text{in}} = 2P_o$. The power difference that must be buffered in the circuit is

$$p_c(t) = \hat{e}\hat{i}_{\text{in}} \sin^2 2\pi f_m t - P_o = -P_o \cos 4\pi f_m t \tag{28}$$

which varies at twice the mains frequency. In terms of energy storage, the circuit absorbs energy in a quarter mains cycle and releases the same amount in the next quarter cycle. The stored energy, $E(t)$, is given by

$$E(t) = -\frac{P_o}{4\pi f_m} \sin 4\pi f_m t + \text{const} \tag{29}$$

The amplitude (peak-to-peak) of the ac component of the energy stored, $|\Delta E_{\text{pp}}|$, is thus given by

$$|\Delta E_{\text{pp}}| = \frac{P_o}{4\pi f_m} \times 2 \tag{30}$$

In the circuit of Figure 13, the capacitor voltage that interfaces the two stages must fluctuate in order to provide the energy buffering action, i.e. $v_C = V_C + \Delta v_C$ where V_C is a static value and Δv_C varies at $2f_m$. Since the amplitude of energy stored in the capacitor is $\frac{1}{2}C(v^2_{C,\max} - v^2_{C,\min})$ or $CV_C|\Delta v_{C_{\text{pp}}}|$, we have, from Reference (30),

$$|\Delta v_{C_{\text{pp}}}| = \frac{P_o}{2\pi f_m C V_C} \tag{31}$$

where $|\Delta v_{C_{\text{pp}}}|$ is the peak-to-peak variation of v_C. We shall examine the merits of different converters in the light of this formula.

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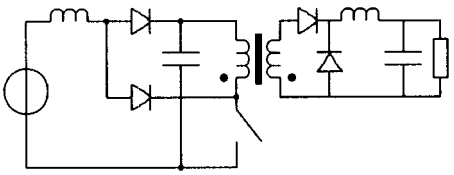

Figure 14. Cascade of a boost converter and a buck converter to form a single-stage PFC voltage regulator.

Table I. Some known single-stage PFC voltage regulators.

Basic combinations	Operating modes	Circuits
Boost + buck (Ćuk derived)	DM–CM	BIBRED (Reference [5])
Boost + buck (Ćuk derived)	DM–DM	SSIPP (ref. [3])
SEPIC derived	DM–CM	BIFRED (Reference [5])
Boost + flyback	DM–DM	SSIPP (Reference [3])

7.2. *Effects of topology choice on regulator design*

Small Δv_C implies that a small duty-cycle variation is sufficient for voltage regulation in the dc/dc converter that follows the PFC stage. Small Δv_C is a desirable feature because:

1. Small duty-cycle variation improves the dynamic range and widens the design headroom especially for applications involving a large input voltage range.
2. Wide duty-cycle variation can disrupt the PFC property since the equivalent input resistance is a function of d^2T.

From Equation (31), we observe that Δv_C can be made small if V_C is allowed to take a large value. Thus, we can appreciate that the boost (step-up) PFC converter can give small Δv_C and hence facilitate the design of the subsequent voltage regulator, while the buck (step-down) PFC converter is a poor choice since it gives large Δv_C.

7.3. *Single-stage PFC voltage regulators*

A common practice in the design of PFC voltage regulators is to combine the two converter stages as shown in Figure 13 to a single stage, especially for low-cost low-power applications. By definition, a single-stage converter employs only one driving signal for turning on and off a switch or a set of switches with a synchronized switching sequence [3–5]. An example is shown in Figure 14 which combines a boost and a buck converter. In theory, provided the front-end converter operates in discontinuous mode, PFC is naturally achieved by virtue of its near zero-order input impedance. Table I summarizes some previously reported configurations.

Our first observation concerns the static value V_C. Two cases can be distinguished: (i) the PFC stage is in discontinuous mode and the subsequent dc/dc converter in continuous mode (DM–CM); (ii) both stages are in discontinuous mode (DM–DM).

When operating in DM–DM, the single-stage converter has a fixed static V_C, for a given input voltage function and regulated output voltage, irrespective of the power level or

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loading condition. We sketch the proof as follows. The input and output currents of any basic discontinuous-mode converter, I_{DM}, invariably take the following form:

$$I_{DM} = d^2 T f(v_{in}, v_{out}) \tag{32}$$

where v_{in} and v_{out} are the input and output voltages of the converter, and $f(.)$ is usually a bilinear function. Thus, for the circuit of Figure 13, the current supplied by the PFC stage, $I_{o,PFC}$, and that demanded by the dc/dc converter stage, $I_{in,DC/DC}$, are given by $I_{o,PFC} = d^2 T f_1(e, v_C)$ and $I_{in,DC/DC} = d^2 T f_2(v_C, u)$. Also, the averaged current that flows in the storage capacitor over one mains cycle must equal zero, i.e.

$$\int_0^{1/f_m} d^2 T (f_1(e, v_C) - f_2(v_C, u))\, \mathrm{d}t = 0 \tag{33}$$

If $\Delta v_C / V_C$ is small and the output is well regulated at U, the duty cycle essentially remains constant. Thus, we may write

$$\int_0^{1/f_m} (f_1(e, V_C) - f_2(V_C, U))\, \mathrm{d}t = 0 \tag{34}$$

The above equation clearly suggests that V_C will be invariant under different loading conditions for a given set of e and U.

In contrast, *when the single-stage converter operates in DM–CM, the static capacitor voltage V_C varies according to the loading current.* We can prove this statement by contradiction. First, we assume that V_C is invariant under two different loading conditions which means that the duty cycle is the same for the two cases since the output remains regulated. From Reference (32), the input current is also invariant under the two loading conditions, which cannot be true. Thus, V_C is expected to take different values for different load currents.

Furthermore, in the case of DM–CM operation, the voltage stress V_C can be controlled by varying the switching frequency since the current charging the storage capacitor, $I_{o,PFC}$, is proportional to $d^2 T$. Thus, increasing the frequency can alleviate the voltage stress on the storage capacitor when the load current becomes small [10].

Our next observation concerns the effects of the choice of operating mode on voltage regulation. With only one switch or one set of switches controlling both PFC and dc/dc stages, the single-stage PFC regulator has the following interesting characteristics. (See Table II.)

1. For DM–DM operation, the use of frequency control for improving power factor can disrupt the voltage regulation because unity power factor is in conflict with the requirement of a constant $d^2 T$ for output voltage regulation.
2. Since the continuous-mode converter is not affected by variation of switching frequency, DM–CM operation allows frequency modulation to be used exclusively for improving power factor and duty-cycle modulation for voltage regulation.
3. For DM–CM operation, the switching frequency can be varied according to the loading condition to control the static voltage stress [10,17].

In Section 13 we will examine in detail the control requirements of a general circuit configuration of PFC voltage regulators. The above discussion can then be seen as specific cases of the more general control viewpoint to be discussed in Section 13.

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Table II. Comparison of operation modes in single-stage PFC voltage regulators.

Operation	V_C	Control
DM–DM	Fixed	d control for regulation; f control not feasible for p.f. improvement
DM–CM	V_C drops as load increases	d control for regulation; f control feasible for p.f. improvement and stress reduction.

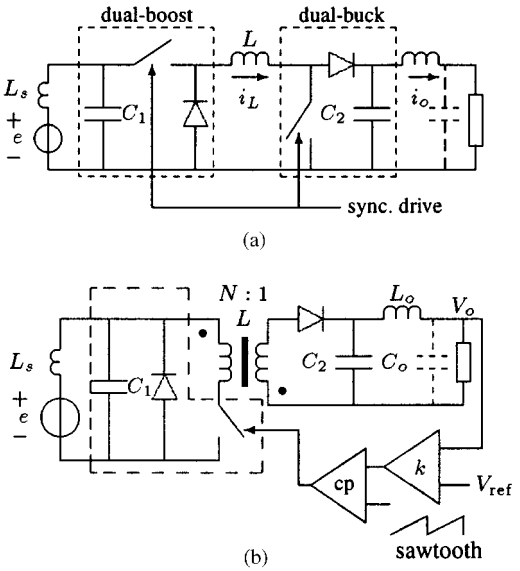

Figure 15. (a) Dual single-stage PFC voltage regulator with C_1 in discontinuous mode; switches are synchronized for single-stage operation; (b) isolated version.

7.4. An example of deriving new PFC voltage regulator by duality

Before we end our discussion on the cascade single-stage PFC voltage regulator, we illustrate the application of the duality principle to the synthesis of new PFC voltage regulators. Specifically, we take the dual of a PFC voltage regulator consisting of a boost and a buck converter. The result is shown in Figure 15(a). Note that in this dual circuit, the inductor L serves as the low-frequency storage element, whereas the capacitor C_1 is a C^0 providing PFC. Referring to Figure 15(a), the storage inductor L, in a dual fashion, maintains a continuous current which is larger in magnitude than the input current. The capacitor C_1 operates in discontinuous mode as shown previously in Figure 11. We refer the readers to Tse-Chow [18] for a detailed analysis of the single-switch isolated version shown in Figure 15(b).

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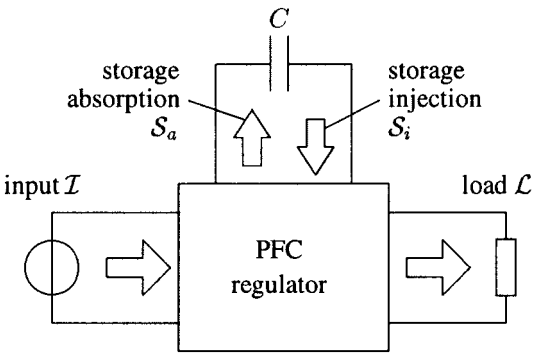

Figure 16. Three-port model of a PFC voltage regulator.

8. GENERAL CONFIGURATION OF PFC VOLTAGE REGULATORS

The requirements of PFC and output voltage regulation do not necessarily imply a cascade structure of two converters, such as the one discussed in the previous section. Such a choice enjoys simplicity of design, but from the efficiency viewpoint, cascade structures are undesirable because power has to be fully processed by two consecutive stages leading to a low overall efficiency.

In this section we discuss the general spatial arrangements of converters that can meet the dual requirement of PFC and tight output regulation. In Section 9 we introduce a *power flow graph* approach for deriving the possible PFC voltage regulator configurations, and in Section 11, we will proceed to synthesize actual converter circuits for selected structures which are of practical importance.

8.1. Three-port model

As discussed previously, the basic requirement of the *PFC voltage regulator* is the presence of an energy storage element which buffers the difference between the instantaneous input power and the output power. We can therefore regard the general configuration of a voltage regulator with PFC capability as a three-port network terminating in an input voltage, a low-frequency storage element and an output load, as shown in Figure 16. Within the three-port, high-frequency power flows occur as usual for switching converters. Here, we will focus on the low-frequency power flows into and out of the three-port network, and attempt to derive a general procedure for synthesizing minimal practical PFC voltage regulator circuits based on the use of only two basic converters. In Sections 10 and 13, the possible circuit configurations will be compared in terms of their efficiency and control requirements. A particularly illuminating result of this study is that efficient PFC voltage regulators can be constructed by selecting appropriate configurations that minimize redundant processing of power by the two constituent converters, as will be demonstrated in Section 10. Furthermore, the study of the control problem in Section 13 provides formal criteria in selecting control parameters and operating modes, and clarifies some previous misconceptions in the design of single-stage PFC voltage regulators.

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The storage needed for PFC is conveniently capacitive, though in theory inductive storage can also be employed under certain conditions [18]. Thus, the *three-port network* generally consists of a number of simple voltage-terminated converters, i.e. the simple buck, boost and buck–boost converters, which connect the input voltage, output load and capacitive storage.

8.2. Minimum number of converters needed

Suppose the input and the load allow energy to be transferred in only one direction, while the storage element allows a bi-directional energy flow, as indicated by the arrows in Figure 16. In this representation, power goes into the three-port network via the input port and the storage port, and power goes out via the load port and the storage port. Effectively we may treat the storage port as being composed of a power injection and a power absorption ports.

As a prelude to the subsequent analysis, we first address the complexity of the circuit construction that is required of a PFC voltage regulator. Specifically we wish to find the minimum number of simple converters that are needed to ensure the right amount of power buffered in the storage at any time.

Theorem 4
Assume that a simple converter has one input port and one output port. The minimum number of simple converters needed to construct a PFC voltage regulator is equal to two.

Proof
Observe that we need to control only two of the three ports of the PFC voltage regulator since the remaining port will automatically be controlled as a result of power conservation. Since each constituent converter is single-input–single-output, it is not possible for a converter to have full separate control of two or more power input (or output) ports of the PFC voltage regulator simultaneously. Furthermore, if two or more converters are used and each port is connected to at least one converter, then at least two of the ports will be fully controlled. □

8.3. Conceptual connections of converters

For ease of reference, we use $\mathscr{I}$, $\mathscr{L}$, $\mathscr{S}_a$ and $\mathscr{S}_i$ to denote, respectively, the power flow at the input port, load port, storage absorption and storage injection ports, as shown in Figure 16.

Suppose each constituent converter has one power input port and one power output port. Two basic rules govern the connection.

1. In order for the PFC voltage regulator to perform the necessary power buffering function, there must exist power conversion from $\mathscr{I}$ to $\mathscr{S}_a$ and from $\mathscr{S}_i$ to $\mathscr{L}$.
2. In order to ensure minimal number of power flow paths (so as to avoid redundant power processing), no converter should convert power from a port back to itself, i.e. input-to-input, storage-to-storage, and load-to-load conversions should be avoided.

Before we attempt to derive the possible connections, we observe that a converter can possibly connect its input or output to more than one power ports of the PFC voltage regulator. Figure 17 shows the three possibilities, regardless of the afore-mentioned connection rules. In general, we let n be the number of converters having any of these connections. We now

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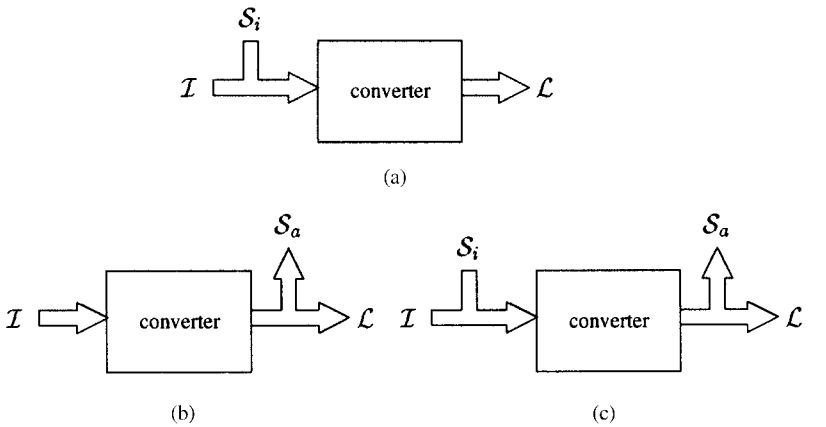

Figure 17. Three possible types of multiple connection to a converter. (a) Converter's input connected to two ports; (b) converter's output connected to two ports; (c) converter's input and output each connected to two ports.

sketch all possible connections of converters in a PFC voltage regulator as follows:

Case 1: $n=0$—Suppose we first connect $\mathscr{I}$ (or $\mathscr{S}_i$) to a converter's input port and $\mathscr{S}_a$ (or $\mathscr{L}$) to its output port. Then, we connect another converter to the remaining ports of the PFC voltage regulator. We may denote the possible connections as follows:

$$\text{(a)} \quad \begin{cases} \mathscr{I} \mapsto \mathscr{S}_a \\ \mathscr{S}_i \mapsto \mathscr{L} \end{cases} \tag{35}$$

$$\text{(b)} \quad \begin{cases} \mathscr{I} \mapsto \mathscr{L} \\ \mathscr{S}_i \mapsto \mathscr{S}_a \end{cases} \quad \text{(rejected)} \tag{36}$$

where '$\mapsto$' denotes power conversion through a converter, or precisely a mapping from a power flow to another power flow. Clearly, case 1b should be rejected as it violates the afore-mentioned connection rules.

Case 2: $n=1$—With no loss of generality we assume that when a power port is connected to two converters simultaneously, power is split in a ratio of k to $(1-k)$, where $0<k<1$. It is readily shown that the following connections satisfy the basic connection rules:

$$\text{(a)} \quad \begin{cases} k\mathscr{I} + \mathscr{S}_i \mapsto \mathscr{L} \\ (1-k)\mathscr{I} \mapsto \mathscr{S}_a \end{cases} \tag{37}$$

$$\text{(a)} \quad \begin{cases} \mathscr{I} \mapsto \mathscr{S}_a + k\mathscr{L} \\ \mathscr{S}_i \mapsto (1-k)\mathscr{L} \end{cases} \tag{38}$$

where '+' denotes algebraic addition. Other connections have been omitted since, like case 1b, they violate the connection rules. (Readers can verify this easily.)

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Case 3: $n=2$—We assume that input power is split in a ratio of k to $(1-k)$ when it is injected into two converters simultaneously, and that the output power is combined at a ratio of k' to $(1-k')$ from the outputs of two converters, where $0<k<1$ and $0<k'<1$. The only connection that does not violate the connection rules is

$$\begin{aligned} k\mathscr{I} &\mapsto \mathscr{S}_a + k'\mathscr{L} \\ (1-k)\mathscr{I} + \mathscr{S}_i &\mapsto (1-k')\mathscr{L} \end{aligned} \tag{39}$$

Thus, we may conclude that any PFC voltage regulator as represented by the three-port network of Figure 16 can be constructed by a minimum of two simple converters, and that four possible types of connections are available, as illustrated above by cases 1a, 2a, 2b and 3. In Section 9, we will discuss a systematic procedure for deriving all possible minimal circuit configurations that fulfill the dual requirement of PFC and voltage regulation.

8.4. Low- versus high-frequency power flows

As mentioned previously it is important to differentiate between *low-frequency power flow* and *high-frequency power flow*. Within a converter, power flow occurs at the switching frequency which is typically several orders of magnitude above the mains frequency. This high-frequency (switching frequency) power flow is controlled, usually through duty cycle or frequency modulation, to result in a certain overall low-frequency power flow function that is required by the design specification. Thus, the power flows into and out of the three-port model are all low-frequency. A simple formulation of the power flow through a converter is as follows. First, we assume that any converter can be controlled through variation of one or more parameters (typically duty cycle and switching frequency), and that such control affects the low-frequency behaviour of the converter. For the sake of theoretical consideration, we let $\xi(t)$ and $\psi(t)$ be the control parameters of a switching converter. Suppose the low-frequency power flow P through a given converter for given input and output conditions is

$$P|_{v_i(t),v_o(t)} = F(\xi(t),\psi(t)) \tag{40}$$

which is dictated by the circuit topology. Also, suppose the required low-frequency power flow function is $f(t)$. For example, for a PFC converter, $f(t)$ takes the form of

$$f(t) = 2P_o \sin^2 2\pi f_m t \tag{41}$$

and for a voltage regulator, it is given by

$$f(t) = P_o \tag{42}$$

where P_o is the output power level. The usual control problem is to find $\xi(t)$ and $\psi(t)$ such that the power flow through the converter fulfills the requirement, i.e.

$$F(\xi(t),\psi(t)) = f(t) \tag{43}$$

It should be stressed that since PFC is a low-frequency requirement, $F(.)$ is a low-frequency function in the steady state when it is controlled to satisfy the PFC requirement. We will use this theoretical formulation in Section 13 to consider the formal control requirement of a PFC voltage regulator.

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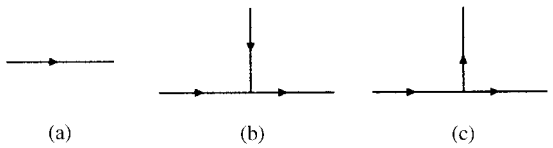

Figure 18. Power flow sub-graphs. (a) Type I; (b) Type II; (c) Type III.

9. CONFIGURATIONS OF PFC VOLTAGE REGULATORS BASED ON POWER FLOW GRAPHS

Since the primary objective of a PFC voltage regulator is to transfer power from the input port to the load port with low-frequency buffering in the storage element, we begin with the basic process of power flow between the three ports of a PFC voltage regulator.

9.1. Power flow sub-graphs

We introduce, for ease of presentation, *power flow graphs* for describing the way in which power is transferred among the three ports. The branches in a power flow graph denote the paths through which power is being transferred, and the arrows on the branches indicate the direction of power flow. One or more branches form a *power flow sub-graph,* or simply *sub-graph.* For a three-port network, it is clear that only three types of sub-graphs can be used to connect the ports:
Type I: Power is transferred from one port to another port (Figure 18(a)).
Type II: Power is transferred from two ports to one port (Figure 18(b)).
Type III: Power is transferred from one port to two ports (Figure 18(c)).

Remark
The power flow sub-graph is introduced here as an alternative and convenient tool for classifying the possible types of power flow scenarios. In fact, as we will see, the above Type I, Type II and Type III sub-graphs are closely related to the connection cases studied previously in Section 8.3.

9.2. Power flow graphs

Now we can construct the complete power flow graph for a PFC voltage regulator using the three types of sub-graphs of Figure 18. Clearly, there are only four possible constructions, each comprising two sub-graphs. For ease of reference, we denote the complete power flow graph by Type I-I if it involves two Type I sub-graphs. For a power flow graph that involves one Type I sub-graph and one Type II sub-graph, we refer to it as Type I-II. Likewise, we also have Type I-III and Type II-III power flow graphs, as shown in Figure 19.

Now, a moment's reflection will convince us that these power flow graphs effectively represent the connection cases 1a, 2a, 2b and 3 of Section 11. The use of power flow graphs provides a more systematic solution to the classification problem.

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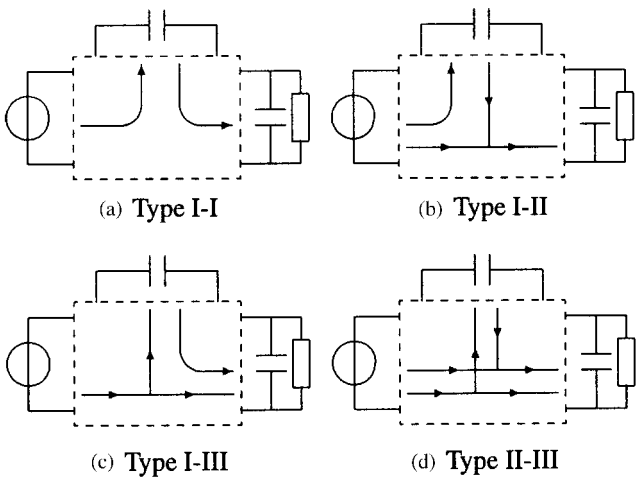

Figure 19. Power flow graphs for PFC voltage regulators. (a) Type I-I; (b) Type I-II; (c) Type I-III; (d) Type II-III.

Table III. Previously reported PFC voltage regulator circuits.

PFC voltage regulator circuit	Configuration
Ćuk, SSIPP [3], BIBRED [5]	I-I
Zeta	I-IIA
SEPIC, BIFRED [5]	I-IIIB
PPFC [14]	I-IIIB
García circuit [19]	I-IIIB

9.3. Minimal configurations of PFC voltage regulators

Finally, since the minimal configuration requires two simple converters, we complete the derivation by putting two converters in the appropriate paths of the power flow graph. In particular we consider putting one converter to each sub-graph in order to take full control of power flow to and/or from each port. Also, for each Type II and Type III sub-graph, we have three possible ways of placing a converter. Hence, 16 *configurations of PFC voltage regulators are possible.* For simplicity, we denote them as Configuration I-I, Configuration I-IIA, Configuration I-IIB, Configuration I-IIC, Configuration I-IIIA, Configuration I-IIIB, Configuration I-IIIC, etc., as shown in Figure 20.

In the past, innovative circuits have been proposed for PFC voltage regulators. Table III shows some previously reported circuits and the types of configuration they belong. It should be noted that among the 16 configurations, only a few have been chosen for practical implementation, and the others are rarely known. Although one can develop practical circuits from any of these configurations (see Section 11 for a synthesis method), the ease of practical implementation often dictates the usefulness of a particular configuration. For instance, as far as isolation is concerned, types I-I, I-IIA, I-IIB, I-IIIA and I-IIIB are more well

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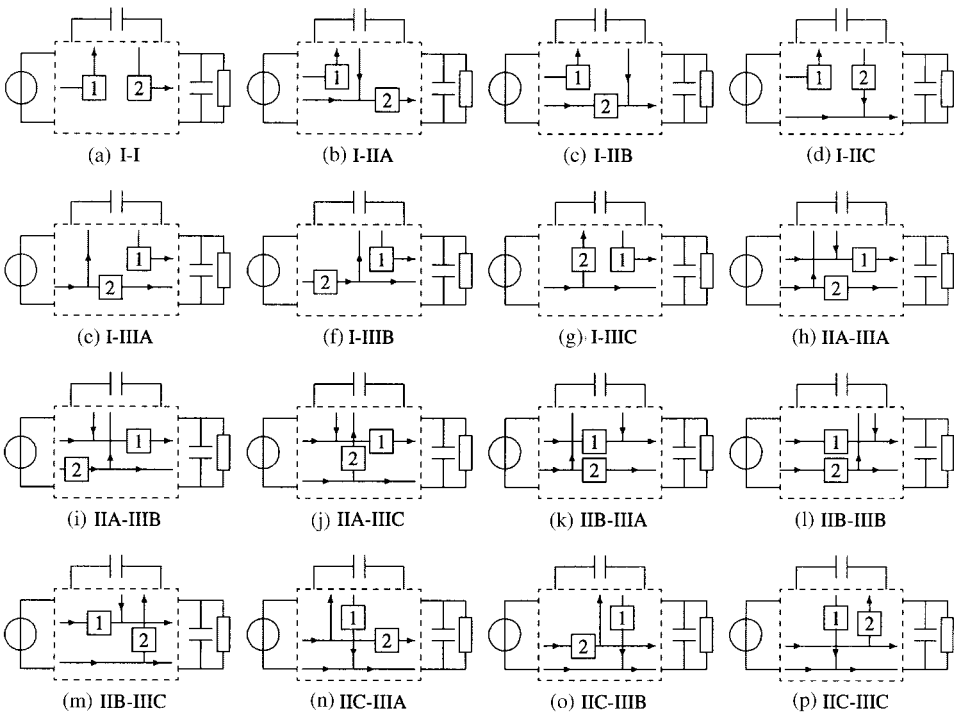

Figure 20. Configurations of PFC voltage regulators in terms of power flow. Solid square boxes denote simple converters.

suited for practical implementation than the other types, as will be discussed in depth in Section 11.

10. COMPARISON OF EFFICIENCY

Intuitively, the cascade configuration, i.e. Configuration I-I, has a poor efficiency since the input power is processed by the two converters 'serially' before reaching the load. If η_1 and η_2 are the efficiencies of the two converters, the overall efficiency of Configuration I-I is given by

$$\eta_{\text{I-I}} = \eta_1 \eta_2 \tag{44}$$

For Configuration I-IIA, the efficiency is expected to be higher than $\eta_1\eta_2$ since part of the input power goes through only one converter stage. Suppose the input power is split, in a ratio of k to $1-k$, into converters 1 and 2, as shown in Figure 20(b). The efficiency in this case is

$$\begin{aligned} \eta_{\text{I-IIA}} &= k\eta_1\eta_2 + (1-k)\eta_2 \\ &= \eta_1\eta_2 + (1-k)\eta_1(1-\eta_2) \\ &> \eta_1\eta_2 \quad \text{for all } 0<k<1 \end{aligned} \tag{45}$$

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For Configuration I-IIB, we assume that the input power is split, in a ratio of k to $1-k$, into converters 1 and 2, as shown in Figure 20(c). The efficiency is given by

$$\begin{aligned}\eta_{\text{I-IIB}} &= k\eta_1 + (1-k)\eta_2 \\ &> \min\{\eta_1, \eta_2\} \quad \text{for all } 0<k<1 \\ &> \eta_1\eta_2\end{aligned} \tag{46}$$

For Configuration I-IIC, we assume that the input power is split, in a ratio of k to $1-k$, into converter 1 and the load, as shown in Figure 20(d). The efficiency is given by

$$\begin{aligned}\eta_{\text{I-IIC}} &= k\eta_1\eta_2 + (1-k) \\ &= \eta_1\eta_2 + (1-k)(1-\eta_1\eta_2) \\ &> \eta_1\eta_2 \quad \text{for all } 0<k<1\end{aligned} \tag{47}$$

For Configuration IIA-IIIB, we assume that a fraction of $1-k$ of the input power is fed to converter 2. The rest of the input power combines with the power released from the storage to supply converter 1, as shown in Figure 20(i). The output of converter 2 is split in a ratio of m to $1-m$ into the load and the storage. Hence, we can write the efficiency as

$$\begin{aligned}\eta_{\text{IIA-IIIB}} &= (1-k)m\eta_2 + [(1-k)(1-m)\eta_2 + k]\eta_1 \\ &= \eta_1\eta_2\left[1 + \frac{(1-k)m}{\eta_1} + \frac{k}{\eta_2} - (m+k) + km\right] \\ &= \eta_1\eta_2\left[1 + m(1-k)\left(\frac{1}{\eta_1} - 1\right) + k\left(\frac{1}{\eta_2} - 1\right)\right] \\ &> \eta_1\eta_2 \quad \text{for all } 0<k<1 \text{ and } 0<m<1\end{aligned} \tag{48}$$

Likewise, the efficiencies of the other configurations can be found, as tabulated in Table IV. It is readily shown that Configurations I-IIA through IIC-IIIC all have a higher efficiency than Configuration I-I. In other words, *the lower bound of the efficiency of a PFC voltage regulator*, η, *is theoretically equal to* $\eta_{\text{I-I}}$, i.e.

$$\eta \leqslant \eta_1\eta_2 \tag{49}$$

It should be noted that the above conclusion remains theoretical and the efficiency of real converters can be affected by a number of such other factors as transformer design, use of soft switching, choice of components, etc. Nonetheless, the above theoretical efficiency calculation does highlight a possible way to the design of inherently efficient PFC voltage regulators, which is to minimize redundant power processing of the two constituent converters.

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Table IV. Theoretical efficiencies (where $0<k<1$ and $0<m<1$). Expressions arranged for easy comparison with $\eta_1\eta_2$.

Config.	Efficiency	
I-I	$\eta_1\eta_2$	
I-IIA	$\eta_1\eta_2+(1-k)\eta_2(1-\eta_1)$	where $(1-k)\eta_2(1-\eta_1)>0$
I-IIB	$k\eta_1+(1-k)\eta_2$	where $k\eta_1+(1-k)\eta_2>\min\{\eta_1,\eta_2\}>\eta_1\eta_2$
I-IIC	$\eta_1\eta_2+(1-k)(1-\eta_1\eta_2)$	where $(1-k)(1-\eta_1\eta_2)>0$
I-IIIA	$k\eta_1+(1-k)\eta_2$	same as I-IIB
I-IIIB	$\eta_1\eta_2+(1-k)\eta_2(1-\eta_1)$	same as I-IIA
I-IIIC	$\eta_1\eta_2+(1-k)(1-\eta_1\eta_2)$	same as I-IIC
IIA-IIIA	$k\eta_1+(1-k)\eta_2$	same as I-IIB
IIA-IIIB	$\eta_1\eta_2+m(1-k)\eta_2(1-\eta_1)+k\eta_1(1-\eta_2)$	where $m(1-k)\eta_2(1-\eta_1)+k\eta_1(1-\eta_2)>0$
IIA-IIIC	$\eta_1\eta_2+m(1-k)(1-\eta_1\eta_2)+k\eta_1(1-\eta_2)$	where $m(1-k)(1-\eta_1\eta_2)+k\eta_1(1-\eta_2)>0$
IIB-IIIA	$\eta_1\eta_2+\eta_1\eta_2[\frac{km}{\eta_1}(\frac{1}{\eta_2}-1)+(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1)]$	where $(1-k)\eta_1+k\eta_2>\eta_1\eta_2$ (see I-IIB)
IIB-IIIB	$k\eta_1+(1-k)\eta_2$	same as I-IIB
IIB-IIIC	$\eta_1\eta_2+\eta_1\eta_2[\frac{km}{\eta_1}(\frac{1}{\eta_2}-1)+(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1)]$	where $(1-k)\eta_1+k\eta_2>\eta_1\eta_2$ (see I-IIB)
IIC-IIIA	$\eta_1\eta_2+\eta_1\eta_2[\frac{(1-k)\eta'+k\eta_1\eta_2}{(\eta_1\eta_2)\eta'}-1]$	where $\eta'=\frac{\eta_1\eta_2}{(1-m)\eta_1+m\eta_2}$ and $(1-k)\eta'+k\eta_1\eta_2>\eta_1\eta_2\eta'$
IIC-IIIB	$\eta_1\eta_2+\eta_1\eta_2[k+(\frac{(1-k)\eta_2+k\eta''}{\eta_2\eta''}-1)]$	where $\eta''=\eta_1\eta_2$ and $(1-k)\eta_2+k\eta''>\eta_2\eta''$
IIC-IIIC	$\eta_1\eta_2+(1-km)(1-\eta_1\eta_2)$	where $(1-km)(1-\eta_1\eta_2)>0$

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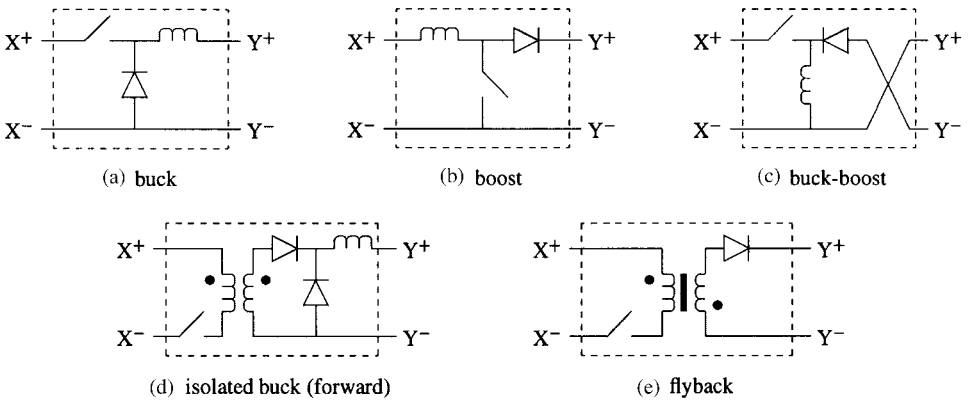

Figure 21. Basic voltage converter circuits: (a)–(c) non-isolated, (d)–(e) isolated.

Remark

The choice of m and k affects the efficiency and control requirements. In practice, efficiency and control specification represent conflicting requirements. For instance, if k is set at the extreme value of 1 for a I-IIB configuration, the efficiency is high, but no power factor correction can be achieved. Also, m and k are related to the voltage ratios of the constituent converters. Thus, depending upon the particular converter topologies used, there are limits to which m and k can be assigned to satisfy the specified control requirements (i.e. power factor and regulation). Selecting m and k is an important practical problem that deserves further investigation.

11. DERIVATION OF PRACTICAL PFC VOLTAGE REGULATOR CIRCUITS WITH REDUCED REDUNDANT POWER PROCESSING

In Section 9, 16 basic configurations of PFC regulators have been derived, each of which is composed of two basic switching converters. One of these is the conventional cascade configuration in which a PFC stage is cascading with a dc/dc converter stage [3–5,12–16]. The other 15 have non-cascading structures which, as shown above, have a higher efficiency compared to the cascade configuration. The improved efficiency can be attributed to the *reduced-redundant-power-processing* (R^2P^2) feature of the non-cascading structures. However, not all 15 configurations can be readily implemented in practical forms. Upon close inspection of these configurations, we can readily conclude that out of the fifteen configurations, four permit simple interconnections and transformer isolation, namely, configurations I-IIA, I-IIB, I-IIIA and I-IIIB (Figures 20(b), 20(c), 20(e) and 20(f)). In the following, we present a systematic procedure for synthesizing PFC voltage regulator circuits that arise from these four basic configurations.

11.1. Transformation of power flow graphs into equivalent circuits

Since the input and load are voltage terminated, the use of voltage converters and capacitive storage becomes a convenient choice. The basic voltage converters are shown in Figure 21.

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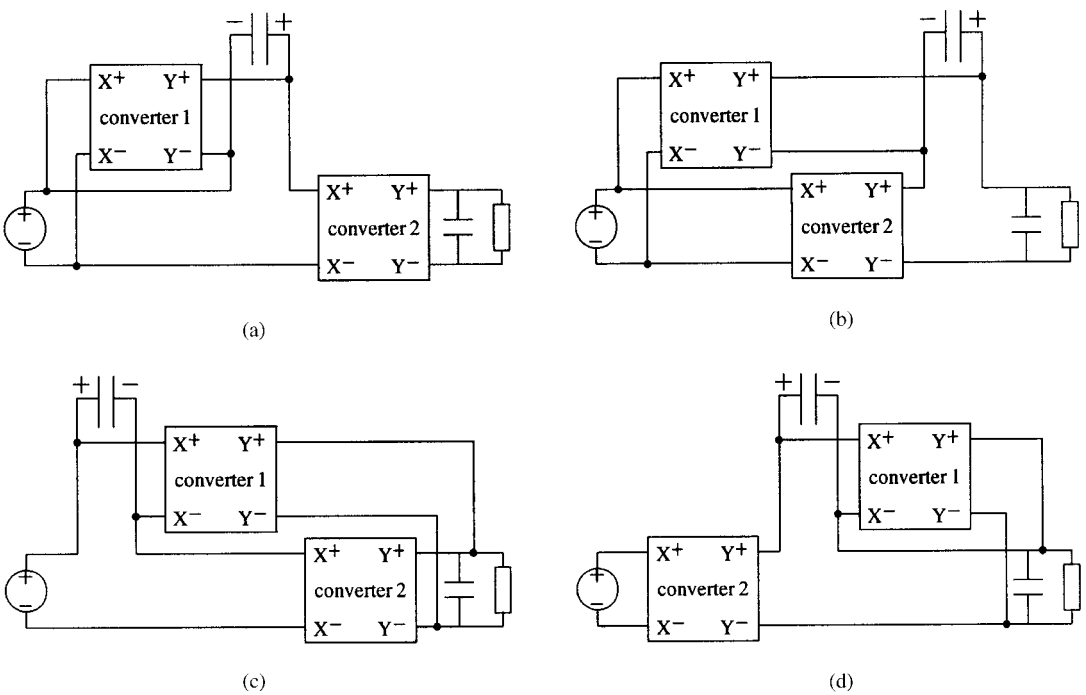

Figure 22. Equivalent circuits of the simplest *reduced redundant power processing* (R^2P^2) configurations. Rectangular blocks denote converters. (a) I-IIA; (b) I-IIB; (c) I-IIIA; and (d) I-IIIB.

In general, an R^2P^2 circuit can be realized by two voltage converters connecting the input, storage and load ports. The crucial question is how to connect the ports with two converters, such that the power flow configuration concerned can be realized.

In transforming the power flow representations of Figures 20(b), (c), (e) and (f) into practical circuits, the following basic connection rules should be observed:

1. Since the ports are voltage terminated, connection of any two ports simultaneously to a converter should be realized by a *series circuit connection.*
2. Connection of a port with the inputs (or outputs) of two converters should be realized by a *parallel circuit connection.*

Based on these rules and Figure 20, we can develop equivalent circuit representations for the four basic configurations of R^2P^2 PFC voltage regulators, as shown in Figure 22.

11.2. Placement of constituent basic converters

The next logical step in the synthesis process is to place converters appropriately in the rectangular boxes of Figure 22, paying attention to the polarity markings of the input and output terminals of the converters. In general, referring to Figure 21, power flows through a converter from terminals X^+X^- to Y^+Y^-. Thus, in order to ensure power flows in the appropriate directions, we place converters in the circuits of Figure 22 in such a way that

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terminals X^+X^- and Y^+Y^- of the basic converters of Figure 21 match those in the R^2P^2 PFC voltage regulator circuits. However, the choice of basic converters to be placed in the R^2P^2 PFC voltage regulator circuits is not arbitrary, as will be discussed in the next subsection.

11.3. Constraints on the choice of basic converters

We now consider using non-isolated basic converters for realizing converters 1 and 2, and examine the constraints in the choice of converters. We first observe that all non-isolated converters have a direct short-circuit path between input and output terminals, during the entire or part of a switching period.

- For the non-isolated buck and boost converters, regardless of how the switch, diode and inductor are re-arranged, there is a short-circuit path either between X^+ and Y^+, or between X^- and Y^-.
- For the non-isolated buck–boost converter, regardless of how the switch, diode and inductor are re-arranged, there is a short-circuit path either between X^+ and Y^-, or between X^- and Y^+.

Clearly, in choosing a non-isolated basic converter for placement in an R^2P^2 circuit, care should be taken to ensure that the short-circuit paths imposed by the basic converters do not affect the intended connections. The allowable short-circuit paths can be readily found by inspection of the R^2P^2 circuits of Figure 22.

1. For Configuration I-IIA, short-circuit paths are allowed between
   (a) X^+ and Y^- of converter 1; and
   (b) any X and Y terminal of converter 2.
2. For Configuration I-IIB, short-circuit paths are allowed between
   (a) X^- and Y^- of converter 1; and
   (b) X^- and Y^+ of converter 2.
3. For Configuration I-IIB, short-circuit paths are also allowed between
   (a) X^+ and Y^- of converter 1; and
   (b) X^+ and Y^+ of converter 2.
4. For Configuration I-IIIA, short-circuit paths are allowed between
   (a) X^- and Y^+ of converter 1; and
   (b) X^+ and Y^+ of converter 2.
5. For Configuration I-IIIA, short-circuit paths are also allowed between
   (a) X^- and Y^- of converter 1; and
   (b) X^+ and Y^- of converter 2.
6. For Configuration I-IIIB, short-circuit paths are allowed between
   (a) X^- and Y^+ of converter 1; and
   (b) any X and Y terminal of converter 2.

From the above observations and the earlier observations regarding the presence of short-circuit paths in the basic non-isolated converters, we can deduce the type of basic non-isolated converters that can be used for converters 1 and 2 in a non-isolated R^2P^2 PFC voltage regulator. The main results are stated as follows and summarized in Table V, along

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Table V. Possible choice of converters for non-isolated R^2P^2 PFC voltage regulator topologies.

Configuration	Conv. 1	Conv. 2	Reported
I-IIA	buck–boost	buck	Zeta Chow *et al*. [20]
I-IIA	buck–boost	buck–boost	–
I-IIA	buck–boost	boost	–
I-IIB	buck	buck–boost	–
I-IIB	boost	buck–boost	–
I-IIB	buck–boost	buck	–
I-IIB	buck–boost	boost	–
I-IIIA	buck–boost	buck	–
I-IIIA	buck–boost	boost	–
I-IIIA	buck	buck–boost	–
I-IIIA	boost	buck–boost	–
I-IIIB	buck–boost	buck	–
I-IIIB	buck–boost	buck–boost	García *et al.* [19]
I-IIIB	buck–boost	boost	SEPIC BIFRED [5]

with some previously reported circuits.

- *For Configuration* I-IIA, *converter* 1 *can only be a buck–boost converter*, *and converter* 2 *can be any converter*.
- *For Configuration* I-IIB, *two cases are possible. If converter* 1 *is a buck or a boost converter*, *converter* 2 *can only be a buck–boost converter. If converter* 1 *is a buck–boost converter*, *converter 2 can be a buck or a boost converter*.
- *For Configuration* I-IIIA, *two cases are possible. If converter* 1 *is a buck–boost converter*, *converter* 2 *can only be a buck or a boost converter. If converter* 1 *is a buck or a boost converter*, *converter* 2 *can only be a buck–boost converter*.
- *For Configuration* I-IIIB, *converter* 1 *can only be a buck–boost converter*, *and converter* 2 *can be any converter*.

11.4. Requirement for isolation between input and load

The requirement of isolation between the input and load necessitates the use of transformer-isolated converters for either or both constituent converters. The simplest implementation for Configurations I-IIA and I-IIIB is to have only converter 2 isolated, and in any such implementation, converter 1 must be a buck–boost converter while converter 2 can be any isolated converter. Of course, if converter 1 is also isolated (though not necessary), any combination of converter types is possible.

Moreover, Configurations I-IIB and I-IIIA would require transformer isolation for both converters 1 and 2, and hence can employ any combination of basic isolated converters.

12. CIRCUIT SYNTHESIS EXAMPLES

In this section we will apply the afore-described synthesis procedure to construct practical R^2P^2 PFC voltage regulators.

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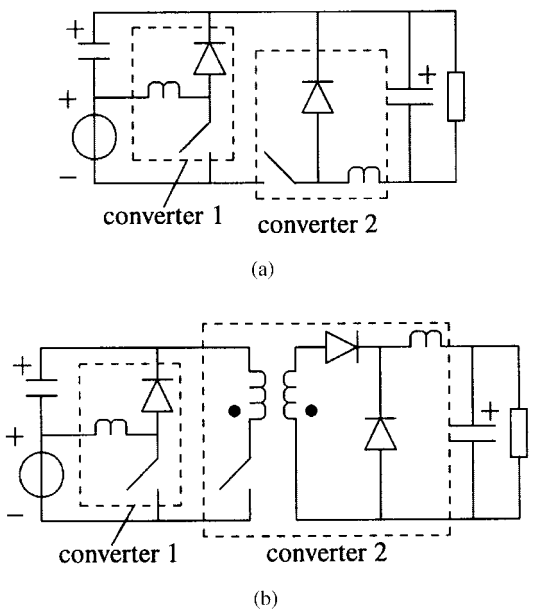

Figure 23. (a) A possible implementation for Configuration I-IIA using a buck–boost and a buck converter for converters 1 and 2; (b) isolated version using a buck–boost and a transformer-isolated forward converter for converters 1 and 2. Core reset arrangement omitted for brevity.

Example 1 (*Realization of Configuration* I-IIA)
As mentioned before, the simplest way to provide isolation between the input and the load for Configuration I-IIA is to use an isolated converter for converter 2. Note that converter 1 need not be isolated. Thus, we can employ any isolated converter for converter 2, but necessarily use a buck–boost converter for converter 1 (to avoid having to use an isolated converter for converter 1). Let us choose a buck converter for converter 2. Placing the two converters appropriately in the equivalent circuit of Configuration I-IIA shown in Figure 23(a), we obtain the circuit shown in Figure 23(a). The transformer isolated version is shown in Figure 23(b). See Reference [20] for experimental data.

Example 2 (*Realization of Configuration* I-IIB)
We consider Configuration I-IIB. Suppose we employ a buck–boost and a buck converter for converters 1 and 2, respectively. Similar to Example 1, we obtain an R^2P^2 PFC regulator, as shown in Figure 24. Note that both isolation is required of both converters 1 and 2 in order to provide isolation for the R^2P^2 PFC regulator.

Example 3 (*Realization of Configuration* I-IIIA)
Consider Configuration I-IIIA. Suppose we employ a buck–boost and a buck converter for converters 1 and 2, respectively. Likewise, we obtain a new PFC regulator, as shown in Figure 25.

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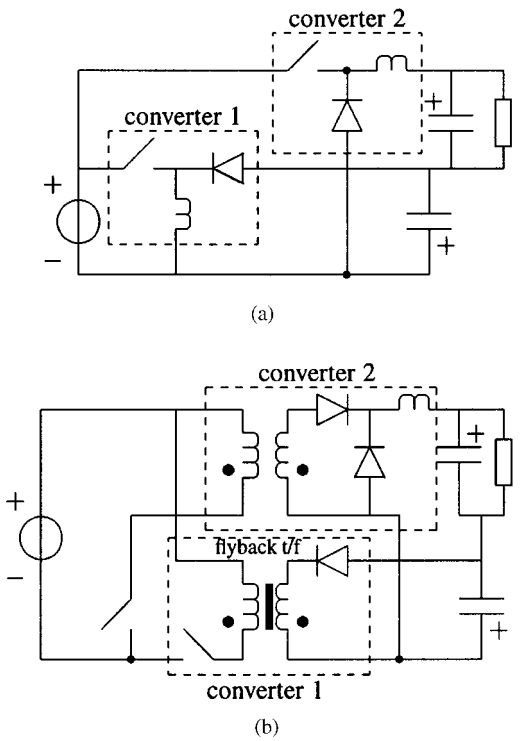

Figure 24. (a) A possible implementation for Configuration I-IIB using a buck–boost and a buck converter for converters 1 and 2; (b) isolated version using a flyback and a forward converter for converters 1 and 2. Core reset arrangement omitted for brevity.

Example 4 (*Realization of Configuration I-IIIB*)
Like Configuration I-IIA, isolation can be achieved for Configuration I-IIIB by employing an isolated converter for converter 2, and there is no need for converter 1 to be isolated. Thus, we can employ any isolated converter for converter 2, but necessarily use a buck–boost converter for converter 1 (to avoid having to use an isolated converter for converter 1). Figure 26 shows a possible R^2P^2 PFC voltage regulator circuit arising from Configuration I-IIIB. This circuit has been tested experimentally by García [19].

13. COMPARISON OF CONTROL REQUIREMENTS

The basic requirement of the control of a PFC voltage regulator is to regulate the power flow among the input, load and storage ports. To order to take full control of the amount of power being injected to and released from the storage, that being injected to the load, and that being taken from the input, the two constituent converters should be controlled separately. The following theorem is instrumental.

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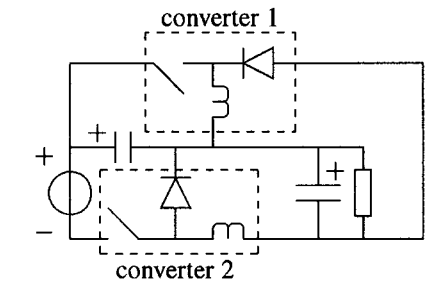
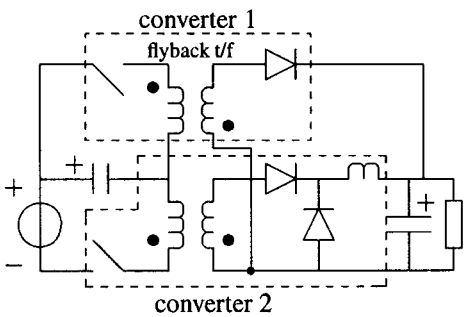


(a)



(b)

Figure 25. (a) A possible implementation for Configuration I-IIIA using a buck–boost and a buck converter for converters 1 and 2; (b) isolated version using a flyback and a forward converter for converters 1 and 2. Core reset arrangement omitted for brevity.

Theorem 5

For any PFC voltage regulator consisting of two simple converters, it is not possible to achieve unity power factor and output regulation simultaneously under the control of only one control parameter.

Proof

We will prove this theorem by contradiction. First we assume that unity p.f. and output regulation are achieved with only one control parameter, $\xi(t)$, controlling both converters. It is worth recalling that we are considering only low-frequency power flows. Suppose the power processed by converter 1 and converter 2 are $F_1(\xi(t))$ and $F_2(\xi(t))$, respectively. Thus, we hope to find $\xi(t)$ such that PFC and output regulation are satisfied simultaneously. We will exemplify the proof with Configuration I-I. Assuming that the converters are lossless, the PFC requirement dictates that, for all t,

$$F_1(\xi(t)) = 2P_o \sin^2 2\pi f_m t$$

$$\Rightarrow \xi(t) = F_1^{-1}(2P_o \sin^2 2\pi f_m t) \tag{50}$$

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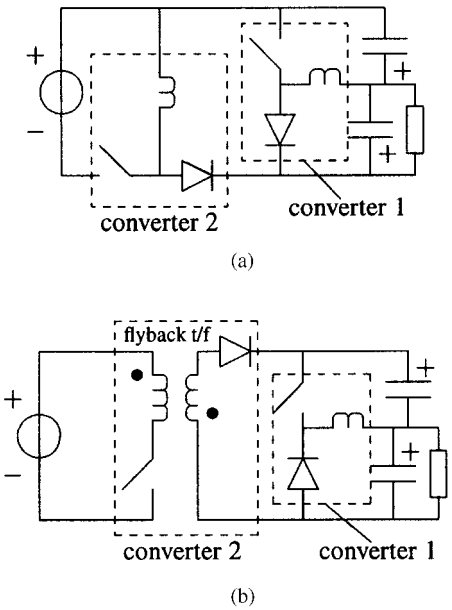

Figure 26. (a) A possible implementation for Configuration I-IIIB using buck–boost converters for converters 1 and 2; (b) isolated version using a flyback and a forward converter for converters 1 and 2.

where P_o is the output power. However, output regulation requires that, for all t,

$$F_2(\xi(t)) = P_o$$
$$\Rightarrow \xi(t) = F_2^{-1}(P_o) \tag{51}$$

which contradicts (50). Likewise, for all other configurations, we will arrive at obvious contradiction if we begin with the assumption of using only one parameter for control. Thus, in general we are not able to maintain PFC and output regulation using only one control parameter. □

It should be apparent that if two separate control parameters are allowed, then the control problem can be solved. (A straightforward proof can be constructed based on Theorem 2's proof.) Two forms of the solution can be logically deduced:

1. The power flow functions F_1 and F_2 are controlled separately by $\xi_1(t)$ and $\xi_2(t)$, where $\xi_1(t) \neq \xi_2(t)$.
2. One of the power flow functions is controlled by two control parameters $\xi(t)$ and $\psi(t)$, while the other one is controlled by either $\xi(t)$ or $\psi(t)$.

As we will see later, the above first solution covers the conventional design of cascading a PFC pre-regulator and a dc/dc converter, which are under separate control. The second solution, moreover, covers the single-stage design utilizing both duty cycle modulation and frequency modulation for achieving almost perfect PFC and fast regulation [21].

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Remark
In formulating practical solutions, the choice of the types of converters is crucial since the power flow functions F_1 and F_2 depend on circuit topologies. In the following discussion we assume that the converters have been properly chosen to ensure satisfaction of the required power flow functions.

14. APPLICATION TO THE CONTROL OF PRACTICAL CONVERTERS

We may now take a step further in applying the above result to real converters. The usual parameters available for control are the duty cycle d and the switching frequency f_s. For converters operating in discontinuous mode, both d and f_s are available control parameters. However, for converters operating in continuous mode, only d is available since such converters are highly immune to variation of switching frequency. For brevity we write the power flow function for a continuous-mode (CM) converter as $F_{\mathrm{CM}}(d(t))$ and that of a discontinuous-mode (DM) converter as $F_{\mathrm{DM}}(d(t), f_s(t))$, respectively.

14.1. Choice of control parameters

As studied in Section 13, we generally need two separate control loops for controlling two parameters. Moreover, operating modes of the converters will affect the complexity of the control problem. It is not difficult to see the following results which are straightforward extensions of the above discussion.

Operating Regime 1: When both converters are in CM operation, the use of two separate duty cycle signals for the two converters is mandatory. The power flow functions are

$$P_1 = F_{\mathrm{CM}_1}(d_1(t)) \tag{52}$$

$$P_2 = F_{\mathrm{CM}_2}(d_2(t)) \tag{53}$$

where P_1 and P_2 denote the power flows through the two converters, $F_{\mathrm{CM}_1}(.)$ and $F_{\mathrm{CM}_2}(.)$ are the respective power flow functions, and $d_1(t)$ and $d_2(t)$ are the duty cycle signals controlling separately the two converters.

Operating Regime 2: When one converter is in CM operation and the other in DM operation, we may employ any combination of two control parameters chosen from two available duty cycles and a switching frequency, i.e.

$$P_1 = F_{\mathrm{CM}_1}(d_1(t)) \tag{54}$$

$$P_2 = F_{\mathrm{DM}_2}(d_2(t), f_{s_2}(t)) \tag{55}$$

Operating Regime 3: When both converters are in DM operation, we may employ any combination of two control parameters chosen from two available duty cycles and two available switching frequencies, i.e.

$$P_1 = F_{\mathrm{DM}_1}(d_1(t), f_{s_1}(t)) \tag{56}$$

$$P_2 = F_{\mathrm{DM}_2}(d_2(t), f_{s_2}(t)) \tag{57}$$

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It is worth noting that the above control cases are applicable to all 16 configurations. In particular, they cover all conventional two-stage designs in which a PFC pre-regulator and a dc/dc converter are cascaded together under the control of two separate loops.

14.2. Application to single-stage design

Due to its popularity, the single-stage PFC voltage regulator may deserve further discussion [3,13,15,16]. Specifically, since only one (set of) active switch(es) exists, it is not possible to use two duty cycle signals as the control parameters. Thus, we must base our design on the combined use of duty cycle and frequency control. This also necessitates the operation of at least one of the converters in DM. Two possibilities exist, corresponding to Operating Regimes 2 and 3. Since only one duty cycle and one switching frequency are available, they become the inevitable choice of control parameters. Specifically, for Operating Regime 2, we have

$$P_1 = F_{\mathrm{CM}_1}(d(t)) \tag{58}$$

$$P_2 = F_{\mathrm{DM}_2}(d(t), f_s(t)) \tag{59}$$

and for Operating Regime 3, we have

$$P_1 = F_{\mathrm{DM}_1}(d(t), f_s(t)) \tag{60}$$

$$P_2 = F_{\mathrm{DM}_2}(d(t), f_s(t)) \tag{61}$$

Obviously, in practice, Operating Regime 2 has advantage over Operating Regime 3 because if one converter is not affected by frequency variation, then frequency modulation can be used solely for controlling the other converter [21]. In short, we may state the results of our analysis of the control requirement of single-stage PFC voltage regulators as follows.

1. Perfect PFC and output regulation are not simultaneously achieveable if both constituent converters are operating in continuous mode.
2. Perfect PFC and output regulation are simultaneously achieveable only if at least one of the constituent converters is operating in discontinuous mode. (We use 'only if' here because we still require the converter topologies be properly chosen.)
3. Combined use of duty cycle and switching frequency control is inevitable in achieving perfect PFC and output regulation.

Notwithstanding the above, control can be simplified in some configurations if performance can be compromised. In fact, imperfect PFC can still be acceptable from a practical point of view since most regulatory standards, e.g. IEC-1000, do not demand perfect unity power factor. For example, Configuration I-I (cascaded converters) can allow the use of one duty cycle signal for achieving reasonably high power factor and fast output transient, thus making the design very easy [3]. Such control simplicity represents an attraction of Configuration I-I, as will be illustrated in the following example.

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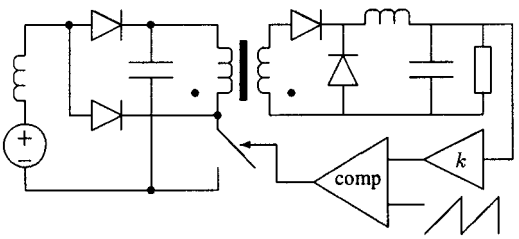

Figure 27. Single-stage single-switch PFC voltage regulator based on Configuration I-I [3].

14.3. Illustrative example: single-stage single-switch PFC voltage regulator

A single-stage PFC voltage regulator employing one switch and comprising a cascade connection of a boost converter and a forward converter has been proposed for some time by Redl *et al.* [3]. This converter, as shown in Figure 27, belongs to Configuration I-I. The original design employs Operating Regime 3 (i.e. with both the boost and the forward stages operating in discontinuous mode), but uses only duty cycle control for output regulation. It has been shown experimentally [3] that a reasonable power factor and fast output response can in fact be obtained without the use of two separate controls. Clearly, from the foregoing discussion, we can improve the performance of this PFC voltage regulator if we have an extra control parameter.

Specifically, to achieve perfect PFC and output regulation, we need two control parameters. Owing to the single-switch design, the combined use of duty cycle and switching frequency control is inevitable, as discussed previously. In Chow *et al.* [21], the same converter is redesigned to employ Operating Regime 2 so as to immunize one converter against frequency variation. Hence, control can be easily achieved with one loop regulating the output via duty cycle modulation and another loop shaping the input current via frequency modulation. Specifically, the boost converter is made to operate in DM, whereas the forward converter is in CM. The control equation for the DM boost converter, as derived in Chow *et al.* [21], is

$$f_s = \frac{f_o}{1 - (v_i(t)/V_c)} \tag{62}$$

where $v_i(t)$ is the input voltage, V_c is the voltage across the storage capacitor, and f_o is the minimum switching frequency. The forward converter is simply controlled by a conventional PWM scheme. Details of practical implementation and experimental results can be found in Chow *et al.* [21].

Remark

It should be noted that the choice between Operating Regimes 2 and 3 is also affected by the problem of variable voltage stress, as studied earlier in Section 7.3. The foregoing discussion only focuses on the control issue.

15. CONCLUSION

Although a number of PFC voltage regulator topologies have been reported recently, they represent isolated cases of innovative circuit design, and very little formal work has been

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performed on the basic procedure for deriving the required circuit configurations that can shed light on the creation of new circuit topologies for such applications [4,7]. This paper formally studies the circuit theoretic aspects of PFC, starting from basic principles and topological requirements. We have identified the ways in which simple dc/dc converters can be made to provide PFC. The key is the destruction of the inductor's dynamics. The dual requirement of PFC and voltage regulation has been studied in depth, leading to the derivation of basic configurations of PFC voltage regulators. Specifically, based on a power flow consideration, we have arrived at 16 possible configurations, from which PFC voltage regulators can be constructed systematically. Since the main purpose is to present a systematic procedure for creating circuits, we focus on the general connection structures rather than specific circuit analysis. By comparing the theoretical efficiencies of these basic configurations, one can appreciate that the way in which power is processed plays a crucial role in determining the overall efficiency of a PFC voltage regulator. A particularly illuminating result, which turns out to be intuitive, is that the overall efficiency can be improved if the power processed by one converter is not re-processed totally by the other converter within the PFC voltage regulator. This leads to the idea of reduced-redundant-power-processing PFC voltage regulators which have been analysed in some depth. A synthesis procedure has been derived for some selected configurations which have practical significance. It is hoped that this study will provide useful reference for engineers to create 'new' efficient PFC voltage regulators.

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REFERENCES

1. Tse CK. *Linear Circuit Analysis*. Addison-Wesley, London, 1998.
2. Krein PT. *Elements of Power Electronics*. Oxford University Press, New York, 2000.
3. Redl R, Balogh L, Sokal NO. A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage. *IEEE PESC Records* 1994; 1137–1144.
4. Tse CK, Chow MHL. Single stage high power factor converter based on the Sheppard–Taylor topology. *IEEE PESC Records* 1996; 1191–1197.
5. Madigan M, Erickson R, Ismail E. Integrated high-quality rectifier-regulators. *IEEE PESC Records* 1992; 1043–1051.
6. Middlebrook RD, Ćuk S. A general unified approach to modelling switching-converter power stages. *IEEE PESC Records* 1976; 18–34.
7. Tse CK, Lee YS, So WC. An approach to modelling DC/DC converter circuits using graph theoretic concepts. *International Journal of Circuit Theory and Applications* 1993; **22**(3):371–384.
8. Seshu S, Reed MB. *Linear Graphs and Electrical Networks,* Addison-Wesley, Reading, MA, 1961.
9. Simonetti DSL, Sebastián J, Uceda J. Control conditions to improve conducted EMI by switching frequency modulation of basic discontinuous PWM preregulators. *IEEE PESC Records* 1994; 1180–1187.
10. Jovanović MM, Tsang DMC, Lee FC. Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency. *Proceedings of IEEE APEC* 1994; 569–575.
11. Makowski MS, Bailly A. Switch voltage control versus switch current control method. Principle and realization. *IEEE PESC Record* 1992; 749–761.
12. Kheraluwala MH, Steigerwald RL, Gurmoorthy R. A fast response high power factor converter with a single power stage. *IEEE PESC Records* 1991; 769–779.
13. Redl R, Balogh L, Design consideration for single stage isolated power factor corrected power supplies with fast regulation of the output voltage. *Proceedings of IEEE APEC* 1994; 569–575.

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14. Jiang Y, Hua G, Tang W, Lee FC. A novel single phase power factor correction scheme. *Proceedings of IEEE APEC* 1993; 287–291.
15. Huber L, Jovanović MM. Single-stage, single-switch, isolated power supply technique with input-current shaping and fast output voltage regulation for universal input-voltage range applications. *Proceedings of IEEE APEC* 1997; 272–280.
16. Schenk K, Ćuk S. A single-switch single-stage active power factor corrector with high quality input and output. *IEEE PESC Records* 1997; 385–391.
17. Chow MHL, Lee YS, Tse CK. Single-stage single-switch PFC voltage regulator with unity power factor, fast transient response and low voltage stress. *IEEE Transactions on Power Electronics* 2000; **15**(1):156–163.
18. Tse CK, Chow MHL. New single stage power-factor-corrected regulators operating in discontinuous capacitor voltage mode. *IEEE PESC Records* 1997; 371–377.
19. García O, Cobos JA, Alou P, Preito R, Uceda J, Ollero S. New family of single stage AC/DC power factor correction converters with fast output voltage regulation. *IEEE PESC Records* 1997; 536–542.
20. Chow MHL, Tse CK, Lee YS. An efficient PFC voltage regulator with reduced redundant power processing. *IEEE PESC Records* 1999; 87–92.
21. Chow MHL, Siu KW, Tse CK, Lee YS. A novel method for elimination of line current harmonics in single-stage PFC regulators. *IEEE Transactions on Power Electronics* 1998; **13**(1):75–82.
22. Tse CK, Chow MHL. Theoretical study of switching converters with power factor correction and output regulation. *IEEE Transactions in Circuits and Systems I* 2000; **47**(7):1047–1055.
23. Tse CK, Chow MHL, Cheung MKH. A family of PFC voltage regulators with reduced redundant power processing. *IEEE Transactions in Power Electronics* 2001; **16**(5):794–802.

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