Class E Full-Wave Low dv/dt Rectifier

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***Abstract*— An analysis and experimental verification for a Class E full-wave current-driven low dv/dt rectifier are given. Basic parameters of the circuit are derived using the time-domain analysis and Fourier series techniques. The rectifier diodes turn on and off at low dv/dt, yielding low switching noise and low switching losses. Diode parasitic capacitances do not adversely affect the circuit operation. The absolute value of di/dt is limited at diode turn-off, significantly reducing the reverse recovery current. The rectifier input voltage waveform differs only slightly from an ideal sinusoid, resulting in a low total harmonic distortion. The circuit has theoretically zero-ripple voltage and, therefore, zero loss in the equivalent series resistance (ESR) of the filter capacitor. The Class E full-wave topology has lower diode conduction loss than the Class E half-wave rectifier. The efficiency is almost constant over the load range from 10% to 100% of the full load. The rectifier offers high-power density, high-frequency rectification and is suitable for low-voltage and high-current applications, as shown by experimental results given for a 75 W rectifier which was operated at 1 MHz with an output of 5 V and 15 A. The theoretical and the experimental results were in good agreement.**

I. Introduction

CLASS E rectifiers are suitable for high-frequency, high-efficiency, and low-noise rectification [1]–[8]. In Class E current-driven half-wave rectifiers, the diode turns on at low dv/dt and turns off at low dv/dt and limited di/dt [3], resulting in low noise and switching losses. Moreover, the diode parasitic capacitances do not adversely affect the circuit operation because they are absorbed into capacitors connected in parallel with the diodes. The combination of a Class E rectifier with a Class E inverter yields dc–dc converters operating with narrow-band frequency regulation over the entire load range [9]–[22]. Unfortunately, conduction losses are the main limitation for Class E half-wave rectifier applications in converters with high-current and low-voltage outputs.

The purpose of this paper is to present an analysis and the experimental results of a Class E full-wave current-driven low dv/dt rectifier. This circuit has lower conduction loss in the diodes and in the parallel capacitors than the Class E half-wave topology. The ac component of the output current is theoretically zero, resulting in zero losses in the filter capacitor ESR. Actually, the filter capacitor loss is about 40 times less than in conventional peak rectifiers and 100 times lower than in Class E half-wave rectifiers. The efficiency is almost constant over 90% of the entire load range. Another important advantage of the Class E full-wave rectifier is that the input voltage waveform only slightly differs from a sinusoid, resulting in a low THD circuit. Finally, the rectifier acts as an impedance inverter and, therefore, it is fully compatible with Class E inverters [9]–[19]. Because of these features, the Class E full-wave rectifier is suitable for high-frequency, high power-density applications, particularly, when a low output voltage and a high load current are required, e.g., 5 V or 12 V with the output power above 50 W [17]–[22].

The rectifier description and the principle of circuit operation are given in Section II. Section III contains the time-domain analysis and design equations for steady-state operation. Section IV presents a design example. Experimental results are given in Section V. Section VI contains the final conclusions. Derivations of the circuit characteristics are included in the Appendix.

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II. Operation of the Rectifier

A. Circuit Description

A circuit of a Class E full-wave current-driven low dv/dt rectifier [3], [22] is shown in Fig. 1(a). It consists of two diodes D_1 and D_2, two capacitors C_1 and C_2 with the same capacitance C, a single-pole low-pass output filter C_f–R_L, and two transformers with a turns ratio n. Resistor R_L is a dc load. An equivalent circuit of the rectifier is shown in Fig. 1(b). L_m represents magnetizing inductances of the secondary windings of the transformers. It is assumed that they are equal and large enough to carry only a dc current and, therefore, can be considered as an open circuit for the ac component of the current. The leakage inductances, the core and the windings resistances, and the transformer stray capacitances are neglected. The diode parasitic capacitances are absorbed into capacitances C_1 and C_2 connected in parallel with the diodes. The ac component of the current flowing into the C_f–R_L circuit is ideally zero, resulting in a constant zero-ripple output voltage V_O. Actually, this is obtained with a small capacitor C_f.

B. Principle of Operation

Fig. 2 shows four topological modes that the rectifier goes through during one switching period, when the maximum on-duty cycle is lower than 0.5. Idealized current and voltage waveforms of the rectifier are depicted in Fig. 3. The input current i is sinusoidal with frequency $f = \omega/2\pi$ and amplitude I_m. Consequently, currents $i_1 = ni$ and $i_2 = -ni$ are

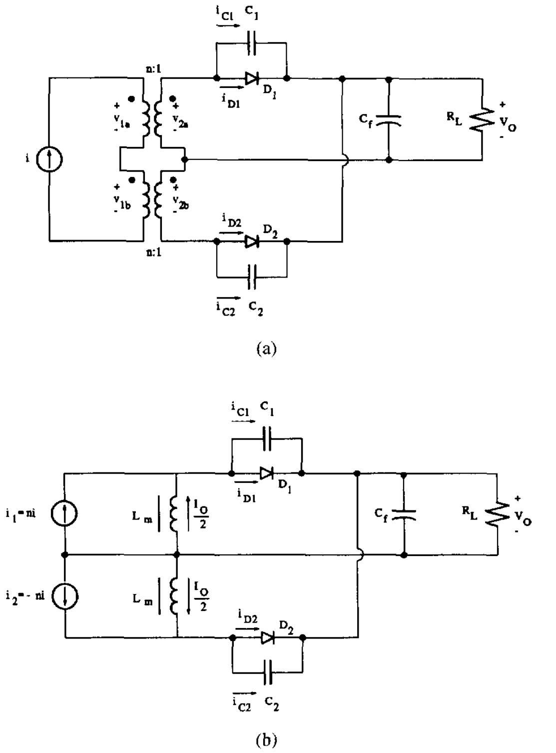


Fig. 1. Class E, full-wave current-driven, low dv/dt rectifier. (a) Circuit. (b) Model of the rectifier.

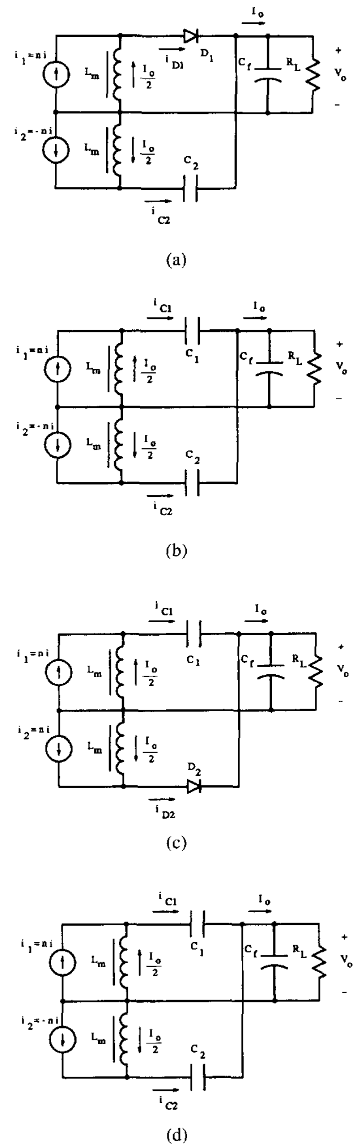


Fig. 2. Models of Class E, full-wave current-driven, low dv/dt rectifier for various time intervals. (a) Model with D_1 ON and D_2 OFF (b) Model with D_1 OFF and D_2 OFF. (c) Model with D_1 OFF and D_2 ON. (d) Model with D_1 OFF and D_2OFF.

also sinusoidal. Since inductances L_m are equal, the current through each of them is $I_O/2$. As a result, the waveforms of the current through the parallel combinations of C_1–D_1 and C_2–D_2 are two sine waves that are 180° out of phase and both are shifted upward by dc component $I_O/2$. These waveforms are $i_{C1} + i_{D1} = I_O/2 + ni$ and $i_{C2} + i_{D2} = I_O/2 - ni$, respectively. Since the current through the circuit C_f–R_L is given by $i_{C1} + i_{D1} + i_{C2} + i_{D2}$, the resulting ac component of the current is zero. Therefore, the output has ideally zero-voltage ripple, even without the filter capacitor C_f. Actually, the capacitor C_f is much smaller than in conventional rectifiers circuit and its ESR produces low losses because the current through it has a low rms value.

The first topological mode of Fig. 2(a) begins at $\omega t = \phi$, when diode voltage v_{D1} reaches the diode threshold voltage, turning on diode D_1. During this phase, the current $I_O/2 + nI_m sin\omega t$ flows through D_1. Diode D_2 is off and its voltage waveform is shaped by the shunt capacitor C_2, according to $i_{C2} = C_2 dv_{C2}/dt$. The first mode ends at $\omega t = \phi + 2\pi D$, when current i_{D1} reaches zero, turning diode D_1 off.

The second topological mode of Fig. 2(b) begins at $\omega t = \phi + 2\pi D$. During this time interval, the current $I_O/2 + nI_m sin\omega t$ flows through C_1 which shapes the waveform of the voltage across D_1, according to $i_{C1} = C_1 dv_{C1}/dt$. Since the capacitor current is zero when diode D_1 turns off, the derivative of the voltage waveform v_{D1} is also zero at $\omega t = \phi + 2\pi D$. After diode D_1 turns–off, its voltage slowly decreases because i_{C1} is negative. Since i_{C2} is positive, the voltage v_{D2} increases and reaches the diode threshold voltage at $\omega t = \phi + \pi$, turning on diode D_2.

The third topological mode of Fig. 2(c) begins at $\omega t = \phi + \pi$, when diode D_2 turns on and ends at $\omega t = \phi + \pi + 2\pi D$, when it turns off. During this time interval, the current $I_O/2 - nI_m sin\omega t$ flows through diode D_2. The waveform of the voltage across diode D_1 is still shaped by C_1. Therefore, it first decreases, reaches its minimum value V_{DRM} when i_{C1} is zero, and then increases when i_{C1} is positive.

The fourth mode of Fig. 2(d) begins, when the current i_{D2} reaches zero. As in the first topological mode, C_2 shapes the voltage waveform of D_2. Hence, v_{D2} slowly decreases from

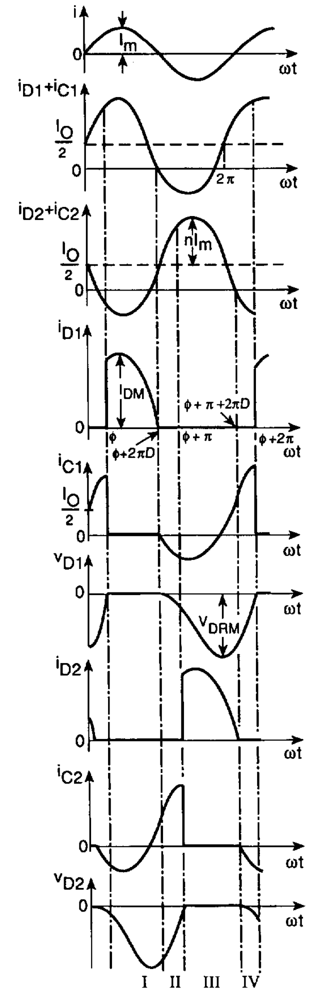


Fig. 3. Current and voltage waveforms in the Class E full-wave rectifier.

zero because i_{C2} is zero at $\omega t = \phi + \pi + 2\pi D$. The current through capacitor C_1 is positive and, therefore, voltage v_{D1} increases. Diode D_1 turns on at $\omega t = \phi + 2\pi$, when v_{D1} reaches the threshold voltage. This ends the fourth topological mode and the entire switching cycle.

The symmetrical behavior of the rectifier is demonstrated by the current and voltage waveforms of Fig. 3 because the waveforms of i_{D1} and v_{D1} and those of i_{D2} and v_{D2} are equal and 180^o out of phase.

The rectifier circuit takes advantage of the externally connected capacitances C_1 and C_2 because they shape the voltage across the diodes when the diodes are off. They also absorb the diode parasitic capacitances and, therefore, these capacitances do not adversely affect the circuit operation. The diodes turn off at zero $dv/dt = 0$ and turn on at a limited dv/dt. As a result, the current through the parasitic capacitances of the diodes is reduced at both transitions. The current source limits the value of di/dt when the diodes turn off. Therefore, the detrimental effect of the reverse-recovery charge is significantly reduced, if pn junction diodes are used. The limited value of dv/dt at both transitions and the limited value of di/dt at the turn–off reduce the level of noise produced by the rectifier and switching losses in the diodes. Current and voltage waveforms of each diode do not overlap during either transition and thus yield low switching losses. Another important advantage of the rectifier is that it has theoretically zero-ripple output-voltage. This is because the ac components of the diode and capacitor currents flowing into the C_f–R_L circuit are equal in magnitude and shifted in phase by 180^o. The circuit is called a Class E rectifier because current and voltage waveforms in each side of the rectifier are mirror images of the corresponding waveforms in the Class E zero-voltage switching amplifiers [9].

III. Analysis

The analysis of the Class E rectifier of Fig. 1(a) begins with the following assumptions:

1) The diodes are ideal, i.e., they have zero threshold voltage, zero on-resistance, infinite off-resistance, and zero minority carrier charge lifetime in the case of the pn junction diode.
2) The on-duty cycle D_{max} of each diode is equal to or less than 50%.
3) The C_f–R_L circuit can be replaced by a dc voltage source.
4) The rectifier is driven by an ideal sinusoidal current source, described by

$$i = I_m sin\omega t \quad (1)$$

where I_m is the amplitude and $\omega = 2\pi f$ is the angular frequency.
5) The transformers are ideal and have a turns ratio of n and secondary magnetizing inductances L_m. The leakage inductances, the winding and core resistances, and the stray capacitances of the transformers are ignored. The magnetizing inductances are assumed to be identical and large enough so that they represent an open circuit for the ac component of the current flowing through the parallel combination of the diode and capacitor.

All derivations are included in the Appendix and only final results are given subsequently. Diode D_1 turn-on delay angle is given by

$$tan\phi = -\frac{\pi(1-D)sin(2\pi D) + sin^2(\pi D)}{\pi(1-D)cos(2\pi D) + sin(\pi D)cos(\pi D)}. \quad (2)$$

Fig. 4 shows a plot of ϕ as a function of D. The phase ϕ decreases from 180^o to 30^o while D decreases from 0.5 to 0. This means that the shorter the duty cycle, the higher the delay angle corresponding to the diode turn-on. Also, the current through the diodes becomes more and more impulsive with a decreasing on-duty cycle. Because of the symmetrical behavior of the circuit, the diode D_2 turn-on delay angle is $\phi + \pi$ and its on-duty cycle is D.

Fig. 5 shows the diode on-duty cycle D as a function of the load resistance R_L normalized with respect to the reactance

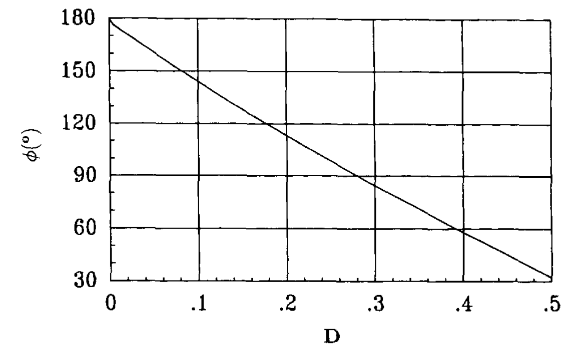


Fig. 4. Initial phase of the inputvoltage ϕ as a function of the diode ON duty cycle D.

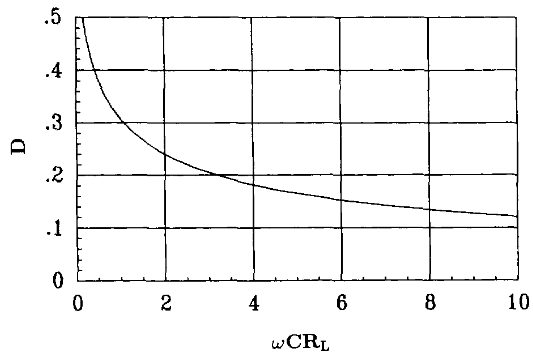


Fig. 5. Diode ON duty ratio D as a function of normalizedload resistance ωCR_L.

of each parallel capacitor $1/\omega C$

$$\omega CR_L = \frac{sin(\phi+2\pi D) - sin\phi + 2\pi(1-D)cos(\phi+2\pi D)}{4\pi sin(\phi+2\pi D)} - \frac{\pi}{2}(1-D)^2. \quad (3)$$

The duty cycle decreases from 0.5 to 0 when ωCR_L is increased from $(\omega CR_L)_{min}$ = 0.1756 to ∞. With a constant value of V_O and an increasing R_L, the output current I_O decreases and so does the current through the parallel combination of the diode and capacitor, causing the on–duty cycle D to decrease. The amplitude of the sinusoidal input current is

$$I_m = \frac{-I_O}{2nsin(\phi+2\pi D)}. \quad (4)$$

Hence, the waveforms of the currents through diodes D_1 and D_2, normalized with respect to the dc output current I_O, are given by

$$\frac{i_{D1}}{I_O} = \begin{cases} \frac{1}{2}[1 - \frac{sin\omega t}{sin(\phi+2\pi D)}], & \text{for} \quad \phi \le \omega t < \phi + 2\pi D \\ 0, & \text{for} \quad \phi + 2\pi D \le \omega t < \phi + 2\pi \end{cases} \quad (5)$$

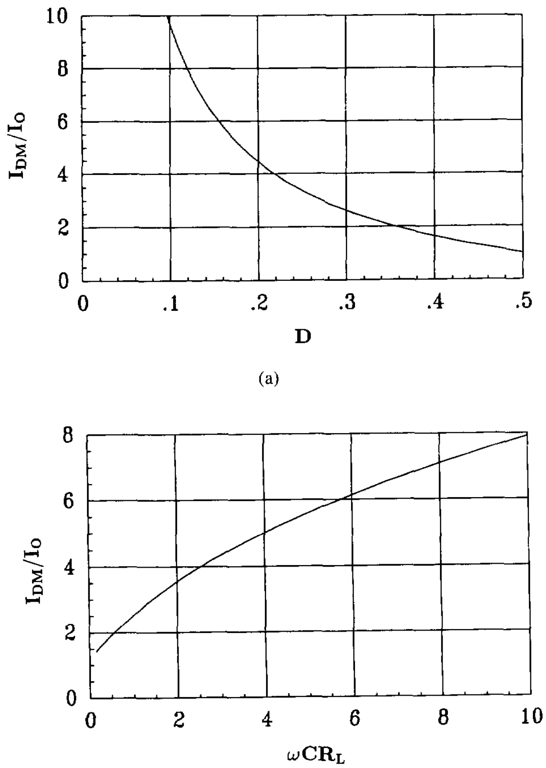
and

$$\frac{i_{D2}}{I_O} = \begin{cases} 0, & \text{for} \quad \phi + 2\pi D - \pi \le \omega t < \phi + \pi \\ \frac{1}{2}[1 + \frac{sin\omega t}{sin(\phi+2\pi D)}], & \\ & \text{for} \quad \phi + \pi \le \omega t < \phi + \pi + 2\pi D \\ 0, & \text{for} \quad \phi + 2\pi D + \pi \le \omega t < \phi + 2\pi. \end{cases} \quad (6)$$

The maximum value of i_{D1} occurs at $\omega t = \pi/2$, if $\phi \le \pi/2$. However, $\phi = \pi/2$ represents a boundary condition. When ϕ is greater than $\pi/2$, the maximum of i_{D1} is not given by $di_{D1}/dt = 0$, but occurs at $\omega t = \phi$. Since the rectifier behavior is symmetrical, the peak currents are the same for D_1 and D_2 and are

$$\frac{I_{DM}}{I_O} = \begin{cases} \frac{1}{2}[1 - \frac{1}{sin(\phi+2\pi D)}], & \text{for} \quad \phi \le \pi/2 \quad (D \ge 0.28) \\ \frac{1}{2}[1 - \frac{sin\phi}{sin(\phi+2\pi D)}], & \text{for} \quad \phi > \pi/2 \quad (D < 0.28). \end{cases} \quad (7)$$

The peak value of the current normalized with respect to the output current I_{DM}/I_O is shown in Fig. 6(a) as a function of D. Its value increases when D decreases. Using (3), the ratio I_{DM}/I_O is plotted versus ωCR_L in Fig. 6 (b).



(b)

Fig. 6. Normalized peak values of diode current I_{DM}/I_O as functions of D and ωCR_L. (a) I_{DM}/I_O versus D. (b)I_{DM}/I_O versus ωCR_L.

The voltages across diodes D_1 and D_2, normalized with respect to the output voltage V_O, are given by

$$\frac{v_{D1}}{V_O} = \begin{cases} 0, & \text{for} \quad \phi < \omega t \le \phi + 2\pi D \\ \frac{1}{2\omega C_1 R_L}[(\omega t - \phi - 2\pi D) + \frac{cos\omega t - cos(\phi+2\pi D)}{sin(\phi+2\pi D)}], & \\ & \text{for} \quad \phi + 2\pi D < \omega t \le \phi + 2\pi \end{cases} \quad (8)$$

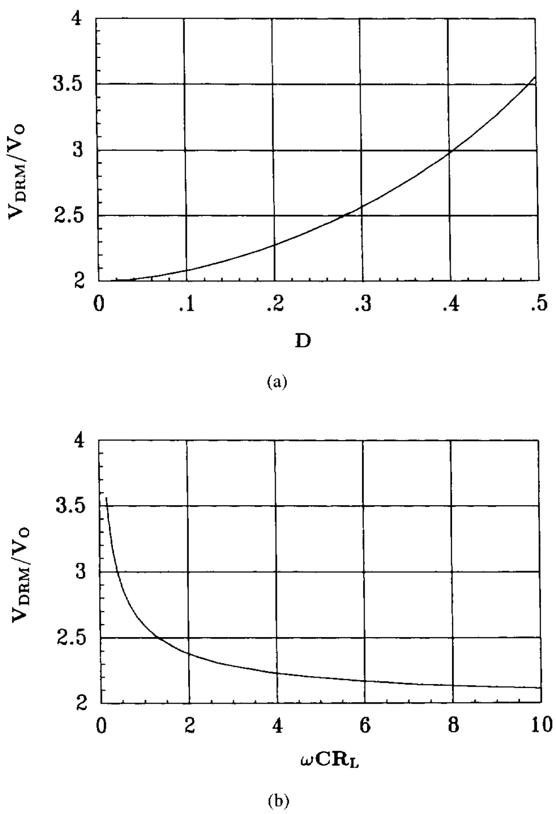


Fig. 7. Normalized peak values of diode reverse voltage V_{DRM}/V_O as functions of D and ωCR_L. (a) V_{DRM}/V_O versus$D$. (b) V_{DRM}/V_O versus ωCR_L.

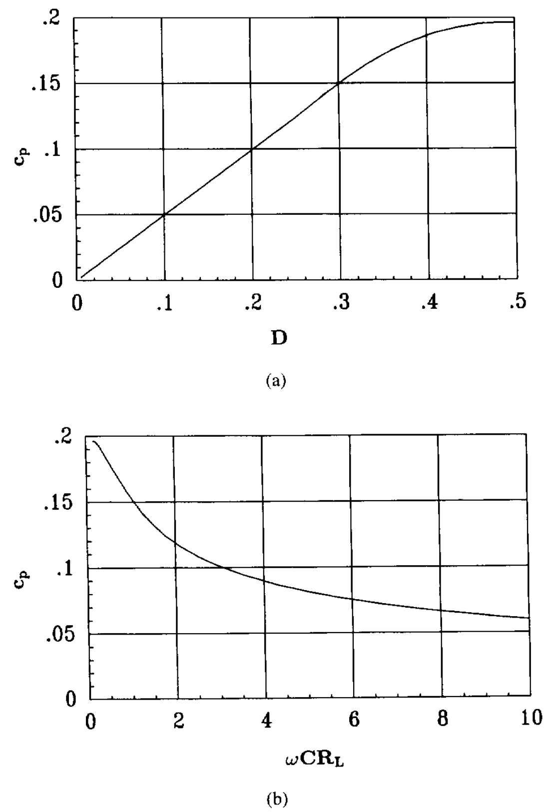


Fig. 8. Power-output power capability c_p as functions of D and ωCR_L. (a) c_p versus$D$. (b) c_p versus ωCR_L.

and

$$\frac{v_{D2}}{V_O} = \begin{cases} \frac{1}{2\omega C_2 R_L}[(\omega t - \phi - 2\pi D + \pi) - \frac{cos\omega t + cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}], \\ \qquad \text{for} \quad \phi + 2\pi D - \pi < \omega t \leq \phi + \pi \\ 0, \qquad \text{for} \quad \phi + \pi < \omega t \leq \phi + 2\pi D + \pi \\ \frac{1}{2\omega C_2 R_L}[(\omega t - \phi - 2\pi D - \pi) - \frac{cos\omega t + cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}], \\ \qquad \text{for} \quad \phi + 2\pi D + \pi \leq \omega t < \phi + 2\pi. \end{cases} \tag{9}$$

The reverse voltage across diode D_1 reaches the peak value when the current through C_1 is zero, i.e., at $\omega t = 3\pi - \phi - 2\pi D$. Substituting this value of ωt into (8), the normalized peak voltage across diode can be determined

$$\frac{V_{DRM}}{V_O} = \frac{1}{\omega CR_L}\left[\frac{3\pi}{2} - \phi - 2\pi D - cot(\phi + 2\pi D)\right]. \tag{10}$$

Using (2), (3), and (10), the normalized peak reverse voltage of the diodes can be plotted as functions of D and ωCR_L as shown in Fig. 7(a) and (b), respectively.

The normalized power-output capability is

$$c_p = \frac{I_O V_O}{I_{DM} V_{DRM}}. \tag{11}$$

Using (2) and (3), the factor c_p was computed and plotted versus D and ωCR_L in Fig. 8(a) and (b), respectively. The maximum value of c_p occurs at $D = 0.5$.

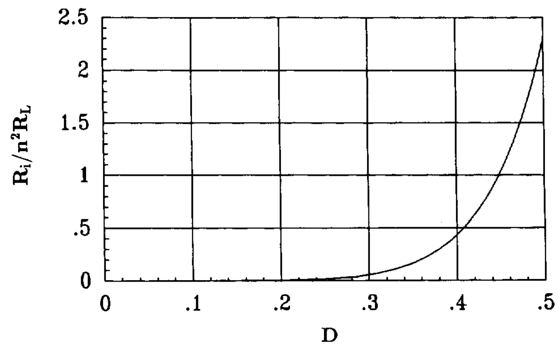
The sinusoidal current source driving the rectifier can actually be obtained using any power inverter with a series-resonant circuit. Hence, the equivalent input impedance of the rectifier at the fundamental frequency must be determined. It can be represented by a series connection of a resistance R_i and a capacitance C_i. The component of the input voltage v_i in phase with the input current i has the amplitude expressed by

$$\begin{aligned} V_{Rim} = \frac{nV_O}{\pi\omega CR_L}&[sin\phi - sin(\phi + 2\pi D) + \pi cos(\phi + 2\pi D) \\ &+ (2\pi D - \pi)cos\phi + \frac{cos\phi - cos(\phi + 2\pi D)}{tan(\phi + 2\pi D)} \\ &+ \frac{cos2(\phi + 2\pi D) - cos2\phi}{4sin(\phi + 2\pi D)}]. \end{aligned} \tag{12}$$

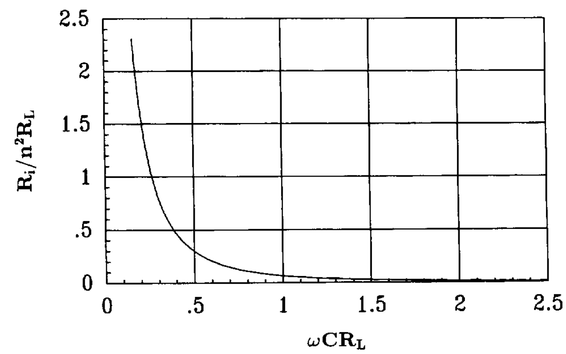
Substitution of (4) and (12) into $R_i = V_{Rim}/I_m$ gives the rectifier input resistance

$$\begin{aligned} R_i = \frac{2n^2 sin(\phi + 2\pi D)}{\pi\omega C}&[sin(\phi + 2\pi D) - sin\phi \\ &- \pi cos(\phi + 2\pi D) - (2\pi D - \pi)cos\phi \\ &- (cos\phi - cos(\phi + 2\pi D))cot(\phi + 2\pi D) \\ &- \frac{cos2(\phi + 2\pi D) - cos2\phi}{4sin(\phi + 2\pi D)}]. \end{aligned} \tag{13}$$

Using (2) and (3), both $R_i/n^2 R_L$ and $\omega CR_i/n^2$ are plotted as functions of D and ωCR_L in Fig. 9 and 10, respectively.

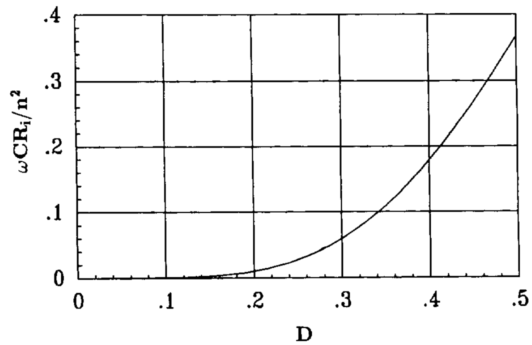


(a)

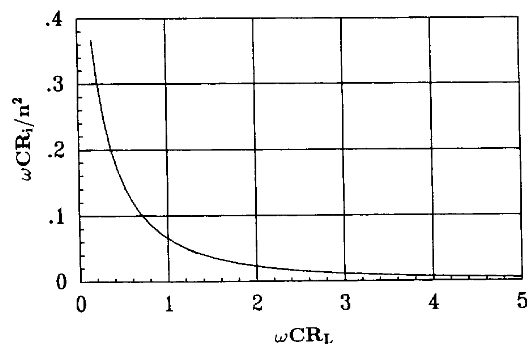


(b)

Fig. 9. Normalized input resistance R_i/n^2R_L as functions of D and ωCR_L. (a) R_i/n^2R_L versus$D$. (b) R_i/n^2R_L versus ωCR_L.



(a)



(b)

Fig. 10. Normalized input resistance$\omega_r CR_i/n^2$ as functions of D and ωCR_L. (a) $\omega_r CR_i/n^2$versus D. (b) $\omega_r CR_i/n^2$ versusωCR_L

The component of the input voltage which is 90^o out of phase with respect to the input current i has the amplitude

$$V_{Cim} = \frac{nV_O}{\pi\omega CR_L}[cos\phi + (\pi - 2\pi D)sin\phi - cot(\phi + 2\pi D)sin\phi - \pi sin(\phi + 2\pi D) + \frac{2(\pi D - \pi)}{sin(\phi + 2\pi D)} - \frac{cos(\phi + 2\pi D)}{2} + \frac{sin\phi cos\phi}{2sin(\phi + 2\pi D)}]. \tag{14}$$

Since $\omega C_i = I_m/V_{Cim}$, (4) and (14) give the rectifier input capacitance C_i normalized with respect to the parallel capacitance C

$$\frac{C_i}{C} = \frac{\pi}{2n^2 sin(\phi + 2\pi D)}[cos\phi + (\pi - 2\pi D)sin\phi - cot(\phi + 2\pi D)sin\phi - \pi sin(\phi + 2\pi D) + \frac{2(\pi - \pi D)}{sin(\phi + 2\pi D)} - \frac{cos(\phi + 2\pi D)}{2} + \frac{sin\phi cos\phi}{2sin(\phi + 2\pi D)}]^{-1}. \tag{15}$$

Substituting (2) and (3) into (15), C_i/C is expressed as functions of D and ωCR_L. Fig. 11(a) and (b) show the plots of the normalized input capacitance n^2C_i/C versus D and ωCR_L, respectively.

The ac-to-dc current transfer function is given by

$$K_i = \frac{I_O}{I_{rms}} = -2n\sqrt{2}sin(\phi + 2\pi D) \tag{16}$$

where $I_{rms} = I_m/\sqrt{2}$. The current transfer function K_i/n is plotted as functions of D and ωCR_L in Fig. 12(a) and (b), respectively.

The ac-to-dc voltage transfer function is

$$M_R = \frac{V_O}{V_{1rms}} = \frac{V_O}{n}\sqrt{\frac{2n^2}{V_{Rim}^2 + V_{Cim}^2}} \tag{17}$$

where $V_{1rms} = \sqrt{(V_{Rim}^2 + V_{Cim}^2)/2}$ is the rms value of the fundamental of the rectifier input voltage. Using (2) and (3), the ac-to-dc voltage transfer function nM_R is plotted in Fig. 13 (a) and (b) as functions of D and ωCR_L, respectively.

The rectifier transconductance is

$$G_R = \frac{I_{rms}}{V_O} = \frac{-1}{R_L 2\sqrt{2}n sin(\phi + 2\pi D)}. \tag{18}$$

Substituting (2) and (3) into (18), the transconductance nG_R is plotted in Fig.14(a) and (b) as functions of D and ωCR_L, respectively.

The conduction loss in each diode is

$$P_D = \frac{P_O}{2}\left\{\frac{V_F}{V_O} + \frac{r_F}{2R_L}\left[D + \frac{2\pi D + sin\phi cos\phi}{4\pi sin^2(\phi + 2\pi D)}\right.\right.$$

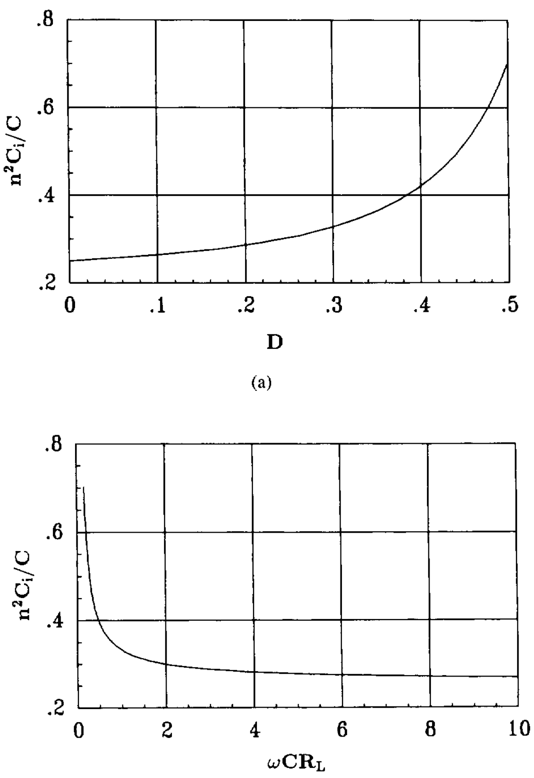


Fig. 11. Normalized input capacitance n^2C_i/C as functions of D and ωCR_L. (a) n^2C_i/C versus$D$. (b) n^2C_i/C versus ωCR_L.

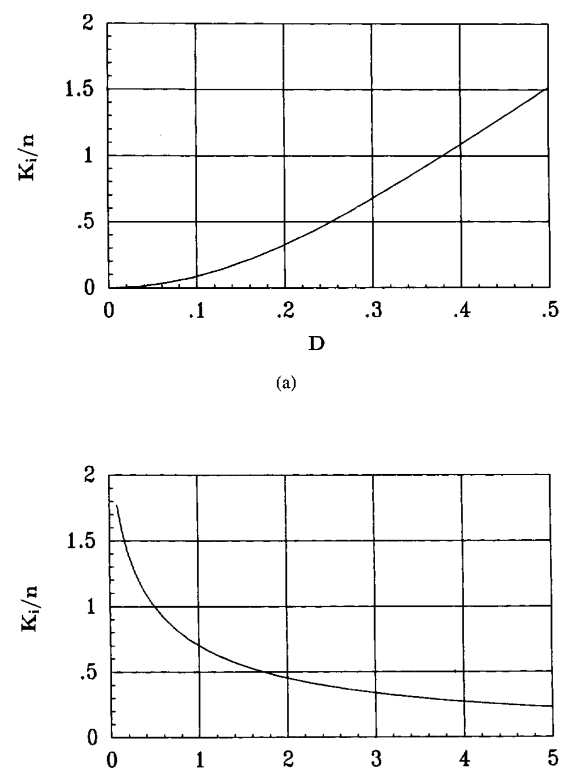


Fig. 12. Current transfer function K_i/n as functions of D and ωCR_L. (a) K_i/n versus$D$. (b) K_i/n versus ωCR_L.

$$+\frac{3}{4\pi tan(\phi+2\pi D)}-\frac{cos\phi}{\pi sin(\phi+2\pi D)}\Bigg]\Bigg\} \quad (19)$$

where V_F is the diode threshold voltage and r_F is the diode forward resistance. The loss in each parallel capacitor is

$$P_C = P_O\frac{r_{ESR}}{4R_L}\left[1-D+\frac{2\pi(1-D)-sin\phi cos\phi}{4\pi sin^2(\phi+2\pi D)}\right.$$
$$\left.-\frac{3}{4\pi tan(\phi+2\pi D)}+\frac{cos\phi}{\pi sin(\phi+2\pi D)}\right] \quad (20)$$

where r_{ESR} is the ERS of the parallel capacitor. The power loss in the ESR of the filter capacitor is ideally zero. The rectifier efficiency is

$$\eta_R = \frac{P_O}{P_O+2P_D+2P_C}. \quad (21)$$

The rectifier efficiency η_R is plotted in Fig. 15 as a function of the normalized load conductance $1/\omega CR_L$ for V_F = 0.3 V, r_F = 0.033 Ω, and r_{ESR} = 0.04 Ω. With this choice of the horizontal axis, the efficiency was easily plotted over the entire load range, that is, from no-load to full load. Note that the rectifier efficiency is almost constant for the load ranging from 10% to 100% of the full load.

The losses in the transformer windings are expressed by

$$P_{Cu} = (r_{w1}+n^2r_{w2})\frac{I_O^2}{8n^2sin^2(\phi+2\pi D)} \quad (22)$$

where r_{w1} and r_{w2} are the resistances of the primary and secondary windings, respectively. The efficiency of the transformers is

$$\eta_T = \frac{1}{1+\frac{P_{Cu}}{P_O+2P_C+2P_D}}. \quad (23)$$

The efficiency of the transformers η_T is plotted in Fig. 15 as a function of the rectifier normalized load conductance $1/\omega CR_L$ for r_{w1} + n^2r_{w2} = 0.4 Ω and n = 6. The overall efficiency of the rectifier is

$$\eta = \eta_R\eta_T = \frac{P_O}{P_O+2P_C+2P_D+P_{Cu}}. \quad (24)$$

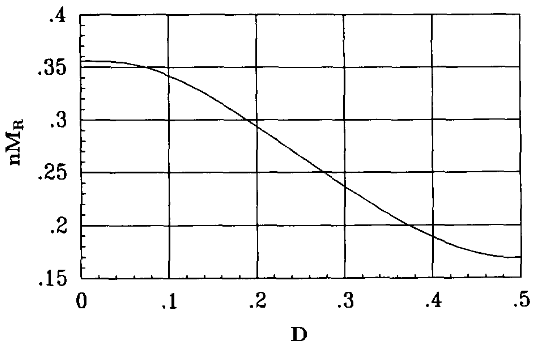
A plot of the rectifier efficiency η is depicted in Fig. 15.

Fig. 16(a) and (b) show the waveforms of the voltage v_i across the primary winding of the transformers for D = 0.5 and D = 0.3, respectively. The waveform of the input voltage v_i has low harmonic content and is almost sinusoidal for $D \leq 0.3$.

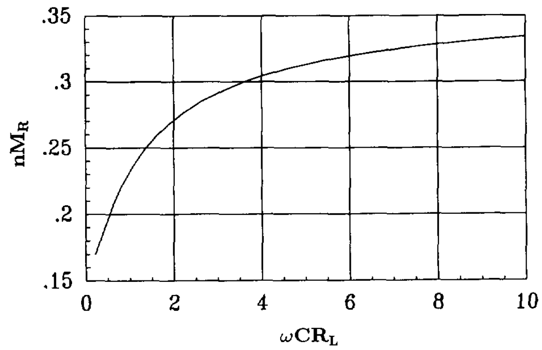
The values of the rectifier parameters are summed up for design purposes in Table I.

IV. Design Example

Design a Class E full-wave rectifier with the following specifications: V_O = 5 V and $I_{O(max)}$ = 15 A. The minimum

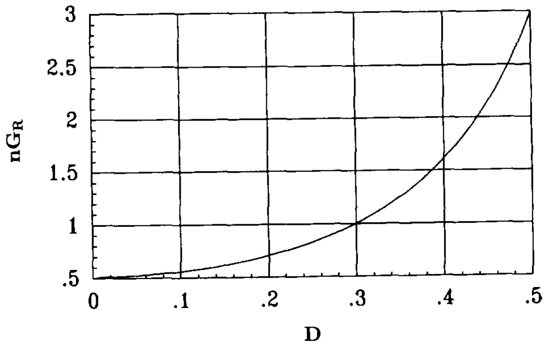


(a)

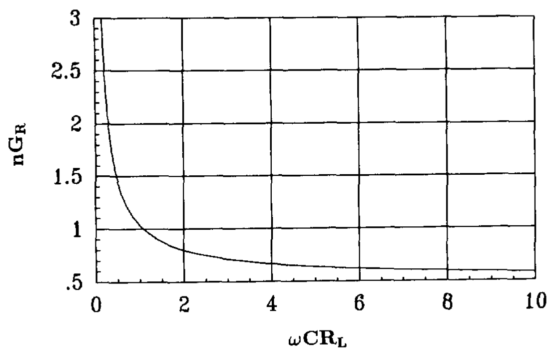


(b)

Fig. 13. Voltage transfer function nM_R as functions of D and ωCR_L. (a) nM_R versus$D$. (b) nM_R versus ωCR_L.



(a)



(b)

Fig. 14. Normalized rectifier transconductance nG_R as functions of D and ωCR_L. (a) nG_R versus$D$. (b) nG_R versus ωCR_L.

load resistance is $R_{Lmin} = V_O/I_{O(max)} = 0.33\ \Omega$ and the maximum load resistance is infinity. The maximum output power is $P_{O(max)} = V_O I_{O(max)} = 75$W. The on-duty cycle of the diodes is assumed to be $D_{max} = 0.45$ at R_{Lmin} to get a high power-output capability and to avoid overlapping of the diode conduction. Using (7), the maximum value of the diode peak current is $I_{DM} = 1.654 I_O = 24.81$ A. From (10), the maximum value of the diode reverse voltage is $V_{DRM} = 3.345 V_O = 16.725$ V. Substitution of $D = 0.45$ into (3) yields $\omega CR_L = 0.241$. Assuming $f = 1$ MHz, we have $C_1 = C_2 = 0.241/\omega R_L = 114$ nF. The filter capacitor C_f is chosen to be 1 nF.

V. Experimental Verification

To verify the results obtained from the theoretical analysis, a rectifier with the ratings given in Section IV was constructed and tested. The input current source was obtained by employing a Class E inverter coupled to the rectifier with two transformers built on EFD30 Siemens N49 ferrite cores. The primary winding of each transformer was obtained using 12 turns of litz wire with a total cross-sectional area of 0.47 mm^2. The secondary winding of each device was built using 2 turns of a copper strip 15 mm wide and 0.12 mm high. Two Motorola Schottky MBR4035 diodes were used. The mean value of the diode current was overrated to reduce the diode forward voltage drop. The Schottky diode parasitic capacitances were included in the externally connected capacitors, each obtained by paralleling four 22 nF and two 10 nF Murata NPO capacitors. The NPO devices were used because their operating temperature is up to 95°C.

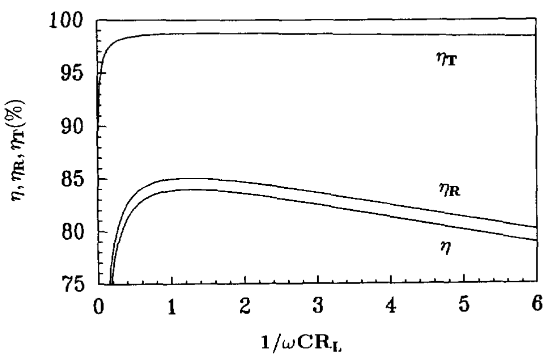


Fig. 15. Transformer efficiency η_T, rectifier efficiency η_R, and overall efficiency η as a function of $1/\omega CR_L$.

Fig. 17 displays an experimental waveform of the input voltage v_i at $V_O = 5$ V, $I_O = 8$ A, and $f = 0.922$ MHz. Fig. 18 shows an experimental waveform of the diode voltage at $V_O = 5$ V, $I_O = 15$ A, and $D = 0.45$. The peak diode voltage was $V_{DM} = 18$ V, while the predicted one was $V_{DM} = 16.7$

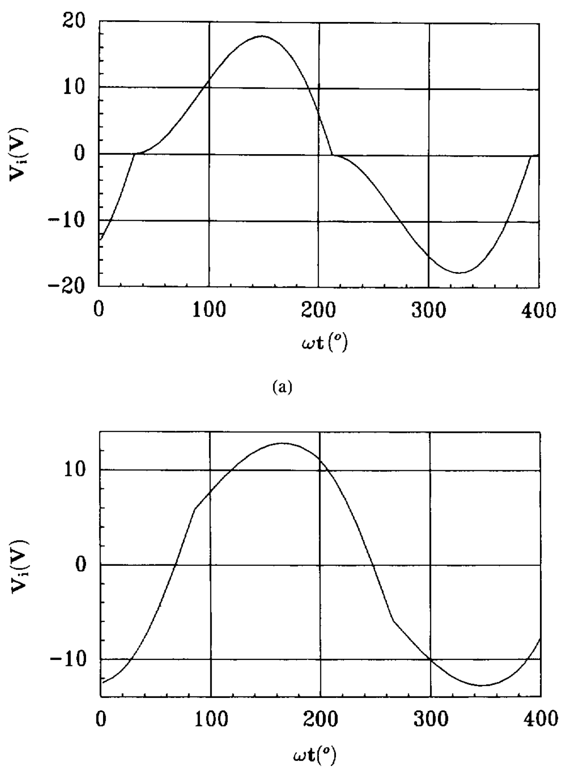


Fig. 16. Waveform of the rectifier input voltage v_i. (a) At D = 0.5. (b) At $D = 0.3$.

TABLE I
PARAMETERS OF CLASS E FULL-WAVE LOW *dv/dt* RECTIFIER

D	ϕ (°)	ωCR_L	I_{DM}/I_O	V_{DRM}/V_O	R_i/n^2R_L	$\omega_r CR_i/n^2$	n^2C_i/C	K_i/n	c_p
0	180.00	∞	∞	2	0	0	0.251	0	0
0.05	160.32	62.669	19.84	2.022	2.01×10^{-7}	1.3×10^{-5}	0.256	0.022	0.025
0.1	143.85	14.982	9.702	2.079	2.5×10^{-5}	0.0004	0.264	0.086	0.049
0.15	128.14	6.199	6.241	2.164	0.001	0.003	0.273	0.189	0.074
0.2	113.10	3.165	4.459	2.273	0.003	0.001	0.286	0.324	0.099
0.25	98.63	1.793	3.356	2.406	0.015	0.027	0.303	0.488	0.124
0.3	84.63	1.247	2.731	2.566	0.058	0.059	0.327	0.672	0.144
0.35	71.04	0.729	2.201	2.754	0.163	0.109	0.364	0.873	0.167
0.4	57.78	0.546	1.857	2.976	0.431	0.178	0.420	1.084	0.183
0.45	44.80	0.241	1.654	3.241	1.032	0.266	0.516	1.301	0.193
0.5	32.06	0.176	1.458	3.562	2.307	0.362	0.703	1.519	0.196

V, resulting in an error of 7%. Note that there were no oscillations because the parasitic capacitances of the diodes do not adversely affect the rectifier operation. A comparison of theoretical and experimental plots of the diode peak voltage is displayed in Fig. 19. Fig. 20 depicts plots of the calculated and measured rms input current.

VI. CONCLUSIONS

A detailed analysis and experimental tests of a Class E full-wave rectifier have been presented. The results predicted theoretically are in good agreement with the experimental tests.

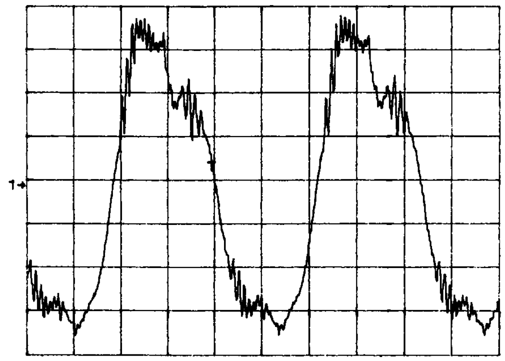


Fig. 17. Experimental waveform of the rectifier input voltage v_i at V_O = 5 V, I_O = 8 A, and f = 0.922 MHz. Vertical: 10 V/div.; horizontal: 250 ns/div.

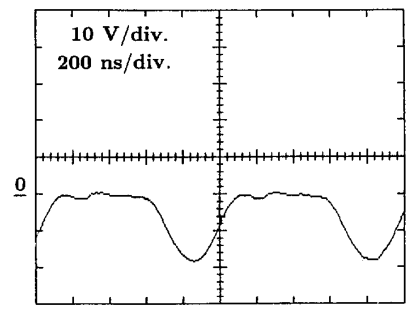


Fig. 18. Experimental waveform of the voltage across diode D_1 at at V_O = 5 V, I_O = 15 A, f = 1.02 MHz, and D = 0.45.

The full-wave rectifier offers several advantages over the Class E half-wave rectifier. It has lower losses, lower THD, and theoretically zero-ripple output voltage. Common features of the Class E rectifiers are as follows. First, the diodes turn on with low dv/dt and turn off at zero current with low dv/dt and low di/dt. Second, current or voltage waveforms do not overlap at the diode transitions, thus significantly reducing the switching losses. Switching losses are also reduced because the reverse-recovery charge effect in pn junction diodes is reduced by the limited value of di/dt at the diode turn-off. Third, the noise level produced by the circuit is drastically reduced by the limited values of the derivatives of the diode current and voltage waveforms at the switching times. Finally, the detrimental effects of the Schottky diode parasitic capacitances are completely overcome by the parallel connection of external capacitors. Consequently, the Class E rectifiers are neither affected by the parasitic oscillations nor by switching losses which take place in a traditional rectifier.

Since the average current in each diode of the Class E full-wave circuit is one-half of that through the diode of the Class E half-wave rectifier, conduction losses in the former circuit are about one-half of those in the latter. Moreover, the Class E full-wave circuit has theoretically zero ac component of the output current. Actually, the ac component of the output current is about 10 times lower than in the half-wave circuit, and hence, losses in the filter capacitor are reduced 100 times lower. Also, diode conduction losses are lower than in the Class E half-wave rectifier. The efficiency is relatively high

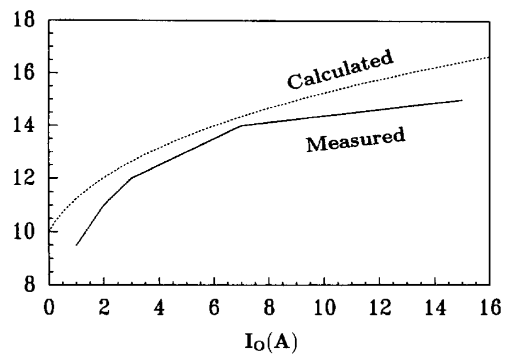


Fig. 19. Measured and calculated maximum voltage across the diodes V_{DRM} as a function of the load current I_O.

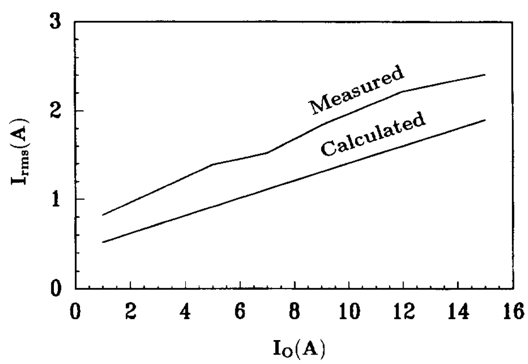


Fig. 20. Measured and calculated rectifier input rms current as a function of the load current I_O.

and almost constant for an output current ranging from 10% to 100% of the full load. Also, the Class E full-wave circuit has a low THD. Because of these features, the rectifier is particularly suitable for high-frequency, high-power density applications requiring a low-output voltage and high-output current. To achieve the proper operation of the rectifier, the circuit must be symmetrical. Hence, the leakage inductances of the transformers must be controlled. This could represent a drawback in the practical realization of the rectifier circuit. Analysis and characterization of dc–dc converters including the Class E full-wave rectifier topologies are recommended for future research.

Appendix: Derivation of Design Equations

Referring to Fig. 1, the primary winding of the transformers is driven by a sinusoidal current source given by (1). This current is reflected to the secondary winding of the full-wave transformers, which can be represented by two secondary magnetizing inductances and two current sources given by

$$i_1 = ni = nI_m sin\omega t \quad (25)$$

and

$$i_2 = -ni = -nI_m sin\omega t. \quad (26)$$

The currents through the secondary magnetizing inductances are equal and expressed by

$$i_L = \frac{I_O}{2}. \quad (27)$$

Using (25), (26), and (27), one obtains the current flowing through the parallel combination D_1–C_1

$$i_{C1} + i_{D1} = \frac{I_O}{2} + nI_m sin\omega t \quad (28)$$

and the current through the parallel combination D_2–C_2

$$i_{C2} + i_{D2} = \frac{I_O}{2} - nI_m sin\omega t. \quad (29)$$

A. Mode I: $\phi < \omega t \leq \phi + 2\pi D$

During this time interval, diode D_1 is on and, therefore, the capacitor current i_{C1} is zero. Hence, the diode current is given by (28). Diode D_1 turns off at the end of the first topological mode, when its current reaches zero, i.e., $i_{D1}(\phi + 2\pi D) = 0$. Thus, from (28) one arrives at (4). Substitution of (4) into (28) yields the diode current i_{D1} given by (5). During this phase, D_2 is off and the current through capacitor C_2 is given by

$$i_{C2} = \frac{I_O}{2} - nI_m sin\omega t = \frac{I_O}{2}\left[1 + \frac{sin\omega t}{sin(\phi + 2\pi D)}\right]. \quad (30)$$

Though the first topological mode begins at $\omega t = \phi$, the voltage across the parallel combination D_2–C_2 is zero when $\omega t = \phi + 2\pi D - \pi$, i.e., $v_{C2}(\phi + 2\pi D - \pi) = 0$. Thus, the voltage waveform across the combination C_2–D_2 is

$$\begin{aligned} v_{C2} &= v_{D2} = \frac{1}{\omega C_2}\int_{\phi+2\pi D-\pi}^{\omega t} i_{C2}(\omega t)d(\omega t) \\ &= \frac{1}{\omega C_2}\int_{\phi+2\pi D-\pi}^{\omega t} \frac{I_O}{2}\left[1 + \frac{sin\omega t}{sin(\phi + 2\pi D)}\right]d(\omega t) \\ &= \frac{I_O}{2\omega C_2}\left[(\omega t - \phi - 2\pi D + \pi) - \frac{cos\omega t + cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}\right]. \end{aligned} \quad (31)$$

Substitution of $I_O = V_O/R_L$ into (31) yields (9).

B. Mode II: $\phi + 2\pi D < \omega t \leq \phi + \pi$

This topological mode begins with the turn-off of D_1. The current flows through C_1 and, according to (28) and (4), is given by

$$i_{C1} = \frac{I_O}{2}\left[1 - \frac{sin\omega t}{sin(\phi + 2\pi D)}\right]. \quad (32)$$

Since $v_{C1}(\phi + 2\pi D) = 0$, as shown in Fig. 3, the voltage across the parallel combination D_1–C_1 is expressed by

$$\begin{aligned} v_{C1} = v_{D1} &= \frac{1}{\omega C_1}\int_{\phi+2\pi D}^{\omega t} i_{C1}(\omega t)d(\omega t) \\ &= \frac{1}{\omega C_1}\int_{\phi+2\pi D}^{\omega t} \frac{I_O}{2}\left[1 - \frac{sin\omega t}{sin(\phi + 2\pi D)}\right]d(\omega t) \\ &= \frac{I_O}{2\omega C_2}\left[(\omega t - \phi - 2\pi D) - \frac{cos\omega t - cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}\right] \end{aligned} \quad (33)$$

which gives (8). In the lower section of the rectifier, diode D_2 is still off and the current through C_2 is given by (30).

C. Mode III: $\phi + \pi < \omega t \leq \phi + \pi + 2\pi D$

At the beginning of mode III, diode D_2 is turned on. Hence, (30) represents the current i_{D2}, yielding (6). The current and voltage of C_1 are still expressed by (32) and (33), respectively.

D. Mode IV: $\phi + \pi + 2\pi D < \omega t \leq \phi + 2\pi$

During this time interval D_2 is off and, therefore, the current through C_2 is given by (30). Since $v_{D2}(\phi + 2\pi D + \pi) = 0$, the equation of the voltage waveform across the parallel combination D_2–C_2 is

$$\begin{aligned} v_{C2} &= v_{D2} = \frac{1}{\omega C_2}\int_{\phi+2\pi D+\pi}^{\omega t} i_{C2}(\omega t)d(\omega t) \\ &= \frac{1}{\omega C_2}\int_{\phi+2\pi D+\pi}^{\omega t} \frac{I_O}{2}\left[1 + \frac{sin\omega t}{sin(\phi + 2\pi D)}\right]d(\omega t) \\ &= \frac{I_O}{2\omega C_2}\left[(\omega t - \phi - 2\pi D - \pi) - \frac{cos\omega t + cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}\right] \end{aligned} \tag{34}$$

which gives (9). The current and the voltage of D_1 and C_1 are still given by (33) and (32). Diode D_1 turns on at zero voltage at the end of this time. Using (8) and the fact that $v_{D1}(\phi + 2\pi) = 0$, one arrives at (2).

The average reverse voltage across D_1 is expressed by

$$\begin{aligned} -V_O = V_{D(av)} &= \frac{1}{2\pi}\int_{\phi+2\pi D}^{\phi+2\pi} v_{D1}(\omega t)d(\omega t) \\ &= \frac{V_O}{4\pi\omega C_1 R_L}\Big[2\pi^2(1-D)^2 - 1 \\ &\quad - 2\pi(1-D)cot(2\pi D + \phi) + \frac{sin\phi}{sin(2\pi D + \phi)}\Big]. \end{aligned} \tag{35}$$

Simplifying (35) gives (3).

As stated before, the rectifier input impedance is given by a series connection of a resistance R_i and a capacitance C_i. Their values can be evaluated at the operating frequency considering the input voltage of the rectifier given by different expressions, according to the topological configurations the circuit goes through during one switching period. Thus,

$$\begin{aligned} v_i &= -nv_{D2} \\ &= \frac{-nV_O}{2\omega C R_L}\left[\omega t - \phi - 2\pi D + \pi - \frac{cos\omega t + cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}\right], \\ &\qquad \text{for} \quad \phi < \omega t \leq \phi + 2\pi D \end{aligned} \tag{36}$$

$$v_i = n(v_{D1} - v_{D2}) = \frac{nV_O}{2\omega C R_L}\left[\pi + \frac{2cos\omega t}{sin(\phi + 2\pi D)}\right], \quad \text{for} \quad \phi + 2\pi D < \omega t \leq \phi + \pi \tag{37}$$

$$\begin{aligned} v_i &= nv_{D1} \\ &= \frac{nV_O}{2\omega C R_L}\left[\omega t - \phi - 2\pi D + \frac{cos\omega t - cos(\phi + 2\pi D)}{sin(\phi + 2\pi D)}\right], \\ &\qquad \text{for} \quad \phi + \pi < \omega t \leq \phi + \pi + 2\pi D \end{aligned} \tag{38}$$

$$v_i = n(v_{D1} - v_{D2}) = \frac{nV_O}{2\omega C R_L}\left[\pi + \frac{2cos\omega t}{2sin(\phi + 2\pi D)}\right], \quad \text{for} \quad \phi + \pi + 2\pi D < \omega t \leq \phi + 2\pi. \tag{39}$$

Using (36)–(39) and Fourier expansion, the fundamental component of the input voltage becomes

$$\begin{aligned} v_{i1} &= V_{Rim} sin\omega t + V_{Cim} sin\left(\omega t + \frac{\pi}{2}\right) \\ &= V_{Rim} sin\omega t - V_{Cim} cos\omega t \end{aligned} \tag{40}$$

and the amplitude V_{Rim} is expressed by

$$V_{Rim} = \frac{1}{\pi}\int_{\phi}^{\phi+2\pi} v_i sin\omega t d(\omega t). \tag{41}$$

Substitution of (36)–(38) into (41) gives (12).

The amplitude V_{Cim} is given by

$$V_{Cim} = \frac{1}{\pi}\int_{\phi}^{\phi+2\pi} v_i cos\omega t d(\omega t). \tag{42}$$

Using (36)–(38), one arrives at (14).

The conduction loss of each diode is given by

$$P_D = \frac{V_F I_O}{2} + r_F I_{Drms}^2 \tag{43}$$

where I_{Drms} is the rms value of the diode current. From (5), the rms value of diode current is found as

$$\begin{aligned} I_{Drms} &= \sqrt{\frac{1}{2\pi}\int_{\phi}^{\phi+2\pi D}\left[\frac{I_O}{2}(1 - \frac{sin\omega t}{sin(\phi + 2\pi D)})\right]^2 d(\omega t)} \\ &= \frac{I_O}{2}\Big[D + \frac{2\pi D + sin\phi cos\phi}{4\pi sin^2(\phi + 2\pi D)} + \frac{3}{4\pi tan(\phi + 2\pi D)} \\ &\quad - \frac{cos\phi}{\pi sin(\phi + 2\pi D)}\Big]^{1/2} \end{aligned} \tag{44}$$

Substitution of this into (43) gives

$$\begin{aligned} P_D = \frac{V_F I_O}{2} + \frac{r_F I_O^2}{4}\Big[D &+ \frac{D}{2sin^2(\phi + 2\pi D)} \\ &+ \frac{3}{4\pi tan(\phi + 2\pi D)} - \frac{cos\phi}{\pi sin(\phi + 2\pi D)} \\ &+ \frac{sin\phi cos\phi}{4\pi sin^2(\phi + 2\pi D)}\Big]. \end{aligned} \tag{45}$$

Using $P_O = V_O I_O = R_L I_O^2$, one obtains (19). The loss in each parallel capacitor is expressed by

$$P_C = r_{ESR} I_{Crms}^2. \tag{46}$$

Using (5), the rms value of the current through the parallel capacitance C_1 is given by

$$I_{Crms} = \sqrt{\frac{1}{2\pi}\int_{\phi+2\pi D}^{\phi+2\pi}\left[\frac{I_O}{2}(1-\frac{sin\omega t}{sin(\phi+2\pi D)})\right]^2 d(\omega t)}$$
$$= \frac{I_O}{2}\left[1 - D + \frac{1-D}{2sin^2(\phi+2\pi D)} - \frac{3}{4\pi tan(\phi+2\pi D)} + \frac{cos\phi}{\pi sin(\phi+2\pi D)} - \frac{sin\phi cos\phi}{4\pi sin^2(\phi+2\pi D)}\right]^{1/2} \quad (47)$$

Using (46) and substituting $P_O = R_L I_O^2$, one can find (20). The losses in the transformer windings are

$$P_{Cu} = (r_{w1} + n^2 r_{w2})\frac{I_m^2}{2}. \quad (48)$$

Substitution of (4) into this equation gives (22).

The efficiency of the transformers is expressed by

$$\eta_T = \frac{P_{To}}{P_{Ti}} \quad (49)$$

where P_{To} is the transformer output power and P_{Ti} is the transformer input power. Neglecting the core losses, we have

$$P_{Ti} = P_{To} + P_{Cu} = P_O + 2P_D + 2P_C + P_{Cu}. \quad (50)$$

Substitution of this into (49) yields (23).

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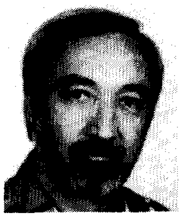

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