Clock Gated Single-Edge-Triggered Flip-Flop Design with Improved Power for Low Data Activity Applications

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Abstract: In this paper, the proposed flip-flop reduces power consumption by reducing the clock switching power that was wasted otherwise. Unlike many other gated flip-flops, the proposed gated flip-flop has state retention property to save power and to switch circuit between idle and active modes smoothly. The feedback path is also improved in the proposed flip-flop to decrease power dissipation. The proposed clock-gating scheme only requires 4 transistors, thus occupies the small silicon area. Further, the proposed clock gating network can be shared among a group of flip-flops to reduce the power and area overhead of the gating network. The simulation results show that for all supply voltages, the proposed flip-flop has the least power dissipation among all the designs for low switching activities. The proposed flip-flop has up to 7.82 times power improvement than the existing flip-flops. However, for 100% data activity, the proposed FF consumes up to 2.71 times power than the existing flip-flops. The proposed clock gated flip-flop structure is best suited for applications where input signal switching activity is low and speed is not a crucial factor.

Keywords: Low power, CMOS digital integrated circuits, transition probability, edge triggered, storage element, VLSI

1. Introduction

The rapid scaling of silicon technology has enabled designers to integrate millions and even billions of transistors into a single chip. However, while the performance increases due to scaling, the power density increases substantially every generation due to higher integration density [1]-[4]. The latest advances in mobile battery-powered devices also have set new goals in digital VLSI design. These devices require high speed and low power consumption. So, the low power design is must for the applications operated by batteries such as pocket calculators, wrist watches, mobile phones, laptops etc. It is important to prolong the battery life as much as possible [5]-[8].

All three types of power (switching power, short-circuit power and leakage power) depend upon supply voltage. The switching power of the digital chips is generally the largest portion of the power dissipation and is proportional to the square of the supply voltage. Hence, reduction of supply voltage (V_{DD}) is the most efficient way of reducing power consumption [9]-[11]. Unfortunately, supply voltage cannot be decreased without bound. As supply voltage is lowered, circuit delays increase leading to reduced system performance. Now power reduction is treated at all design levels of VLSI chips, from architecture through block and logic levels, down to gate-level, circuit and physical implementation [12]. To minimize the power consumption, many low-power design techniques have been introduced such as power gating [13], [14], replacing non-timing-critical cells with their high-threshold voltage counter parts [15], [16], dynamic voltage/frequency scaling [17]-[19] and clock gating [20], [21]. Among these techniques, clock gating is very important in reducing dynamic power consumption of a system on chip (SoC).

Flip-flops and latches are heavily studied circuits, as they have a large impact on both cycle time and energy consumption in modern synchronous systems [22], [23]. A conventional Application Specific Integrated Circuit (ASIC) design mainly uses an edge-triggered flip-flop as a sequencing element because of the simplicity of flip-flop's timing model. Specifically, the amount of time available to a combinational block that lies between two flip flops is fixed. This constrains timing uncertainties within each combinational block [24]. The flip flops are used extensively in all kinds of digital designs as the basic storage elements. In particular, digital designs nowadays often adopt

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intensive pipelining techniques and employ many flip flops rich modules such as register file, shift register and FIFO [25], [26]. In many digital VLSI designs, the clock system that includes clock distribution network and flip-flops is one of the highest power consuming components. It accounts for 30% to 60% of the total system power, out of which 90% is consumed by the flip-flops and the last branches of the clock distribution network that are driving the flip-flops. As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in both clock distribution networks and flip-flops [27]. This paper focuses on the minimization of power dissipation in both clock distribution network and the edge-triggered flip-flop.

Clock power is a key design constraint in modern VLSI design. Despite increases in leakage power, clock power remains a significant part of the total power dissipation in modern microprocessors [28]. As timing components, flip-flops capture data with the active edge of the clock signal. Sometimes this capture is not required due to unchanged data value. Because of the constant activity of the clock signal, timing components (i.e., latches and flip-flops) are the most power-consuming components in the VLSI system [29]-[31]. Disabling the clock signal (clock gating) while the input data value matches the current state is the most obvious power reduction method. So clock-gating techniques [32] have been developed to disable unnecessary clock switching when there is no change on the input to the flip-flop. Traditionally, the system clock is connected to the clock pin on every flip-flop in the design. This results in three major components of power consumption:

- Power consumed by combinatorial logic whose values are changing on each clock edge.
- Power consumed by flip-flops – this has a non-zero value even if the inputs to the flip-flops are steady and the internal state of the flip-flops is constant.
- Power consumed by the clock buffer tree in the design.

Clock gating has the potential of reducing both the power consumed by flip-flops and the power consumed by the clock distribution network [33]. Clock gating works by identifying groups of flip-flops sharing a common enable signal (which indicates that a new value should be clocked into the flip-flops). This enable signal is ANDed with the clock to generate the gated clock, which is fed to the clock input of all of the flip-flops that have the common enable signal. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Gated clock contributes to clock skew and is also sensitive to glitches, which can cause design failure. So, there are several considerations in implementing clock gating. First, the enable signal should remain stable when clock is high and can only switch when clock is in low phase. Second, in order to guarantee correct functioning of the logic implementation after the gated-clock, it should be turned on in time and glitches on the gated clock should be avoided. Third, the AND gate may result in additional clock skew. For high-performance design with short-clock cycle time, the clock skew could be significant and needs to be taken into careful consideration. Clock gating network also introduces delay that affects timing performance. So, the delay in the clock gating network should be taken into careful consideration.

The rest of this paper is organized as follows. Section 2 reviews previous designs of SETFFs. The proposed Clock gated SET flip-flop is discussed in section 3. Section 4 shows the simulation conditions. Section 5 shows the results and comparison. The conclusion is given in the last section.

2. Conventional Single-Edge-Triggered Flip-Flops

To improve the performance of a conventional Transmission Gate Flip-Flop (TGFF shown in Figure 1) [34], [35], an inverter and transmission gate is added in [36] between the output of master latch and the output of slave latch to accomplish a push–pull effect at the slave latch. The static Push Pull Flip-Flop (PPFF) is shown in Figure 2. This increased 4 transistors. To compensate this increment of transistor count, two transmission gates are eliminated in the Push Pull Flip-Flop from the feedback paths of conventional TGFF. To save power, the number of transistors of the proposed flip-flop was reduced in [37]. The four transistors in the feedback path of conventional TGFF are replaced by single PMOS transistor. Hence, total 6 transistors are reduced in this flip-flop. This semi-static Pass Flip-Flop (Pass FF) is shown in Figure 3. To activate the feedback path of pass FF only during OFF cycle, a PMOS transistor was added in the feedback in [37]. This semi-static Pass

Isolation Flip-Flop (PIFF) is shown in Figure 4. As compare to Pass FF, the number of transistors of this flip-flop is increased by two but this reduces short circuit current during ON cycle. It also improves speed as compare to Pass FF.

To reduce the area of the conventional TGFF, [38] removed the two feedback transmission gates of conventional TGFF. This Low-Area Flip-Flop (LAFF) is shown in Figure 5. The Area Efficient Flip-Flop (AEFF) was proposed in [39]. This semi-static flip-flop is illustrated in Figure 6. In this design the feedback circuit of the master section is removed and in slave section, feedback loop consists of a transmission gate. In Low Voltage Flip Flop (LVFF), a feedback is provided from the output node of the slave inverter to a specific internal node in the master-stage as shown in Figure 7. This flip-flop was proposed by [40]. This feedback is provided by only a single transistor. So this has lesser number of transistor as compare to other flip flops. Figure 8 shows the static C^2MOS Flip-Flop [41]. This flip-flop consists of a C^2MOS feedback at the outputs of the master and the slave latches. There are 20 transistors in this circuit. So C^2MOSFF has largest area but this flip-flop shows the shortest delay. Area and Power Efficient Flip-Flop (APEFF), proposed by [42], is shown in Figure 9. In this flip-flop, an NMOS transistor with complemented clock signal is used to make feedback path functional only during OFF cycle of the clock. This reduces short circuit current during ON cycle. To reduce the number of transistor, only NMOS transistor is used in both master and slave latches.

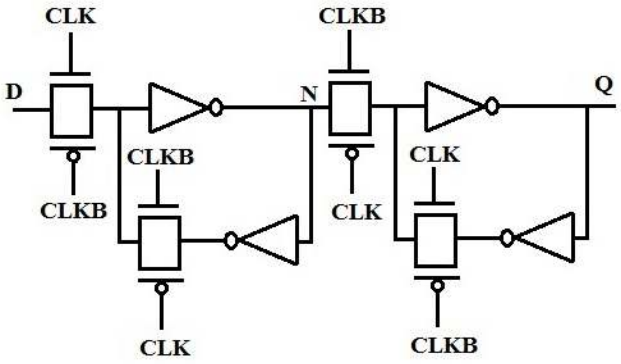

Figure 1. Conventional Transmission Gate Flip-Flop (TGFF)

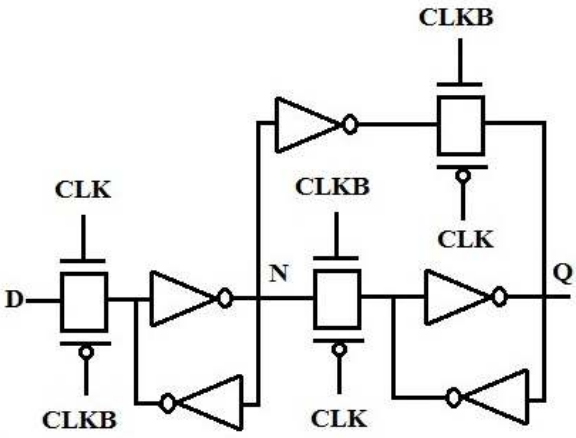

Figure 2. Push Pull Flip-Flop (PPFF)

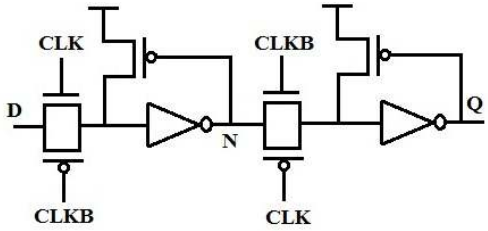

Figure 3. Pass Flip-Flop (Pass FF)

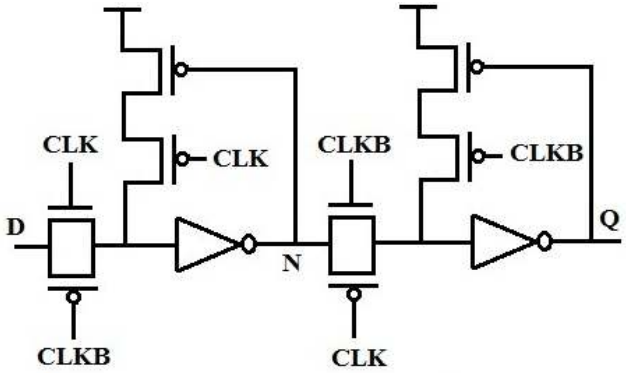

Figure 4. Pass Isolation Flip-Flop (PIFF)

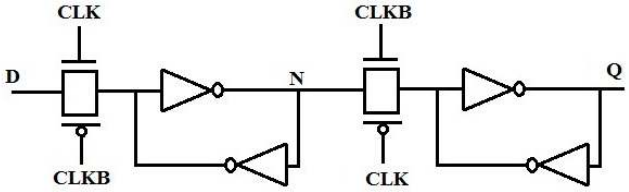

Figure 5. Low Area Flip-Flop (LAFF)

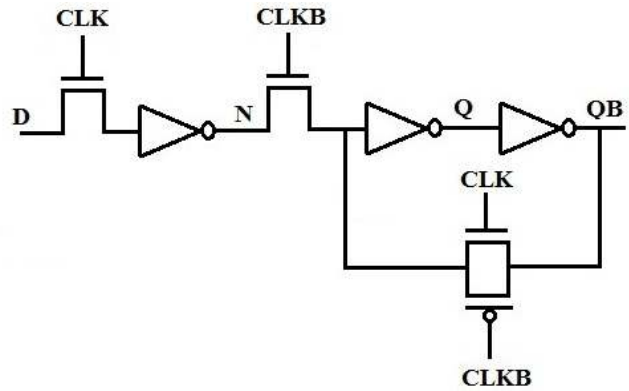

Figure 6. Area Efficient Flip-Flop (AEFF)

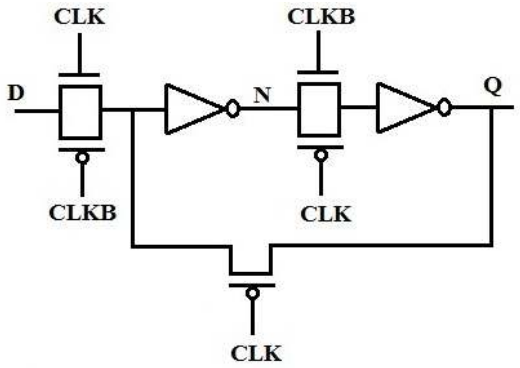

Figure 7. Low Voltage Flip-Flop (LVFF)

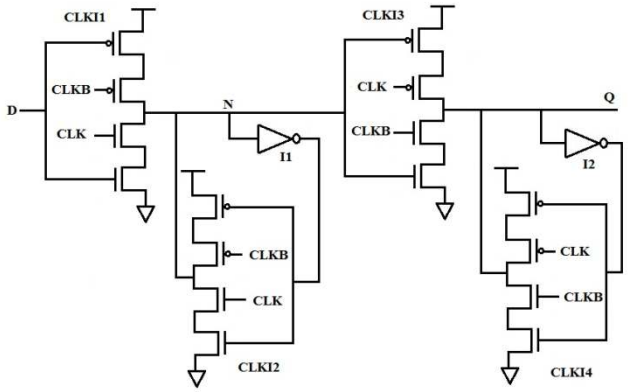

Figure 8. C^2MOS Flip-Flop (C^2MOS FF)

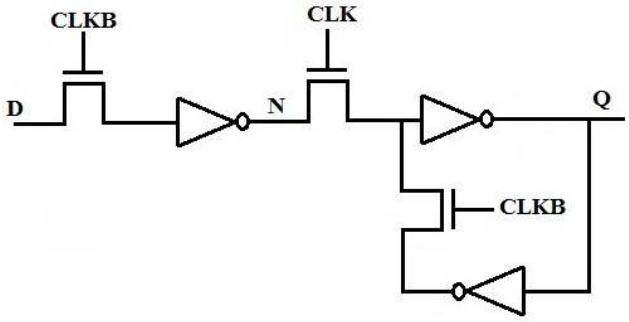

Figure 9. Area and Power Efficient Flip-Flop (APEFF)

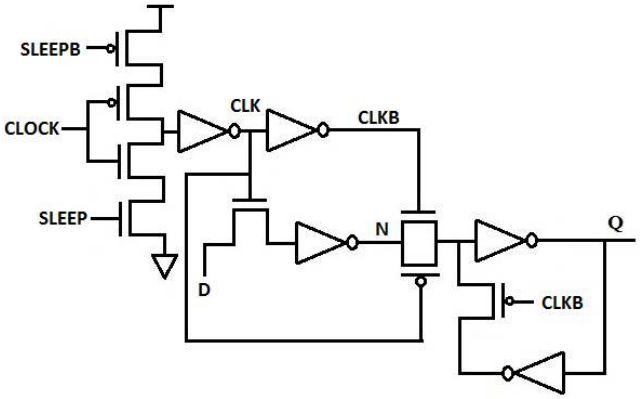

Figure 10. Proposed Clock Gated SET Flip- Flop

3. Proposed Clock Gated Single-Edge-Triggered Flip-Flop Design

In this paper, a new clock gated single-edge-triggered flip-flop has been developed. The clock gating technique avoids unnecessary power dissipation from clock switching. Clock gating has been shown to be an efficient technique to significantly reduce dynamic power dissipation [43]-[45]. The proposed flip-flop reduces power consumption by reducing clock switching. The feedback path is also improved in the proposed flip-flop to reduce the power consumption. The feedback loop is needed because of the drop due to the threshold of the transistors and due to the leakage in the capacitors of the transistors. Many gated flip-flops like [46] may present problem when the Control/Sleep signal is low. In these conditions the output node of the flip-flop is in a dynamic memory state and there is no possibility of any refresh operation until the sleep signals remains low. This means that sleep condition can be maintained for no more than few milliseconds. If the sleep condition is maintained for longer times:

1) The flip-flop state may not be correctly maintained during sleep
2) The transistors driven by Q output within the flip-flop and all other gates driven by the output Q could result in a large short circuit power dissipation.

Using SETFFs with state retention property makes it possible to save power and switch circuit between idle and active modes smoothly. The proposed flip-flop has state retention property. In this structure, the circuit can be switched between idle and active modes smoothly. Most of the conventional static designs use two feedback loops one each in the master as well as the slave stage. This increases the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. This also results in total chip area overhead due to increased transistor count [47]. In the proposed flip-flop, the feedback of master section is removed and in slave section a PMOS transistor with an inverter is used to make the flip-flop semi-static in nature. So, the feedback path is improved in the proposed flip-flop. This PMOS is grounded, so this transistor is permanently ON to reduce the switched capacitance. This further improves the power efficiency of the proposed flip-flop. In the slave latch of the proposed flip-flop, the transmission gate is used to overcome the drawbacks of the pass transistors to make the output signal clean and stable. This flip-flop is negative edge-triggered flip-flop. In Figure 10, when SLEEP input is logic LOW (SLEEPB is logic HIGH), clock is disabled and disconnected from the main circuit. When SLEEP is logic HIGH (SLEEPB is logic LOW), clock is connected to the main circuit and the circuit works in normal mode. This can be expressed mathematically by the following equations:

$$CLOCK\ STOPED\ and\ Q_{n+1} = \begin{matrix} if\ SLEEP = 0, \\ Q_n \\ if\ SLEEP = 1, \end{matrix} \quad (1)$$

$$CLOCK\ ACTIVATED\ and\ Q_{n+1} = \begin{Bmatrix} D\ when\ negedge\ clk \\ Q_n\ \ otherwise \end{Bmatrix} \quad (2)$$

The gated clock signal encodes whether the flip-flop retains its earlier value or takes a new input value. In the proposed FF when gated clock level is 'HIGH', master latch is activated and inverse of the data is stored to an intermediate node N (output of master latch). When gated clock goes to 'LOW' logic level, slave latch becomes functional and produces data at the output Q.

Clock-gating can also help to reduce leakage power, which has an exponential dependence on the temperature [48]. Since dynamic power is reduced, the local temperature will decrease, resulting in lower leakage power. Thus leakage power is also reduced in the proposed flip-flop. The proposed clock-gating scheme only requires 4 transistors, thereby occupying less silicon area. Further, the proposed clock gating network can be shared among a group of flip-flops to reduce the power and area overhead of the gating network. If clock gating network is shared among a group of flip-flops, the result would improve drastically. Even for a single flip-flop, the proposed circuit has good improvement in power consumption for low data activity rates by reducing static and dynamic power consumption in both the clock network and the flip-flop.

As stated in [49], the internal clock gating technique is appropriate for flip-flops with low switching rate in the input data. However, its advantage decreases as the switching rate increases because of the associated overhead. So, the proposed clock gated flip-flop structure is suited for applications with reduced switching activity. An example is a binary counter, in which input switching activity for each flip-flop is known beforehand. Other application includes slow-varying signals (compared with the sampling rate). This occurs, for instance, in the sampling of audio and video signals. The proposed structure can also be used in signals in which the values are most of the time close to a fixed point. This occurs, for instance, in systems that monitor physical quantities, such as temperature and pressure.

4. Simulation Conditions

Simulation parameters used for comparison, are shown in Table 1. All simulations are performed on TSpice using BSIM 3v3 level 53 models in 130 nm process node. The supply voltage is varied from 1.3V to 2V. The results are carried out for the period of 16 data sequences. Under nominal condition, a 16-cycle sequence 0100000000000000 that is a low data activity is supplied at the input for average power measurements. However the dynamic power consumption is dependent on switching activities at various nodes of the circuit. It varies with different data rates and circuit topologies. Hence to obtain a fair idea of power dissipation for a circuit topology, different data patterns should be applied with different activity rates [50]. So in simulations, following four different data sequences also have been adopted to compare the power consumption of flip-flop structures discussed in this paper:

Table 1. CMOS Simulation Parameters

Particulars	Value	Particulars	Value
CMOS Technology	130 nm	Nominal Supply Voltage	1.3V
Min. Gate Width	260 nm	Rise Time of Clock & Data	100 ps
Max. Gate Width	1.44 μm	Fall Time of Clock & Data	100 ps
MOSFET Model	BSIM 3v3 level 53	Sequence Length	16 Data Cycles
Temperature	25° C	Nominal Clock Frequency	400MHz
Duty Cycle	50%		

(i). 1111111111111111(DA=0)
(ii). 0000000000000000 (DA=0)
(iii). 1111010110010000 (DA=0.5)
(iv). 1010101010101010 (DA=1)

Where 'DA' is the data activity.

In this paper, total power as the power metric and clock to Q delay as the performance metric are taken. The transistors, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation.

5. Simulation Results Comparison

Table 2 shows the power consumption in microwatts at different supply voltages for nominal conditions. LAFF failed at 1.3V and 1.4V supply voltages. The simulation results show that the proposed FF has the least power dissipation among all flip-flop designs for all supply voltages. The average results show that the power improvement compared to existing flip-flops is approximately 1.39, 1.42, 1.53, 1.84, 1.13, 1.45, 1.84 and 1.39 times respectively. Figure11 shows the power consumption in microwatts at different supply voltages at 1GHz clock frequency. It is clear from the figure that the proposed FF has the least power dissipation among all the designs for all supply voltages except 2V. At this voltage the proposed FF consumes the second lowest power and LAFF consumes slightly lesser power than the proposed FF. But this flip-flop failed at 1.3V and 1.4V supply voltages. Figure 12 shows the power consumption in microwatts at different data pattern from 0% switching activity to 100% switching activity. The simulation results show that the proposed FF has the least power dissipation among all the designs for low switching activities.

Table 2. Power consumption in µW as a function of supply voltage for nominal conditions

V_{DD} (V)	1.3	1.4	1.6	1.8	2.0	Avg
PPFF	3.89	4.42	6.24	7.69	9.24	6.30
Pass FF	4.18	4.82	5.98	7.52	9.64	6.43
PIFF	4.38	5.05	6.88	8.22	10.24	6.95
LAFF	Failed	Failed	7.82	7.73	9.41	8.32
AEFF	3.02	3.54	4.89	6.24	8.01	5.14
LVFF	4.32	4.98	6.48	7.56	9.39	6.55
C^2MOSFF	5.31	6.18	8.02	10.27	11.98	8.35
APEFF	2.73	3.47	5.52	8.88	10.78	6.28
Proposed FF	2.44	2.81	3.97	5.62	7.79	4.53

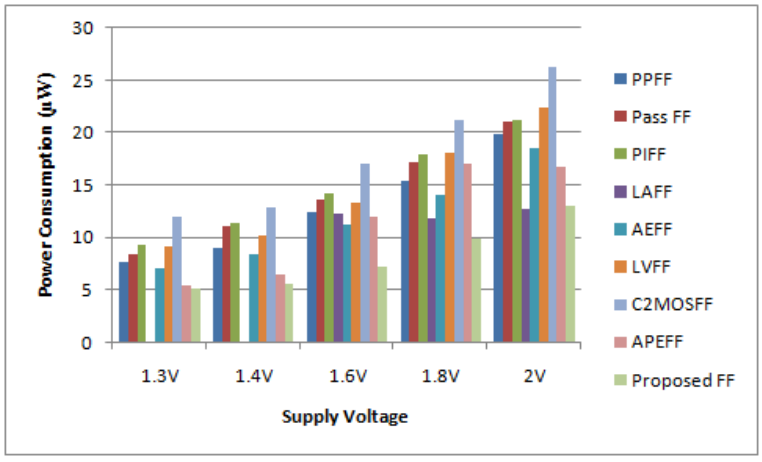

Figure 11. Power consumption in µW as a function of supply voltage for 1GHz clock frequency

There is only one exception. For all ones data pattern APEFF consumes lesser power than the propo sed FF. For high data activities, the proposed FF consumes the highest power. LAFF failed for these conditions except all ones data pattern. The proposed flip-flop consumes up to 2.71 times power for higher data activities and the proposed flip-flop saves up to 6.86 times power compared to existing flip-flops for low data activities.

Table 3 shows the delay in Pico second for different supply voltages at nominal conditions. Main drawback of the proposed flip-flop is the reduction of timing performances. This problem has already been reported in previous papers for gated flip-flops like in [51]. This is due to the presence of gating logic that causes a propagation delay between clock and gated clock signals. The simulation results show that the proposed FF has longer delay in most of the cases than the non-gated existing designs due to delay in clock network. For 1.3V and 1.4V supply voltages, LAFF failed. For remaining supply voltages, LAFF has longer delay than the proposed FF. For 1.6V supply voltage, the proposed FF has shorter delay as compared to PPFF, Pass FF, LAFF and AEFF. For 2V supply voltage, PPFF and LAFF have longer delay than the proposed FF. The average results show that the proposed FF has 39.92%, 53.41%, 71.32%, 25.69%, 74.46%, 91.46% and 62.06% longer delay than the flip-flops discussed in section 2 except LAFF. The proposed FF has 0.31% shorter delay than LAFF.

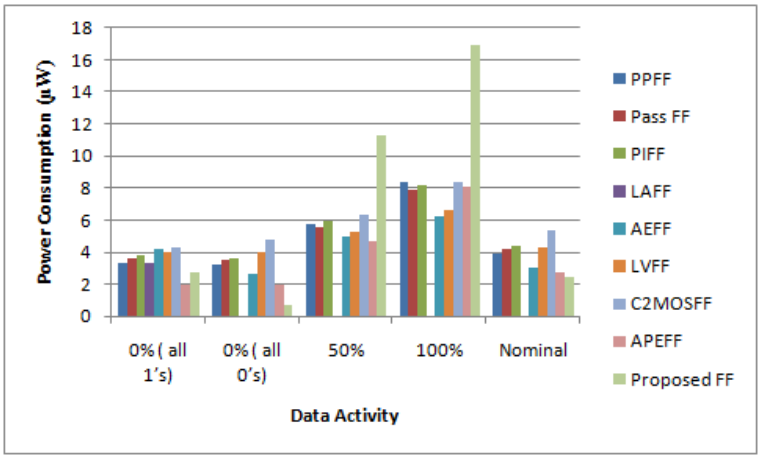

Figure 12. Power consumption in µW as a function of data activity

Table 3. Delay in pS as a function of supply voltage

V_{DD} (V)	1.3	1.4	1.6	1.8	2.0	Avg
PPFF	99.99	116.4	132.4	111.75	95.3	111.17
Pass FF	79.77	103.55	100.3	81.3	66.15	86.21
PIFF	63.78	43.52	9.9	78.61	69.54	53.07
LAFF	Failed	Failed	285.36	157.31	114.19	185.62
AEFF	293.43	193.65	98.25	58.4	43.75	137.5
LVFF	74.31	56.35	41.25	34.05	30.3	47.25
C^2MOSFF	25.61	18.25	13.35	11.55	10.3	15.81
APEFF	156.93	117.39	33.15	24.63	18.92	70.20
Proposed FF	374.41	254.54	95.09	117.84	83.32	185.04

Table 4 shows the power consumption in microwatts at different supply voltages for 0% data activity and 1GHz clock frequency. The simulation results show that the proposed FF has the least power dissipation among all the designs for all supply voltages. The average results show that the power improvement compared to existing flip-flops is approximately 4.80, 5.53, 5.90, 5.26, 4.44, 5.84, 7.10 and 3.40 times respectively. The proposed flip-flop has up to 7.82 times power

improvement compared to existing flip-flops.

Table 4. Power consumption in µW as a function of supply Voltage for 0% data activity and 1GHz clock frequency

V_{DD} (V)	1.3	1.4	1.6	1.8	2.0
PPFF	6.79	7.89	11.09	13.73	17.90
Pass FF	7.87	10.46	12.56	15.9	19.33
PIFF	8.68	11.07	13.25	16.86	20.63
LAFF	Failed	8.02	11.08	13.98	17.14
AEFF	6.66	7.89	10.33	12.38	15.86
LVFF	8.68	9.71	12.56	17.36	21.51
C^2MOSFF	11.1	12.35	16.21	20.19	24.95
APEFF	4.27	4.99	9.57	12.19	9.65
Proposed FF	1.42	1.8	2.32	2.8	3.62

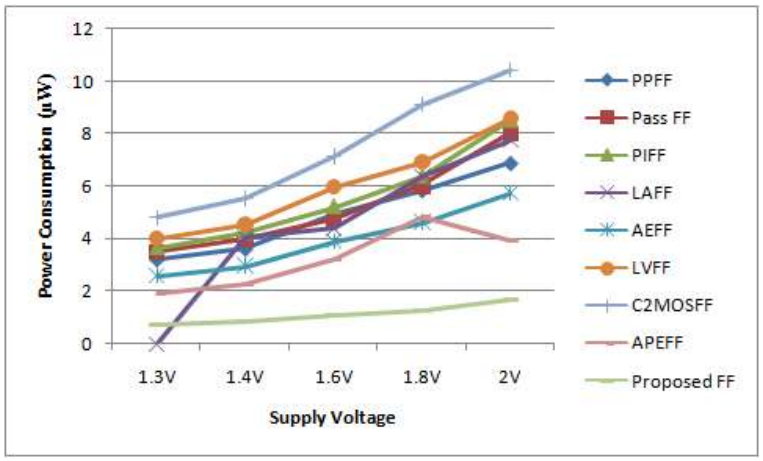

Figure 13. Power consumption in µW as a function of supply Voltage for 0% data activity and 400MHz clock frequency

Figure 13 shows the power consumption in microwatts at different supply voltages for 0% data activity and 400MHz clock frequency. The simulation results show that the proposed FF has the least power dissipation and C2MOSFF has the highest power dissipation among all the designs for all supply voltages. Figure 14 shows the power consumption in microwatts at different clock frequencies for nominal conditions. It is clear from the figure that the proposed FF has the least power dissipation among all the designs for all clock frequencies except 100MHz. At this clock frequency the proposed FF consumes the second lowest power and AEFF consumes slightly lesser power than the proposed FF. For these conditions LAFF completely failed. C2MOSFF consumes the highest power at all clock frequencies.

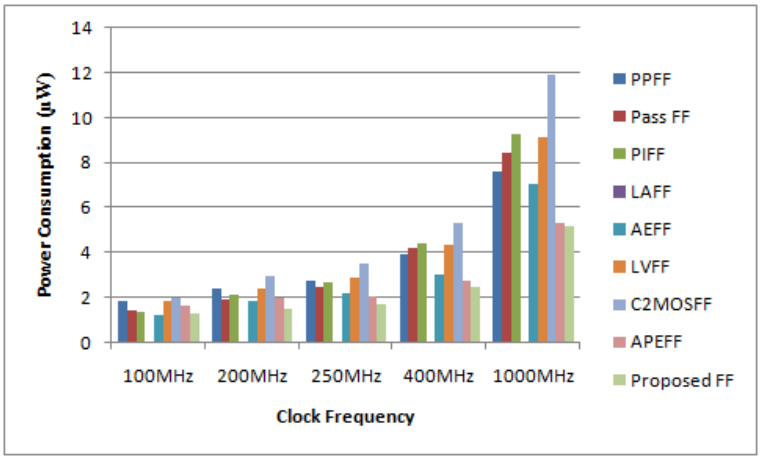

Figure 14. Power consumption in µW as a function of clock frequency

6. Conclusion

Synchronous systems require the clock that dictates the temporal behavior of the system. A significant amount of energy is wasted for proper synchronization among different components. The clock gating technique avoids unnecessary power dissipation from clock switching. In this paper, a new clock gated single-edge-triggered flip-flop has been developed to reduce the waste of energy in flip-flops with low data activity. The proposed flip-flop reduces power consumption by reducing the clock switching. Unlike many other gated flip-flops, the proposed flip-flop has state retention property to save power and to switch circuit between idle and active modes smoothly. The feedback path is also improved in the proposed flip-flop to decrease the total parasitic capacitance at the internal flip-flop nodes and to reduce dynamic power dissipation. In the slave latch of the proposed flip-flop, the transmission gate is used to overcome the drawbacks of the pass transistors to make the output signal clean and stable. The proposed clock-gating scheme only requires 4 transistors, thereby occupying less silicon area. Further, the proposed clock gating network can be shared among a group of flip-flops to reduce the power and area overhead of the gating network. If clock gating network is shared among a group of flip-flops, the result would be more interesting. Even for a single flip-flop, the proposed circuit has good improvement in power consumption for low data activity rates by reducing static and dynamic power consumption in both the clock network and the flip-flop.

The simulation results show that for all supply voltages, the proposed FF has the least power dissipation among all the designs for low switching activities. The proposed flip-flop has up to 7.82 times power improvement than the existing flip-flops for low data activity applications. However the proposed FF is not suited for higher data activity applications. The proposed FF consumes higher power for 50% and 100% data activities as compared to existing flip-flops. For these two higher data activities, the proposed FF consumes 2.42 and 2.71, times power than the existing flip-flops respectively. Gated flip-flops present a significant increase of timing parameters. This is due to the presence of gating logic that causes a propagation delay between clock and gated clock signals. The simulation results show that the proposed FF has longer delay in most of the cases than the existing non-gated designs due to delay in clock network. The proposed flip-flop has up to 14.62 times longer delay. However in many cases the proposed flip-flop has shorter delay than the existing flip-flops and the proposed flip-flop has up to 3.0 time shorter delay.

By clock gating technique a significant power dissipation reduction is obtained if input signal switching activity is low. However, its advantage decreases as the switching rate increases because of the associated overhead. So, the proposed clock gated flip-flop structure is best suited for applications where input signal switching activity is low. An example is a binary counter, in which input switching activity for each flip-flop is known beforehand. Other application includes slow-varying signals (for instance, in the sampling of audio and video signals). This flip-flop can also be

used in signals where the values are most of the time close to a fixed point (for instance in systems that monitor physical quantities, such as temperature and pressure). As a conclusion proposed flip-flop is best suited for applications in which input activity is kept low and speed is not a crucial factor.

7. References

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