Clock Recovery Circuit for Optical Packets

C. Bintjas, K. Yiannopoulos, N. Pleros, G. Theophilopoulos, M. Kalyvas, H. Avramopoulos, and G. Guekos

***Abstract*—We demonstrate an all-optical clock recovery circuit for operation with short data packets of 10-Gb/s rate. The circuit uses a Fabry–Pérot etalon and a nonlinear UNI gate and is capable of acquiring the clock signal within a few bits.**

***Index Terms*—All-optical clock recovery, Fabry–Pérot filter, optical packet switched networks, semiconductor optical amplifier, ultrafast nonlinear interferometer.**

I. Introduction and Concept

DESPITE the recent slowdown in sales in the telecommunications industry, Internet-based traffic continues to expand in volume and to set aggressive requirements for telecommunication network systems. All-optical packet switching has been heralded as a means to deploy more efficient transport networks and achieve cost reduction through better network resource utilization [1], [2]. In recent years research in all-optical signal processing has made significant inroads [3], so that it may be possible for a number of key functionalities required by packet switched networks to be performed in the optical domain. Such functionalities include bit and frame synchronization [4] and clock recovery is an important circuit to do this.

Several techniques for optical clock recovery have been demonstrated, so far, including synchronized mode-locked ring lasers [5], [6], electronic phase-locked loops [7] and self-pulsating distributed feedback (DFB) [8]. Like all techniques for clock recovery, these circuits need a time interval for synchronization to the data streams. Generally speaking a clock recovery circuit consists of a high-Q filter tuned to the data line rate with purpose to average out the incoming data pattern and an active element to generate the new clock signal. In the case of optical clock recovery circuits, these two functions are generally provided by a single element, a laser oscillator. Given that the lifetime of such oscillators is determined of their cavity length and Q as well as upper state dynamics of the active medium, these have a minimum capture time to synchronize to the incoming data, which may be too long for optical packet switching. This is because the clock recovery time must be accommodated by guard-bands between the packets. As the line rate increases or the packet size decreases for better network resource utilization, an increasingly larger proportion of the channel bandwidth will have to be allocated for synchronization purposes and therefore will be wasted. Clock recovery with fast time synchronization has also been demonstrated using a Fabry–Pérot (FP) etalon [9], but this scheme cannot be used on its own with bursty packet traffic, because it will result in severe amplitude modulation in the derived clock signal.

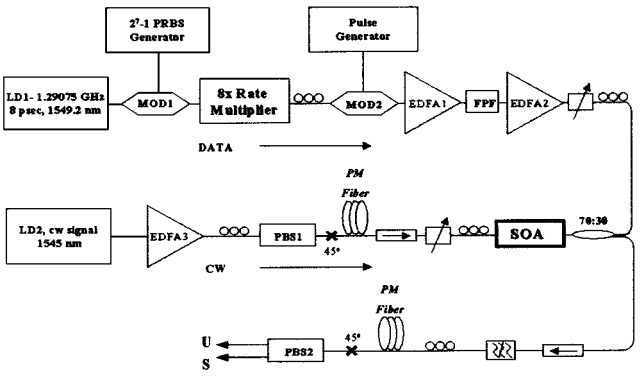

Fig. 1. Experimental Setup.

In the present work, we present a clock recovery circuit that separates the filtering function by using a FP etalon tuned to the line rate and a high-speed amplitude equalization function that is provided by the nonlinear switching function [10] of an all-optical gate. A very interesting feature of a FP etalon is that its impulse response function in time, is a decaying exponential function whose lifetime is determined by the filter finesse [11]. This means that if a RZ modulated data signal is introduced in a FP filter with a free spectral range (FSR) equal to the line rate, at the output of the filter the "0s" of the incoming data stream will be partially filled by preceding "1s." If this amplitude modulated clock signal is next fed as control signal in an interferometric high-speed nonlinear optical gate like the UNI [13], [14] so as to generate approximately a differential π-phase change, the resulting output will become a nearly equal amplitude clock signal, of similar length to the original packet. In this letter, we propose and demonstrate this novel concept for optical packets and continuous data streams at 10 Gb/s. It is the first time, to our knowledge, that a clock recovery scheme can capture clock within a few bits and provide a clock signal of similar length to the original packet. A further significant feature of this scheme is that it is self-synchronizing and does not require any high-speed electronics. The proposed scheme is particularly applicable to optical packet switched architectures and is expected to assist the implementation of all-optical signal processing and routing functions.

II. Experimental Setup

The experimental configuration is depicted in Fig. 1. The UNI gate has been optimized for operation at 10 Gb/s, so that the lengths of polarization-maintaining fiber (PMF) at the two ends of the gate induce 50 ps of birefringent delay between their two

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axes. The active element was a commercially available (Opto Speed S.A.), 1.5 mm bulk InGaAsP–InP ridge waveguide semiconductor optical amplifier (SOA) with 30-dB small signal gain at 1560-nm 3-dB polarization gain dependence and a recovery time of 100 ps, when driven with 700-mA dc current. The UNI is powered from a DFB laser source (LD2) used to generate the continuous-wave (CW) signal at 1545 nm. The CW signal is amplified in erbium-doped fiber amplifier (EDFA) EDFA 3 and enters the UNI via the input polarization beam splitter (PBS1) to produce two orthogonal polarization components. The data signal originates from a DFB laser source (LD1), gain-switched at 1.290 75 GHz to provide 8-ps pulses at 1549.2 nm after linear compression. The pulse train is modulated to form a $2^7 - 1$ pseudorandom binary sequence (PRBS) signal using a PRBS generator and a $LiNbO_3$ modulator (MOD1). This sequence is then three-times bit interleaved to generate a 10.326-Gb/s pseudodata stream with controllable sequences of consecutive "0s." Variable length and period data packets were formed from this pseudodata stream using a second $LiNbO_3$ modulator (MOD2) driven from a programmable pulse generator. The sequence of pseudodata packets is then amplified in EDFA 1 and enters a FP etalon with FSR equal to the line rate and a finesse of 20.7, corresponding to a $1/e$ lifetime roughly of 7 bits. The signal from the FP etalon is further amplified in EDFA2 and is launched into the UNI gate as the control signal in counter-propagating fashion, so as to effect a differential phase change between two orthogonal polarization components. On exiting the SOA, the two polarization components of the CW signal were filtered in a 2-nm filter, had their relative delay removed and were made to interfere in PBS2. Isolators were used to avoid undesirable reflections in the circuit. The interferometer is biased so that with no optical control signal, the CW signal appears in the unswitched port (U) of the gate. In the presence of control pulses the UNI operates as an AND gate and the signal appears in the switched port, S.

III. Results

Data packets of different length, period and content, were introduced in the clock recovery circuit by changing the width, period and delay of the electrical pulse driving MOD2, so as to evaluate its operation. Fig. 2 shows representative results. Fig. 2(a) and (b) show the contents of two such packets which contain only 30 bits, they have 3-ns duration, and they arrive with a period of 6.2 ns. The packets have been selected so as to have different distributions of "1s" and the first packet contains a sequence of six consecutive "0s." Fig. 2(c) and (d) show the output from the FP etalon. This is a clock-resembling signal, highly amplitude modulated. Its length is roughly equal to the original packet length and is extended at its leading edge by the rise time of the FP and at its trailing end by its lifetime. By adjusting the polarization state of this signal so that it is co-polarized with one of the CW components in the SOA and feeding it as control into the UNI, a nearly equal amplitude clock packet is obtained at the output. Fig. 2(e) and (f) show the corresponding clock packets. Switching power and mean energy per pulse for the CW and the control signal were 155 μW and 30 fJ, respectively. These two parameters determine the degree of saturation

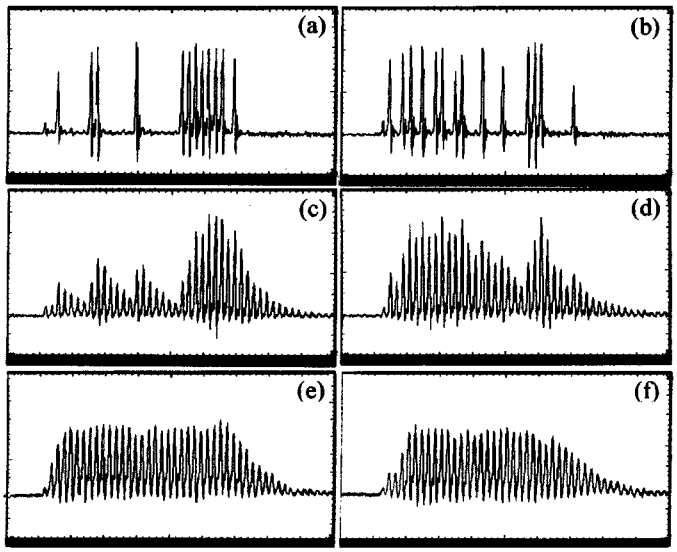

Fig. 2. (a), (b) Two incoming data packets, (c), (d) FP etalon output and (e), (f) Recovered packet clock at exit of UNI gate. The time base is 500 ps/div.

of the SOA so as to enable the control pulses to affect a differential phase change of roughly π between the two components of the CW signal. The amplitude modulation (highest to lowest pulse ratio) on the 30 clock pulses corresponding to the original packet was less than 1.5 dB.

It is interesting to note that the rising time at the leading edge of the clock packet is shorter than the FP lifetime due to the saturation properties of the SOA. The SOA is less saturated and therefore can provide higher gain to the first bits of the packet. In this way, even the low energy pulses at the front of the packet cause enough phase shift on the CW component. For all the input data packet examples examined in this study, the rise time for the recovered clock was always less than 5 bits. Therefore if this clock recovery unit is used for bit-wise processing in an all-optical circuit, a fixed guard-band of less than 5 bits is required at the front of the packet and a guard-band of less than 10 bits is required at its trail end. These guard-bands depend on the finesse of the FP, which in turn must be determined by the expected sequence of continuous "0s" in the data stream. A theoretical model has been developed [10], [12] to simulate the performance of the FP filter and the interferometric gate for different incoming data packets, including the worst case for a packet containing a sequence of consecutive zeros followed by 31 consecutive "1s." Results are shown in Fig. 3. Fig. 3(a) and (b) show the amplitude modulation at the output of the FP filter and UNI gate respectively, as a function of consecutive "0s" in the incoming packet for FP filters of different finesse. Assuming that the clock recovery circuit should be able to handle data packets that may contain up to 30 consecutive "0s," a FP etalon of finesse 80 would be required. It is also clear that the nonlinear gate reduces the amplitude modulation by 16.5 dB, depending on the saturation level of the SOA. Fig. 3(c) shows the rise and fall times of the recovered packet clock as a function of the filter finesse for the worst-case packet described before. For these results we have defined that the tail of the signal at the output of the FP filter persists up to the bit that has 30-dB lower peak power than the first. Fig. 3(c) shows that even for a finesse

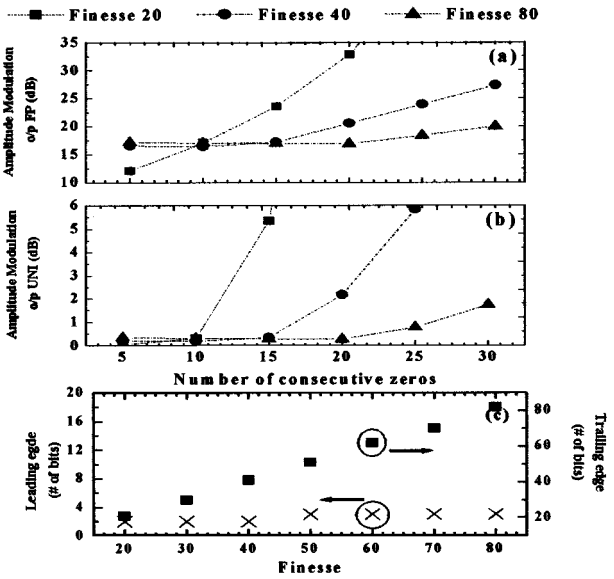

Fig. 3. Amplitude modulation at the output of (a) the FP filter and (b) the UNI gate as a function of consecutive zeros in the data packet and different FP finesse. (c) Leading and trailing edge of recovered packet clock against FP finesse.

of 80 the leading edge consists of 3 bits, while the trailing edge consists of 82 bits. Therefore it is expected that using a FP with a higher finesse will assist to reduce the amplitude modulation of the packet clock, at the expense of slower rising and fall times of the derived signal. It should also be noted that these rise and fall times are defined by the finesse of the FP as fixed numbers of bits and are independent of the rate. Therefore given that the UNI gate has been shown to operate at significantly higher data rates, by choosing a FP of the appropriate FSR, operation of this clock recovery circuit should be extendable to higher rates, while the required guard-bands will scale with the bit period and will not increase in numbers of bits as the rate increases. Finally, it should be mentioned that further reduction in amplitude fluctuations in the packet clock should be possible by using a second deeply saturated SOA at the output of the circuit [5].

The clock recovery circuit was tested for continuous data streams and operated equally well providing a clock signal with amplitude modulation at the output of the gate of less than 1.2 dB. The extracted clock signal was also monitored on a 50-GHz microwave spectrum analyzer for both packet and continuous data signal inputs. The derived clock signal displayed suppression of the data modes in excess of 40 dB compared to the clock component and the rms timing jitter was less than 5 ps. It should be mentioned that timing jitter of the incoming data signal was of the same magnitude due to the 8 times rate interleaver.

IV. Conclusion

In conclusion, we have presented a novel clock recovery scheme, which can be used for packet switched networks and which is appropriate for all-optical switching and routing operations. The circuit is simple, has no high-speed electronic components, does not require synchronization and acquires locking within a few bits. Given that the UNI gate has been shown to operate in excess of 100 Gb/s, this circuit should be possible to operate at comparable rates and with a guard-band of a fixed number of bits defined by the passive FP element.

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