Clocking and Cell Placement for QCA

V. Vankamamidi* M. Ottavi* and F. Lombardi*
*Department of Electrical and Computer Engineering
Northeastern University, Boston, MA 02115, USA
Email: (vvankama,mottavi,lombardi)@ECE.NEU.EDU

***Abstract*— In this paper we propose a novel two-dimensional clocking and timing scheme for systems which permit a reduction in the longest line length in each clocking zone. The proposed clocking schemes utilize logic propagation techniques which have been developed for systolic arrays. Placement of QCA cells is modified to ensure correct signal generation and timing. The significant reduction in the longest line length permits a fast timing and efficient pipelining to occur, while guaranteeing kink-free behavior in switching.**

***Index Terms*— Quantum-dot Cellular Automata, adiabatic switching, timing**

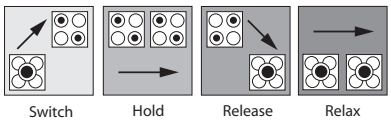

Fig. 1. **QCA clock phases.**

Fig. 2. **Four-phased signal for clocking, adiabatic switching.**

I. Introduction

Among emerging technologies, *Quantum-dot Cellular Automata* (QCA) not only gives a solution at nano-scale, but it also offers a new method of computation and information transformation (often referred to as processing-in-wire). In terms of feature size, it is projected that a QCA cell of few nanometer size can be fabricated through a molecular implementation by a self-assembly process. Sequential as well as combinational designs can be realized using QCA. Usually, QCA circuits and systems follow the clocking zone partition scheme of [1]. Designs are partitioned into multiple clocking zones only along one dimension (say the X-axis), thus effectively creating *columns* (as *zones*). Clocking and pipelining require designs to maintain sets of four adjacent zones at any time (as per the four phases, i.e. Switch, Hold, Release and Relax). During the Switch phase, extra electrons in a cell are polarized under the influence of neighboring cells; in this phase, a cell attains a definite binary value. Interdot barriers are raised in the Hold phase, so that electrons do not switch and retain their polarity. Interdot barriers are reduced in the Release phase and cells lose their polarity. In the Relax phase, there is no interdot barrier and a cell has no influence on its neighbors. Figure 1 depicts a cell in its *four clock phases*. Clocking to each zone of a QCA design is applied through an underlying circuitry which generates a signal, as shown in Figure 2 [4]. This signal generates the electric field for modulating the tunneling barrier of all cells in the zone (adiabatic switching).

In this paper, we consider issues pertaining to timing and clocking of QCA systems for high performance computing and kink-free (error-free) behavior. Initially, we study the effects of thermal fluctuations on QCA designs as a function of their size. Unfortunately, we show that tolerance to thermal fluctuations and high performance computing necessitate a different mechanism than the one-dimensional criteria of clocking proposed in [1]. To address this problem, a novel strategy is proposed for timing and clocking of QCA systems. This strategy is based on a two-dimensional characterization of information transfer across different timing zones arranged into grids. Issues such as clocking circuitry (as interfaced to CMOS) and operating temperature, are also addressed.

II. Clocking Analysis

For QCA, *adiabatic switching* is commonly preferred to abrupt switching [1]. In an adiabatic approach, switching is accomplished by modulating the interdot tunneling barrier of the QCA cells. When applying an input signal, barriers are lowered such that cells begin to polarize. By raising back the barriers, cells are held or 'crystallized' in their new states. If the change in the interdot potential barrier is gradual, then adiabatic theory guarantees that the system always remains in the *ground state* and does not permanently move to excited or metastable states [6]. A system is said to be in the *ground state* if it has minimum energy, i.e. all cells polarize and attain a state as expected by cell-to-cell interactions. In an excited state, cells align contrary to cell-to-cell electron repulsion and a *kink* is said to have occurred.

In an adiabatic switching scheme, fluctuations in operating temperature may excite QCA cells above their ground state and produce erroneous results at the output.

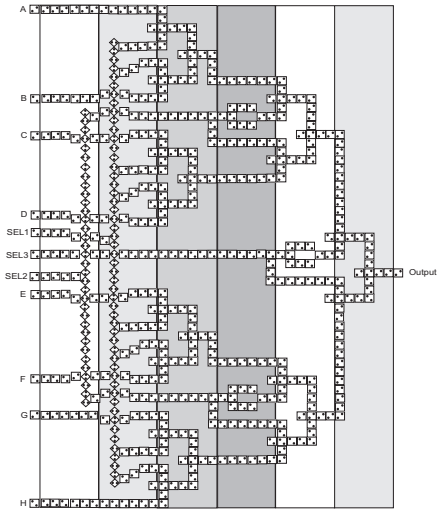

Fig. 3. **8-to-1 QCA multiplexer, one-dimensional clocking.**

[2] provides an analysis of these thermal effects on a linear array (or line) of QCA cells. Let E_k represent the energy required for a QCA cell to encounter kink (i.e. to align differently from its expected polarization). As the number of QCA cells in the linear array increases, then the ground state remains unique and the energy separation between the ground state and the first excited state remains E_k. However, with an increasing number of cells, the number of locations increases and so multiple kinks may occur. Therefore, the probability for kink-free behavior is a function of N (as denoting the number of cells in the array). Also at nonzero Kelvin, higher is the operating temperature (T), higher are the thermal fluctuations which may lead to an increase in the probability of kink occurrence. Finally, the probability for a system to be in an excited state (kink), is a function of the energy required for a kink to occur in a QCA cell, E_k. A higher value of E_k reduces the probability of kink occurrence (with scaling of cell dimension to a molecular-level the correlation between electrons in neighboring cells increases, thus resulting in an increase of E_k). These parameters are quantified in the following equation (derived in [2]),

$$\Delta F_n = nE_k \left[1 - \frac{k_B T}{E_k} \ln(N) \right] \tag{1}$$

ΔF_n is the energy separation between the ground state and the n^{th} excited state, i.e. a zone with n kinks and k_B is Boltzmann's constant. As long as the energy separation ΔF_n is greater than zero, then the QCA system does not settle in an excited thermodynamic equilibrium state. This implies that the energy required for *n* kinks (nE_k) must be greater than for the kinks caused by thermal fluctuations, $K_B T\ nln(N)$. From this inequality, for a given kink energy E_k and operating temperature T, a bound on the number of QCA cells for avoiding kinks is given by

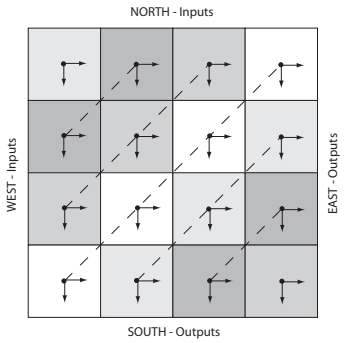

Fig. 4. **Clocking for two-dimensional wave propagation.**

$$N \leq e^{\frac{E_k}{k_B T}} \tag{2}$$

The bound on line (array) length obtained from (2) can be utilized in determining the largest zone dimension under the worst case conditions. Consider a bound on N for the vertical and horizontal dimensions of a zone. From (2), thermodynamic effects can then be avoided in all QCA lines within that zone. Therefore, kink-free behavior can be accomplished by establishing an upper bound on N for the dimension of a clocking zone. For QCA pipelining, only one zone (among a set of four adjacent zones) is in the Switch phase at any time; so, the effective length of a long QCA line (which may span across multiple zones) is only equal to the dimension of the switching zone.

III. Two-Dimensional Wave Clocking

The clocking mechanism for QCA proposed in [1] partitions a design into different zones only along one direction of signal flow, i.e. the X-axis. Such a scheme considers long horizontal lines and divides them among multiple (vertical) clocking zones, thus keeping their length bounded in any zone. A vertical line (in the Y-axis) is always contained within a column as a single clocking zone; for complex designs, the height of a clocking zone (along the Y-axis) could be significant, thus creating long vertical lines.

The problem of long vertical lines is solved in this paper by partitioning the QCA design along the Y-axis (row-wise) in addition to the X-axis (column-wise). This two-dimensional (2D) arrangement effectively generates a *grid of clocking zones* for a given QCA design. A bound for the zone dimensions restricts the length of the QCA lines and makes QCA designs tolerant to thermodynamic effects. The principles of this clocking scheme are based on the similarity between systolic arrays and QCA with respect to signal propagation. Systolic arrays are special purpose VLSI architectures introduced in the late 1970s [5]; they are made of simple processing elements with

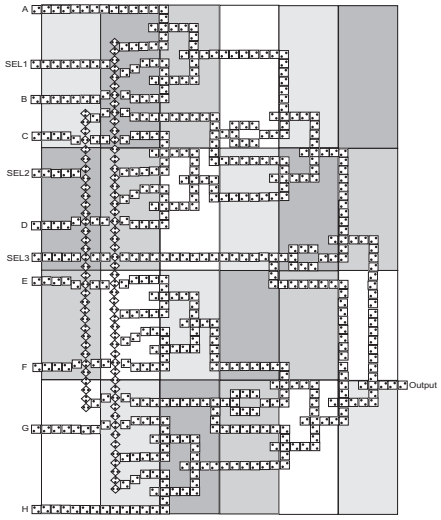

Fig. 5. **8-to-1 QCA multiplexer, two-dimensional wave clocking**

local interconnections usually arranged in a grid layout. Each processing element receives data from one or more neighboring processing elements (at its primary inputs); it then performs local computation and transfers its results to other neighboring processors (connected to its primary outputs). As partitioning scheme for clocking zones, the proposed two-dimensional arrangement is similar to a grid with orthogonal interconnections. Computational results move from north-west to south-east; this is similar to the implementation in a two-dimensional systolic array (such as for matrix multiplication). Due to these similarities, logic-wavefront propagation techniques developed for systolic arrays can be considered for QCA architectures to increase data pipelining and parallel processing.

Figure 4 shows a logic propagation technique for the proposed two-dimensional diagonal wave scheme (2DDWave). To retain similarity to the two-dimensional (square) systolic array, each zone must accept input signals only from two zones (north, west) and pass its outputs to the other two zones (south, east), i.e. each column should have an *equal number* of zones (perfect grid). In this *perfect grid* scheme the correct switching of a zone requires that only two zones (one located above the Switch phase zone and one located to the left of the Switch phase zone) to be in the Hold phase. Similarly, a zone needs to be in the Hold state only until the zones located below (south) and right (east) are switched. With this switching arrangement, the proposed diagonal wavefront propagation scheme (denoted as 2DDWave) produces at the output the same results as the one-dimensional scheme presented previously.

In a one-dimensional clocking scheme, the length of the vertical lines are not bounded because they increase as a function of design size. As the operating temperature (T) changes with the number of cells (N) in the longest QCA line of a clocking zone, then T becomes a function of design size. However, in the proposed two-dimensional schemes, independent of the design size, line lengths can be bounded as partitioning occurs along both the X-axis and Y-axis. Therefore, QCA designs under two-dimensional schemes are robust to thermal fluctuations and can be operated at higher temperatures, mostly independent of size.

Characteristics	**1D**	**2DDWave**
No.of Cells (C)	575	576
No.of Zones (Z)	6	24
Max. Wire Len (L)	51	13
$\frac{E_k}{kT}$ for kink-free operation	3.9	2.6
Max. Temp for kink-free operation	195k	300k
Computation Time	$\sim$24 time units	$\sim$ 9 time units
Pipelining	Four-staged	Four-staged
Clocking Circuitry	Modest	Modest

TABLE I

COMPARISON OF 1D AND 2D CLOCKING SCHEMES.

In the proposed two-dimensional wave clocking scheme (2DDWave), switching is performed in *parallel*; all zones that are located *along the diagonals* are *switched* simultaneously. Therefore, the proposed 2DDWave scheme performs better in terms of processing speed than 1D scheme (switching speed for a clocking zone is proportional to lenght of longest QCA line in it i.e. clock zone dimension; please refer [1]).

Table I shows the characteristics of the two clocking schemes discussed in this paper for the 8-to-1 QCA multiplexer design (Figures 3, and 5) as example.

As reported previously [1] [8], QCA designs can be clocked by an electric field generated by a set of parallel CMOS wires buried under the substrate. For the one-dimensional scheme, these metal wires are vertically oriented such that columns of clocking zones are formed. By keeping the set of four adjacent metal wires out of phase by $\frac{\pi}{2}$ and applying the signal shown in Figure 6, clocking requirements can be satisfied.

The two-dimensional wave (2DDWave) scheme also requires a simpler arrangement because all zones along the diagonals are clocked simultaneously and are in the same phase. However in this case, the set of parallel metal wires run diagonally to the QCA design, i.e. a wire runs under all clocking zones located diagonally to each other. To provide an uniform electric field across a clocking zone two layers of metal wires are required as shown in Figure 6. The diagonal metal wires run in layer 1 (bottom) over the entire QCA design; metal wires in layer 2 (top) are small, disjoint and extend only over a single clocking zone

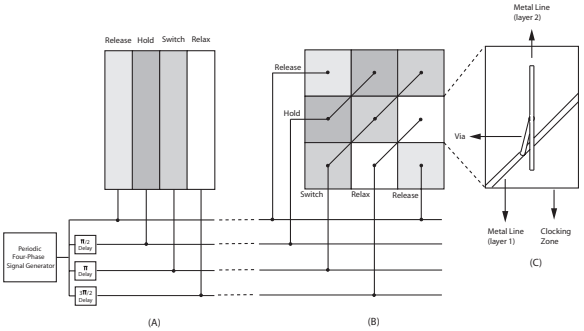

Fig. 6. **CMOS clocking circuitry for QCA designs. A) Circuitry for one-dimensional (1D) clocking scheme. B) Clocking scheme for two-dimensional wave (2DWave) clocking scheme. C) Second layer of metal wires to provide uniform electric field over a clocking zone in 2DDWave scheme.**

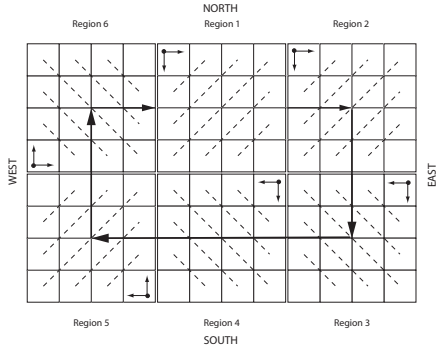

Fig. 7. **Feedback path for two-dimensional clocking schemes.**

to provide a uniform electric field. Metal wires in layer 1 and layer 2 are insulated through an oxide layer such that the electric field generated by metal layer 1 does not interfere with the electric field of metal layer 2. The signal in metal layer 1 is transferred to the metal wires in layer 2 (for the diagonal clocking zones) through vias.

Logic level effects due to interference in the electric field between adjacent metal wires used for clocking is minor because cells that are at the boundary must belong to either of the two adjacent clocking zones (depending on the strength of electric fields in their corresponding layer 2 metal wires). By designing circuits such that QCA cells at clock zone boundries can belong to either of cloking zones and still not modify logic functionality, we can tolerate the interference of electric fields.

IV. Feedback Paths

One of the main issues arising in clocking schemes for QCA is the ability to handle feedback paths. In both traditional one-dimensional clocking scheme and the proposed two-dimensional clocking schemes, signal propagation is strictly uni-directional (west to east in the 1D case (Figure 3) and north-west to south-east in the 2D case (Figure 4)). Hence, although clocking schemes are readily applicable to combinational circuits, feedback paths (as in sequential circuits) may require a different technique.

[3] has proposed a trapezoid clocking mechanism for the one-dimensional scheme to enable feedback paths in QCA designs and better utilize the layout area (by exploiting the tournament bracket structure of QCA circuits). This mechanism can also be adopted for the proposed two-dimensional clocking schemes to allow feedback paths. Figure 7 shows the loop of clocking zones for implementation under a two-dimensional scheme. To allow feedback paths, zones in each region are clocked using the 2DD wave scheme, such that signal propagations are as follows: from north-west to south-east in region 1 and region 2, north-east to south-west in region 3 and region 4, south-east to north-west in region 5 and south-west to north-east in region 6. Thus, circuits in all six regions can receive their outputs as one of their inputs using feedback paths. Circuits can also receive new inputs and propagate their outputs; for example, while region 2 receives a feedback input from west and propagates the feedback path through south, it can receive new inputs from north and send out the outputs through east.

V. Conclusion

In this paper, we have considered issues pertaining to timing and clocking of QCA systems for high performance computing and kink-free behavior. Differently from previous works, the QCA design is partitioned into a grid of zones along both directions (vertically and horizontally) of signal flow which permits a reduction in the longest line length in each clocking zone.

References

[1] C.S. Lent and P.D. Tougaw, "A device architecture for computing with quantum dots," *Proc. of the IEEE 85,* pp.541-557, 1997.

[2] C.S. Lent , P.D. Tougaw and W. Porod, "Quantum Cellular Automata: The Physics of Computing with Arrays of Quantum Dot Molecules," *PhysComp '94: Proceedings of the Workshop on Physics and Computing,* IEEE Computer Society Press, 1994.

[3] M.T. Niemier and P.M. Kogge, "Problems in designing with QCAs: layout=timing," *International Journal of Circuit Theory and Applications,* Vol.29(1), pp. 49-62, 2001.

[4] K. Hennessy and C.S. Lent, "Clocking of molecular quantum-dot cellular automata," *JOURNAL OF VACUUM SCIENCE and TECHNOLOGY B,* Vol.19(5), pp. 1752-1755, 2001.

[5] H.T. Kung and C.E. Leiserson, "Systolic arrays (for VLSI)," In I.S. Duff and G.W. Stewart, editors, *Sparse Matrix Proceedings,* pp. 256-282, 1978.

[6] D.J. Griffiths, *Introduction to Quantum Mechanics,* Prentice Hall, Eaglewood Cliffs, NJ 1994.

[7] P.D. Tougaw and C.S. Lent, "Logical Devices Implemented Using Quantum Cellular Automata", *Journal of Applied Physics*, Vol 75(3), pp. 1818-1825, 1994.

[8] C.S. Lent, B. Isaksen, "Clocked molecular quantum-dot cellular automata", *IEEE Trans. on Electron Devices,* vol.50, pp. 1890-96, 2003.