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Clocking Schemes for High Speed Digital Systems

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Stephen H. Unger*
Computer Science Department
Columbia University

Chung-Jen Tan
IBM T. J. Watson Research Center

*This author's contribution to the work was made largely as a sabbatical leave employee, summer employee, and consultant at IBM.

Index Terms

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Abstract

A key element (one is tempted to say the *heart*) of most digital systems is the clock. Its period determines the rate at which data is processed, and so should be made as small as possible, consistent with reliable operation.

Based on a worst-case analysis, clocking schemes for high-performance systems are analyzed. These are 1- and 2-phase systems using simple clocked latches, and 1-phase systems using edge-triggered D-flip-flops. Within these categories (any of which may be preferable in a given situation), it is shown how optimal trade-offs can be made by appropriately choosing the parameters of the clocking system as a function of the technology parameters. The trade-offs involve the clock period (which of course determines the data rate) and the tolerances that must be enforced on the propagation delays through the logic. Clock-pulse edge tolerances are shown to be an important factor. It is shown that, for systems using latches, their detrimental effects on the clock period can be converted to tighter bounds on the short-path delays by allowing D-changes to lag behind the leading edges of the clock pulses and by using wider clock pulses or, in the case of 2-phase systems, by overlapping the clock pulses.

1. Introduction

Virtually all contemporary computers and other digital systems rely on clock pulses to control the execution of sequential functions. A number of different general schemes are used, along with several different types of flip-flops or similar storage elements. Despite the deceptively simple outward appearance of the clocking system, it is often a source of considerable trouble in actual systems. The number of parameters involved, particularly in 2-phase systems, is large, and a close analysis reveals a surprising degree of conceptual complexity.

If one is not particularly interested in maximizing performance, then a 2-phase system with non-overlapping clocks, or a 1-phase system with edge-triggered FF's is not difficult to design. However, if minimizing the clock period is a prime issue, then the problem becomes far more complex. However, significant performance gains are possible by carefully choosing the clocking parameters (period, pulse-widths, overlap), and further gains may be achieved by using well designed latches.

In this study we develop sets of relations for 3 basic types of systems that make possible intelligent trade-offs between speed maximization (period minimization) and the difficulty of satisfying constraints on the logic path delays. We begin with discussions of the state devices considered, the nature of imprecision in clock-pulse generation and distribution systems, logic block delays, and the design goals. We then analyze the simple case of the 1-phase system using edge-triggered FF's. After this warm-up, we proceed to treat the 1-phase system using latches, a considerably more complicated case. An extension of the

methodology used in that section is then applied to the case of 2-phase systems using latches. Some overall conclusions are then presented in the final section.

1.1. State Devices and Their Parameters

The state devices (or storage elements) treated here are:

The *latch* [2, 6, 1] (sometimes referred to as the *polarity hold* latch. This is a device with inputs C and D, and output Q (often Q', the complement of Q is also generated), such that, ideally, while C = 0, Q remains constant (regardless of the value of D), and while C = 1, Q = D, changing whenever D changes (see Fig.1-1). (For real latches, as is explained below, there are non-zero delays in the response times, and there must be constraints on the behavior of the inputs.) The C- and D-inputs are usually referred to as the clock and data inputs respectively. Although it is not, in general, necessary to do so, in the applications treated here, the system clock signals are indeed fed to the C-inputs of the latches. A variety of implementations of latches are known, differing in such factors as suitability for various technologies, load driving ability, and relative values of the parameters to be discussed subsequently. Latches with logic hazards have been used in some systems. In order to eliminate the possibility of malfunction due to those hazards, the *complement* of the C-signal is distributed independently to the latches with its edges carefully controlled relative to the corresponding edges of the C-signals. We do not discuss such systems here, where it is assumed that the latches are free of hazards.

The *edge-triggered D-flip-flop* (ETDFF) [2, 6] has the same inputs and outputs as the latch, but Q responds to changes in D only on one edge of the C-pulse (see Fig.1-2). That is, Q can change only at the time that C changes from 0 to 1 (the rising edge of the C-signal), and then only if necessary to assume the same value that D has at that time. (There are also ETDFF's that change state on the negative-going edge of the C-signal. Furthermore, it is possible to build a double-edge-triggered D-FF [9] that will respond on *both* edges of the C-pulse)

(See hand drawn figures at end of manuscript)

Figure 1-1: Behavior of an Ideal Latch

(See hand drawn figures at end of manuscript)

Figure 1-2: Behavior of Ideal Positive Triggered ETDFF

1.1.1. Latch Parameters

The significant parameters for a latch are listed below, with rough definitions (illustrated in Fig. 1-3). These definitions are then refined to take into account dependencies that exist among the parameters.

(See hand drawn figures at end of manuscript)

Figure 1-3: Latch Parameters

C_{Wm}: Minimum clock-pulse width, the minimum width of the clock pulse such that the latch will operate properly even under worst-case conditions, and such that widening the C-pulse further by making its leading edge occur earlier will not affect the values of D_{DQ}, U, or H, as defined below.

D_{CQ}: Propagation delay from the C-terminal to the Q-terminal, assuming that the D-signal has been set early enough relative to the leading edge of the C-pulse.

D_{DQ}: Propagation delay from the D-terminal to the Q-terminal, assuming that the C-signal has been turned on early enough relative to the D-change.

U: The *set-up time*, the minimum time between a D-change and the trailing edge of the C-pulse such that, even under worst-case conditions, the Q-output will be guaranteed to change so as to become equal to the new D-value, assuming that the C-pulse is sufficiently wide.

H: The *hold time*, the minimum time that the D-signal must be held constant *after* the trailing edge of the C-signal so that, even under worst-case conditions, and assuming that the most recent D-change occurred no later than U prior to the trailing edge of C, the Q-output will remain stable after the end of the clock-pulse. (It is not unusual for the value of this parameter to be negative.)

Note that D_{DQ}, for example, may vary significantly depending on whether the latch output is being changed from 0 to 1 or vice versa. A similar situation exists for D_{CQ}. Where appropriate it is useful to add subscripts R or F to these parameters to distinguish between the rising and falling output cases. This will not be done here. Instead, we shall confine ourselves to using overall maximum and minimum values, as indicated below.

The addition to the subscripts of D_{DQ} or D_{CQ} of an M or m make these parameters the maximum or minimum values respectively. These are the extremes with respect to variations in the parameters of the components from which the latches are constructed, the directions of signal changes, and the destinations (Q or Q') of the signals.

In the definition of D_{CQ}, it is assumed that D has assumed its proper value early enough. We can make this concept more precise by requiring that the change in D occur sufficiently

early so that making it appear any earlier would have no effect on when Q changes. For any real latch it is always possible to define such an interval. Similarly, when defining D_{DQ}, it is assumed that the leading edge of C appears sufficiently early so that turning C on any earlier would not make Q change any sooner. Again this is possible for any real latch.

Now we state an important postulate regarding propagation delays:

Suppose that C goes on at time t_C, and that D changes, making D different from Q, at time t_D. Then we postulate that the time, t_Q, at which Q changes is, at the latest:

$$t_Q = \mathrm{MAX}[t_C + D_{CQM}, t_D + D_{DQM}] \tag{1}$$

Although for some latches there are higher order effects, depending on the technology, that may cause t_Q to be larger when the difference between the arguments of the MAX is small, the error is small enough to justify our postulate for most practical purposes. Refining the model to take such effects into account is left for further research.

A related assumption about latch behavior is that, provided that the set-up, hold-time, and minimum pulse-width constraints are observed, the propagation delay will not be affected by the clock-pulse going off before the output changes in response to a D-change. An examination of a variety of latch designs appears to justify this assumption.

There are other possibilities for refining our results, by using more complex definitions of latch parameters. If we define the actual interval between the occurrence of a D-change and the trailing edge of C as u (note that proper operation requires that $u \geq U$), then, for many latch designs it will be found that the hold time, H, is, over some range of values of u, a decreasing function of u. There are also possibilities for reducing the clock-pulse width below C_{Wm} (within limits), usually at a cost of increasing propagation delays and/or set-up and hold times. For the sake of making the analysis more tractable, we shall not consider these alternatives, but instead shall assume that there is a fixed, consistent, set of latch parameters, as described above.

In summary, we assume that the minimum clock-pulse width is large enough so that further increases cannot reduce any of the other latch parameters, that U is minimal, that H is minimal given U, and that the postulate stated above regarding propagation delays is valid.

1.1.2. Edge-Triggered-D-FF Parameters

The significant parameters for an ETDFF are defined below (see also Fig.1-4:

U: The *set-up time*, the minimum time that the D-signal must be stable prior to the triggering edge of the C-pulse.

H: The *hold time*, the minimum time that the D-signal must be held constant *after* the triggering edge of the C-pulse. (The value of H may be 0 or even negative for some ETDFF's.)

C_{Wm}: Minimum clock-pulse width, the minimum width of the clock pulse such that the ETDFF will operate properly even under worst-case conditions.

D_{CQ}: *Propagation delay* from the C-terminal to the Q-terminal, assuming that the D-signal has been set up sufficiently far in advance as specified by the set-up time constraint.

(See hand drawn figures at end of manuscript)

Figure 1-4: Parameters of a Positive-Edge-Triggered-D-FF

1.2. Clock-Pulse Edge Deviation

In any real world system there are limits to the precision with which events can be timed. Our concern here is with synchronous systems with clock-pulses distributed to a multitude of devices for the purpose of coordinating events. The intent is to have certain clock-pulse edges occur simultaneously at all devices (in some cases fixed displacements may be specified for corresponding signals at different devices). In designing clocking schemes, it is necessary to take into account the extent to which this goal cannot be fully attained.

The approach taken here is to assume that, at each significant clock-pulse edge, there is a specified tolerance range, within which we can assume the errors will be confined. This is, essentially, a "worst-case" approach. No attempt will be made to exploit statistical information that could make possible more precise estimates of errors, nor will any effort be made to consider the effects of correlations between errors or between delays.

The most elaborate situation that we deal with is that of 2-phase systems using latches as storage elements. Here both the leading and trailing edges of both clock-pulses are of interest (although the analysis makes it clear that certain edges are more significant than others). We define tolerances for all 4 edges, designating them as T_{1L}, T_{1T}, T_{2L}, and T_{2T}, corresponding to the leading and trailing edges of C1 and C2 respectively. Assume that, for example (see Fig. 4-2), the leading edge of the C1-pulse for some period would have arrived at every latch at time t (which we refer to as its *nominal* arrival time) if there were no inaccuracies in timing. Then, in the actual system, this edge is received at every latch somewhere in the time interval, $(t - T_{1L}, t + T_{1L})$. Corresponding assumptions of course apply for the other 3 edges. Our goal is to design our systems so that if this assumption, and corresponding assumptions about the precision of the components used, are valid, then there will be no failures due to timing, even if some malicious demon is, in each case, permitted to choose the extreme deviations most likely to cause trouble. Of course in 1-

phase systems we need only define 2 edge tolerances, T_L and T_T.

We are lumping together in these edge tolerances all sources of imprecision in clock timing and distribution. These are principally in the circuits used to determine the clock-pulse widths, often called "shapers", and in the networks used to distribute the pulses to the individual latches (or other similar devices). This latter factor is generally referred to as clock-pulse skew. In the case of 2-phase systems, it is also necessary to consider the circuits that determine the phase relationship between the C1- and C2-clocks.

Relative to other sources of error, the precision with which the clock frequency can be maintained, at least in high performance systems, is so great (due to the use of crystal controlled oscillators) that we can safely neglect this factor. (If this assumption is not justified in any particular case, it is not difficult to introduce a tolerance factor on the clock period, which can be superposed on our basic results.)

By representing all of the timing deviations in terms of the edge tolerances, we simplify our analysis, making it easier to treat, as a separate issue, the mechanisms whereby precision is lost.

The precision with which clock-pulse widths can be controlled is generally a function of how precisely delay elements can be specified. The same factor usually is involved in controlling the phase between the C1- and C2-pulses of a 2-phase system. The ratio of 2 delays on the same chip can be specified with much greater precision than is the case for delays on different chips. Usually one edge of the output of a shaper can be controlled more precisely than the other. In the 2-phase case, there are techniques for minimizing the edge-tolerances for particular pairs of edges. As is shown in the sequel, T_{2L} and T_{1T} are usually more significant. They should therefore be kept smaller, relative to the other 2 edge tolerances.

Several factors contribute to clock-pulse skew. Despite all efforts to equalize conduction path lengths between the clock source and each clock-pulse "consumer", differences inevitably occur in both off-chip wiring and in paths on chips. Since it is usually necessary to provide amplifiers in the distribution paths, variations in the delays encountered in such devices along different paths produce significant amounts of skew.

Another contribution to skew results from the fact that pulse edges are never vertical as shown in our idealized diagrams, and that there is variability among individual latches, even on the same chip, with respect to the voltage thresholds that effectively distinguish 1's from 0's. Thus even if a pulse edge should arrive simultaneously at the inputs to 2 different latches, its effect might be felt at different times due to a difference in thresholds. The result is the same as if the delays in the paths leading to the 2 latches differed. Hence such effects are considered as part of the skew. Note that, unlike the factor due to varying length conduction paths, this effect could result in the delayed sensing of a *positive*-going edge at a latch that is relatively quick in sensing a *negative*-going edge. (This would occur if the device involved had a relatively high threshold.)

1.3. Logic Block Delays

In addition to the various parameters associated with the clocking system and with the latches or FF's, a very important pair of parameters is that associated with the logic circuitry: the *maximum* and *minimum* delays in any path through the logic block, designated as D_{LM} and D_{Lm} respectively. As is made evident in our analysis, large variations among logic path delays are clearly detrimental. That is, for a given value of D_{LM}, it is desirable to keep the *smallest* path delay as close to D_{LM} as possible.

It is frequently the case, when choosing the clocking parameters, that the value of D_{LM}, the *long-path* delay is given; it is a function of the maximum number of stages of logic, the amount of fan-in and fan-out associated with gates in the longest paths, and of the technology, which determines propagation delay through individual gates. The lower bound on the *short-path* delay D_{Lm}, on the other hand, can often be dictated, within limits, by the clock system designer, using such means as adding delay pads to increase the delays in the shortest paths, or adjusting the power levels of certain key gates.

The ultimate limits on how tightly the short-path delays can be controlled, that is, on how high a lower bound, D_{LmB}, on them is feasible, depend on the tolerances with which gate delays can be specified, as well as on how well wire lengths, both on and off chip can be predicted at design time. It is these factors that determine, for a given value of D_{LM}, what the largest feasible value of D_{LmB} is.

1.4. Goals for Design of Clocking Schemes

It is assumed here that a principal goal in the specification of a clocking scheme is to make the period as small as possible, which is tantamount to maximizing the speed of the system. But of course this must be done within the confines of a design that results in a system that can be made to operate reliably.

It is obvious that minimizing D_{LM} is basic to minimizing the clock period. But, as pointed out above, it is also important to keep the *smallest* path delay as large as possible. But it is by no means easy to make the logic path delays uniform in value. For this reason, we have developed procedures for finding the minimum possible value of P given the maximum achievable lower bound, D_{LmB}, on the short-path delays.

2. Optimum Parameters for 1-Phase Clocking with ETDFF's

For 1-phase systems using ETDFF's, the clocking parameters to be determined, (see Fig.1-4) are the period, P, and the clock-pulse width, W. A block diagram of the systems under consideration is shown as Fig.2-1.

(See hand drawn figures at end of manuscript)

Figure 2-1: Block Diagram of a 1-Phase System

We develop a set of constraints, such that if all are satisfied, and if the D-signals arrive on time for the first cycle, then they will also arrive on time for the next cycle and will remain stable long enough to ensure that the FF's react properly. By induction, it follows

that, for all succeeding cycles, the FF-inputs are also stable over the appropriate intervals, so that the system will behave according to specifications.

For any clock-pulse period, proper operation requires that the D-signals become stable at least U prior to to the earliest possible occurrence of the triggering edge. (It is assumed here that this is the positive-going edge. Precisely the same arguments apply where the triggering edge is negative going- or even if the FF's trigger on both edges.) If we assume that t = 0 coincides with the nominal time of the leading edge of the current clock pulse, then the earliest possible occurrence time of that edge is $-T_L$. (See part (a) of Fig.2-2.) Hence, the latest possible arrival time, under worst-case conditions, of the D-signals for the current clock pulse, t_{DLArr}, must meet the constraint:

$$t_{DLArr} \leq -T_L - U$$

(See hand drawn figures at end of manuscript)

Figure 2-2: Ensuring that D-Signals Don't Arrive Too Late in ETDFF Systems

Defining the latest possible arrival time, under worst-case conditions, of the D-signals for the *next* clock-pulse as t_{DLArrN}, it follows that "on time arrival" of D for the next cycle means:

$$t_{DLArrN} \leq P - T_L - U \tag{2}$$

Since the *latest* possible occurrence of the leading edge of the current clock-pulse is at T_L, it follows that the latest arrival time of the D-signals for the next cycle is:

$$t_{DLArrN} = T_L + D_{CQM} + D_{LM} \tag{3}$$

(See part (b) of Fig.2-2.)

Replacing t_{DLArrN} in relation (2) by its value from equation (3), we have the required constraint to ensure that D-signals are not late:

$$P - T_L - U \geq T_L + D_{CQM} + D_{LM}$$

Solving for P converts it to a more meaningful form:

$$P \geq 2T_L + U + D_{CQM} + D_{LM} \tag{4}$$

Next it is necessary to constrain the system so as to ensure that the *earliest* arrival time of a D-signal for the *next* cycle does not arrive so early as to violate the hold-time constraint for the current cycle. (See Fig.2-3.)

(See hand drawn figures at end of manuscript)

Figure 2-3: Ensuring that D-Signals in ETDFF Systems Don't Arrive Too Early

Given that the latest occurrence time of the leading edge of a clock pulse is T_L, the hold-time constraint mandates that the earliest occurrence time of a D-signal for the next cycle, t_{DEArrN}, satisfy:

$$t_{DEArrN} > T_L + H \tag{5}$$

Since the *earliest* occurrence of a leading edge of a clock pulse is at $-T_L$, we can express t_{DEArrN} in terms of the FF propagation delay and the logic delay as:

$$t_{DEArrN} = -T_L + D_{CQm} + D_{Lm}$$

Inserting the value of t_{DEArrN} from the above equation into relation (5) gives us a relation, the satisfaction of which is a necessary and sufficient condition for preventing, under worst-case assumptions, premature changes in D-signals:

$$-T_L + D_{CQm} + D_{Lm} > T_L + H$$

Simplifying and re-arranging terms yields the basic constraint that defines D_{LmB}, the lower bound on the short-path delays:

$$D_{Lm} > D_{LmB} = 2T_L + H - D_{CQm} \tag{6}$$

In addition to constraints (4) and (6) on the period and short-path delays, it is necessary to add a third constraint to ensure that the minimum pulse-width specification for the FF's is satisfied. Since, under worst-case assumptions skew might make the leading edge late and the trailing edge early, the minimum width specification for the clock pulses is:

$$W \geq 2T_L + C_{Wm} \tag{7}$$

The procedure for choosing optimum clocking parameters for 1-phase systems using ETDFF's is usually very straightforward. We simply set W at any convenient value satisfying constraint (7) and set P to satisfy constraint (4) with equality. In most cases it will be found that the constraint on the short-path bound given by (6) is not difficult to meet. In the unlikely event that this is not the case, it may be necessary to insert delay pads at the outputs of the FF's. The procedure for doing this is the same as that for the 1-phase case with latches, treated in Section 3.4 on page 15.

3. Optimum Parameters for 1-Phase Clocking with Latches

Fig.2-1 is a block diagram of the 1-phase systems treated here. Clock signals with parameters noted are shown in Fig.3-1. We shall develop a set of constraints, involving the various parameters we have discussed, such that if and only if they are all respected, the system will operate properly in the sense that the D-inputs to all the latches will arrive on time for each clock cycle (as specified by the set-up time parameter), and will remain stable for a sufficient interval (as specified by the hold-time parameter).

(See hand drawn figures at end of manuscript)

Figure 3-1: Parameters for 1-Phase Systems

The argument is in the form of induction on the clock periods. It is assumed at the outset that the D-signals arrive on time for the first clock cycle. Constraints are developed to ensure that, given this assumption, the D-signals will arrive on time for the next cycle. Additional constraints are then found to ensure that the D-signals remain stable for an adequate interval during the first cycle. It is then obvious by induction that the same will be true for all subsequent clock cycles.

More specifically, our initial assumption is that, under worst-case conditions (of delay values, edge tolerances, etc.), every D-signal must arrive (at a latch input terminal) no later than U prior to the trailing edge of the clock pulse. Taking $t = 0$ as the *nominal* time of occurrence of the *leading* edge of the clock pulse for the current cycle (i.e. the time this edge would arrive if the tolerance on this edge, T_L, were 0) , the earliest possible occurrence time of the *trailing* edge would be $W - T_T$.

Since the D-signal must arrive at least U prior to this edge, we have for the latest permissible arrival time for D, t_{DLArr}:

$$t_{DLArr} \leq W - T_T - U \tag{8}$$

Assume now that the above constraint is satisfied for the first clock cycle.

3.1. Preventing Late Arrivals of D-Signals

The latest (under worst-case conditions) arrival time of D-signals for the next cycle is designated as t_{DLArrN}. The maximum permitted value of t_{DLArrN} is found by simply adding P to the right side of (8):

$$t_{DLArrN} \leq W - T_T - U + P \tag{9}$$

(See part (a) of Fig.3-2).

The worst-case value of t_{DLArrN} is the latest time at which the output of a latch could respond to a D-signal, plus the maximum delay through the logic. Designating the latest occurrence time of a leading edge of a clock pulse as t_{CLL}, and using postulate (1) (see page 4) for determining the latest time at which the output of a latch could change, we obtain:

$$t_{DLArrN} = MAX[t_{CLL} + D_{CQM}, t_{DLArr} + D_{DQM}] + D_{LM}$$

(See hand drawn figures at end of manuscript)

Figure 3-2: Ensuring that D Arrives Sufficiently Early

(The discussions pertaining to the left and right parts respectively of the MAX expression are illustrated by parts (b) and (c) of Fig.3-2) The value of t_{CLL} is clearly T_L, and the value of t_{DLArr} is given by (8), so replacing those variables in the above relation gives us:

$$t_{DLArrN} = MAX[T_L + D_{CQM}, W - T_T - U + D_{DQM}] + D_{LM} \tag{10}$$

Combining (9) with (10) produces:

$$MAX[T_L + D_{CQM}, W - T_T - U + D_{DQM}] + D_{LM} \leq W - T_T - U + P$$

Solving for P yields:

$$P \geq MAX[T_L + T_T + U + D_{CQM} - W, D_{DQM}] + D_{LM}$$

This expression can be decomposed into 2 constraints that, in combination, are equivalent to it:

$$P \geq D_{CQM} + D_{LM} + U + T_L + T_T - W \tag{11}$$

and

$$P \geq D_{DQM} + D_{LM} \tag{12}$$

The constraint (12) can be intuitively justified by noting that it represents the total time for a signal to traverse a complete loop, under worst-case conditions. If the period were any less, then, if the worst-case conditions were actually realized, a signal following a sequence of such maximum delay paths would fall increasingly far behind the clock pulses until it eventually violated a set-up time constraint.

Constraint (11) can also be justified intuitively. (Transposing the W-term makes this clearer.) It can be interpreted as stating that, starting at the leading edge of a clock pulse, there must be time, under even worst-case conditions, before the trailing edge of the *next* clock pulse, for a signal to get through a latch, and the logic block in time to meet the set-up time constraint at the input to some latch.

The D-signals for the next cycle will arrive on time if, and only if, both (11) and (12) are

satisfied, and if (8) is satisfied for the current cycle.

3.2. Preventing Premature Arrivals of D-Signals

If the D-signal for the next clock cycle is generated too soon, then the hold-time constraint for a latch might be violated. This is where the short-path delays become important. In order to prevent the possibility of a hold-time violation, it is necessary that, in the worst-case, a D-change for the next cycle not occur until at least H after the latest possible occurrence of the trailing edge of the clock-pulse defining the current cycle. With t_{CLT} as the latest occurrence of a clock-pulse trailing edge, and t_{DEArrN} as the earliest possible arrival of a D-signal for the next cycle, this constraint is expressed as:

$$t_{DEArrN} > t_{CLT} + H$$

(This discussion is illustrated by part (a) of Fig.3-3.) Replacing t_{CLT} by its value, W + T_T, we obtain:

$$t_{DEArrN} > W + T_T + H \tag{13}$$

Letting t_{CEL} represent the earliest possible arrival time of a clock-pulse leading edge, and t_{DEArr} represent the earliest arrival time of a D-signal for the *current* cycle, we again utilize postulate (1) to obtain:

$$t_{DEArrN} = MAX[t_{CEL} + D_{CQm}, t_{DEArr} + D_{DQm}] + D_{Lm}$$

(See hand drawn figures at end of manuscript)

Figure 3-3: Ensuring that D Doesn't Arrive Too Early

(The discussion involving the left part of the MAX is illustrated in Fig.3-3(b).) Replacing t_{CEL} by its value, $-T_L$, and bringing D_{Lm} inside the MAX, yields:

$$t_{DEArrN} = MAX[-T_L + D_{CQm} + D_{Lm}, t_{DEArr} + D_{DQm} + D_{Lm}] \tag{14}$$

Inserting the above value of t_{DEArrN} in (13) yields:

$$MAX[-T_L + D_{CQm} + D_{Lm}, t_{DEArr} + D_{DQm} + D_{Lm}] > W + T_T + H \tag{15}$$

Now we show that, for a system that operates properly even under worst-case conditions, (15) is satisfied if, and only if, the left part of the MAX in (15) exceeds the right side of the inequality. The "if" part of this assertion is obviously true.

To prove necessity (the "only if" part) let us assume that (15) is valid but that the left part of the MAX does *not* exceed the right part of the inequality. Then it follows that the

right part of the MAX must satisfy the inequality, and hence must exceed the left part of the MAX. In that case, (14) is reduced to:

$$t_{DEArrN} = t_{DEArr} + D_{DQm} + D_{Lm} \tag{16}$$

But from relation (12) it is clear that:

$$P > D_{DQm} + D_{Lm}$$

Adding t_{DEArr} to both sides yields:

$$t_{DEArr} + P > t_{DEArr} + D_{DQm} + D_{Lm}$$

From the above and from (16) we then obtain:

$$t_{DEArr} + P > t_{DEArrN}$$

But this means that, for each cycle (in the worst case), D arrives earlier and earlier relative to the trailing edge of C. Therefore, even if t_{DEArr} is comfortably above the minimum for the first cycle, it will eventually violate the hold-time constraint, and hence the system would not operate properly under worst-case conditions. Hence, by contradiction, we have completed the argument that (15) is equivalent to

$$-T_L + D_{CQm} + D_{Lm} > W + T_T + H$$

or, solving for D_{Lm}:

$$D_{Lm} > D_{LmB} = T_L + T_T + H + W - D_{CQm} \tag{17}$$

The above expression gives us the lower bound, D_{LmB}, on the short-path delay. Satisfying this bound is necessary and sufficient to ensure against the premature arrival of a D-signal.

3.3. Consequences of the Constraints

The basic constraints derived in the previous subsections are reproduced below:

$$P \geq D_{CQM} + D_{LM} + U + T_L + T_T - W \tag{11}$$

$$P \geq D_{DQM} + D_{LM} \tag{12}$$

$$D_{Lm} > D_{LmB} = T_L + T_T + H + W - D_{CQm} \tag{17}$$

To these we must add one more to ensure that, even under worst case conditions, the clock-pulse width at any latch input meets the minimum clock pulse width specifications of the latches. This is:

$$W \geq C_{Wm} + T_L + T_T \tag{18}$$

W in (11) cannot usefully be increased beyond the point where the right side of (11) would, if equality held, violate (12), which of course also represents a lower bound on P. Note that it is undesirable to increase W gratuitously, since this would, as indicated by constraint (17), raise the lower bound on the short-path delays. To find the maximum useful value of W, treat (11) and (12) as equalities and solve them simultaneously (eliminating P) to obtain:

$$W = U + T_L + T_T + D_{CQM} - D_{DQM} \tag{19}$$

When W is less than the above value, relation (11), with equality, specifies the minimum value of P. When W equals that value, the minimum value of P is given by (12). The maximum useful value of D_{LmB} is found by substituting into (17) the maximum useful value of W. This gives us:

$$D_{LmB} = H + U + 2(T_L + T_T) + D_{CQM} - D_{CQm} - D_{DQM} \tag{20}$$

If the value of the lower bound on the short-path delays given by the above relation is attainable, then the minimum P-value of (12) is attainable. If not, then, to find the minimum P-value as a function of an achievable value of D_{LmB}, solve (17) and (11) (as equations) simultaneously for P, eliminating W. this results in:

$$P = H + U + 2(T_L + T_T) + D_{CQM} - D_{CQm} + D_{LM} - D_{LmB} \tag{21}$$

Since W must also satisfy constraint (18), there is a corresponding lower bound on D_{LmB}, which is found by substituting into (17) the right side of (18) for W to obtain:

$$D_{LmB} = 2(T_L + T_T) + H - D_{CQm} + C_{Wm} \tag{22}$$

The relations developed here are the basis for the optimization procedure of the next subsection. First, however we must consider a possible variation of the development thus far.[1] The initial assumption in the discussion of 1-phase systems was that the D-signals

[1]The necessity for considering this possibility was pointed out by Vijay Pitchimani and Gordon Smith.

must appear at latch inputs no later than U prior to the trailing edges of the clock pulses. In what followed, this constraint was consistently observed. But what if we had made a stronger assumption, i.e. that the D-changes must appear even earlier, say at U + r (r >0) prior to the trailing edges of the clock pulses? Is it possible that there might be some advantages to this?

The key to analyzing this question is to observe that the proposal is exactly equivalent to assuming a larger value of the set-up time U. The effect of this can be determined by looking at those constraints and derived relations that involve U, namely (11), (19), (20) and (21). The value of D_{LmB} necessary to achieve the minimum P increases with U. So does the minimum value of P for any value of D_{LmB} in the range for which equation (21) is valid. Thus there are clear disadvantages to this alternative of effectively increasing U, and no apparent advantages to compensate for them. It follows then that any 1-phase clocking scheme that violates any of our constraints will, under the worst-case assumption, either be vulnerable to failure, or will be suboptimum in that either P or D_{LmB} would be reducible without increasing the other.

3.4. When the Short-Path Bounds Cannot be Met

Now observe that neither the basic constraint (17) on D_{LmB}, nor either of the derived extremes of D_{LmB} given by (20) and (22) involve D_{LM}. Thus there is no inherent reason why the range found for D_{LmB} (in terms of the afore-noted extremes) should be much below- or indeed not *above*- D_{LM}. If, despite all efforts, including the use of delay pads in critical paths, it is still not possible to satisfy the lower bound on the short-path delays represented by (22), then (assuming that the relevant latch or other parameters cannot be favorably altered so as to remedy this situation), it is necessary to resort to more drastic measures.

The most practical technique appears to be to introduce uniform delay elements into *all* logic paths so as to increase the minimum path delays by an amount sufficient to get us into the desired range. Suppose, for example that the largest value of D_{LmB} that can be reliably guaranteed, is less than the bound of (22) by the amount d_x. Then we could add delay pads with *minimum* values d_x to the outputs of all latches. The effect would be to increase the attainable D_{LmB} to the desired minimum, and to increase D_{LM} by the amount corresponding to the *maximum* value of delay elements with minimum values d_x. If we define T_d as the delay element tolerance ratio, d_M/d_m, then the addition to D_{LM} is $T_d d_x$. Note that P increases by $T_d d_x$ over the value obtained for it if the D_{LmB} from (22) is used in equation (21). The graph of Fig.3-4 illustrates how P varies with the maximum attainable value of D_{LmB}. It is piece-wise linear, with the left part corresponding to the region where uniform pads must be added as just indicated, and with the right part generated directly from equation (21). The value P_1 corresponds to the value given by relation (12).

(See hand drawn figures at end of manuscript)

Figure 3-4: P As a Function of the Largest Achievable Lower Bound on Short-Path Delay

3.5. Procedure for Optimizing the Clocking Parameters

We are now in position to describe a procedure for finding the minimum clock period, given D_{MLmB}, the maximum lower bound we can enforce on the short-path delays. The corresponding value of W is also determined.

A complicating factor is the possibility that the lower bound on W, given by (18), might exceed what we have called the "maximum useful value of W", given by (19). In that event, the W-value is given by (18), and D_{LmB} is given by (22). Note that, when D_{MLmB} is less than the required value of D_{LmB}, it is necessary to pad the outputs of all latches with delay elements whose *minimum* values make up the difference. This adds to the period an amount T_d times this minimum value.

The procedure is as follows:

```
IF the right side of (18) ≤ the right side of (19)
THEN
  IF D_MLmB ≥ right side of (20)
  THEN
    D_LmB ⇐ right side of (20)

    W ⇐ right side of (19)
    P ⇐ right side of (12)
  ELSE
    D_LmB ⇐ D_MLmB
    IF D_MLmB ≥ right side of (22)
    THEN
      P ⇐ right side of (21)
      Solve (17) to determine W
    ELSE
      d ⇐ right side of (22) - D_MLmB
      In all latch outputs put delay pads with minimum value d
      W ⇐ right side of (18)
      P ⇐ right side of (11) + T_d d
ELSE
  W ⇐ right side of (18)
  D_LmB ⇐ right side of (22)
  IF D_MLmB ≥ right side of (22)
  THEN
    P ⇐ right side of (12)
  ELSE
    d ⇐ right side of (22) - D_MLmB
    In all latch outputs put delay pads with minimum value d
    P ⇐ right side of (12) + T_d d
```

Other procedures based on the constraints developed here may be useful under special circumstances.

4. Optimum Parameters for 2-Phase Clocking with Latches

Fig.4-1 is a general block diagram of the 2-phase clocked systems treated here. Clock signals (shown in Fig.4-2) go directly to the C-inputs of the latches. Facilities for scan-in and scan-out are not included as they do not affect the basic arguments.

The strategy to be followed is based on the assumption that if the D-inputs to all of the latches are valid in the intervals specified by the U and H parameters, then the system will operate as specified. A set of constraints will be derived, such that if the D-inputs to all of the L1-latches arrive early enough for the first clock cycle, then if, and only if, all of the constraints are satisfied, the inputs to the L2-latches will arrive on time for the first C2-clock interval, and the D-inputs to the L1-latches will arrive early enough for the next C1-clock interval. Also, the D-inputs to the L1-latches will remain valid long enough during the first C1-interval, and the D-inputs to the L2-latches will remain valid sufficiently long during the first C2-interval. By induction, it then follows that, for all subsequent clock periods, the latches will all have valid inputs during the prescribed intervals.

(See hand drawn figures at end of manuscript)

Figure 4-1: Block Diagram of a 2-Phase Clocked System

(See hand drawn figures at end of manuscript)

Figure 4-2: Parameters for 2-Phase Systems

Throughout the following discussion it is assumed that t = 0 at the *nominal* time (by "nominal time" we mean what the time would be if the edge tolerances were 0) of the leading edge of the C2-clock. (The *actual* arrival time of this edge at any L2-latch may be anywhere between $-T_{2L}$ and $+T_{2L}$). It follows then that the earliest arrival time of the trailing edge of the C1-pulse is $V - T_{1T}$. To ensure that the L1-latch set-up time constraints are met, even under worst-case conditions, t_{D1LArr}, the latest arrival time for D1-signals during the current clock cycle, must satisfy:

$$t_{D1LArr} \leq V - T_{1T} - U_1 \tag{23}$$

In all that follows, it is assumed that, for the first clock period, all D1-signals arrival times satisfy constraint 23.

The argument that the constraints developed here are *necessary* as well as sufficient is dependent on the assumption that, in the worst case, (23) is satisfied with equality. Since this is not actually necessary, it follows that the constraints are not strictly necessary. However, enforcing a more stringent constraint on arrival times of D1-signals, namely that they be required to be earlier by some additional amount, is equivalent to assuming that U_1 has increased by this same amount. The effect of this is considered at the end of this section, where it is shown that, as compared with the disadvantages, there is very little to be gained by increasing U_1 (or U_2, which is equivalent to insisting that the D2-signals arrive at a time earlier than required by the set-up time requirements).

4.1. Latest Arrival times of D2-Signals For First Clock Interval

First we develop constraints to ensure that, if the D1-signals arrive on time, the D2-signals will also arrive on time. (Refer here to Fig.4-3(a).) In this case, "on time" means that, in order to respect the set-up time constraint for the L2-latches, the D2-signals must arrive no later than U_2 prior to the trailing edge of the C2-pulses. *At the earliest*, the trailing edge of a C2-pulse might occur at $W_2 - T_{2T}$.

So the latest arrival time, t_{D2LArr}, of the D2-signals must satisfy:

$$t_{D2LArr} \leq W_2 - T_{2T} - U_2 \,. \tag{24}$$

(See hand drawn figures at end of manuscript)

Figure 4-3: D2 Arrival Time

Let t_{C1LL} be the latest arrival time of the leading edge of a C1-pulse. Then, recalling postulate (1) (see P.4) about latch propagation delays, the latest time when the output of an L1-latch changes (an alternate description of t_{D2LArr}) is as follows (the left side of the MAX is illustrated by part (c) of Fig.4-3, and the right side by part (b)):

$$t_{D2LArr} = \mathrm{MAX}[t_{D1LArr} + D_{1DQM},\ t_{C1LL} + D_{1CQM}]$$

Replacing t_{C1LL} by its value, $V - W_1 + T_{1L}$, and t_{D1LArr} by the value given in relation (23) (assuming that (23) is satisfied with equality) gives us:

$$t_{D2LArr} = \mathrm{MAX}[V - U_1 - T_{1T} + D_{1DQM},\ V - W_1 + T_{1L} + D_{1CQM}] \tag{25}$$

Combining (24) with (25) we obtain:

$$\mathrm{MAX}[V - U_1 - T_{1T} + D_{1DQM},\ V - W_1 + T_{1L} + D_{1CQM}] \leq W_2 - T_{2T} - U_2$$

This can be expressed as 2 separate constraints:

$$V - U_1 - T_{1T} + D_{1DQM} \leq W_2 - T_{2T} - U_2$$

and

$$V - W_1 + T_{1L} + D_{1CQM} \leq W_2 - T_{2T} - U_2$$

which can be rewritten, respectively, as:

$$W_2 \geq V + U_2 - U_1 + D_{1DQM} + T_{2T} - T_{1T} \tag{26}$$

and:

$$W_1 + W_2 \geq V + U_2 + D_{1CQM} + T_{1L} + T_{2T} \tag{27}$$

If (23) is satisfied, then (26) and (27) are sufficient conditions for ensuring that, even under worst-case conditions, the D2-signals arrive on time. If (23) is satisfied with equality, then they are also sufficient for this purpose.

4.2. Latest Arrival Times of D1-Signals During the Next Cycle

Now consider what is required to ensure that the D1-signals arrive on time for the *next* clock cycle, assuming that the D1- and D2-signals are on time for the present cycle. (Refer here to part (a) of Fig.4-4.) The upper bound on the latest arrival time, $t_{D1LArrN}$, of a D1-signal during the next cycle is obtained from (23), which gives the latest permissible arrival time for the first cycle, by simply adding the period, P, to the right side. This gives us:

$$t_{D1LArrN} \leq P + V - U_1 - T_{1T} \tag{28}$$

(See hand drawn figures at end of manuscript)

Figure 4-4: D1 Arrival Time

Now consider how long it might take a signal to get through an L1-latch, through the following L2-latch, and through the logic to reach an L1-latch input in time for the next C1-pulse. (See Fig.4-1). In terms of the latest arrival time at an L2-input, t_{D2LArr}, and the latest possible occurrence of a C2 leading edge, t_{C2LL}, postulate (1) (p.4) gives us for the latest arrival time, t_{Q2LArr}, for a signal at an L2-output:

$$t_{Q2LArr} = MAX[t_{D2LArr} + D_{2DQM}, t_{C2LL} + D_{2CQM}]$$

Adding the maximum delay through the logic, D_{LM}, gives us the latest arrival time, $t_{D1LArrN}$, for a signal at an L1-input during the *next* cycle:

$$t_{D1LArrN} = MAX[t_{D2LArr} + D_{2DQM}, t_{C2LL} + D_{2CQM}] + D_{LM}$$

Equation (25) gives us t_{D2LArr}, and t_{C2LL} is simply T_{2L}. Substituting in the above relation yields:

$$t_{D1LArrN} = MAX[MAX[V - U_1 - T_{1T} + D_{1DQM},$$

$$V - W_1 + T_{1L} + D_{1CQM}] + D_{2DQM},$$

$$T_{2L} + D_{2CQM}] + D_{LM}$$

Expanding the inner MAX yields:

$$t_{D1LATTN} = MAX[V - U_1 - T_{1T} + D_{1DQM} + D_{2DQM},$$
$$V - W_1 + T_{1L} + D_{1CQM} + D_{2DQM},$$
$$T_{2L} + D_{2CQM}] + D_{LM} \tag{29}$$

There are 3 factors restricting the propagation of signals thru the 2 latches: propagation thru the D-inputs of both L1- and L2-latches, propagation from the C-inputs of the L1-latches (involving the location of the C1-leading edge) through the D-inputs of L2-latches, and propagation from the C-inputs of the L2-latches (involving the location of the C2-leading edge). These are all accounted for in the above expression. They are illustrated in parts (b), (c), and (d), respectively of Fig.4-4.

Replacing $t_{D1LATTN}$ in (28) by the value found in (29) gives us:

$$MAX[V - U_1 - T_{1T} + D_{1DQM} + D_{2DQM},$$
$$V - W_1 + T_{1L} + D_{1CQM} + D_{2DQM},$$
$$T_{2L} + D_{2CQM}] + D_{LM} \leq P + V - U_1 - T_{1T}$$

Solving for P and simplifying yields:

$$P \geq MAX[D_{1DQM} + D_{2DQM},$$
$$- W_1 + D_{1CQM} + D_{2DQM} + U_1 + T_{1L} + T_{1T},$$
$$T_{1T} + T_{2L} - V + D_{2CQM} + U_1] + D_{LM} \tag{30}$$

Relation (30) can be decomposed into the following 3 equivalent constraints which, taken together, are equivalent to it:

$$P \geq D_{1DQM} + D_{2DQM} + D_{LM} \tag{31}$$

$$P \geq - W_1 + D_{1CQM} + D_{2DQM} + U_1 + D_{LM} + T_{1L} + T_{1T}$$

or, solving for W_1:

$$W_1 \geq - P + D_{1CQM} + D_{2DQM} + U_1 + D_{LM} + T_{1L} + T_{1T} \tag{32}$$

$$P \geq -V + D_{2CQM} + U_1 + D_{LM} + T_{1T} + T_{2L} \tag{33}$$

Each of the above constraints can be justified intuitively:

Constraint (31) indicates that the period cannot be less than the total time it would take a signal, under worst case conditions, to propagate around a loop (i.e. thru an L1- L2-latch pair and the logic).

Constraint (33) (when the -V is transposed) states that, starting at the leading edge of a C2-pulse, there must be time, prior to the end of the *next* C1-pulse, for signals to get through L2-latches and the logic to the inputs of L1-latches prior to the set-up times for those latches, under worst case conditions of logic delay, latch delay and edge tolerances.

Similarly, (32) states (transposing the -P term helps make this clearer) that a similar relation holds with respect to starts made at the leading edge of C1-pulses and ending at the trailing edges of C1-pulses during the next cycle.

Note that if (26) is satisfied with equality, and if (27) is satisfied, then, it is not difficult to show, with the aid of (31), that (32) is implied. Alternatively, satisfying both (32) with equality and (27) ensures that (26) is satisfied.

4.3. Premature Changes of D1-Signals

Next we ensure that changes in D1-signals do not propagate through the L1- and L2-latches and the logic so fast that they cause some D1-inputs to change to their values for the *next* cycle prematurely, i.e. before the hold times for the current cycle have expired. (Refer here to part (a) of Fig.4-5.) The earliest arrival time, $t_{D1EArrN}$, of such "short-path" signals for the next cycle must be later than H_1 after the latest possible occurrence of a C1-trailing-edge; that is:

$$t_{D1EArrN} > V + T_{1T} + H_1 \tag{34}$$

(See hand drawn figures at end of manuscript)

Figure 4-5: Premature D1-Changes

The earliest time that a D1-signal can change as a result of signal changes generated during the same clock period getting around the loop is arrived at analogously to the way relation (29) was produced; the same 3 categories of constraints must be considered. Now, however, since we seek the *minimum* delays, we use *minimum* values for the delays within the MAX expressions, and the *earliest* times for the critical clock-pulse edges.

With t_{C2EL} as the earliest occurrence time of a C2-pulse leading edge, and with t_{D2EArr} as

the earliest arrival time of a D2-input change, postulate 1 indicates that the earliest output from an L2-latch can occur at t_{Q2E}, given by:

$$t_{Q2E} = \mathrm{Max}[t_{C2EL} + D_{2CQm}, t_{D2EArr} + D_{2DQm}]$$

Adding D_{Lm} to each component of the MAX of the right side of the above relation, and replacing t_{C2EL} by its value $-T_{2L}$ gives us $t_{D1EArrN}$, the earliest arrival time of a D1-change for the *next* clock cycle:

$$t_{D1EArrN} = \mathrm{MAX}[-T_{2L} + D_{2CQm} + D_{Lm}, t_{D2EArr} + D_{2DQm} + D_{Lm}] \tag{35}$$

To find t_{D2EArr} is the same as finding the earliest output of an L1-latch. If we represent the earliest occurrence time of a C1-pulse leading edge by t_{C1EL}, and the earliest arrival of a D1-input for the current cycle as t_{D1EArr}, then we have:

$$t_{D2EArr} = \mathrm{MAX}[t_{C1EL} + D_{1CQm}, t_{D1EArr} + D_{1DQm}] \tag{36}$$

Replacing t_{C1EL} in the above equation by $V - W_1 - T_{1L}$, and inserting the resulting expression for t_{D2EArr} in (35), yields:

$$t_{D1EArrN} = \mathrm{MAX}[-T_{2L} + D_{2CQm} + D_{Lm}, \mathrm{MAX}[V - W_1 - T_{1L} + D_{1CQm}, t_{D1EArr} + D_{1DQm}] + D_{2DQm} + D_{Lm}]$$

Expanding the inside MAX in the above equation gives us:

$$t_{D1EArrN} = \mathrm{MAX}[-T_{2L} + D_{2CQm} + D_{Lm}, V - W_1 - T_{1L} + D_{1CQm} + D_{2DQm} + D_{Lm}, t_{D1EArr} + D_{1DQm} + D_{2DQm} + D_{Lm}] \tag{37}$$

(The first 2 parts of the MAX are illustrated in parts (b) and (c) respectively of Fig.4-5.)

Now we show that, for a system that operates properly even under worst-case conditions, inequality (34) is valid if, and only if, it is valid when the value used for $t_{D1EArrN}$ is that of (37) with the third part of the MAX deleted. The "if" part of this assertion is obviously true.

To prove necessity (the "only if" part), let us assume the contrary, namely that (34) is valid and that neither of the first 2 parts of the MAX of (37) exceeds the right side of inequality (34).

Then, since $t_{D1EArrN}$ *must* satisfy inequality (34), it follows that the *third* part of the MAX must do so. Therefore it must exceed each of the first 2 parts, both of which can therefore be deleted from relation (37), reducing it to:

$$t_{D1EArrN} = t_{D1EArr} + D_{1DQm} + D_{2DQm} + D_{Lm} \tag{38}$$

But, from relation (31) it is clear that:

$$P > D_{1DQm} + D_{2DQm} + D_{Lm}$$

Adding t_{D1EArr} to both sides gives us:

$$t_{D1EArr} + P > t_{D1EArr} + D_{1DQm} + D_{2DQm} + D_{Lm}$$

From the above and from (38) we have:

$$t_{D1EArrN} < t_{D1EArr} + P$$

But this means that, for each cycle (in the worst case), D1 arrives earlier and earlier relative to the trailing edge of C1. Therefore, even if t_{D1EArr} is comfortably above the minimum for the first cycle, it will eventually violate the hold-time constraint, so that the system would not operate properly. Hence, by contradiction, we have completed our argument.

Thus we can replace $t_{D1EArrN}$ in inequality (34) with the right side of (37), omitting the third part of the MAX (and factoring out D_{Lm}), which gives us:

$$\mathrm{MAX}[-T_{2L} + D_{2CQm},\ V - W_1 - T_{1L} + D_{1CQm} + D_{2DQm}] + D_{Lm}$$
$$> V + T_{1T} + H_1$$

Solving for D_{Lm} produces:

$$D_{Lm} > D_{LmB} = \mathrm{MIN}[V + H_1 + T_{1T} + T_{2L} - D_{2CQm},$$
$$W_1 + H_1 + T_{1L} + T_{1T} - D_{1CQm} - D_{2DQm}]$$

The above expression can be partitioned into 2 relations, at least one of which must be satisfied:

$$D_{Lm} > D_{LmB} = V + H_1 + T_{1T} + T_{2L} - D_{2CQm} \tag{39}$$

$$D_{Lm} > D_{LmB} = W_1 + H_1 + T_{1T} + T_{1L} - D_{1CQm} - D_{2DQm} \tag{40}$$

While it is conceivable that a system might exist for which the right side of (40) is less than the right side of (39), an examination of the 2 expressions suggests that this is very unlikely. Hence, in most cases it is constraint (39) that should be relied upon.

4.4. Premature Changes of D2-Signals

Now consider how to ensure that the D2-signals, once on, remain stable long enough for proper operation, i.e. that the hold-time constraints for the L2-latches are satisfied. It is necessary to ensure that $t_{D2EArrN}$ the time of the earliest change in a D2-signal resulting from a signal passed by the *next* C1-pulse satisfies the following relation, where t_{C2LT} is the latest occurrence time of the trailing edge of C2:

$$t_{D2EArrN} > t_{C2LT} + H_2 \tag{41}$$

The latest appearance of the trailing edge of C2, C_{2LT}, occurs at $W_2 + T_{2T}$. (Refer now to Fig.4-6 (a).) Replacing t_{C2LT} in (41) by this value, we obtain:

$$t_{D2EArrN} > W_2 + T_{2T} + H_2 \tag{42}$$

(See hand drawn figures at end of manuscript)

Figure 4-6: Premature D2-Changes

Noting that the earliest time that any D1-signal is permitted to change as a result of a previous D1-change during the same cycle is $V + H_1 + T_{1T}$ (see relation (34)), and that the leading edge of the next C1-pulse occurs no earlier than $P + V - W_1 - T_{1L}$, we can compute $t_{D2EArrN}$ as below:

$$t_{D2EArrN} = MAX[V + H_1 + T_{1T} + D_{1DQm}, P + V - W_1 - T_{1L} + D_{1CQm}] \tag{43}$$

Combining (42) and (43) yields:

$$MAX[V + H_1 + T_{1T} + D_{1DQm}, P + V - W_1 - T_{1L} + D_{1CQm}]$$
$$> W_2 + H_2 + T_{2T} \tag{44}$$

The left and right parts of the MAX of (44) are illustrated in parts (b) and (c) respectively of Fig.4-6.

Relation (44) can be expressed as the following pair of relations, *at least one of which* must be satisfied:

$$V + H_1 + T_{1T} + D_{1DQm} > W_2 + H_2 + T_{2T}$$

$$P + V - W_1 - T_{2T} + D_{1CQm} > W_2 + H_2 + T_{2T}$$

These may be more conveniently expressed respectively as

$$W_2 < H_1 - H_2 + D_{1DQm} + V + T_{1T} - T_{2T} \tag{45}$$

and

$$W_1 + W_2 < D_{1CQm} + V + P - H_2 - T_{1L} - T_{2T} \tag{46}$$

They constitute necessary and (along with the other constraints developed above) sufficient conditions for ensuring that the inputs to the L2-latches will remain on for a sufficiently long time relative to the trailing edges of the C2-pulses. Under most circumstances, it would appear that (46) is much more likely to be satisfied than is (45)

4.5. Intervals During Which Output Signals are Valid

(Since the material in this subsection is not essential to what follows, it may be skipped at first reading.)

If outputs are taken from the logic block, and are thereafter sent to external receivers instead of to L1-latches, then it is clear that those signals will be stable and valid at least over the interval during which we have ensured that the D1-signals are valid, namely:

$(V - U_1 - T_{1T}, V + H_1 + T_{1T})$.

If the outputs are taken directly from L2-latches, then we can compute the stable output interval as follows.

The *un*stable interval begins at the earliest time at which a Q2-signal can change (i.e. the earliest time an L2-latch output can change). This time, t_{StUn}, can be found in terms of the time of occurrence of the earliest leading edge of a C2-pulse, which is $-T_{2L}$, and t_{D2EArr}, the earliest time at which a D2-input can change:

$$t_{StUn} = MAX[-T_{2L} + D_{2CQm}, t_{D2EArr} + D_{2DQm}]$$

We have already found an expression for t_{D2EArr} in equation (36), which we can insert in the above expression. Let us do so, also replacing the t_{C1EL} term by its value as indicated on page 22, namely $V - W_1 - T_{1L}$. This gives us:

$$t_{StUn} = MAX[-T_{2L} + D_{2CQm},$$
$$MAX[V - W_1 - T_{1L} + D_{1CQm}, t_{D1EArr} + D_{1DQm}] + D_{2DQm}]$$

Expanding the inner MAX yields:

$$t_{StUn} = MAX[-T_{2L} + D_{2CQm},$$
$$V - W_1 - T_{1L} + D_{1CQm} + D_{2DQm},$$
$$t_{D1EArr} + D_{1DQm} + D_{2DQm}] \tag{47}$$

As was shown earlier (page 21 in connection with relation (34)) the earliest change of D1 permitted for the next cycle is at time:

$$H_1 + V + T_{2T} .$$

Therefore, the earliest time we can expect D1 to change for the *current* cycle, i.e. the value of t_{D1EArr} is P less than that amount, or:

$$t_{D1EArr} = -P + H_1 + V + T_{1T}$$

Substituting this value into (47) gives us:

$$t_{StUn} = MAX[-T_{2L} + D_{2CQm},$$
$$V - W_1 - T_{1L} + D_{1CQm} + D_{2DQm},$$
$$-P + H_1 + V + T_{1T} + D_{1DQm} + D_{2DQm}] \tag{48}$$

The Q_2-signals become stable again after the latest D2-change prior to the set-up time propagates to the latch outputs. Using the value for the latest D2-change given in (24) (see page 18), we get for t_{EndUn}, the latest time that the unstable period can end:

$$t_{EndUn} = MAX[W_2 - T_{2T} - U_2 + D_{2DQM}, T_{2L} + D_{2CQM}] \tag{49}$$

At all other times, the Q_2-signals are guaranteed to be stable and valid.

4.6. Consequences of the Constraints

The necessary and sufficient constraints derived above are reproduced below:

$$W_2 \geq V + U_2 - U_1 + D_{1DQM} + T_{2T} - T_{1T} \tag{26}$$

$$W_1 + W_2 \geq V + U_2 + D_{1CQM} + T_{1L} + T_{2T} \tag{27}$$

$$P \geq D_{1DQM} + D_{2DQM} + D_{LM} \tag{31}$$

$$W_1 \geq -P + D_{1CQM} + D_{2DQM} + U_1 + D_{LM} + T_{1L} + T_{1T} \tag{32}$$

$$P \geq -V + D_{2CQM} + U_1 + D_{LM} + T_{1T} + T_{2L} \tag{33}$$

At least one of the following 2 constraints on D_{Lm} must be satisfied. In most cases constraint (39) is less stringent (its right side is smaller) and so determines D_{LmB}, the lower bound on D_{Lm}.

$$D_{Lm} > D_{LmB} = V + H_1 + T_{1T} + T_{2L} - D_{2CQm} \tag{39}$$

$$D_{Lm} > D_{LmB} = W_1 + H_1 + T_{1T} + T_{1L} - D_{1CQm} - D_{2DQm} \tag{40}$$

At least one of the following 2 constraints must be satisfied. In most cases this will be (46).

$$W_2 < H_1 - H_2 + D_{1DQm} + V + T_{1T} - T_{2T} \tag{45}$$

$$W_1 + W_2 < D_{1CQm} + V + P - H_2 - T_{1L} - T_{2T} \tag{46}$$

In addition to the above constraints, 2 more are necessary to ensure that the clock-pulse widths satisfy the minimum requirements of the latches themselves. These are:

$$W_1 \geq C_{W1m} + T_{1L} + T_{1T} \tag{50}$$

and

$$W_2 \geq C_{W2m} + T_{2L} + T_{2T} \tag{51}$$

Our objective is to choose the clock parameters (widths, period and overlap) so as to maximize the speed of the system (clearly this is achieved when the period, P, is minimized), while making it as insensitive as possible to parameter variations. That is, we would like to make the tolerances as large as possible. We often start out with a desired value for the maximum logic delay, D_{LM}, in a logic path (the *long-path delay*) as this is largely

determined by the given technology and the desired maximum number of stages of logic. The crucial factor determining feasibility with known tolerances for delay per logic stage is then the *minimum* delay in a logic path, D_{Lm}, or *short-path delay*. If the required lower bound on the short-path delay is too large compared to the long-path delay, then the system may be difficult or impossible to realize reliably.

We therefore define the problem as that of finding the minimum value of P such that the lower bound on the short-path delay (D_{LmB}) is acceptable (not too large). It is assumed that we are given all of the latch parameters, the clock-pulse edge tolerances, and the long-path delay, D_{LM}.

The key constraint on D_{Lm} is almost always (39). Hence we set D_{LmB} equal to the right side of that constraint and solve for V:

$$V = D_{LmB} - H_1 - T_{1T} - T_{2L} + D_{2CQm} \tag{52}$$

Now substitute the above right side for V in relation (33), which is the key constraint on P, to obtain an expression for the minimum value of P as a function of the short-path delay:

$$P = H_1 + U_1 + D_{2CQM} - D_{2CQm} + D_{LM} - D_{LmB} + 2(T_{1T} + T_{2L}) \tag{53}$$

This expression is valid provided that the value of P obtained does not violate constraint (31). Thus to find the maximum value of D_{LmB} beyond which no further reductions in P are possible, we must first find the maximum value of V for which (33) is valid (i.e. the value for which (31) is not violated). We do this by substituting the right side of (31) for P in (33) and, treating the resulting expression as an equality, solving for V:

$$V = T_{1T} + T_{2L} + D_{2CQM} + U_1 - D_{1DQM} - D_{2DQM} \tag{54}$$

There is clearly nothing to be gained by making the overlap any larger than the value given in expression (54), since the effect would be to increase the lower bound on the short-path delay without reducing P beyond the absolute minimum given by (31).

Now we can compute the maximum useful value of D_{LmB} by substituting into (39) the above value of V:

$$D_{LmB} = 2(T_{1T} + T_{2L}) + H_1 + U_1 - D_{1DQM} - D_{2DQM} + D_{2CQM} - D_{2CQm} \tag{55}$$

Now we are in position to discuss the question mentioned at the beginning of this section as to the consequences of forcing the D1- and/or the D2-signals to appear earlier than the minimum bounds dictated by the set-up times for the latches. The effect of doing this is the same as if the values of the set-up times (the U_i's) were increased. Let us examine the

relations derived here to see what effects such increases would have.

First observe that U_1 appears in constraints (26), (32), and (33), as well as in expression (54) for the maximum useful overlap, in expression (55) for the value of D_{LmB} corresponding to the absolute minimum bound on P, and in expression (53) for the minimum value of P as a function of the lower bound on the short-path delay. The direct effects of increasing U_1 are detrimental in all cases except that corresponding to (26). That is, the period would have to be increased and/or D_{LmB} would have to be increased (various trade-offs are possible), both of which are bad, but the lower bound on the width of the C2-pulse would be relaxed, a benefit, but seldom one that is needed.

The U_2-term appears only in constraints (26) and (27), and in expression (49) for the end of the unstable period for the outputs of L2. In the first 2 cases it tightens (by increasing) the lower bounds on the pulse widths, which is mildly bad, and in the last case it increases the interval during which the Q2-signals are stable, which might conceivably be advantageous in some situation.

It therefore does not seem useful to consider requiring the D-inputs to the latches to arrive earlier than necessary, unless a very special circumstance should make important one of the factors discussed above. An interesting, and perhaps useful, added conclusion from the above discussion is that the set-up time for the L2-latches is of less importance with respect to speed and tolerances than is the set-up time for the L1-latches.

4.7. Computing Optimum Clock Parameters

Let D_{MaxLmB} be the largest lower bound that we can enforce on the short-path delays. To compute optimum clock parameters, proceed as follows:

```
IF D_MaxLmB ≥ right side of (55)
THEN
  D_LmB ⇐ right side of (55)
  P ⇐ right side of (31)
  V ⇐ right side of (54)
ELSE
  D_LmB ⇐ D_MaxLmB
  P ⇐ right side of (53)
  Compute V from relation (39)
W_2 ⇐ MAX[right side of (26), right side of (51)]
Compute W_1 from relation (27) (use equality)
Increase W_1 if necessary to satisfy constraint (50)
IF W_1 + W_2 > right side of (46) (Not likely.)
THEN
  IF W_2 violates (45) (It probably will.)
  THEN increase P to satisfy constraint (46)
IF D_LmB > right side of (40) (Not likely.)
THEN decrease D_LmB until (40) is satisfied with equality
```

The procedure given above is intended as a general guide to the use of the constraints developed here. In particular cases alternative procedures may be more appropriate.

5. Conclusions

As is evident from the length of the corresponding section, the task of determining optimum clocking parameters for systems using ETDFF's is relatively simple. The clock-pulse width is not critical, and the constraint on the short-path delays is seldom stringent. The price paid for this is that the minimum clock period is the sum, not only of the maximum delays through the logic and the FF's, but also of the set-up time and twice the edge tolerance. No trade-offs are possible to reduce this quantity.

For 1-phase systems using latches, it may be possible to make the period as small as the sum of the maximum delays through a latch (from the D-input) and the logic. In order to do this, the clock-pulse width must be made sufficiently wide (usually past the point where the leading edge of the clock-pulse precedes the appearance of the D-signals). Wider clock pulses imply increased values of D_{LmB}, the lower bound on the short-path delays. If this bound is not to become unreasonably high, it is necessary to keep the edge tolerances small. It is also helpful if the difference between the maximum and minimum values of the propagation delays from the C-inputs of the latches are small.

The 2-phase system with latches is inherently more complex in that more variables are involved. As in the previous case, trade-offs are possible between P and D_{LmB}. Here the intermediate variable is V, the amount of overlap between the C1- and C2-pulses. In very conservative designs there is a negative overlap and D_{LmB} is zero. If positive overlaps are permitted, P can be decreased, but at the cost of making D_{LmB} non-zero. A continuum of trade-offs exists to the point where P is reduced to the sum of the maximum propagation delays through the L1- and L2-latches (from the D-inputs) and the logic. Again it is possible to absorb the effect of edge tolerances in terms of short-path rather than long-path problems.

An important advantage of 2-phase over 1-phase systems is that, for every 2-phase system, simply by varying the overlap (i.e. the phasing between the C1- and C2-clock pulses), D_{LmB} can be varied continuously from zero to the highest useful value (with the minimum P of course changing in the opposite direction). On the other hand, for 1-phase systems, the range of variation of D_{LmB} possible by varying the clock-pulse width is often much smaller, particularly at the low end. As illustrated in the graph of Fig.3-4, there may be a significant range of values of D_{LmB} that is attainable only by adding delay pads at the outputs of all latches.

In 1-phase systems, if the designer is overly aggressive and it becomes apparent during the test phase that the short-path bound cannot be met, then it is usually necessary to add delay pads at the latch outputs as well as to increase the clock period. This usually means very extensive changes, affecting many chips. Should the same situation arise in connection with a 2-phase system, in addition to increasing the clock period, all that need be done is to reduce the amount of overlap, adjustments that affect only the clocking system, usually a much simpler process affecting far fewer chips. Hence designers of 2-phase systems can

afford to be bolder in choosing the clock period since the penalty for over-reaching is less severe.

With only one latch in each feedback path, the lower limit on the clock period is lower for 1-phase systems, although this factor is somewhat attenuated by the fact that some latches in 1-phase systems will have both inputs from sources that fan out to other latches, and outputs that fan-out to many gate-inputs. Both of these are factors that reduce speed. But in 2-phase systems each L1-latch feeds only one other device (an L2-latch), and each L2-latch receives its D-input from a source (an L1-latch) feeding no other device. Hence, all other things being equal, we would expect the delays through the 2 latches in the feedback paths of 2-phase systems to have less than twice the delays of the one latch in the feedback path of a 1-phase system.

An advantage of 2-phase systems over both of the other types considered here is that they are somewhat more compatible with the LSSD concept for system testing [1, 2].

It appears that all three types of systems have their places. Where there is a willingness to exert great efforts to suppress skew (e.g. by hand-tuning the delays in clock distribution paths), and to control other related factors very precisely, the 1-phase system may be the best choice, as in the case of the CRAY I machine. In other cases of high performance machines, 2-phase clocking may be more suitable. Use of ETDFF's seems to have advantages for less aggressive designs.

The results presented here in such precise looking relations obviously depend heavily on the precision with which the parameters of those relations can be determined. Realistic figures must be obtained that take into account such matters as power supply and temperature variations, as well as data sensitive loading considerations.

The relations developed here may be useful in determining what latches to use in certain situations and to determine how to modify latch designs so as to improve system performance. For example, an examination of the constraints developed in Section 3.3 (see page 13) for 1-phase systems with latches suggests that the *minimum* value of D_{DQ} is of no importance, whereas the minimum value of D_{CQ} *is* important in that the larger it is, the less stringent is the constraint on short-path delays.

In the 2-phase case, minimizing (D_{2CQM} - D_{2CQm}) is clearly helpful. It relaxes the requirement on D_{LmB} imposed by equation (55), which, if it can be satisfied, allows P to be set to the minimum value given by (31). If (55) cannot be satisfied, then P is given by equation (53), and will therefore vary directly with (D_{2CQM} - D_{2CQm}).

On the other hand, neither D_{1CQM}, D_{1CQm}, D_{1DQm}, nor D_{2DQm} seem to be of primary importance. As was pointed out on page 29, the set-up and hold-time requirements for the L1-latches are much more important than are the corresponding parameters for the L2-latches. It is clear that there are different optimum requirements for L1- and L2-latches. Furthermore different choices may be appropriate depending upon whether or not an effort is being made to attain the minimum period corresponding to the maximum loop delay.

It is clear from the results developed here that minimizing clock edge tolerances is of considerable importance in high performance digital systems. In 2-phase systems, a special effort is warranted to minimize T_{1T} and T_{2L}, which appear in key several constraints. Unfortunately, technology trends are such as to emphasize factors that cause skew. For example, as the dimensions of logic elements on chips shrink, the ratio of wiring delays to gate delays grows. A high priority must therefore be given in wiring algorithms to the clock distribution system. Off-chip wiring forming part of the clock distribution network must be carefully controlled. In some cases the insertion of adjustable delays in these paths may be warranted. It is quite likely that the continuation of the trends that exacerbate the skew problem will soon make it worthwhile to consider systems that do not use clock pulses or that use clock pulses only locally. Discussions of such asynchronous, self-timed, or speed-independent systems are in [4, 8].

Logic designers and those developing computer aids for logic design customarily pay a great deal of attention to minimizing long-path delays. It is also important to consider techniques for increasing short-path delays. In line with this there is a need for circuit designers to develop techniques for introducing *precisely controlled* delay elements where needed. At present, in many technologies, logic designers are forced to cascade inverters to produce delays. This is wasteful in terms of both chip area and power. In general, the idea that greater speed may result from better delay elements should be conveyed to those developing digital technology.

Further developments along the lines developed here would include the use of statistical rather than worst-case analyses, which would allow us to choose clocking parameters such that the likelihood of a timing failure is very small, but not zero. This usually implies shorter clocking periods. In using this approach it is important to be able to take into account correlations among delay values, skew etc. in various parts of the system [5, 7]

It is also possible to speed up systems by exploiting detailed knowledge of the logic paths. There may be, for example, constraints on the sequencing of signals through certain combinations of paths that allow us to consider consecutive pairs, triples, etc. of cycles together and thereby realize that shorter periods are feasible than would be the case if each period were considered separately. Research along this line is being conducted by Klim Maling [3].

An earlier presentation of the work discussed here, in a different form with different notation was issued by the authors several years ago [10, 11]. The idea that clocked systems could be speeded up by permitting the D-inputs to latches to lag behind the leading edges of the clock-pulses and by allowing the C1- and C2-clock pulses to overlap is not new. These ideas are included in the very interesting book on digital systems design by Langdon [2], and have been pointed out by David Chang of IBM's Poughkeepsie Laboratories a number of years ago in at least one internal memorandum.

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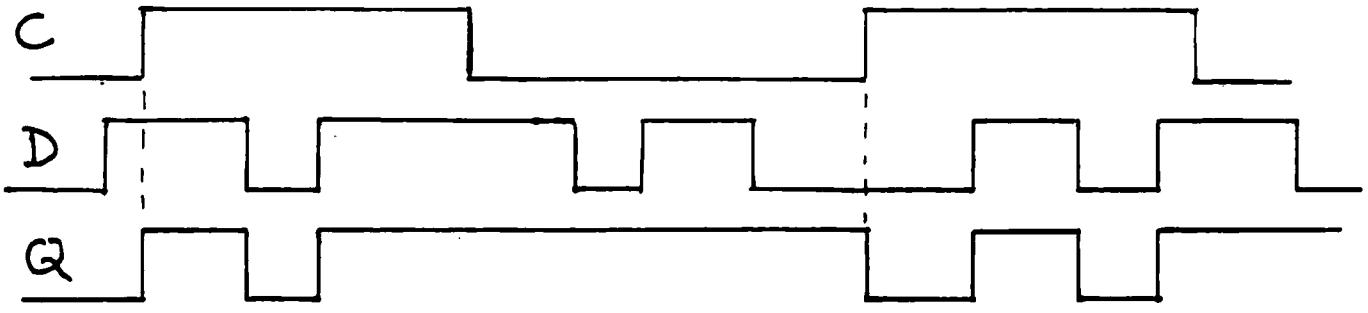


FIG. 1-1 BEHAVIOR OF AN IDEAL LATCH

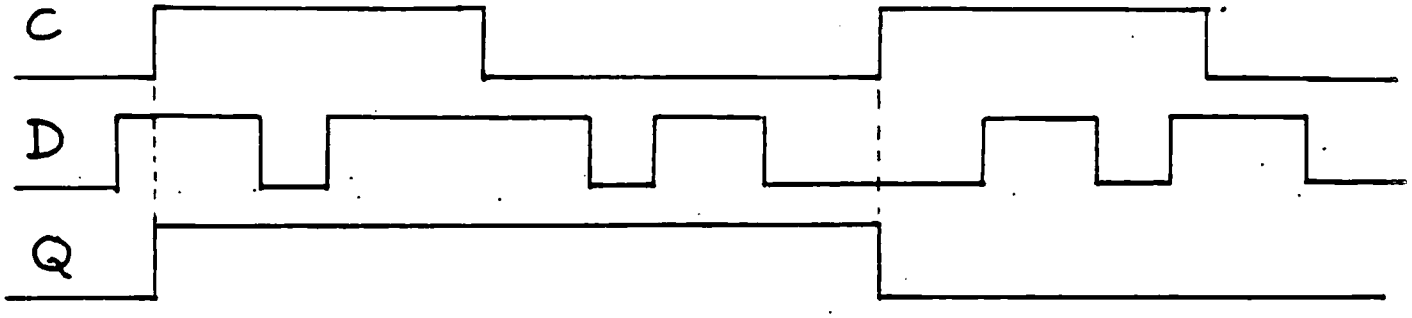


FIG. 1-2 BEHAVIOR OF AN IDEAL POSITIVE TRIGGERED ETDFF

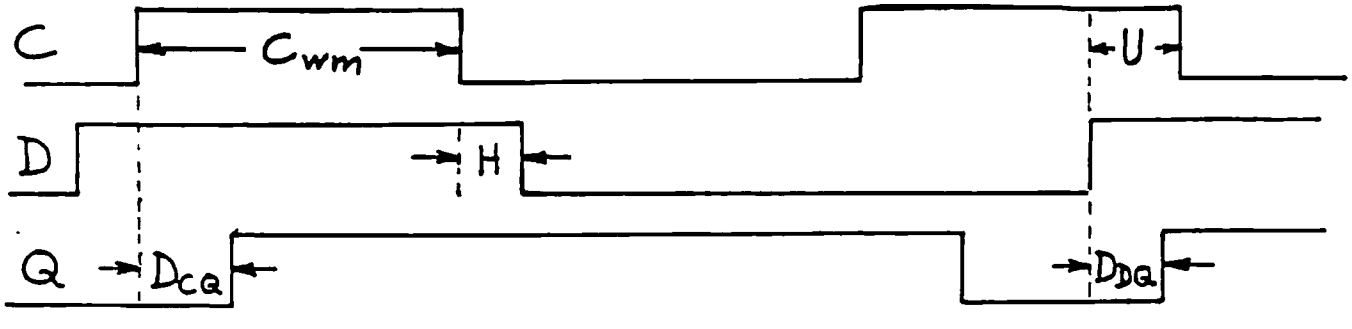


FIG. 1-3 LATCH PARAMETERS

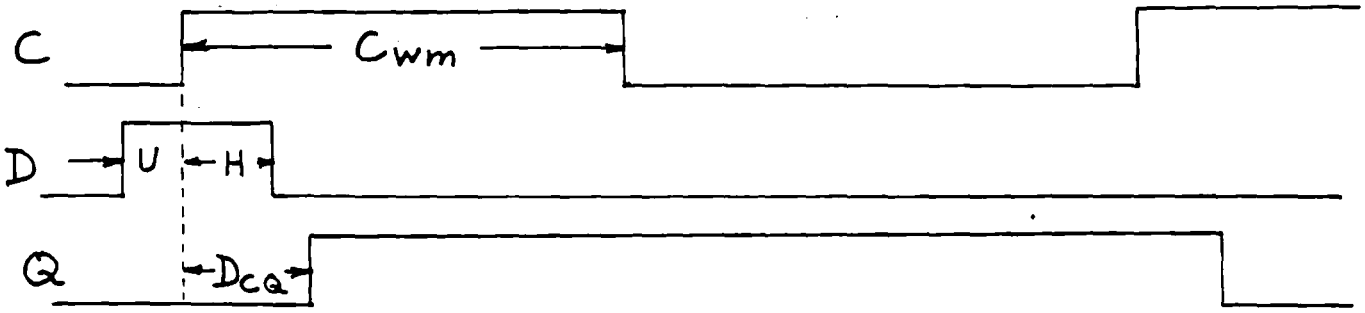


FIG. 1-4 PARAMETERS OF A POSITIVE TRIGGERED ETDFF

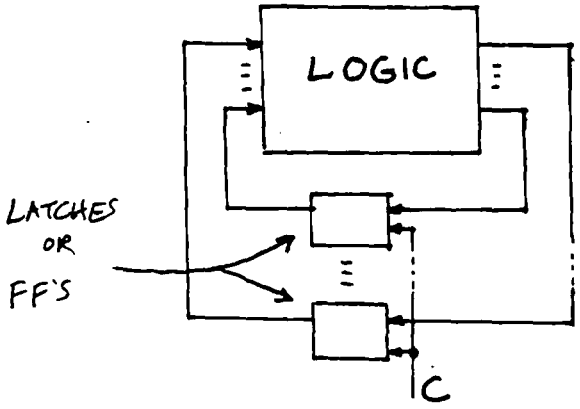
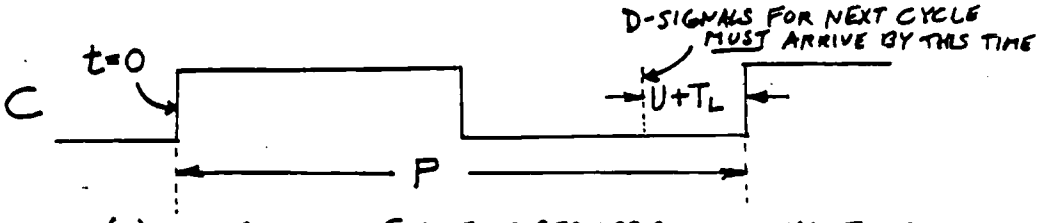
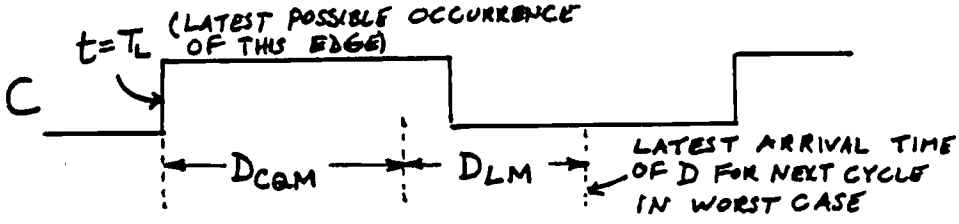


FIG. 2-1 BLOCK DIAGRAM OF A 1-PHASE SYSTEM

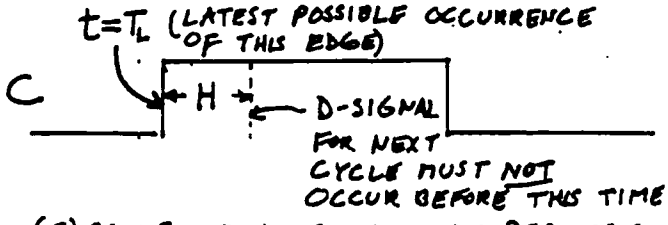


(a) SPECIFICATION OF LATEST PERMISSIBLE ARRIVAL TIME OF D-SIGNAL FOR NEXT CYCLE

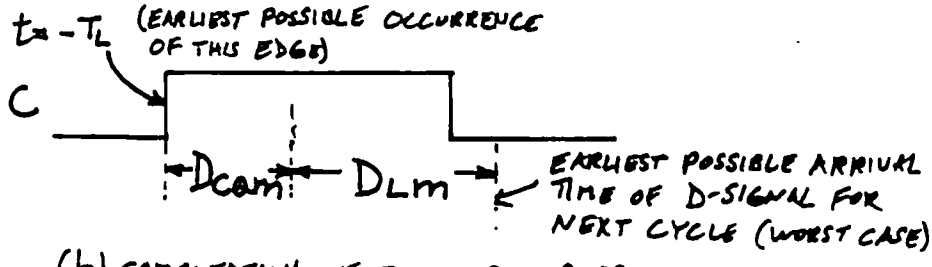


(b) ARRIVAL TIME (WORST-CASE) FOR D-SIGNAL FOR NEXT CYCLE

FIG. 2-2 ENSURING THAT D-SIGNALS DON'T ARRIVE TOO LATE IN ETFF SYSTEMS



(a) SPECIFICATION OF EARLIEST PERMISSIBLE ARRIVAL TIME OF D-SIGNAL FOR NEXT CYCLE



(b) COMPUTATION OF EARLIEST POSSIBLE ARRIVAL TIME OF D-SIGNAL FOR NEXT CYCLE

FIG. 2-3 ENSURING THAT D-SIGNALS IN ETDFF SYSTEMS DON'T ARRIVE TOO EARLY

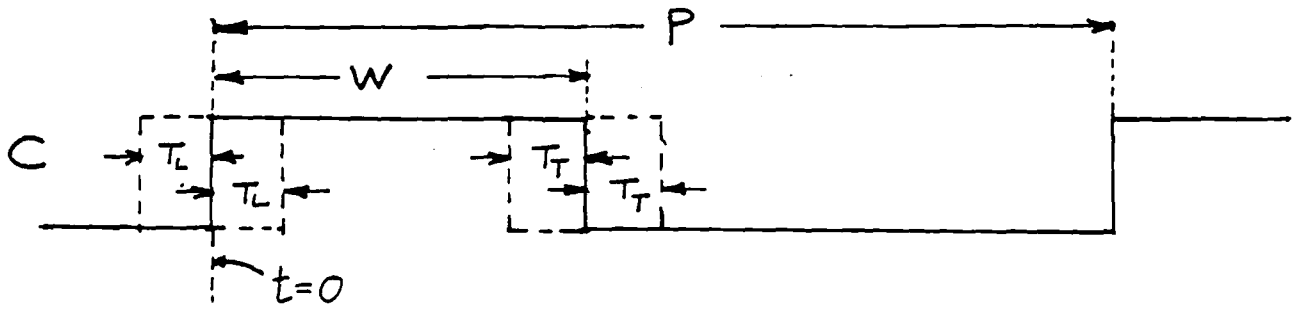
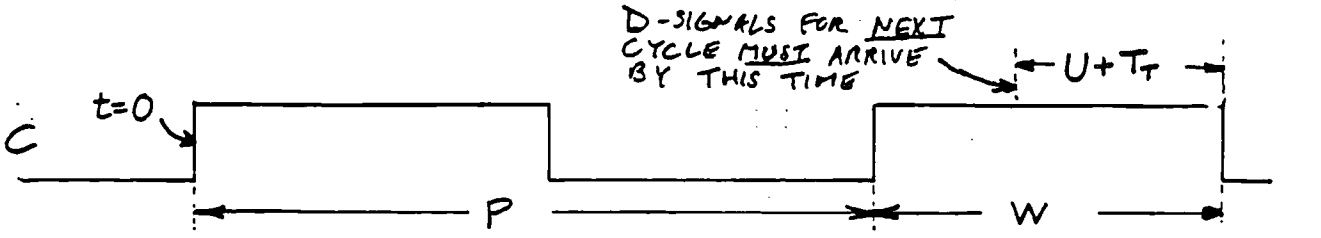
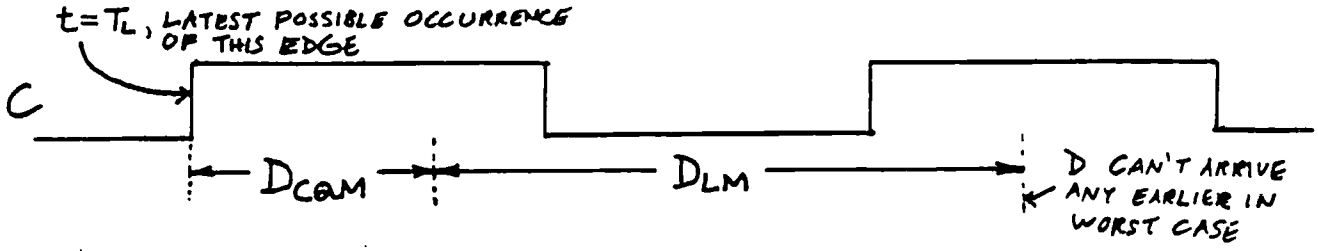


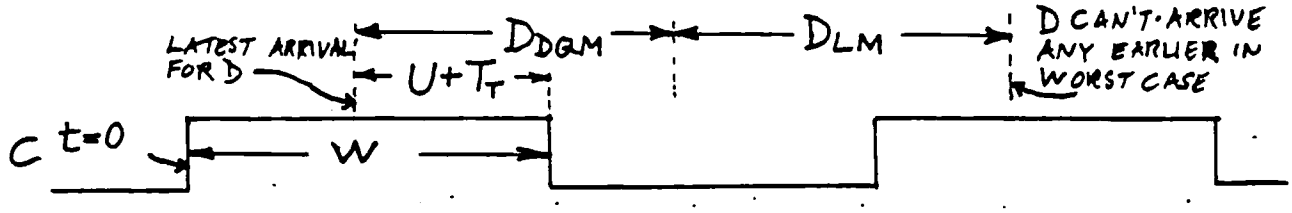
FIG. 3-1 PARAMETERS FOR 1-PHASE SYSTEM



(a) DEADLINE FOR ARRIVAL OF D-SIGNALS

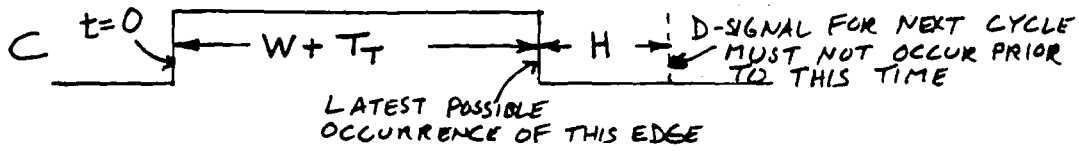


(b) BOUND ON D-ARRIVAL DUE TO LEADING EDGE OF C

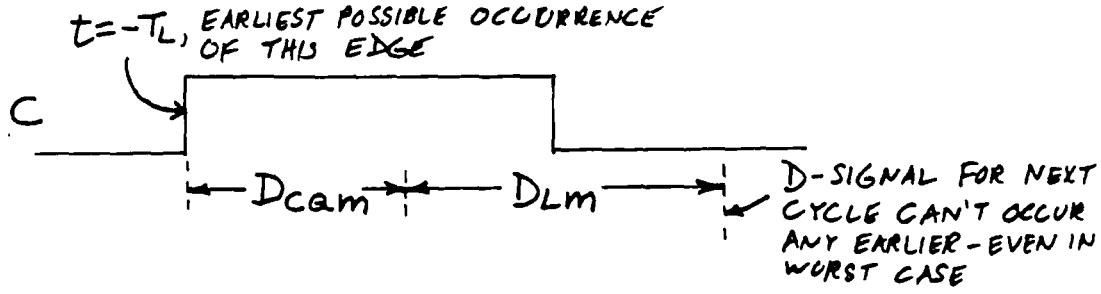


(c) BOUND ON NEXT-CYCLE D-ARRIVAL DUE TO ARRIVAL TIME OF D FOR CURRENT CYCLE

FIG. 32 ENSURING THAT D ARRIVES SUFFICIENTLY EARLY.



(a) EARLIEST PERMISSIBLE ARRIVAL TIME OF D



(b) LOWER BOUND ON D-ARRIVAL FOR NEXT CYCLE DUE TO LEADING EDGE OF C

FIG. 3-3 ENSURING THAT D DOESN'T ARRIVE TOO EARLY

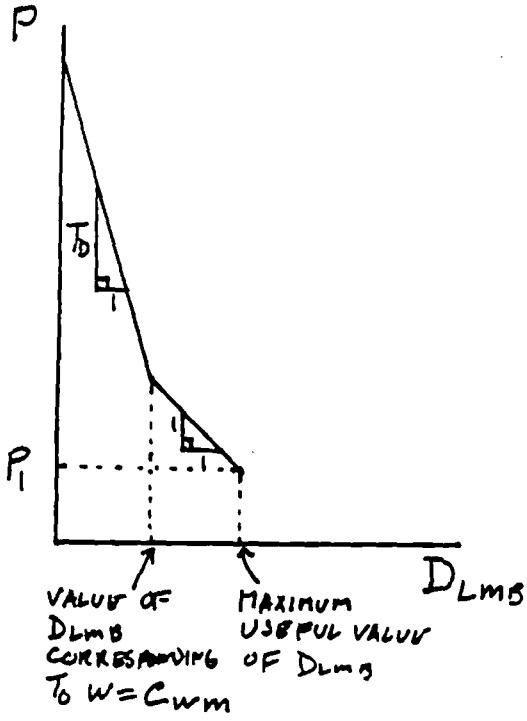


FIG. 3-4

P AS A FUNCTION OF THE LARGEST ACHIEVABLE LOWER BOUND ON THE SHORT-PATH DELAY

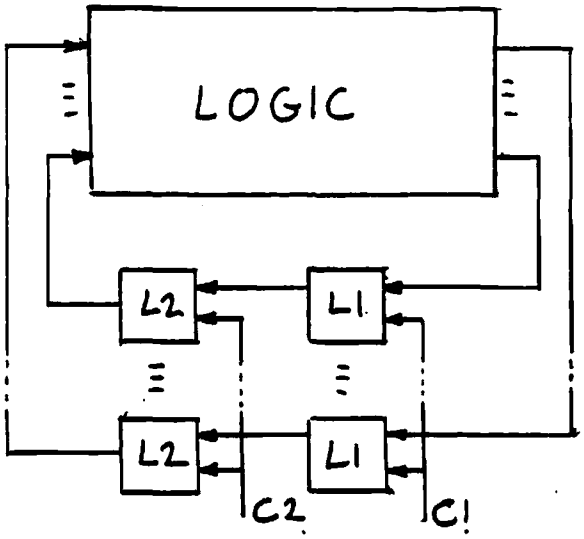


FIG. 4-1 BLOCK DIAGRAM OF A 2-PHASE SYSTEM

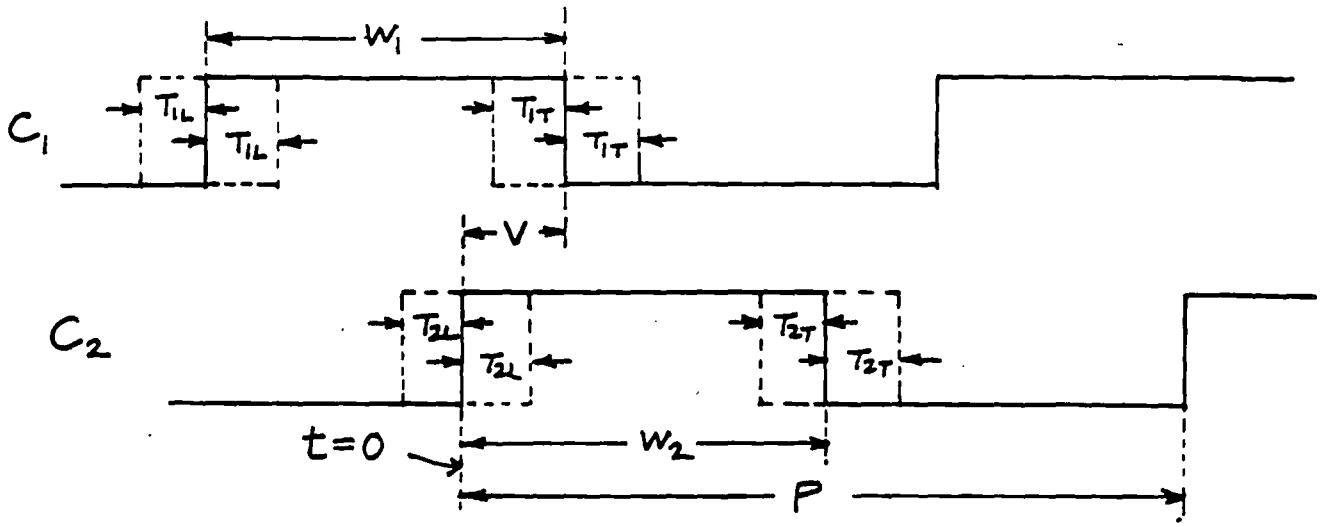
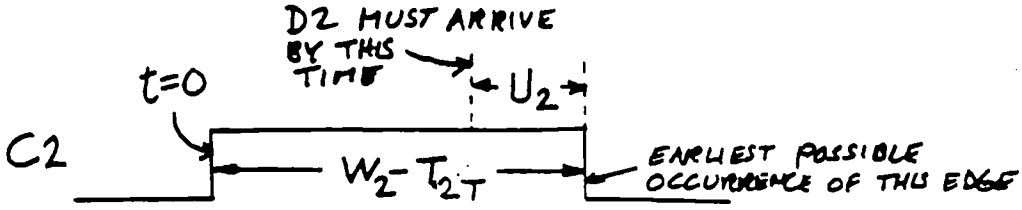
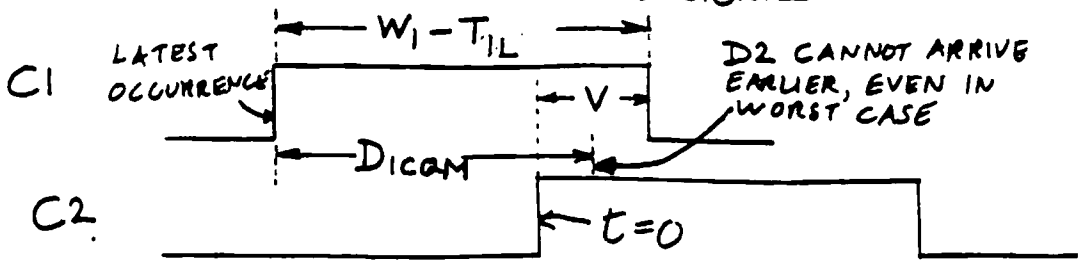


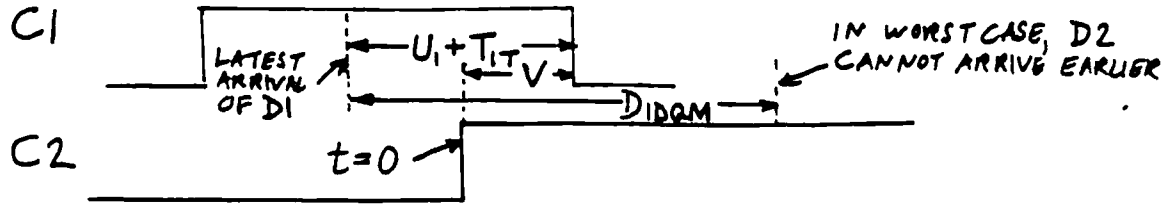
FIG. 4-2 PARAMETERS FOR 2-PHASE SYSTEM



(a) DEADLINE FOR ARRIVAL OF D2-SIGNALS

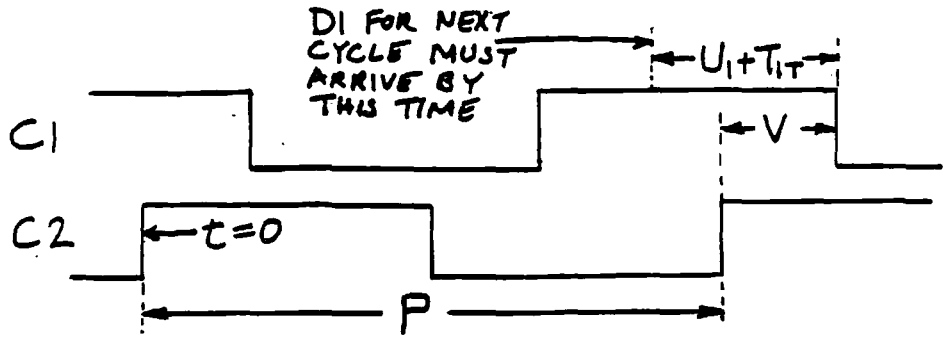


(b) LOWER BOUND ON D2-ARRIVAL DUE TO C1 LEADING EDGE

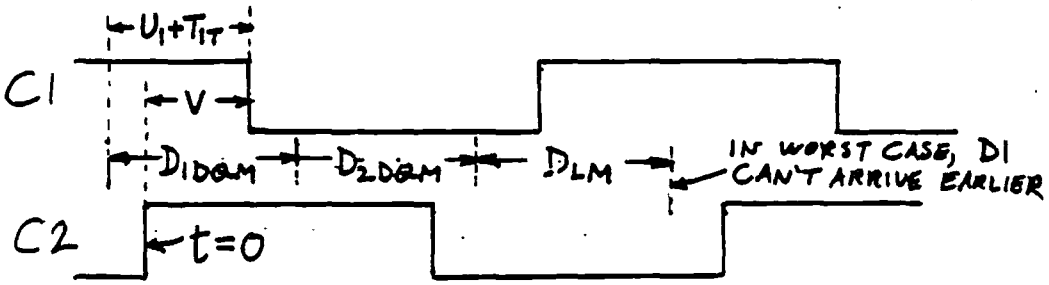


(c) LOWER BOUND ON D2-ARRIVAL DUE TO ARRIVAL OF D1-SIGNAL

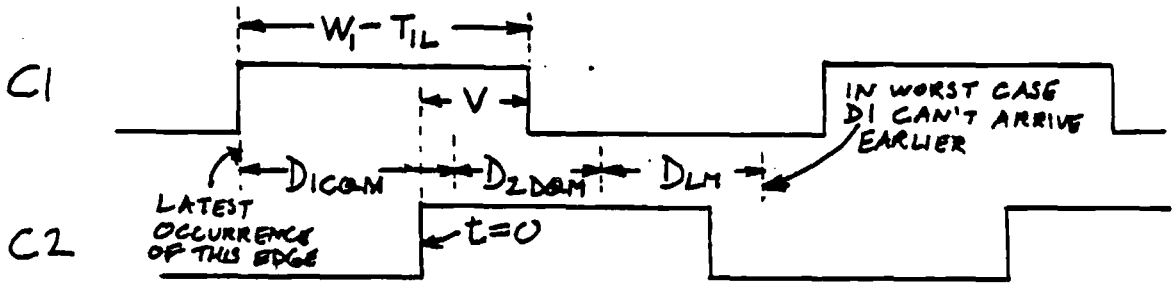
FIG. 4-3 D2 ARRIVAL TIME



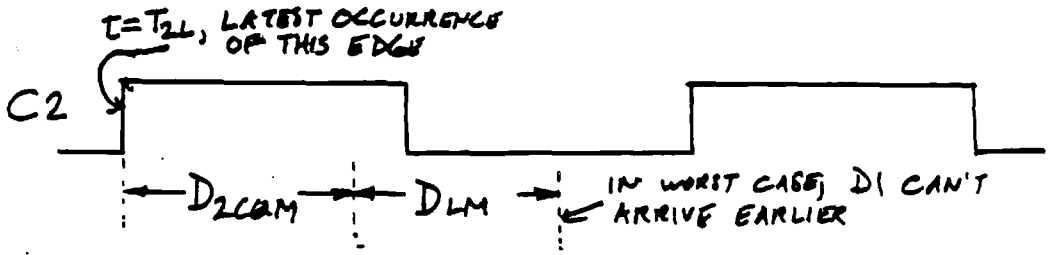
(a) DEADLINE FOR DI-ARRIVAL DURING NEXT CYCLE



(b) LOWER BOUND ON NEXT-CYCLE DI-ARRIVAL DUE TO PROPAGATION DELAYS THROUGH D-INPUTS OF LATCHES

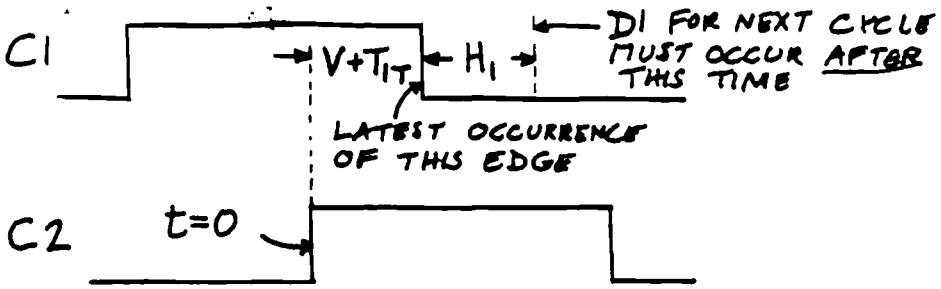


(c) LOWER BOUND ON NEXT CYCLE DI-ARRIVAL DUE TO C1 LEADING EDGE

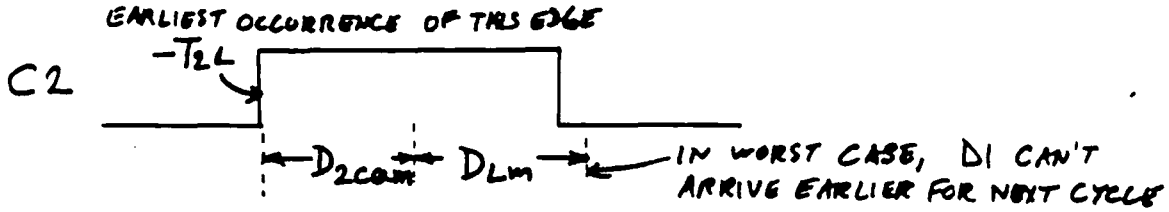


(d) LOWER BOUND ON DI-ARRIVAL FOR NEXT CYCLE DUE TO C2 LEADING EDGE

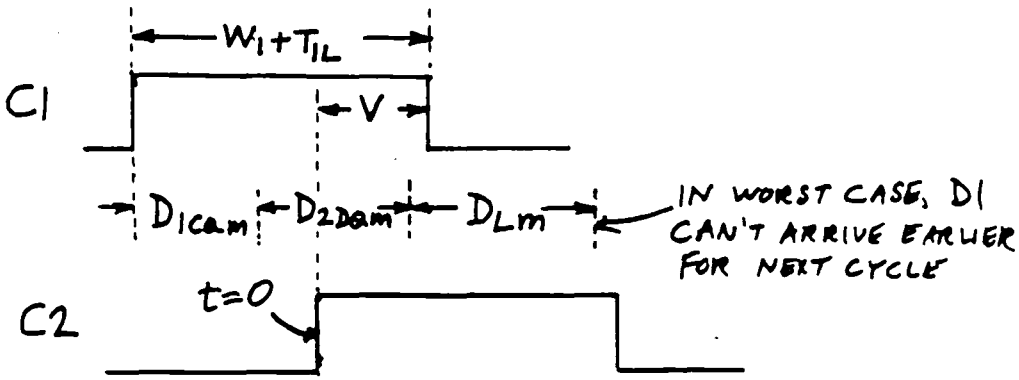
FIG. 4-4 DI ARRIVAL TIME



(a) LOWER BOUND FOR OCCURRENCE TIME OF DI FOR NEXT CYCLE

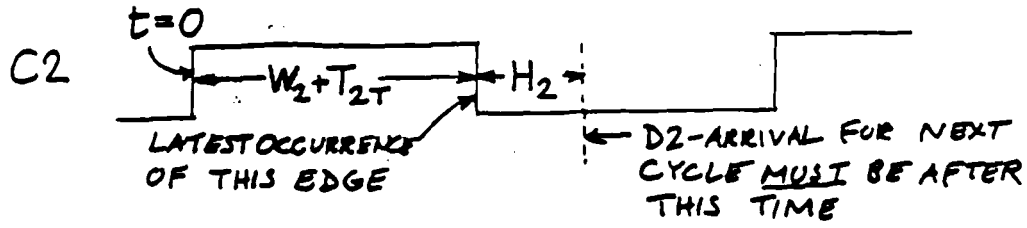


(b) LOWER BOUND ON NEXT CYCLE DI-ARRIVAL DUE TO LEADING EDGE OF C2.

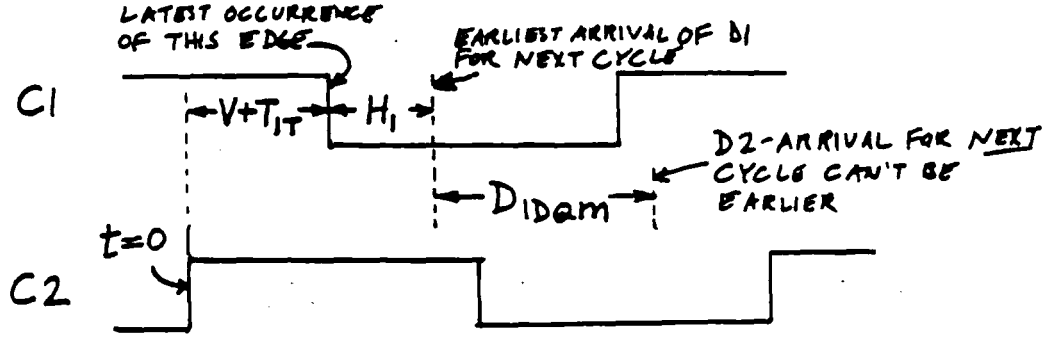


(c) LOWER BOUND ON DI-ARRIVAL FOR NEXT CYCLE DUE TO LEADING EDGE OF C1

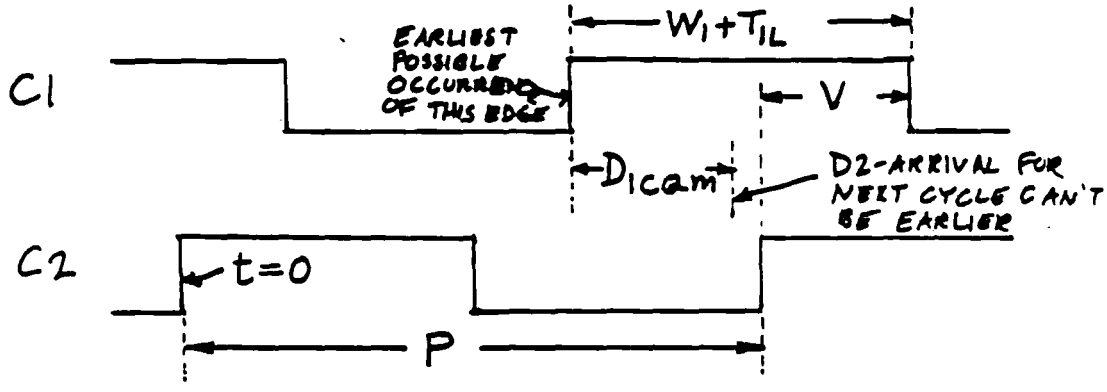
FIG. 4-5 PREMATURE DI-CHANGES



(a) EARLIEST PERMISSIBLE ARRIVAL TIME OF D2



(b) LOWER BOUND ON D2-ARRIVAL TIME FOR NEXT CYCLE DUE TO D1-ARRIVAL TIME



(c) LOWER BOUND ON D2-ARRIVAL FOR NEXT CYCLE DUE TO THE LEADING EDGE OF C1 FOR THE NEXT CYCLE

FIG. 4-6 PREMATURE D2-CHANGE

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