Invited paper

Closed-form 2D modeling of sub-100 nm MOSFETs in the subthreshold regime

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Abstract — Closed-form 2D modeling of deep-submicron and sub-100 nm MOSFETs is explored using a conformal mapping technique where the 2D Poisson equation in the depletion regions is separated into a 1D long-channel case and a 2D Laplace equation. The 1D solution defines the boundary potential values for the Laplacian, which in turn provides a 2D correction of the channel potential. The model has been tested for classical MOSFETs with gate lengths in the range 200–250 nm, and for a super-steep retrograde MOSFET with a gate length of 70 nm. With a minimal parameter set, the present modeling reproduces both qualitatively and quantitatively the experimental data obtained for such devices.

Keywords — sub-100 nm MOSFET, two-dimensional device modeling, conformal mapping, threshold voltage, subthreshold regime, leakage current.

1. Introduction

Very important issues in the development of modern semiconductor device technology are the increasing levels of complexity in the fabrication process and the many subtle mechanisms that govern the properties of advanced devices. These mechanisms, which are explained by a careful consideration of the device physics, have to be formulated and implemented into process modeling and circuit design tools, to empower the circuit designers with means to fully utilize the potentials of modern technology.

However, it is recognized that the development of commercial circuit design tools lags significantly behind the pace of progress in device processing. This time lag creates a costly delay in the adoption of new technology in circuit designs, especially for the many companies that depend on chip foundries for the fabrication of their proprietary circuits. They consistently have to contend with designs based on relatively conservative design rules. Hence, a strong impetus exists for focusing on advanced device modeling for circuit simulators and other computer aided design (CAD) tools.

For silicon CMOS technology, the present industry modeling standards for circuit simulation, such as BSIM3 [1, 2], BSIM4 [3, 4], EKV [5], MOS Model 9 [6], and MOSA1 [7, 8], are based on one-dimensional (1D) theory, initially developed for long-channel FETs. However, the steady reduction in feature size, with gate lengths presently well into the sub-100 nm regime [9], has strongly enhanced a number of phenomena, collectively known as short-channel effects, related to the two- and even the three-dimensionality of the device structures. To keep pace with technology, this has necessitated extensive, phenomenological modifications of the 1D models, resulting in a steady erosion of their physical basis and a plethora of model parameters, many of which are of an obscure origin.

Therefore, as a prerequisite to obtaining very precise descriptions of the next generations of MOSFETs, the consideration of 2D models based on a self-consistent solution of the 2D field-pattern in the device [10–15] has become necessary. In such an approach, short-channel effects and scaling properties will be intrinsic to the model, which, accordingly, may require a minimum set of parameters of clear physical origin. Hence, a close accord is established with the fabrication process. For the same reason, such models will represent a significant and needed improvement for use in CAD tools aimed at the next generation of circuit design. In particular, the 2D strategy is expected to yields precise scaling information on important properties, such as threshold voltage and the subthreshold leakage current. Above threshold properties will have to be solved self-consistently using appropriate transport formalisms for the channel current.

Here, we consider closed-form 2D solutions of the subthreshold properties of deep submicron and of sub-100 nm MOSFETs. Following the procedure by Klös and Kostka [15], the 2D Poisson equation for the depletion regions is separated into a 1D long-channel problem and a Laplacian with well-defined boundary conditions for the 2D region under the gate. The latter is solved using conformal mapping techniques [16]. In this work, the definition of the 2D boundary conditions and the mapping functions used in the Laplace problem have been improved compared to those of [15], and the technique has been extended to sub-100 nm range MOSFETs.

This method applies to classical MOSFETs as well as to non-classical structures [17]. We note that the classical MOSFET approach is directly applicable to super-steep-retrograde (SSR) channel doped devices, to Si-Si/Ge strained devices, and to sidewall vertical MOSFETs with a partially depleted body. Likewise, the same approach, with somewhat different boundary conditions for the Laplacian, may be applicable to double-gate fully depleted vertical MOSFETs and double-gate SOI MOSFETs.

The device geometry for the classical MOSFET and the corresponding boundary conditions of the Laplacian are discussed first. Next, the conformal mapping technique is

presented. This approach is then applied to classical MOSFETs with gate lengths between 200 and 250 nm, where results for the channel potential profile, the scaling of the threshold voltage with the gate length, the drain induced barrier lowering (DIBL) effect, and the subthreshold leakage current are presented and compared to experiments. Finally, corresponding results for sub-100 nm SSR MOSFET are presented.

2. Modeling approach

Consider the schematic classical MOSFET geometry of Fig. 1, which shows the actual source and drain contact regions and the depletion region outlined by dashed lines. Starting from the work by Klös and Kostka [15], the contact regions in the present analysis are approximated by rectangular boxes, and the potential distributions of the source and drain depletion regions (Regions 2 and 3) are calculated by means of a 1D Poisson equation.

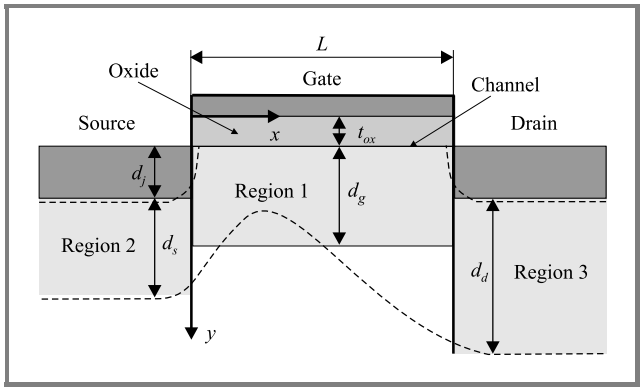

Fig. 1. Schematic MOSFET geometry. The lower dashed line indicates the depletion boundary resulting from a 2D analysis.

A 2D analysis may be performed in the central region under the gate, where the superposition principle allows us to partition the actual 2D potential distribution into that corresponding to a 1D Poisson equation and that of a Laplacian. We note that the only adjustable parameter in this procedure is the effective thickness used for the source and drain contacts (to compensate for the rounded shape of the actual contacts near the gate). The threshold and subthreshold properties of this device are largely determined by the channel potential profile $\Phi_o(x) = \phi_o = \varphi_o(x)$, where ϕ_o is the channel potential according to the 1D long-channel case and $\varphi_o(x)$ is the contribution from the 2D Laplacian in Region 1. All the potentials are measured relative to that of the substrate interior.

The 2D contribution to the channel potential profile can be determined by either considering Region 1 as consisting of only the semiconductor slab under the oxide or by including the gate oxide as well [15]. In the first case, the channel is a boundary for the Laplacian. In the second case, the oxide-metal interface is the boundary. It is therefore necessary to scale the actual oxide thickness t_{ox} to $t'_{ox} = t_{ox}\varepsilon_s/\varepsilon_i$, where ε_s and ε_i are the semiconductor and the oxide permittivities, respectively. Also the "oxide" part must remain neutral and non-conducting. Since the second approach provides a better definition of the boundary condition for the Laplacian, it will be used in the present analysis.

From the channel potential profile $\Phi_o(x)$ resulting from our analysis, we can determine the threshold voltage V_T and the subthreshold current I_{sub}. V_T corresponds to the gate-source voltage V_{GS} for which the minimum value in the channel potential satisfies the threshold condition, $\Phi_{o,\min} = 2\varphi_b$. Here $\varphi_b = V_{th}\ln(N_s/n_i)$, where V_{th} is the thermal voltage, N_s is the substrate doping, and n_i is the intrinsic carrier density in silicon. I_{sub} for a given V_{GS} is determined by the channel potential profile and, in particular, by the value of $\Phi_{o,\min}$.

In practice, the channel potential $\Phi_o(x)$ has to be determined from the normal electrical field $E_n(x)$ pointing into Region 1 from the channel. As will be shown below, $E_n(x)$ consists of the field contribution E_o from the 1D analysis and the contribution $E_{2D}(x)$ from the 2D analysis. The latter is found by performing an integration over all the boundaries of Region 1.

Here we assume for simplicity that the substrate is uniformly doped. Non-uniform doping profiles in the vertical direction may be approximated by two or more horizontal layers of different but uniform doping (see below). The same would apply for strained Si-Si/Ge MOSFETs.

2.1. 1D boundary conditions

The boundary conditions for the 2D Laplace problem in Region 1 (including the oxide) are defined in terms of the potential distributions along at the oxide-metal interface ($y = 0$) and at the vertical boundaries at $x = 0$ and $x = L$. At the vertical boundaries, the potential distributions are derived from the 1D Poisson equations in Regions 1–3, the potentials of the source and drain contacts, and the potential at the vertical sidewalls of the oxide.

1D potential distribution in Region 1. In the 1D approximation, the potential distribution $\phi_g(y)$ relative to the substrate interior in Region 1 becomes:

$$\phi_g(y) = \begin{cases} \varphi_g + (\phi_o - \varphi_g)\dfrac{y}{t'_{ox}}, & 0 \le y < t'_{ox} \\ \phi_o + \dfrac{qN_s}{2\varepsilon_s}\left(y - t'_{ox}\right)^2 - E_o(y - t'_{ox}) & \\ \qquad\qquad t'_{ox} \le y < d_g + t'_{ox} & \\ 0, \qquad\qquad y \ge d_g + t'_{ox} & \end{cases}, \quad (1)$$

where φ_g is the potential at the gate-"oxide" interface,

$$d_g = \sqrt{\frac{2\varepsilon_s\phi_o}{qN_s}} \quad (2)$$

is the depletion depth, and

$$E_o = \frac{qN_s}{\varepsilon_s} d_g = \sqrt{\frac{2qN_s\phi_o}{\varepsilon_s}} \tag{3}$$

is the magnitude of the vertical 1D electric field contribution at the semiconductor-oxide interface.
At threshold, the 1D channel potential is $\phi_o = V_{SB} + 2\varphi_b$, and below threshold it becomes:

$$\phi_o = V_{GB} - V_{FB} + \frac{qN_s}{\varepsilon_s} t'^{\,2}_{ox} + \\ -2t'_{ox}\sqrt{\frac{qN_s}{2\varepsilon_s}\left(V_{GB} - V_{FB} + \frac{qN_s}{2\varepsilon_s} t'^{\,2}_{ox}\right)}, \tag{4}$$

where V_{GB} is the gate-substrate voltage and V_{FB} is the flat band voltage. It is assumed in Eq. (1) that the oxide thickness is much smaller than the gate length.
We note that the total 2D potential distribution in Region 1 is

$$\Phi_g(x, y) = \phi_g(y) + \varphi_g(x, y), \tag{5}$$

where $\varphi_g(x, y)$ is the solution of the Laplacian.

1D potential distribution in Regions 2 and 3. The potential distributions in Regions 2 and 3 are initially approximated by 1D distributions of the following form:

$$\phi_{s,d}(y) = \begin{cases} \phi_g + (V_{s,d} - \phi_g)\dfrac{y}{t'_{ox}}, & 0 \le y < t'_{ox} \\ V_{S,D}, & t'_{ox} \le y \le d_j + t'_{ox} \\ V_{S,D} + \dfrac{qN_s}{2\varepsilon_s}\left(y - d_j - t'_{ox}\right)^2 - E_{o(s,d)}(y - d_j - t'_{ox}) & \\ \qquad\qquad d_j \le y \le d_j + d_{s,d} \\ 0, & y > d_j + d_{s,d} + t'_{ox} \end{cases} \tag{6}$$

Here $V_S \equiv V_{SB} + V_{bi}$ and $V_D \equiv V_S + V_{DS}$, are the potentials at the source and drain contact regions relative to the substrate interior, V_{bi} is the built-in voltage, and V_{DS} is the drain-source bias. The 1D depletion widths of the two regions are given by

$$d_{s,d} = \sqrt{\frac{2\varepsilon_s V_{S,D}}{qN_s}}. \tag{7}$$

E_{os} and E_{od} are the vertical electric fields at the interface of the source and drain contact regions, respectively, at the effective contact depth $y = d_j$ (see Fig. 1):

$$E_{o(s,d)} = \frac{qN_s}{\varepsilon_s} d_{s,d} = \sqrt{\frac{2qN_s V_{S,D}}{\varepsilon_s}}. \tag{8}$$

Boundary conditions of the Laplacian in Region 1. To solve the Laplacian in Region 1, we must determine the boundary conditions for the three interfaces indicated in Fig. 2.

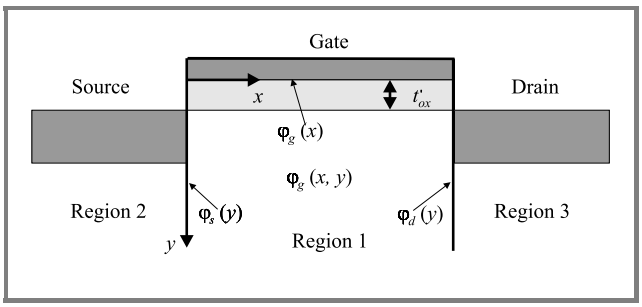

Fig. 2. Boundary conditions for the Laplacian of Region 1.

At the metal-"oxide" interface, we have

$$\varphi_g(x) \equiv \varphi_g(x, 0) = V_{GB} - V_{FB}. \tag{9}$$

At the vertical boundaries, we require the potential to be continuous. Hence, from Eqs. (1) and (5), we obtain for the source and drain side interfaces:

$$\varphi_{s,d}(y) = \phi_{s,d}(y) - \phi_g(y) = \\ = \begin{cases} (V_{S,D} - \phi_o)\dfrac{y}{t'_{ox}}, & 0 \le y \le t'_{ox} \\ V_{S,D} - \phi_o + E_o(y - t'_{ox}) - \dfrac{qN_s}{2\varepsilon_s}\left(y - t'_{ox}\right)^2, & \\ \qquad\qquad t'_{ox} \le y \le d_j + t'_{ox} \\ V_{S,D} - \phi_o + E_{o(s,d)} d_j + \dfrac{qN_s}{2\varepsilon_s} d_j^2 + & \\ + \left(E_o - E_{o(s,d)} - \dfrac{qN_s}{\varepsilon_s} d_j\right)(y - t'_{ox}), & \\ \qquad\qquad d_j + t'_{ox} \le y \le d_g + t'_{ox} \\ V_{S,D} - E_{o(s,d)}(y - d_j - t'_{ox}) + \dfrac{qN_s}{2\varepsilon_s}\left(y - d_j - t'_{ox}\right)^2, & \\ \qquad\qquad d_g + t'_{ox} \le y \le d_j + d_{s,d} + t'_{ox} \\ 0, & y > d_j + d_{s,d} + t'_{ox} \end{cases} \tag{10}$$

We can see from Eq. (1) that the intitial 1D estimate for the channel potential is $\Phi_o(x) = \phi_o$, or $\varphi_o(x) = 0$. As will be discussed below, solving for the above boundary conditions, we eventually will arrive at an improved $\Phi_o(x)$ that is properly adjusted for the 2D effects.

3. Conformal mapping

As discussed by Klös and Kostka [15], the Laplacian in the semi-infinite slab denoted as Region 1, can be solved by conformal mapping, given the boundary conditions discussed above. This is done by considering the (x, y) plane as a complex plane, and mapping Region 1 of this plane (see Fig. 2) into the upper half of a transformed, complex (u, v) plane, as shown in Fig. 3. The relative simplicity of the boundary conditions in the transformed plane allows us to derive potential distributions in this plane, from which they can be transformed back to the (x, y) plane.

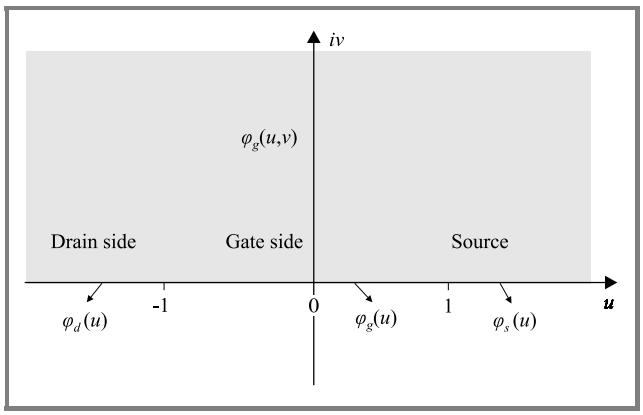

Fig. 3. Conformal mapping of Region 1 of the (x, y) plane into the upper half of the complex (u, v) plane.

The mapping between the two planes is achieved by means of the following Schwartz-Christoffel transformation [16]:

$$z = \int \frac{dz}{dw}\,dw = \frac{L}{\pi}\int \frac{dw}{\sqrt{w-1}\sqrt{w+1}} = \\ = 2\,\frac{L}{\pi}\,\ln\left(\frac{\sqrt{w-1}+\sqrt{w+1}}{\sqrt{2}}\right). \tag{11}$$

The solution of the Laplacian in the (u, v) plane is given by the following integral along the u-axis:

$$\varphi(u,v) = \frac{v}{\pi}\int_{-\infty}^{+\infty} \frac{\varphi(u')}{(u-u')^2+v^2}\,du', \tag{12}$$

where $\varphi(u)$ is the boundary condition transformed to the u-axis. This result can then be transformed back to the (x, y) plane by means of Eq. (11). Note that along the u-axis, the transformation in Eq. (11) can be written as:

$$x = \frac{L}{\pi}\mathrm{Arcos}(u), \quad y = 0, \quad \text{for} \quad |u| \le 1, \tag{13}$$

$$x = 0, \quad y = \frac{L}{\pi}\ln\left(|u| + \sqrt{u^2-1}\right) \equiv \\ \equiv \frac{L}{\pi}\,\mathrm{Arcosh}(|u|), \quad \text{for} \quad |u| > 1\,. \tag{14}$$

For MOSFET modeling, we will only be needing the electric field component E_n normal to the channel. This field includes the 1D electrical field E_o and the 2D vertical field component $E_{2D}(x)$ associated with the Laplacian. Assuming that the oxide thickness is much smaller than the gate length, the latter can be taken to be the same at the channel as at the metal interface. Hence, in the (x, y)-plane, we have:

$$E_n(x) = E_o + E_{2D}(x)\,. \tag{15}$$

The contribution $E_{2D}(u)$ from the Laplacian can easily be obtained from Eq. (12) as the mapped derivative of $\varphi(u, v)$ with respect to v in the limit of $v \to 0$ (see also [15, 16]):

$$E_{2D}(u) = \lim_{v\to 0}\left|\frac{\partial w}{\partial z}\right|\frac{d\varphi(u,v)}{dv} = \\ = \frac{1}{\pi}\left|\frac{\partial w}{\partial z}\right|\int_{-\infty}^{+\infty}\frac{1}{u-u'}\left.\frac{\partial \varphi}{\partial u}\right|_{u'} du'\,. \tag{16}$$

The integral in this expression can be solved piecewise for the various sections of the boundaries indicated in Fig. 1. Along the u-axis, the integration limits are as follows:

$$-\infty, -u_4 = -\cosh\left(\frac{\pi(d_j+d_d+t'_{ox})}{L}\right), -u_2, -u_1, -1\,, \\ 1, u_1 = \cosh\left(\frac{\pi(d_j+t'_{ox})}{L}\right), u_2 = \cosh\left(\frac{\pi(d_g+t'_{ox})}{L}\right), \\ u_3 = \cosh\left(\frac{\pi(d_j+d_s+t'_{ox})}{L}\right), \infty \tag{17}$$

We note that since $\varphi(u) = 0$ for $u < -u_4$ and for $u > u_3$, we have no contributions to the integral from these intervals.

3.1. Some approximations

In order to find analytical solutions to the integral of (16), we have to introduce some additional approximations. Specifically, we have to replace the mapping functions for x and y in the integrand by more manageable functions.
For the channel region $(-1 \le u \le 1)$, we propose to use the following approximation:

$$x = \frac{L}{\pi}\mathrm{Arcos}(u) \approx \\ \approx \frac{L}{\pi}\left[\sqrt{2}\left(\sqrt{1-u}-\sqrt{1+u}\right)+\frac{\pi}{2}+\left(2-\frac{\pi}{2}\right)u\right]. \tag{18}$$

The transformation and the error of the approximate function are shown in Fig. 4. We note that the maximum error is about 0.2%.
We note that the derivative of x with respect to u has the following exact form:

$$\frac{dx}{du} = -\frac{L/\pi}{\sqrt{1-u^2}}\,. \tag{19}$$

Outside the channel region $(|u| > 1)$, we have the exact mapping function shown in Eq. (14). Here we propose to use the following approximate function:

$$y = \frac{L}{\pi}\mathrm{Arcosh}(|u|) \approx \\ \approx \frac{L}{\pi}\times\begin{cases}\sqrt{2(|u|-1)}, & \text{for } |u| < u_o \\ \sqrt{2(|u|-1)}-k(|u|-u_o), & \text{for } |u| \ge u_o\end{cases}, \tag{20}$$

where $u_o = 1.2$ and $k = 0.14$.

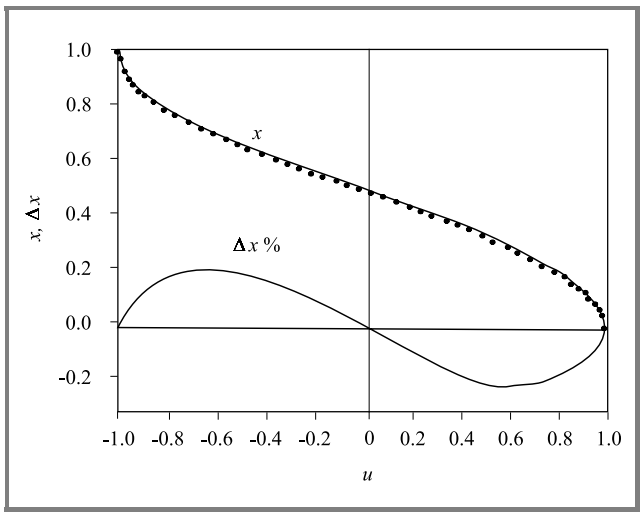

Fig. 4. Comparison between the exact (dots) and the approximate (top solid curve) mapping functions for the channel region. The error of the approximate function is shown in the lower curve.

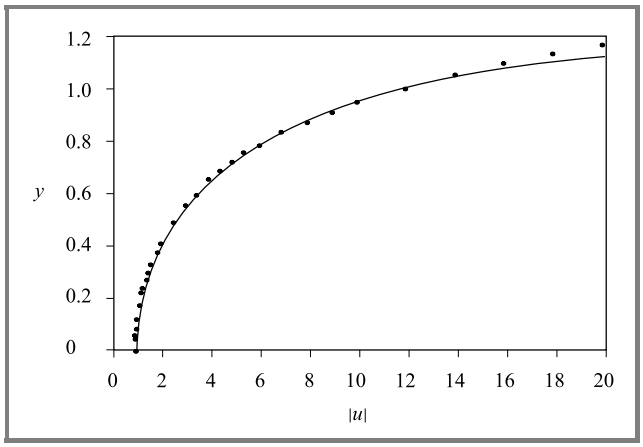

Fig. 5. Comparison between the exact (dots) and the approximate (solid curve) mapping functions for the channel region.

A comparison of these expressions is shown in Fig. 5 for $1 \leq |u| < 20$. We note that the derivative of y with respect to u has the exact form:

$$\frac{dy}{du} = \frac{L/\pi}{\sqrt{u^2-1}}. \tag{21}$$

The error associated with the approximate mapping is very small, less than 0.01 for $|u|$ less than about 15, then increases to about 0.05 at $|u| = 20$, and continues to increase for higher values of $|u|$. However, we note that the contributions from the boundaries to the potential and the electrical field at or near the channel vanishes for values of $|u| > u_3$ (source side) and $|u| > u_4$ (drain side) (see Eqs. (16) and (17) and Fig. 1). For well-designed transistors, typical values of u_3 and u_4 are within the range of u shown in Fig. 5.

3.2. Channel potential profile

Using the above formalism, the partial integrals from all the boundary sections of Eq. (16) have analytical solutions (although with somewhat lengthy expressions in most cases). The transformation from the (u, v)-plane to the (x, y)-plane is straightforward using the inverse of Eqs. (13) and (14) for the coordinate.

In order to determine the channel potential profile, $\Phi_o(x) = \phi_o + \varphi_o(x)$, in the subthreshold regime, we have to consider the layer of mobile channel charge with sheet density $qn(x)$. Using Gauss' law on a small section of this sheet charge, we find the following relationship (see Eqs. (15) and (16)):

$$qn(x) = \left[E_i(x) - E_n(x)\right]\varepsilon_s, \tag{22}$$

where E_i is the total normal field in the "oxide". Again, noting that the oxide thickness is very small compared to the channel length, we can safely assume that the vertical field is constant inside the "oxide", which means that it can be expressed in terms of the difference between the potentials at the metal boundary and at the channel, i.e.:

$$E_i(x) = \left[V_{GS} - V_{FB} - V_{BS} - \Phi_o(x)\right]/t'_{ox}, \tag{23}$$

where V_{GS} is the gate-source voltage. Combining (22) and (23) and using elementary electron statistics, we obtain the following expression for the total potential profile $\Phi_o(x)$ in the channel:

$$q\frac{n_i^2}{N_s}\exp\left(-\frac{\Phi_o(x,0)}{V_{th}}\right) =$$

$$= \left\{\frac{\left[V_{GS} - V_{FB} - \Phi_o(x)\right]}{t'_{ox}} - E_n(x)\right\}\varepsilon_s, \tag{24}$$

where n_i is the intrinsic carrier concentration and V_{th} is the thermal voltage. We observe that, except for the portions of the channel close to the source and drain, the term on the left side of this expression can be ignored. Hence, for the central part of the channel, we obtain the following potential profile:

$$\Phi_o(x) \approx V_{GS} - V_{FB} - E_n(x)t'_{ox} =$$

$$= V_{GS} - V_{FB} - \frac{\varepsilon_s}{\varepsilon_i}\left[E_o + E_{2D}(x)\right]t_{ox}. \tag{25}$$

A satisfactory, approximate, analytical solution of Eq. (24), that covers the full length of the channel, is also available using the "generalized diode equation" approach discussed in [18].

3.3. Threshold voltage

We recall that the threshold condition is satisfied when the minimum of the channel potential just reaches the value

$\Phi_{o,\min} = V_{SB} + 2\varphi_b$. From Eq. (25), we find the following expression for the threshold voltage:

$$V_T = V_{FB} + V_{SB} + 2\varphi_b + E_{n,\max} t'_{ox}, \tag{26}$$

where $E_{n,\max}$ is the maximum of the normal electric field in the channel at threshold.

3.4. Subthreshold current

The subthreshold drain current I_{sub} can be expressed either in terms of a thermionic emission current I_{tem} in short-channel devices, or as a drift-diffusion current I_{dd} for longer channels. To cover a wide range of channel lengths, we may apply the following unified approximation [19], which is always dominated by the "rate limiting" transport mechanism:

$$I_{sub} \approx \left(\frac{1}{I_{tem}} + \frac{1}{I_{dd}} \right)^{-1}. \tag{27}$$

The thermionic emission current is given by:

$$I_{tem} \approx W \, \delta A^* T^2 \exp\left(\frac{\Phi_{g,\min} - V_{bi}}{V_{th}} \right), \tag{28}$$

where $\Phi_{g,\min}$ is the minimum value of the channel potential, δ is the effective thickness of the channel at the potential minimum, W is the width of the channel, A^* is Richardson's constant. An expression for the drift-diffusion current was discussed in [19], for which an approximation applicable to subthreshold MOSFETs was presented in [15].

4. Quarter-micron MOSFET

We first consider conventional n-channel MOSFETs with device lengths of 250 nm and 210 nm by comparing our results with the experimental data by Chung *et al.* [20]. The experimental data used here came from devices with $N_s = 2 \cdot 10^{17}$ cm^{-3} and $t_{ox} = 8.6$ nm, except for the subthreshold characteristics that came from a device with $N_s = 4 \cdot 10^{17}$ cm^{-3} and $t_{ox} = 5.6$ nm. The junction depth in all cases was about 0.16 μm, and the gate-junction overlap was 0.1 μm. The devices from [20] were chosen since they did not include any halo doping or LDD. Hence, the devices displayed the type of short-channel behavior expected also for classical sub-100 nm MOSFETs (see below).

Figure 6 shows comparisons of the modeled and experimental results for the threshold voltage versus applied drain-source bias and versus the gate length, respectively, for MOSFETs with $t_{ox} = 8.6$ nm. To arrive at the experimental data in the latter case, a calculated long-channel threshold voltage of 0.42 V was used.

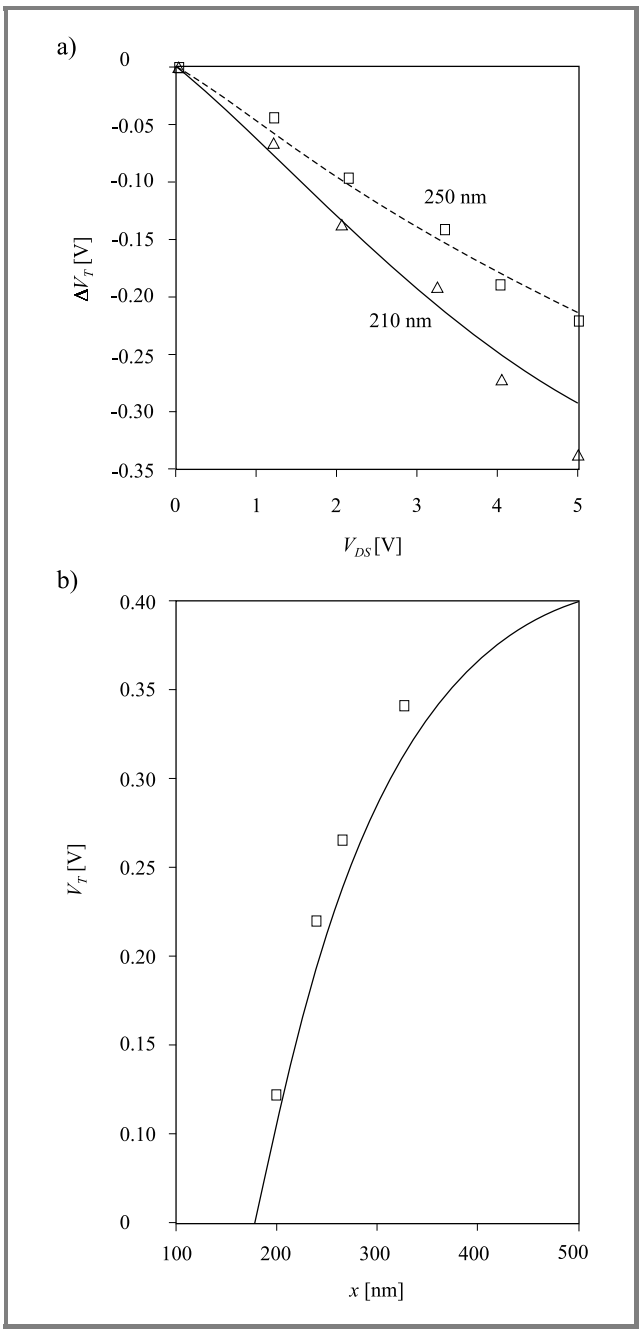

Fig. 6. Comparison of experimental (symbols) and modeled (lines) variation in threshold voltage: (a) versus applied drain-source bias for $t_{ox} = 8.6$ nm MOSFET with 210 nm and 250 nm gate lengths, and (b) versus gate length for $V_{DS} = 0.05$ V.

The modeled threshold voltages were determined from the minimum channel potential for a set of gate-source voltages, selecting the ones that comply with the threshold condition. The calculations were based on processing and geometric parameters for the two devices.

Figure 7 shows the corresponding central parts of the potential distributions in the channel at threshold, calculated using Eq. (27) for $V_{DS} = 0.05$ V and at 3 V.

These curves clearly illustrate the lowering of the threshold voltage (DIBL-effect) related to the reduction of

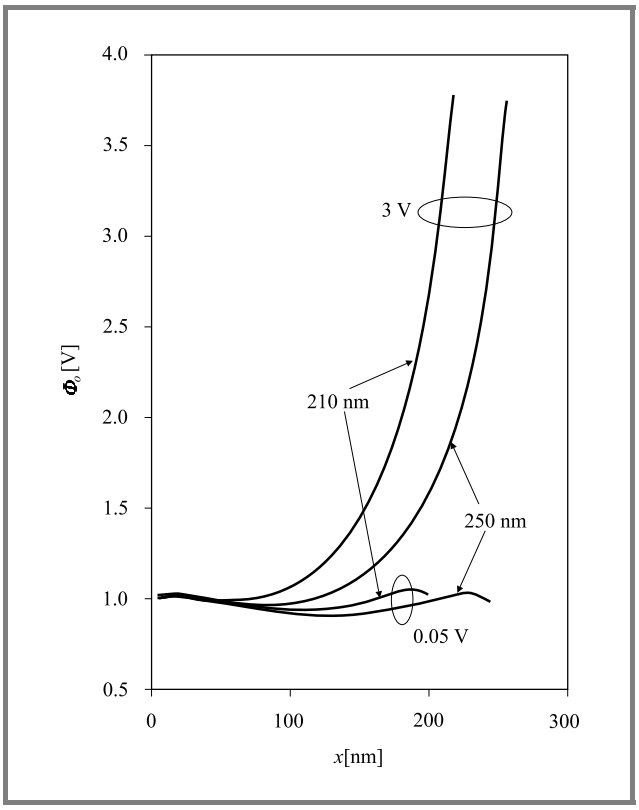

Fig. 7. Model calculations of the channel potential relative to the substrate for $V_{DS} = 0.05$ V and 3 V for gate lengths of 210 nm and 250 nm and $t_{ox} = 8.6$ nm.

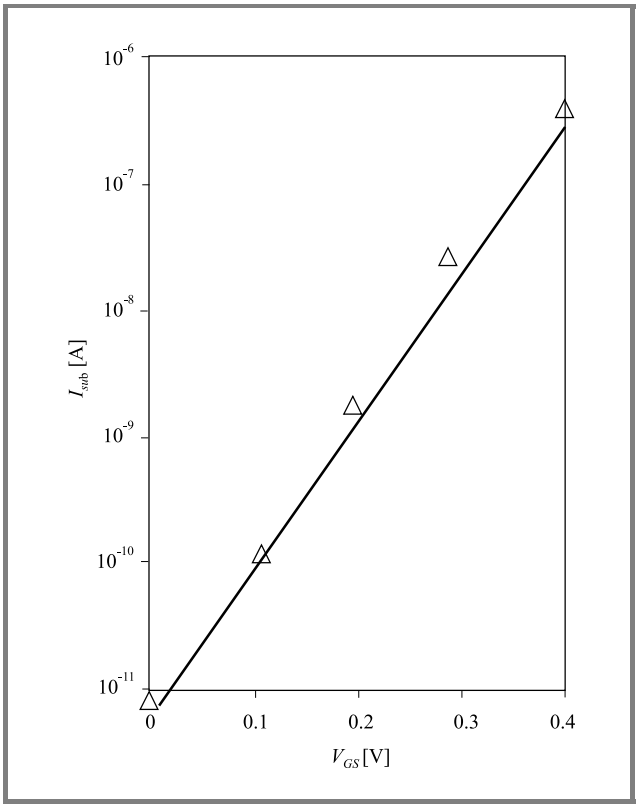

Fig. 8. Measured (symbols) and modeled (line) subthreshold transfer characteristics for a 250 nm MOSFET with and $t_{ox} = 5.6$ nm at $V_{DS} = 0.05$ V.

the energy barrier with increasing drain-source bias. Also the shift of the potential minimum in the direction of the source with increasing drain-source bias is indicated.

A comparison of an experimental and modeled subthreshold transfer characteristics for a 250 nm device with $t_{ox} = 5.6$ nm is shown in Fig. 8 for $V_{DS} = 0.05$ V. Note that this device has a different oxide thickness and doping than the 250 nm device discussed in Figs. 6 and 7. However, except for N_s and t_{ox}, the same parameter values were used in the simulations.

The data shown here indicate that the present 2D modeling strategy is quite suitable for deep submicron MOSFETs operating in the subthreshold regime. The deviations observed can mostly be attributed to the deviations of the processing variables from those reported. As indicated above, the only adjustable parameter in the present modeling is the effective depth source and drain contact, which accounts for the rounding of the contacts towards Region 1 (see Fig. 1). Next, we will also test the approach for an experimental MOSFET in the sub-100 nm range.

5. Sub-100 nm MOSFET

One of the problems of scaling classical MOSFETs into the sub-100 nm range is that the substrate doping density has to be increased into the 10^{18} cm^{-3} range in order to contain the source and drain depletion layers. However, this high doping has several detrimental effects on the MOSFET properties, such as degradation of the channel mobility and too large threshold voltages.

One solution to this problem is to use a much lower doping in the substrate and instead ion implant a higher doping of desired concentration under the surface. After annealing, a thin layer of lower doping concentration remains at the surface, typically to a depth of less than 100 nm. The much higher doping needed to prevent severe short-channel effects and punch-through stretches for another 100 nm or so into the substrate. This is the so-called SSR (super-steep-retrograde) channel MOSFET structure.

Here, we consider such an n-channel MOSFET with a 70 nm gate length, reported by Xu *et al.* [21]. The doping at the surface of this device is about $2.8 \cdot 10^{17}$ cm^{-3} and increases almost exponentially to about $1.8 \cdot 10^{18}$ cm^{-3}

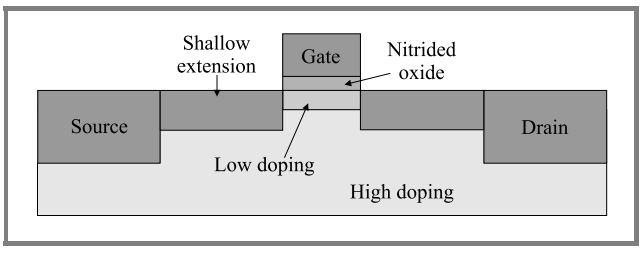

Fig. 9. Schematic view of a super-steep-retrograde channel MOSFET. For the modeling, we assume that the low-doped and the high-doped regions each have a constant doping density.

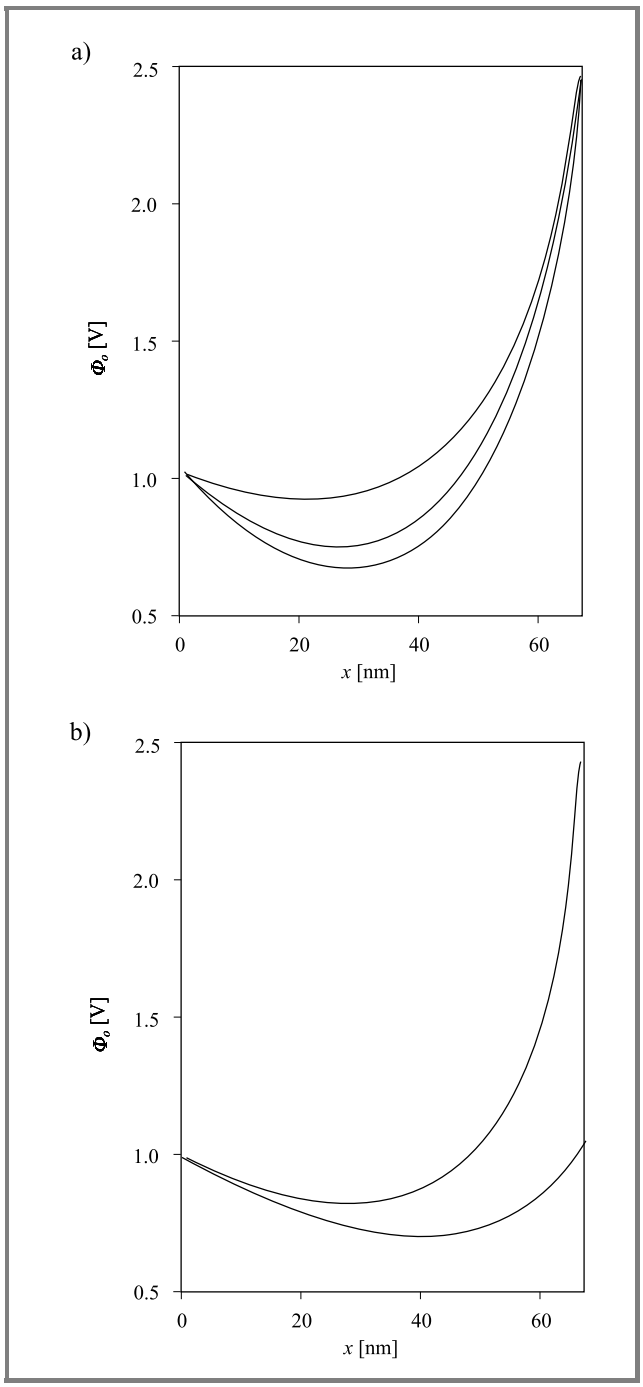

Fig. 10. Model calculations of the channel potential profiles in 70 nm SSR MOSFET relative to the substrate for (a) $V_{DS} = 1.6$ V at $V_{GS} = 0$ V (lower curve), 0.1 V (middle curve), and 0.31 V (upper curve), and (b) $V_{GS} = 0.1$ V at $V_{DS} = 0$ V (lower curve) and 1.5 V (upper curve).

at a depth of 60 nm. It also has the added benefit of very shallow source and drain extensions, with a thickness of about 50 nm, realized by means of a SALICIDE process.

The variable substrate doping of the SSR channel MOSFET is modeled as a two-layer structure, as indicated in Fig. 9, where each layer has a constant doping. The thickness and the doping concentration in the shallow top region are chosen to be 35 nm and $9.2 \cdot 10^{17}$ cm^{-3}, respectively, which accounts for all the doping atoms in the graded region near the surface. At threshold and zero drain-source bias, the depletion layer stretches into the highly doped region. The thickness of the highly doped layer is such that it is never penetrated by the gate depletion layer.

The modeling of the SSR MOSFET proceeds as described above for the 250 nm MOSFET, except that the vertical boundaries of the central region under the gate (Region 1) now include an extra section to account for the shallow layer of reduced substrate doping. Region 1, where the Laplacian is defined, is still assumed to include the gate oxide and a semi-infinite slab of semiconductor below (see Fig. 2).

5.1. Modeling results for 70 nm SSR MOSFET

Again, the threshold voltages were determined from the minimum channel potentials for a set of gate-source voltages, selecting the ones that comply with the threshold condition. Figure 10 shows the calculated channel potential profiles for some combinations of drain-source and gate-source biases in the subthreshold regime.

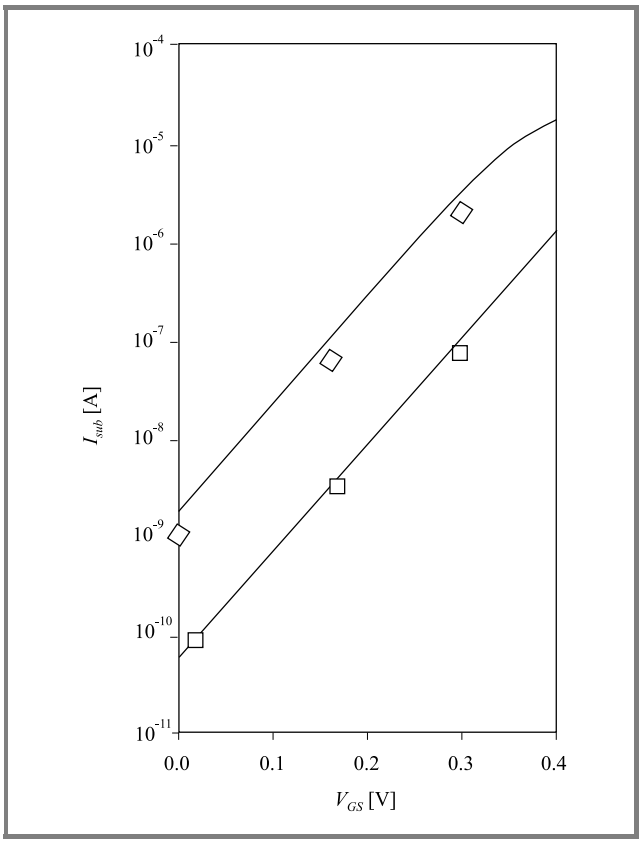

Fig. 11. Experimental (symbols) and modeled (lines) subthreshold transfer characteristics for a 70 nm SSR MOSFET with $t_{ox} = 3$ nm. $V_{DS} = 0.1$ V (lower curve) and 1.6 V (upper curve).

At zero drain-source bias we obtain the threshold voltage $V_T = 0.3$ V, in close agreement with the value reported in [21]. From the calculated variation of the threshold voltage with the applied drain-source bias, we find a DIBL parameter of $\sigma = \Delta T / V_{DS} = 80$ mV/V. This value is reasonably close to the value of about 70 mV/V obtained from the experimental subthreshold transfer NMOS characteristics of [21].

Figure 11 shows a comparison of the experimental and modeled subthreshold characteristics of the 70 nm SSR MOSFET.

6. Summary

A closed-form 2D modeling technique for deep-submicron and sub-100 nm MOSFETs has been investigated. The technique is based on conformal mapping, where the 2D Poisson equation in the depletion regions is separated into a 1D long-channel case and a 2D Laplace equation. From the straightforward 1D solution, the boundary potential values of the Laplacian is obtained, from which a 2D correction to the channel potential is derived. The model has been tested for classical MOSFETs with gate lengths in the range 200–250 nm, and for a super-steep retrograde MOSFET with a gate length of 70 nm. With a minimum set of parameters, the present modeling reproduces both qualitatively and quantitatively the experimental data obtained for such devices.

This method applies to classical MOSFETs as well as to non-classical structures. As shown here, the classical MOSFET approach is directly applicable to SSR MOSFETs, and may also be applied to Si-Si/Ge strained devices and to sidewall vertical MOSFETs with a partially depleted body. We foresee that the same approach, with somewhat adjusted boundary conditions for the Laplacian, may also be applicable to double-gate fully depleted vertical MOSFETs and to double-gate SOI MOSFETs.

References

[1] Y. Cheng and C. Hu, *MOSFET Modeling & BSIM3 User's Guide*. Boston: Kluwer, 1999.

[2] W. Liu and C. Hu, "BSIM3V3 MOSFET model", in *Silicon and Beyond: Advanced Device Models for Circuit Simulators*, M. S. Shur and T. A. Fjeldly, Eds. Singapore: World Scientific, 2000, pp. 1–31.

[3] W. Liu *et al.*, *BSIM4 User's Manual*. Berkeley: University of California, 2000.

[4] T. Ytterdal, Y. Cheng, and T. A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design.* London: Wiley, 2003.

[5] C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", in *Analog Integrated Circuits and Signal Processing.* Boston: Kluwer, 1995, vol. 8, pp. 83–114.

[6] R. Velghe, D. Klaassen, and F. Klaassen, "MOS Model 9". Unclassified Report NL-UR 003/94, Philips Electronics N.V, 1994.

[7] K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling for VLSI*. Englewood Cliffs, NJ: Prentice Hall, 1993.

[8] T. A. Fjeldly, T. Ytterdal, and M. Shur, *Introduction to Device Modeling and Circuit Simulation*. New York: Wiley, 1998.

[9] ITRS – International Technology Roadmap for Semiconductor. Austin: Semiconductor Industry Assoc., 2001.

[10] K. N. Ratnakumar and J. D. Meindl, "Short-channel MOSFET threshold voltage model", *IEEE J. Solid-State Circ.*, vol. 17, pp. 937–948, 1982.

[11] Y. A. El-Mansy and A. R. Boothroyd, "A simple two-dimensional model for IGFET operation in the saturation region", *IEEE Trans. Electron Dev.*, vol. 40, pp. 254–262, 1977.

[12] V. K. De and J. D. Meindl, "An analytical threshold voltage and subthershold current model for short-channel MESFETs", *IEEE J. Solid-State Circ.*, vol. 28, pp. 169–172, 1993.

[13] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double gate and cylindrical, surrounding-gate MOSFETs", *IEEE Electron Dev. Lett.*, vol. 21, no. 9, 2000.

[14] Y.-S. Pang and J. R. Brews, "Analytical subthreshold surface potential model for pocket n-MOSFETs", *IEEE Trans. Electron Dev.*, vol. 49, pp. 2209–2216, 2002.

[15] A. Klös and A. Kostka, "A new analytical method of solving 2D Poisson's equation in MOS devices applied to threshold voltage and subthreshold modeling", *Solid-State Electron.*, vol. 39, pp. 1761–1775, 1996.

[16] E. Weber, *Electromagnetic Fields*, vol. 1: *Mapping of Fields*. New York: Wiley, 1950.

[17] P. M. Zeitzoff, J. A. Huchby, and H. R. Huff, "MOSFET and front-end process integration: scaling trends, challenges, and potential solutions through the end of the roadmap", in *Int. J. High Speed Electron. Syst.*, 2002, vol. 12, pp. 267–293.

[18] T. A. Fjeldly, B. J. Moon, and M. S. Shur, "Approximate analytical solution of the generalized diode equation", *IEEE Trans. Electron Dev.*, vol. 38, pp. 1976–1977, 1991.

[19] T. A. Fjeldly and M. S. Shur, "Threshold voltage modeling and the subthreshold regime of operation of short-channel MOSFETs", *IEEE Trans. Electron Dev.*, vol. 40, pp. 137–145, 1993.

[20] J. E. Chung, M.-C. Jeng, J. E. Moon, P.-K. Ko, and C. Hu, "Performance and reliability design issues for deep-submicrometer MOSFET's", *IEEE Trans. Electron Dev.*, vol. 38, no. 3, pp. 545–554, 1991.

[21] Q. Xu, H. Qian, H. Yin, H. Ji, B. Chen, Y. Zhu, M. Liu, Z. Han, H. Hu, Y. Qiu, and D. Wu, "The investigation of key technologies for sub-0.1-μm CMOS device fabrication", *IEEE Trans. Electron Dev.*, vol. 48, no. 7, 2001.

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