Closed-loop Compensation of Charge Trapping Induced by Ionizing Radiation in MOS Capacitors

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***Abstract*—The objective of this work is to explore the capability of a charge trapping control loop to continuously compensate charge induced by ionizing radiation in the dielectric of MOS capacitors. To this effect, two devices made with silicon oxide have been simultaneously irradiated with gamma radiation: one with constant voltage bias, and the other working under a dielectric charge control. The experiment shows substantial charge trapping in the uncontrolled device whereas, at the same time, the control loop is able to compensate the charge induced by gamma radiation in the second device.**

***Index Terms*—MOS capacitors, MIS capacitors, charge trapping control, radiation effects, ionizing radiation.**

I. Introduction

Charge trapping induced by ionizing radiation in MOS devices represents a reliability issue in space applications [1]. Under the influence of high energy ionizing radiation, these devices suffer from a drift in the threshold voltage, an increase of the leakage current, and a decrease of the transconductance [2]. This results in a degraded performance thereby increasing the failure rate of the device operation [3]–[6].

In the opposite direction, RADFETs are MOS structures specially designed for radiation sensing. In recent years, some works have focused on obtaining a trapped hole annealing in order to delay the saturation of the sensor and to keep it working in near optimal conditions. This has been achieved by applying bias switching [7]. In [8] periodical charge neutralization of radiation-induced trapped charge is performed to keep the threshold voltage of RADFETs between some predetermined limits. Measurement is carried out in open loop configuration between bias switching operations. On the other hand, Fowler-Nordheim tunnelling is used in [9] to compensate holes trapped in the buried oxide layer of a monolithic pixel detector used in high-energy physics, X-ray imaging, etc. As a consequence, techniques focused on controlling the total charge in dielectrics may have many different applications (drift avoidance or sensor optimization).

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Dielectric charge controls, first proposed in [10], have been recently achieved in the case of electrostatic MEMS [11], [12] and MOS capacitors [13]. This work presents results obtained in gamma radiation experiments carried out to observe how dielectric charge induced by ionizing radiation can be effectively compensated by a charge control loop. In particular, we prove that the control loop presented in [13] can also be used to compensate the charge induced by ionizing radiation in MOS capacitors with silicon oxide as dielectric. A first result in this direction has already been obtained for electrostatic MEMS [14]. To the best knowledge of the authors, this is the first time that charge induced by ionizing radiation has been compensated in a MOS structure. This new approach opens the possibility of establishing active compensation techniques of radiation-induced charge in MOS structures.

II. The Charge Control Loop

The control method implemented in this work, presented in [13], is based on sigma-delta modulation [15], used as a tool to provide a sliding mode control of net trapped charge [16], [17].

A. Sigma-delta modulation and sliding mode control

Sigma-delta modulators are extensively used in analog-to-digital and digital-to-analog conversion. In the analog-to-digital case, they are oversampled circuits that use rough quantizers (reaching even the 1-bit case, or sign function) to produce a stream of symbols from which the final digital conversions are obtained by filtering and decimation. These modulators provide quantization noise shaping, which means that the circuit moves the quantization noise out of the frequency band of interest of the analog input. By finally filtering the stream of symbols in the band of interest the quantization noise is removed to a large degree, depending on the oversampling ratio and the order of the converter.

The discrete-time circuit shown in Fig. 1 corresponds to a first order 1-bit sigma-delta converter. This circuit generates a bit stream at its output, $b(n)$, from the analog signal at its input, $x(n)$. The final digital conversion is obtained by low pass filtering and decimating the output bitstream. Note also that the circuit of Fig. 1 is basically composed of an integrator and a quantizer (sign function). In many applications this integrator is not in the electrical domain. It can be in the

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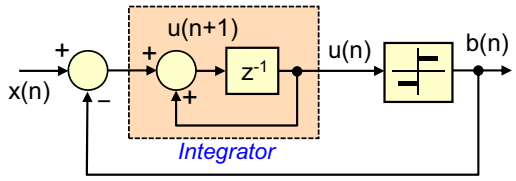

Fig. 1. First-order sigma-delta modulator.

thermal domain, as in thermal sigma-delta modulators [18], or in the mechanical domain, as in the case of some force feedback accelerometers [19].

Sigma-delta modulators have also been linked to sliding mode controllers, [16], [17]. The link comes from the fact that the modulator tries to minimize the quantization noise of the quantizer (in the case of Fig. 1 the sign function), in the frequency band of interest. In Fig. 1, for example, the modulator tries to enforce a zero average value of the integrator: $\overline{u(n)} \approx 0$. This may be seen as a sliding motion on a desired control surface within the space of state variables (in Fig. 1, only one state variable: the integrator output). In order to obtain this result, the average value of the bitstream must be the same as the average value of the input signal: $\overline{x(n)} = \overline{b(n)}$. Finally $\overline{b(n)}$ is therefore the well-known equivalent control signal of sliding mode controllers.

B. Charge trapping control

The charge control circuit used in this paper is shown in Fig. 2, [13]. The dielectric in the MOS capacitor can be seen as a reservoir of trapped charge which is continuously being filled/emptied by three different contributions:

- the trapped charge injected/extracted by the applied voltage actuation,
- the trapped charge being leaked out, and
- the trapped charge generated by radiation.

All three contributions will depend on the instantaneous applied electric field and on the state of the trapped charge, among other parameters. The generated control signal, composed of a sequence of voltage waveforms tries in average to inject the necessary charge into the dielectric to keep the total net charge constant. This can be seen as forcing the system to 'slide' on the control surface: 'total net charge equal to a desired value'.

Since the net trapped charge is a hidden variable it is indirectly obtained by keeping track of the capacitance of the device measured at a constant reference voltage, V_1, chosen beforehand. The objective of the control is therefore to keep this value constant, and at a desired level C_{th}. Any displacement or stretching of the C-V curve due to radiation will generate unwanted shifts in this capacitance. This is perceived by the control loop (a discrete time circuit) as a deviation from the target value for the capacitance, and therefore it tries to generate the adequate compensation in the next sampling period.

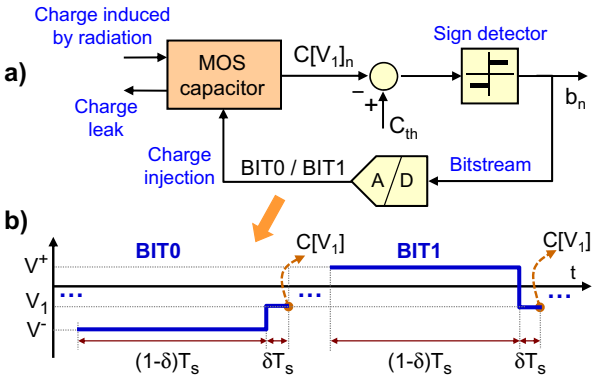

Fig. 2. a) Sigma-delta feedback loop. The device capacitance at voltage V_1 is measured periodically and compared with C_{th}. Depending on the result, either a BIT1 or BIT0 waveform is applied during the next sampling period. b) BIT0 and BIT1 waveforms. Capacitance measurements are taken at the end of each V_1 application.

This compensation is achieved by choosing between two different voltage waveforms, BIT0 and BIT1, see Fig. 2. Both waveforms have the same duration T_S but take different voltage values $\{V^-, V_1\}$ and $\{V^+, V_1\}$. For our devices, applying BIT0s (V^-<0 dominant) tends to increase the amount of negative charge in the dielectric and thus produces C-V shifts to the right. On the other hand, the application of BIT1s (V^+>0 dominant) produces left C-V shifts (positive charge injection). This means that by choosing between a BIT0 and a BIT1 waveform, the control loop tries to compensate any deviation from its objective, which is keeping a constant predetermined target capacitance, measured at V_1: $C[V_1]_n = C[V_1](nT_S) = C_{\text{th}}$.

The sequence of BITs applied, which is the output of the control loop, provides real-time information about the charging dynamics [12], [13].

III. Experimental Results and Discussion

In order to analyze the behavior of the charge trapping control method applied to devices under radiation, two different capacitors, Dev-1 and Dev-2, have been irradiated simultaneously. Dev-1 was kept at a constant voltage bias of +1V, whereas the control was applied to Dev-2 to achieve and maintain a previously given target capacitance, C_{th}. A third device, Dev-3, identical to Dev-1 and Dev-2, will be used later to discuss charge injection.

A. Device fabrication

Devices 1-3 were fabricated on a p-type c-Si <100> substrate with a thickness of 280 μm and a resistivity of 2.5±0.5 Ωcm. The process starts with an RCA clean followed by 30 minutes of thermal oxidation with a temperature ramp between 850-1080°C. A SiO_2 layer of ~43 nm thick is grown on both sides of the wafer. The SiO_2 of the back side is etched with hydrofluoric acid (HF) while the front side is protected with photoresist. To form the upper contact, a stack of Ti/Al is

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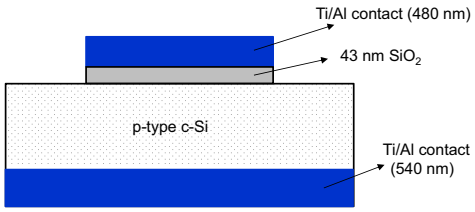

Fig. 3. Cross section of the MOS capacitors.

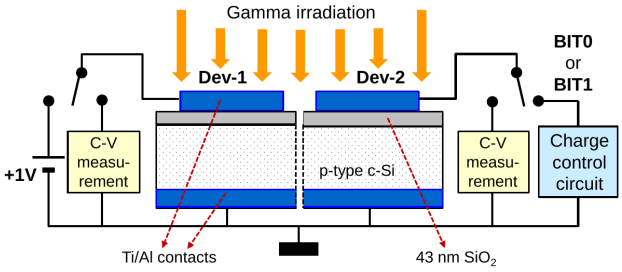

Fig. 4. Experimental setup: MOS capacitors Dev-1 and Dev-2 are irradiated simultaneously with the same dose rate patterns. Dev-1 is 1V biased, whereas the control is being applied to Dev-2 to set a target capacitance. Short C-V measurements are taken in Dev-1 in constant time intervals, whereas only initial and final C-V measurements are taken for Dev-2.

deposited by RF sputtering with a thickness of 480 nm on the front side of the wafer. The active area of the device is patterned by photolithography and wet etching. Then, a stack of Ti/Al of 540 nm was deposited on the back surface by RF sputtering. A final annealing in N_2 atmosphere at 400°C for 30 min was performed to reduce the resistance and improve the adherence of the contacts. A cross section of the devices is shown in Fig. 3. The area of the devices is $1mm^2$.

B. Experimental setup

In the experimental setup, a Precision LCR Meter was used to generate the BIT0/BIT1 waveforms and to perform all capacitance measurements. A sampling period $T_S = 350$ms and $\delta = 1/3$ were chosen for BIT0 and BIT1. This sampling time is smaller than the shortest time constant observed in the charging dynamics for the voltages applied in the experiment. The value of δ, on the other hand, allowed simplifying operation: there are three sub-bits inside each bit. That is, during a BIT0 (BIT1) the voltage sequence $\{V^-, V^-, V_1\}$ ($\{V^+, V^+, V_1\}$) is applied. The values of V^-, V^+ and V_1 are carefully chosen to obtain the desired behavior under control: opposite shift for both BIT0 and BIT1, and sensitivity to shifts of the C-V characteristic in the case of V_1. Finally, the capacitance measurements have been performed using a 2 MHz AC test signal.

The experimental arrangement, shown in Fig. 4, allowed simultaneous irradiation of both capacitors, one under constant +1V bias during all the experiment (Dev-1) and the other one controlled with the sigma delta loop described in the previous section (Dev-2). Periodical C-V measurements of Dev-1 were also performed.

The irradiation test was performed at the ESTEC ^{60}Co Facility [20], exposing the devices to the gamma rays emitted by the decay of a radioactive source of ^{60}Co. The ^{60}Co source emits photons of 1.17 MeV and 1.33 MeV, its activity was 76.7 TBq at the time of testing. The setup was positioned at a distance corresponding to a dose rate of 11 Gy(water)/h. Real time dosimetry was performed using a 2670 Farmer Dosimeter equipped with a 2571 Farmer 0.6 cc air Ionisation Chamber, the associated uncertainty is 4.4% to the dose rate measurement. The facility is accredited against ISO17025 standard.

C. Results and discussion

1) Radiation experiment and discussion: A long-time radiation experiment of 70 hours has been scheduled, with the following phases:

a) Initial phase: no radiation applied for the first 4 hours.
b) Irradiation phase: a constant radiation dose rate DR = 11 Gy(water)/h applied for the next 24 hours. The TID at the end of this phase was 264 Gy(water).
c) Rest phase: no radiation applied for 42 hours.

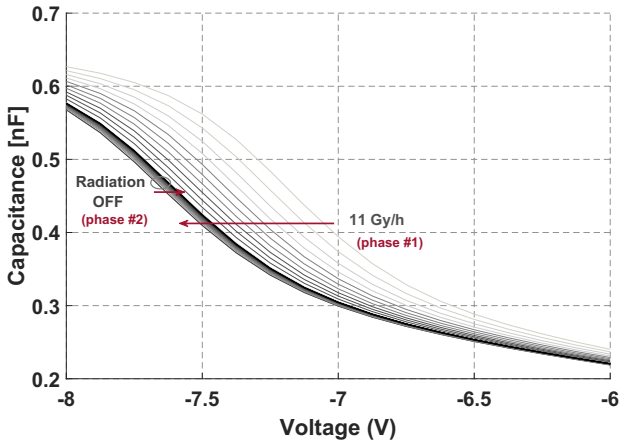

Fig. 5. Plot of successive CVs periodically obtained in the open loop device Dev-1 polarized at 1V bias. The first plot is just after having switched on radiation (DR=11 Gy(water)/h).

For the case of Dev-1, which was +1V biased, fast C-V measurements have been taken in 2-hour intervals during all the experiment. Fig. 5 shows how the C-V characteristic of Dev-1 evolved. It is seen there that the first exposure phase (DR=11 Gy(water)/h) caused a left-shift of the C-V. It can also be observed in Fig. 5 that the closely spaced C-Vs correspond to the final rest phase, in which no radiation was applied. During this last phase, the curves become stabilized and even begin a small shift to the right.

The evolution of the voltage shift of the C-V curves with Dev-1 during the experiment is depicted in Fig. 6, along with the dose rates applied. The time evolution of the capacitance measured at V_1 = -7.25 V is also plotted. There is a maximum voltage shift at the end of the irradiation phase of approximately -450 mV and a large variation of the capacitance of the

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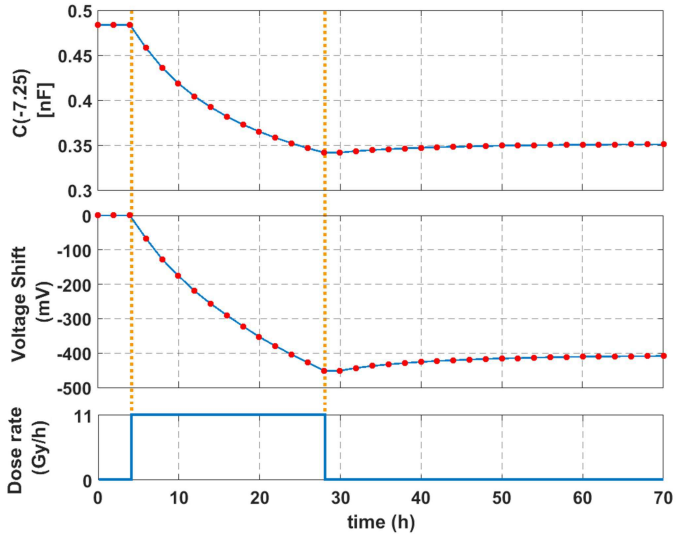

Fig. 6. Top: Time evolution of the capacitance of Dev-1, biased at +1V during the irradiation experiment. Middle: time evolution of the voltage shift of the C-V curve of the same device. Bottom: sequence of dose rates applied.

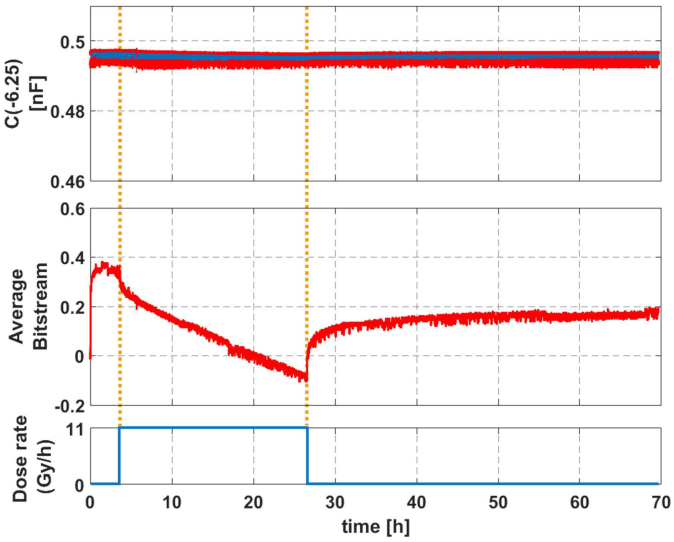

Fig. 7. Closed loop experiment with Dev-2, simultaneously irradiated with Dev-1. Top: time evolution of the capacitance measured at the reference voltage, $V_1 = -6.25V$. Middle: Average bitstream evolution (each sample is the average of 500 bits of the bitstream). Bottom: Sequence of dose rates applied.

device measured at constant voltage. The total dose is 237.6 Gy(SiO_2) and therefore this represents an average voltage shift of 1.9 mV/Gy(SiO_2).

Focusing on p-substrate MOS devices with oxide thickness around d=40 nm, under gamma irradiation with total doses below 1.5 kGy(SiO_2), voltage shifts similar to that reported here can be found in the literature. For instance, the transistors and capacitors measured in [21], 10V biased during irradiation, exhibit displacements of 1.33 mV/Gy(SiO_2) for a total dose of 300 Gy(SiO_2), decreasing to 0.8 mV/Gy(SiO_2) for 1kGy(SiO_2). Similarly, 1.2 mV/Gy(SiO_2) is obtained at 500 Gy(SiO_2) in [22], and 0.4 mV/Gy(SiO_2) at 1 kGy(SiO_2) is obtained in [23], both with n-channel transistors. Finally, in [24], 0.625 mV/Gy(SiO_2) at 1.2 kGy(SiO_2) is obtained with 5 V biased MOS capacitors.

On the other hand, Fig. 7 summarizes the results obtained with Dev-2 operating under the control method and the same sequence of irradiation and rest phases. In this case the feedback loop was configured to set the capacitance to a target value C_{th} = 0.495 nF at V_1 = -6.25 V, being the control voltages V^+= 4 V and V^-= -8 V.

Fig. 7 shows the time evolution of the controlled device: as soon as control starts working at t=0, only BIT1s are applied until the capacitance of Dev-2 rapidly reaches the target value. Once the desired capacitance C_{th} is reached, the feedback loop applies the required bitstream to maintain such capacitance approximately constant during the entire experiment.

As discussed above, the moment that radiation is switched on, the charge trapping being induced in the oxide tends to shift the C-V to the left (positive charge trapping), therefore decreasing $C[V_1]_n$. This implies that in order to keep the target capacitance, $C[V_1]_n \approx C_{\text{th}}$ constant, less BIT1s must be applied. Decreasing the average number of BIT1s tends to displace the CV curve to the right, therefore increasing $C[V_1]_n$ and compensating the charge generated by radiation.

This is clearly seen in the irradiation phase, in which the average bitstream decreases while the accumulated dose grows. On the other hand, during the final rest phase (no radiation) the bitstream suddenly recovers until it reaches a quite stable regime. Moreover, the behavior of the average bitstream shown in Fig. 7 for Dev-2 can be related to that of the voltage shift shown in Fig. 6 for Dev-1. This clear correlation indicates that the control loop is continuously compensating the effect of the dielectric charge induced by the radiation regime applied.

Fig. 8 shows the C-Vs of Dev-2 obtained at the beginning and at the end of the experiment. It can be seen that the curves are almost undistinguishable. That is, even under ionizing radiation the control loop guarantees a long-time stable C-V characteristic.

Fig. 9 compares the I-V characteristics of the devices after the experiment ended. There is no large difference between both curves, although the leakage current for the controlled device is smaller in this experiment. This result points towards the fact that the control may serve to decrease the damage caused by radiation, although more studies are needed. However, it has been proved that it is possible to keep almost constant the main electrical characteristics of the device (in this case the C-V curve).

2) Discussion about charge injection efficiency: The selection of the actuation voltages V^+, V^- must be done carefully because it determines the robustness of the control. As it has been mentioned before, more than one injection mechanism may coexist in any device and, furthermore, this injection may depend on the state of the device (for example on the instantaneous net trapped charge).

In order to analyze the time evolution under different voltage

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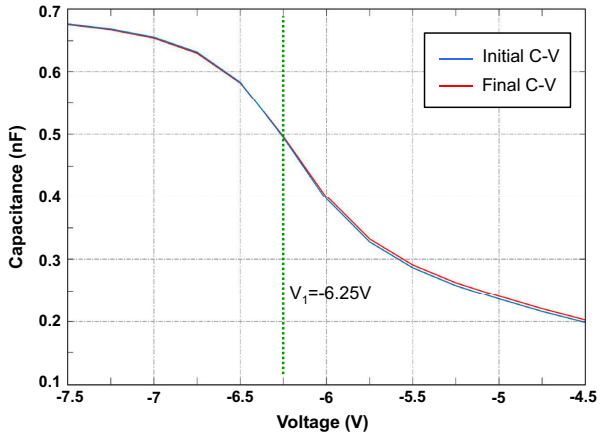

Fig. 8. Initial and final C-V of Dev-2 during the irradiation experiment. This device was controlled with a target capacitance value of C_{th} = 0.495nF at V_1 = -6.25V.

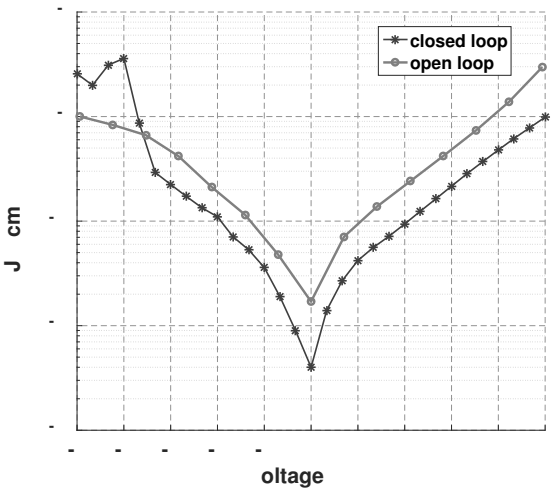

Fig. 9. Comparison of the I-V characteristics of Dev-1 and Dev-2, after being irradiated with a total dose of 237.6 Gy(SiO_2) during the same experiment. Dev-1 was kept in open-loop configuration at +1V bias, while Dev-2 was being controlled during the whole experiment.

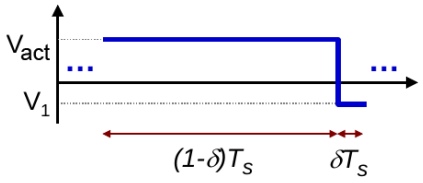

Fig. 10. Waveform generated to excite in open loop the device and observe the dynamics of charge trapping by monitoring $C[V_1](nT_S)$.

stresses, a useful tool is to apply a sequence of voltage waveforms as the one shown in Fig. 10, with different actuation voltages, V_{act}. These waveforms allow to observe the time evolution of the capacitance, measured at constant voltage V_1, with the device being stressed by different actuation voltages.

As an example, Fig. 11 shows the time evolution of the capacitance of Dev-3, measured at $V_1 = -5.3V$, while the device has been excited with a specific sequence of actuation voltages: $V_{\text{act}} = -10V, -7V$ and $+3V$.

The actuation stress is switched from -7V to 3V three times at the beginning of the experiment. As it can be observed, the application of $-7V$ tends to increase the capacitance while the application of $3V$ tends to decrease it. Since the substrate is p-type, the C-V curve of the MOS capacitance has a decreasing shape, i.e. see Fig. 5. This means that $-7V$ displaces the curve to the right (decreasing net charge trapping), while $+3V$ displaces the curve to the left (increasing net charge trapping).

In the same experiment of Fig. 11, at $t = 2.5$h, a long sequence of bits is applied with $V_{\text{act}} = -10V$. As it can be observed, the capacitance of the device increases. At approximately $t = 7$h the actuation voltage is again switched from -7V to +3V three times. As it can be observed the injection has clearly changed. For $3V$ a mixed behavior can be observed while, for $-7V$ the capacitance decreases. This behavior is very different from the one found in the initial part of the experiment. Control in certain regions may then require an inversion of the actuation law.

The device is brought back to approximately the initial state by the application of bits with a $V_{\text{act}} = +3V$ for 2.5h, and the whole sequence is repeated. As it can be observed the behavior in both segments of the experiment is similar. Fig. 12 shows the C-Vs measured at the beginning and end of the experiment. So, for this device and the voltage stresses applied, the change in behavior of charge injection can be accomplished within a voltage shift of approximately $0.55V$.

The main conclusion is that charge injection depends on the applied voltages, but also on the net charge present in the dielectric. This indicates that indeed the charge injection in the devices is complex and must be taken into account when planning for a control.

IV. Conclusion

A long-time experiment involving Gamma radiation in a MOS capacitor under a charge control loop has been performed. The evolution of the voltage shift of the C-V curve and the correlation between the control bitstream and the dose rates applied indicate that the dielectric charge induced by radiation can be compensated. This technique can be used to improve the reliability of MOS-related devices working in hardness environments. Additionally, real-time information about the charge being induced by radiation is obtained from the bitstream provided by the control loop. This may allow to use this technique in radiation detection applications, although embedding these controls with the normal use of the devices is generally an open problem that may present different solutions depending on the specific applications.

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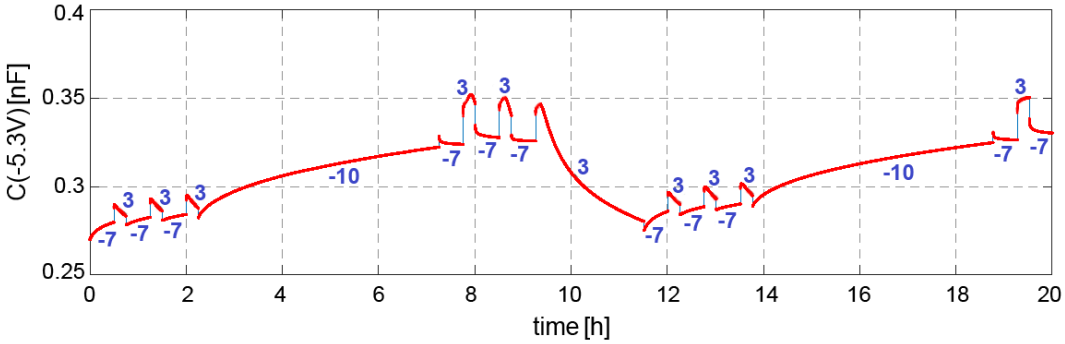

Fig. 11. Time evolution of the capacitance of Dev-3 under the actuation of the waveform shown in Fig. 10, with $\delta = 1/3, T_S = 350$ms, different actuation voltages (-10V, -7V and 3V) and a common observation voltage (-5.3V). The values plotted are the capacitances measured at -5.3V. Depending on the charging state of the dielectric, the injection of charge for the same voltage may be substantially changed.

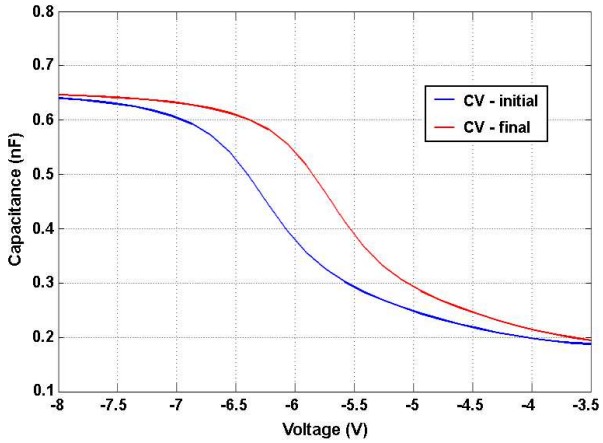

Fig. 12. C-Vs measured at the beginning and end of the experiment shown in Fig. 11.

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